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A Single-Chip NMOS Analog Front-End LSI for Modems

YOSHIAKI KURAISHI, TAKAYOSHI MAKABE, AND KENJI NAKAYAMA

Abstract—This paper presents a fully integrated analog front-end LSI chip which is an interface system between digital signal processors and existing analog telecommunication networks. The developed analog LSI chip includes many high level function blocks such as A/D and D/A converters with 11 bit resolution, various kinds of SCF's, an AGC circuit, an external control level adjuster, a carrier detector, and a zero crossing detector. Design techniques employed are mainly directed toward circuit size reductions. The LSI chip is fabricated in a 5 μm line double polysilicon gate NMOS process. Chip size is 7.14 × 6.51 mm. The circuit operates on ±5 V power supplies. Typical power consumption is 270 mW. By using this analog front-end LSI chip and a digital signal processor, modem systems can be successfully constructed in a compact size.

I. Introduction

RECENTLY, inexpensive hardware for implementing digital signal processing (DSP) techniques have been increasingly developed. Many voiceband signal transmitting and processing systems have been successfully realized using highly advanced digital LSI techniques [1]. Some commercial service equipment has already been established. On the other hand, there are enormous installed analog telecommunication networks and many digital signal sources, such as terminals and computers. These situations require interfaces between the digital sources and the analog telecommunication networks.

In voiceband data transmission systems, digital implementation has been rapidly promoted, and some digital modems have been reported [2], [3]. In these systems, however, digital signals must be converted into analog signals so as to be transmitted through the existing analog telecommunication networks. Therefore, how to implement the conversions by using fully integrated circuits has been a very important subject for construcing LSI data modems in compact form.

This paper presents an NMOS analog front-end LSI chip developed for high speed telephone channel modems. A system block diagram is illustrated in Fig. 1. This LSI chip converts digital signals generated in a digital signal processor [4] connected in cascade into band-limited analog signals which are transmitted through existing telephone channels and vice versa. Furthermore, additional functions, such as cable amplitude and delay equalizations, are realized using switched capacitor filter techniques [5].

The LSI chip has various kinds of high level analog function blocks: analog-to-digital (A/D) and digital-to-analog (D/A) converters with 11 bit resolution, band-limiting filters, an automatic gain control circuit, cable amplitude and delay equalizers, a carrier level detector, and a zero crossing detector. To realize these analog functions in an NMOS process and to minimize an LSI chip area, several new circuit design techniques are introduced.

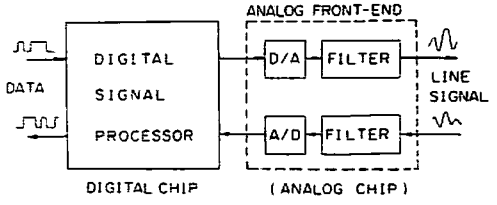

Fig. 1. Block diagram of LSI modem.

This introduction does not define the type of modem, speed, duplex/nonduplex, coding, etc.

II. System Description

Fig. 2 shows a block diagram of the chip. The upper part of the diagram is the transmit section and the lower part is the receive section. The DSP interface is on the left and the telephone line interface is on the right.

In the transmit section, 9 bit digital data from the DSP are converted to analog signals by the D/A converter. The D/A converter uses the charge redistribution technique [6]. It operates at a 7.2-9.6 kHz sampling rate and ±2.5 V full scale.

The second-order *RC*-active low-pass filter is used for anti-aliasing of the following switched capacitor filters. The −3 dB frequency is 42 kHz.

The low-pass filter is a fifth-order switched capacitor filter (SCF) and operates at a 288 kHz clock rate. The cutoff frequency is 3.4 kHz.

The transmit section includes an attenuator for transmit signal level adjustments. By using a 5 bit control signal, the output level can be adjusted from 0 to −31 dB in 1 dB steps. The cable equalizer is also included to compensate for amplitude distortions in the transmission lines. The cable equalizer is a first-order programmable SCF. It has four-step variable frequency response via pin selection.

The output smoothing filter is the same *RC*-active filter as the anti-aliasing filter with a 42 kHz −3 dB frequency. It is used for clock noise reduction purposes. Attenuation is more than 34 dB at 288 kHz.

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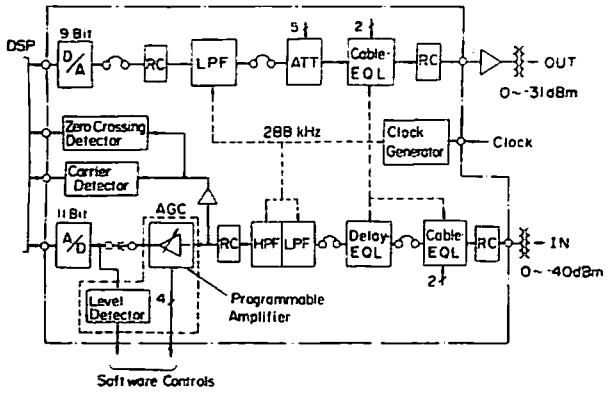

Fig. 2. Analog front-end block diagram.

The receive section contains a delay equalizer to compensate for delay distortions in the transmission lines. The equalizer is realized by a sixth-order SCF. It equalizes a fixed group delay for two links in voice channels.

The receive band-limiting filter consists of fifth-order low-pass and fourth-order high-pass filters. The upper cutoff frequency is 3.4 kHz and the lower cutoff frequency is 0.4 kHz. A 288 kHz clock rate is used in the high-pass filter to ease the output smoothing by the second-order *RC*-active filter. The large capacitor ratio problem in the high-pass filter is solved by using resistive dividers in the SCF.

The automatic gain control (AGC) circuit is needed to accommodate the large dynamic range of the receive signals. The AGC circuit consists of a programmable amplifier and a level detector. These circuits are controlled by the DSP. The programmable amplifier gain can vary in 16 steps of 2.7 dB. The AGC circuit operates over a ⁻40–0 dBm receive signal range, and the operation limits the level variation to a maximum 2.7 dB at the A/D converter input.

The AGC circuit output signals are converted to 11 bit codes by the A/D converter. Rather high accuracy is necessary to equalize the 2.7 dB variation in the input level by the digital AGC method. An external coupling capacitor is used for dc offset error rejection. The capacitor eliminates dc error in the receive SCF's and AGC circuit.

The receive section includes an anti-aliasing filter, a smoothing filter, and a cable equalizer. These circuits are the same as the transmit section.

All the SCF's operate on a 288 kHz clock, which is generated by counting down an external clock. Because of the synchronous SCF's operation, analog loop-back tests are possible. The transmit low-pass filter output can be connected to the receive low-pass filter input for the test, and the receive cable equalizer output can be connected to the attenuator input.

The *RC*-active filters, on the input of the transmit low-pass filter and the output of the receive high-pass filter, allow asynchronous A/D, D/A, and SCF's operation.

Receive filter output signals are used in the carrier detector and zero crossing detector. The carrier detector monitors receive signal levels. The zero crossing detector is used for 300 bit/s FSK decoding.

III. Switched Capacitor Filters

Many SCF's are employed in the developed analog front-end LSI chip, and they occupy major chip areas. Therefore, it is very important to design the SCF's to be small in size. In other words, reductions in both unit capacitor area and capacitance ratios must be achieved. For this purpose, stray capacitance insensitive circuit configurations and a capacitance ratio reduction technique are employed. Design considerations and fabrication results for each filter are described in this section.

A. RC-Active Filters

Transfer functions for *RC*-active filters are determined by resistor and capacitor values. It is usually difficult to control resistor and capacitor values with high accuracy in an LSI fabrication process. Therefore, the fabricated filter responses deviate from the designed values to a certain extent. For this reason, it is desirable to employ simple specifications for the *RC*-active filters. For this purpose, a sufficiently high sampling frequency of 288 kHz, compared to the passband, is utilized for operating the SCF's. The *RC*-active filter cutoff frequency is designed to be 42 kHz. The second-order *RC*-active filters are realized using the well-known Sallen-Key configuration [7].

B. Transmit and Receive Low-Pass Filters

Since the sampling frequency for the SCF's is determined to be sufficiently high compared to the passband, transfer function approximations for the SCF's are carried out in the $S(=j\omega)$ domain.

In order to decrease the unit capacitor area, a stray capacitance-insensitive leapfrog circuit is employed for building the transmit and receive LPF's. Stray-sensitive circuits require predistortion to compensate for stray capacitances. However, this stray capacitance compensation varies with fabrication errors. Therefore, it is difficult to decrease the unit capacitor area without regard to the stray capacitance. Prefilters are included in both LPF's to suppress the spectrum at the sampling frequency. The circuit configuration is illustrated in Fig. 3. Fifth-order LPF's result, and their designed amplitude responses in decibels, including the high-pass filter, are shown in Fig. 4(a) and (b) with dashed lines.

C. High-Pass Filter

In the high-pass filter, the sampling frequency to cutoff frequency ratio is extremely high. This implies that the capacitance ratio becomes very large. As is well known, capacitors are constructed using several unit capacitors on monolithic integrated circuits. Therefore, the total capacitance becomes extremely large in order to guarantee accuracy for each capacitance ratio. These situations mean that capacitance ratio reductions are very important for building SCF's which are compact in size. A voltage-dividing technique is introduced for this purpose, by which the output voltage from an operational amplifier is divided using resistive circuits. The basic concept of the resistive voltage divider is illustrated in Fig. 5. Since the

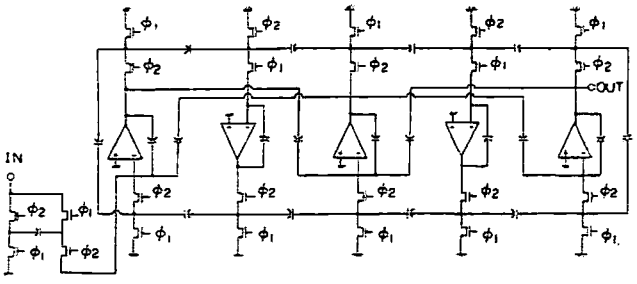

Fig. 3. Fifth-order stray-insensitive leapfrog SCF circuit.

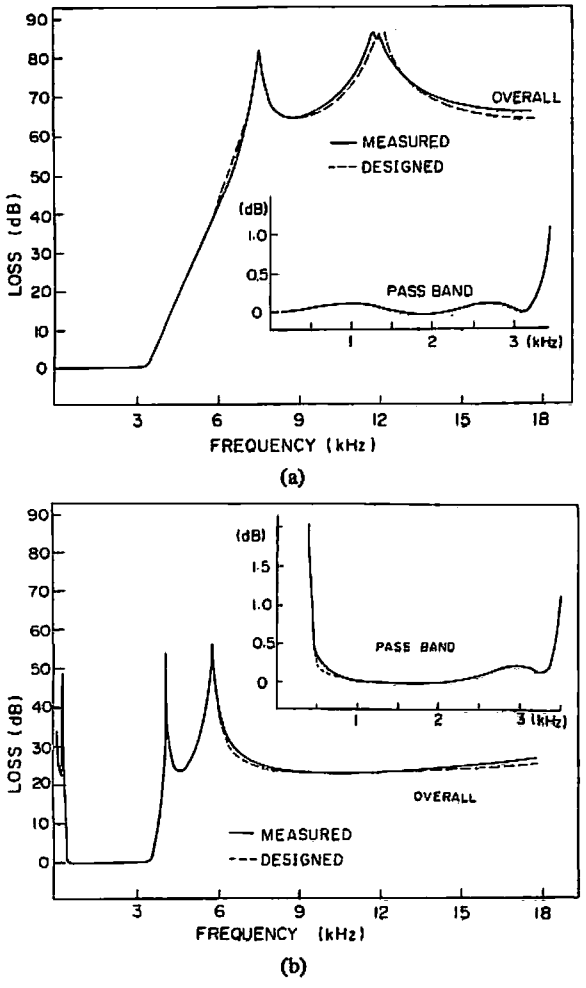

Fig. 4. Amplitude responses in decibels for fifth-order LPF's. Designed and measured responses are illustrated with dashed and solid lines, respectively. (a) Transmit filter. (b) Receive filter.

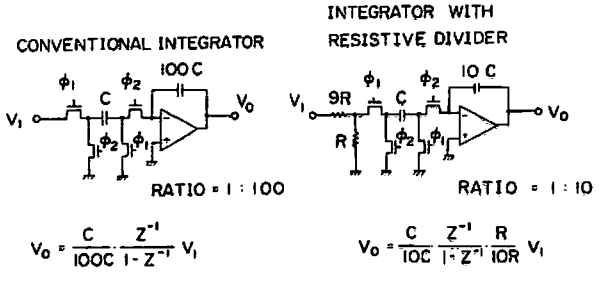

Fig. 5. Capacitor ratio reduction by resistive divider.

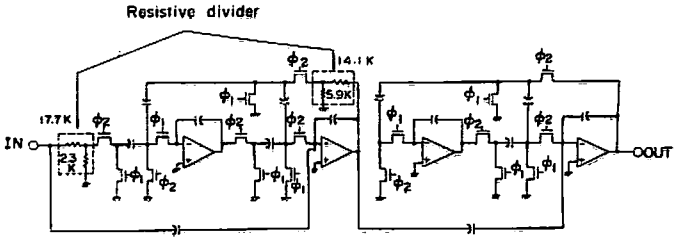

Fig. 6. HPF circuit configuration with resistive dividers.

resistive voltage dividers are free from the effects of parasitic capacitances, the unit capacitance area can be decreased without regard to the parasitic effects. The 0.25 pF unit capacitance is utilized for the high-pass filters. The high-pass filter circuit configuration, where two resistive dividers are employed, is shown in Fig. 6. A large capacitance ratio (400:1), required in the original circuit without the voltage dividers, can be reduced to 140:1 by using the resistive voltage divider. Accordingly, the total capacitance becomes 140 pF by using the 0.25 pF unit capacitance.

D. Delay Equalizer

As mentioned previously, the sampling frequency to the passband frequency ratio is high; therefore, a delay equalizer transfer function can be approximated in the s domain. A z-transfer function is obtained through the bilinear z transform. The designed delay time is illustrated in Fig. 7(a) with a dashed line. The delay equalizer is built in cascade form, using three biquad sections.

E. Cable Equalizer

First-order SCF's are utilized for building the transmit and receive cable equalizers. Their amplitude responses can be controlled by changing capacitance ratios. Four variable amplitude responses are prepared. They can be selected by external control signals. Designed results are shown in Fig. 8 with dashed lines.

F. Experimental Results

Transmit and Receive Filters: Measured amplitude responses in decibels for transmit and receive filters are illustrated with solid lines in Fig. 4(a) and (b), respectively. These figures show that the differences between designed and measured filter responses are small. The 0.44 pF unit capacitor, employed for these SCF's, can be recognized to guarantee high accuracy fabrication of capacitance ratios.

Delay Equalizer: Measured group delay time and amplitude response in decibels are illustrated in Fig. 7(a) and (b) using solid lines, respectively. The fabrication error for the group delay time is small. Amplitude error is about 0.16 dB (peak-to-peak) in the passband and satisfies the requirement.

Cable Equalizer: Fig. 8 shows measured amplitude responses in decibels using solid lines.

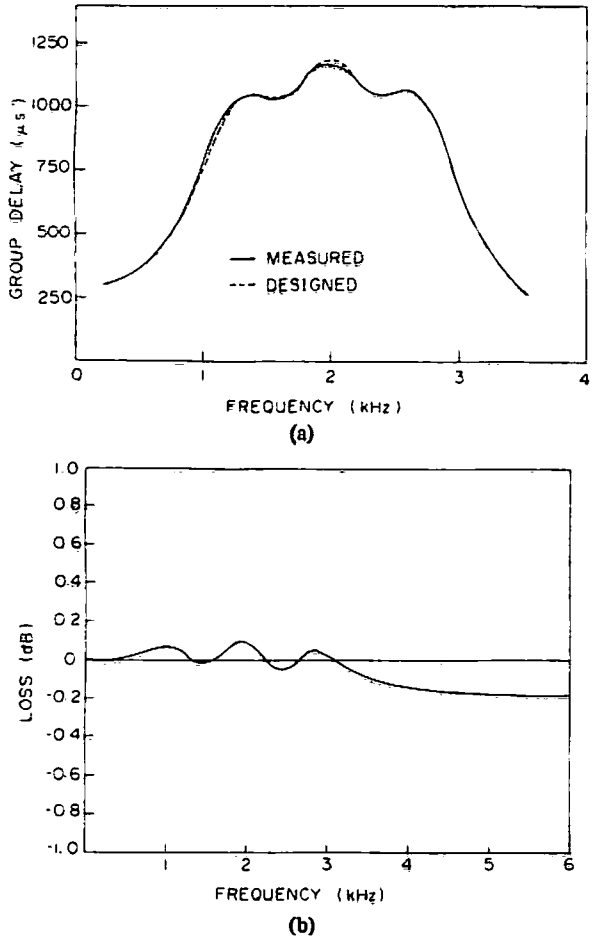

Fig. 7. Delay equalizer responses. (a) Group delay time. (b) Amplitude response in decibels.

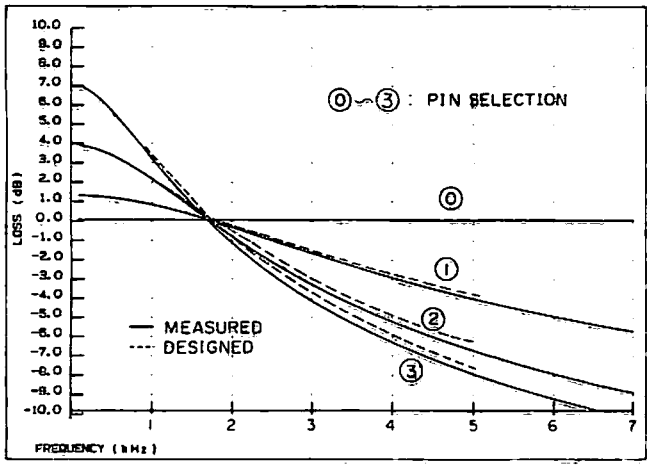

Fig. 8. Amplitude response in decibels for cable equalizer.

IV. Carrier Detector

One of the problems in developing the analog front-end LSI was the realization of a carrier detector on an MOS chip. The carrier detector monitors receive carrier levels and registers the absence of a carrier when the line level becomes lower than −45 dBm. This requires a small signal detection technique. The key point is realization of high gain amplifier and rectifier circuits with high accuracy. Fig. 9 shows a carrier detector

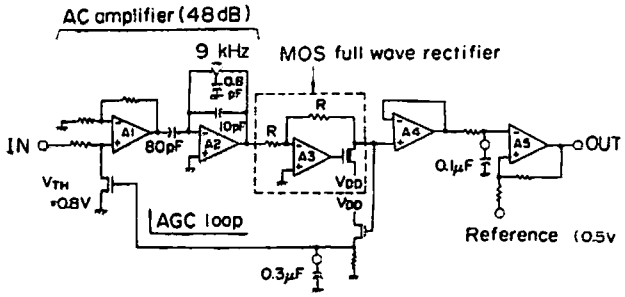

Fig. 9. Carrier detector schematic.

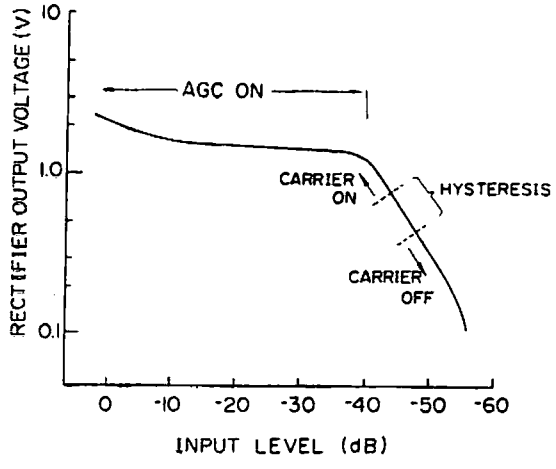

Fig. 10. Carrier detector performance.

circuit diagram. The carrier detector consists of a high gain amplifier, a precision rectifier, a smoothing filter, a hysteresis circuit, and an AGC loop.

The ac amplifier contains two operational amplifiers whose total gain is 48 dB. The first stage has a 30 dB gain, determined exactly by the resistor ratio for the feedback circuit. The second stage is an 18 dB ac amplifier. Its gain is determined by the capacitor ratio (80:10). The dc offset errors from the input signals and the first stage are eliminated by the 8 pF on-chip capacitor. The dc bias for the second stage is given by a 0.8 pF switched capacitor. The sampling rate is 9 kHz.

The rectifier consists of an operational amplifier, two well matched resistors, and a depletion transistor. The circuit works as follows. When the rectifier input voltage is positive the depletion transistor turns off. So the input signal passes through the resistors and the input voltage appears at the output. For a negative input, the depletion transistor becomes a source follower, and the circuit operates as an inverting amplifier with a gain of −1. The enhancement transistor is also applicable for this rectifier. However, the depletion transistor is used for large output swings. This full-wave rectifier shows linear response in the 100 mV-4 V range. The nonlinearity in low levels is caused by offsets of amplifiers $A2$ and $A3$ which are evaluated to be 10 mV.

The AGC loop is required for fast response. If there were no AGC loop, the amplifier and rectifier would be saturated for high level carrier. As a result, the carrier-off detection would have required a larger delay.

Fig. 10 shows the measured transfer chracteristic for a carrier detector. The output voltage is limited at 2 V by the AG

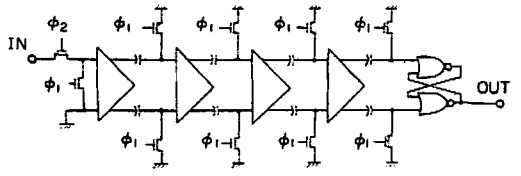

Fig. 11. Zero crossing detector schematic.

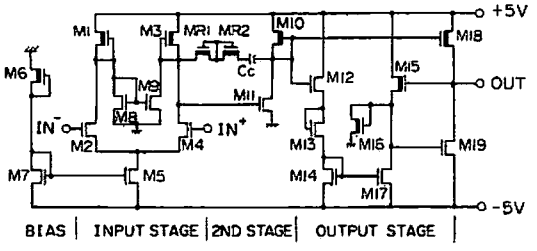

Fig. 12. Operational amplifier schematic.

TABLE I
DESIGN PARAMETERS AND PERFORMANCES FOR OPERATIONAL AMPLIFIER

dc Gain	62dB
Unity Gain Frequency	3MHz
Phase Margin	31°
Gain Margin (For 25pF Load)	20dB
1 % Settling Time (For 2.5V Step)	2.2μs
Slew Rate	3.5 V/μs
Positive PSRR	71 dB
Negative PSRR	54 dB
Output Swing	±4.5V
Input Noise At 1kHz	190nV/√Hz
Power Consumption	2.7 mW
Active Area	0.09 mm²

loop, and linear response is obtained at lower levels than -40 dBm with 2-5 dB hysteresis. The AGC loop allows saturation-free operation, so the carrier-off detection time is less than 4 ms for over a 45 dB input range.

V. Other Function Blocks

The A/D and D/A converters are based on the charge redistribution technique. To realize the 11 bit A/D converter, a capacitor array is used, which consists of 255 unit capacitors, a $\frac{1}{2}$ unit capacitor, and a $\frac{1}{4}$ unit capacitor. The 9 bit D/A converter contains a capacitor array with 255 unit capacitors. The unit capacitance value is 1.26 pF for the A/D converter and 0.33 pF for the D/A converter. Sampling rate ranges from 7.2 to 9.6 kHz and full scale is ±2.5 V. Measured linearity error is $\frac{3}{4}$ LSB for the 11 bit A/D converter and $\frac{1}{2}$ LSB for the 9 bit D/A.

The zero crossing detector, shown in Fig. 11, is an autozeroing comparator, using the chopper amplifier technique. It consists of four differential amplifiers, coupling capacitors, and a flip-flop circuit. It has about 3.5 mV hysteresis to make the circuit insensitive to AM noise.

The attenuator consists of a multitapped resistor string and switches which give access to the desired tap. The attenuator loss can be varied from 0 dB to 31 dB in 1 dB steps. Since the attenuator level is determined by the relative value of each resistor, it is accurate and stable within ±0.2 dB.

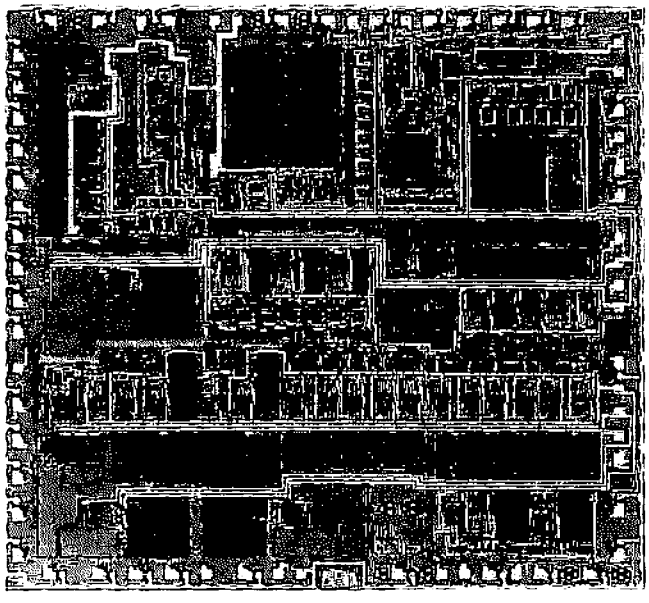

Fig. 13. Chip microphotograph for analog front-end LSI.

VI. Operational Amplifier

An operational amplifier has been designed to have a low power consumption and a wide bandwidth using a new circuit configuration for an input stage. A schematic of the operational amplifier is shown in Fig. 12. The amplifier consists of three stages.

An input stage has both functions of a differential amplification and a differential to single-ended conversion that is achieved by a current mirror circuit with $M8$ and $M9$. Therefore, the amplifier does not need the differential to single-ended conversion stage following the input stage. The amplifier can also reduce a pole, and can have a wide bandwidth with small dc current. The input stage has a 30 dB gain.

The second gain stage is a normal inverter with $M10$ and $M11$. This stage operates with a single power supply in order to reduce power consumption. It has a 28 dB gain.

An output stage $M12$-$M19$ operates class A push-pull. $M14$ and $M17$ compose a current mirror circuit that reverses the second gain stage output signal phase. $M16$ operates as a current source in order to increase $M17$ mutual conductance gm. $M15$ is used in a local negative feedback loop to reduce the output impedance required to drive large capacitive loads. $M18$ and $M19$ are push-pull transistors. The output stage has a 4 dB gain.

Frequency compensation is accomplished by a small value Miller capacitor Cc and resistors formed by depletion transistors $MR1$ and $MR2$. The threshold voltages for the depletion transistors are -3 V with zero-body bias and 0.8 V for enhancement transistors. Amplifier performance parameters for a 25 pF capacitive load are listed in Table I. The output swing is decreased by the resistive load. It is ±3.5 V for a 20 kΩ load.

VII. Implementation

Fig. 13 shows a photograph of the chip. The chip was fabricated in a double polysilicon NMOS process. The NMOS

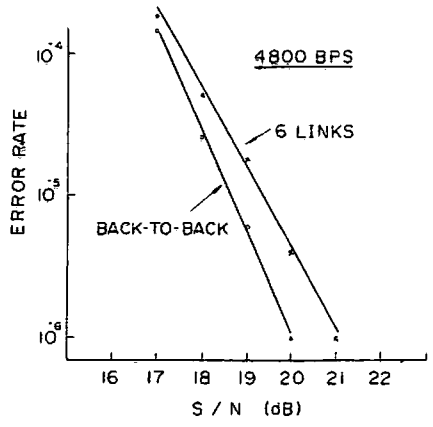

Fig. 14. Measured error rates relating to signal-to-noise ratio in modem system.

process was used for its high density circuits and low cost wafers. Chip size is 7.14 X 6.51 mm. The chip contains 39 amplifiers, 4 comparators, 400 digital gates, 2100 pF polysilicon-polysilicon capacitance, and 690 kΩ polysilicon resistance. The minimum gate length for a transistor is 6 μm, and the minimum width for a line is 5 μm. The unit switched capacitor is 0.25 pF in the high-pass filter and delay equalizer, and the 0.44 pF unit capacitor is used in low-pass filters.

The polysilicon-polysilicon capacitance and polysilicon resistance are used for the low voltage coefficient. Capacitors are used for the SCF's, *RC*-active filters, A/D and D/A converters, operational amplifier compensation, and ac coupling. Polysilicon resistors are used for *RC*-filters, resistive dividers, and feedback amplifiers.

The circuit operates on ±5 V power supplies. The power consumption is about 270 mW. The chip is mounted in a 64-pin quad-in-line package.

VIII. System Performance

With this LSI, the 2400-9600 bit/s modem, which is compatible with CCITT recommendations, can be realized.

Fig. 14 shows the error performance for a 4800 bit/s modem, which includes the analog front-end chip. The curves show good performance, and the error rate is less than 10^{-5} at a 20 dB signal-to-noise ratio.

IX. Conclusion

A fully integrated analog front-end LSI chip is presented in this paper. It is effectively applied to an interface system between a digital signal processor and existing analog telecommunication networks. The developed LSI chip includes many high level function blocks: A/D and D/A converters, various kinds of SCF's, an AGC circuit, an external control level adjuster, a carrier detector, and a zero crossing detector. Several circuit design techniques are employed, directed toward minimizing chip area. Experimental results show that the fabricated LSI chip has good performance. By using the developed analog front-end LSI chip and a digital signal processor, compact size modem systems can be successfully constructed.

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