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A Single DC Source Nine-Level Switched-Capacitor Boost Inverter Topology With Reduced Switch Count

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ABSTRACT This paper presents a new boost inverter topology with nine level output voltage waveform using a single dc source and two switched capacitors. The capacitor voltages are self-balancing and thus is devoid of any sensors and auxiliary circuitry. The output voltage is twice higher than the input voltage, which eliminates the need for an input dc boost converter especially when the inverter is powered from a renewable source. The merits of the proposed topology in terms of the number of devices and cost are highlighted by comparing the recent and conventional inverter topologies. In addition to this, the total voltage stress of the proposed topology is lower and have a maximum efficiency of 98.25%. The operation and dynamic performance of the proposed topology have been simulated using PLECS software and are validated using an experimental setup considering a different dynamic operation.

INDEX TERMS Multilevel inverter, nine-level inverter, step-up inverter, switched capacitor, reduce switch count.

I. INTRODUCTION

Multilevel inverters (MLIs) have emerged and evolved as a perfect solution for the medium and high voltage/power applications where high-quality dc-ac power conversion is needed. The classical topologies for the MLIs are neutral point clamped (NPC), flying capacitor (FC) and cascade H-bridge (CHB). These topologies are widely researched and are well established in industrial applications. However, for a higher number of output levels, the increased in the number components required for NPC and FC becomes quixotic. Similarly, for CHB, the higher number of isolated dc voltage sources for a higher number of levels limits its applications [1]–[5].

One category of the MLI topologies has been based on the multiple isolated dc voltage sources. In this category,

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the topologies have been classified as symmetrical and asymmetrical configured topologies. In symmetrically configured topologies, the dc voltage sources have the same magnitude. In asymmetrically configured topologies, the dc voltage sources have different magnitude resulting in a higher number of levels with a lower number of switches as well as dc voltage sources. In both types of topologies, the need for a higher number of isolated dc voltage sources limits their applications [6]–[9].

In order to reduce the number of dc voltage sources, the use of topologies with switched capacitor (SC) units have been recommended. The SC unit has been used with different arrangements resulting in different output voltage levels. One topology based on capacitors has been proposed in [10] and named as packed E-cell (PEC) topology. With two dc voltage sources and two capacitors, a nine-level output voltage waveform can be achieved, however, the topology lacks the boosting of the input voltage. Similar to [10], nine-level MLI topologies with two dc voltage sources and two capacitors have been proposed in [11], [12]. The authors in [13] proposed two new topologies with two dc voltage source along with two capacitors. Both topologies generate nine levels of the voltage across the load. However, both topologies use H-bridge for the polarity change, which requires switches with a higher voltage rating. The topologies also lack boosting ability. A *K*-type topology has been proposed in [14] in which two dc voltage sources along with two capacitors have been used for 13 levels at the output. However, the rating of both capacitors is different. In addition, both capacitors need to discharge for the last three levels, which results in a non-steady response in the capacitor voltage and unequal voltage steps across the load.

Most of the SC-based topologies use single dc voltage source and the SC units are used to create different dc-link voltages for the multilevel output across the load. Some of the topologies with SC units have a distinctive feature of boosting the output voltage, i.e., the peak of the output voltage is higher than the input supply. The SC-based MLI topology based on H-bridge has been proposed in [15], and [16] in which SC is connected through H-bridges for charging and discharging purposes. Several H-bridge with SC can be connected for a higher number of levels, which increases the number of switches.

A new seven-level boost inverter topology has been proposed in [17] with triple voltage gain. A hybrid switched-capacitor based nine-level MLI topology has been proposed in [18], however, the boosting feature is absent from the topology of [18]. Few more seven-level boost inverter topologies have been proposed in [19]–[25], however, the higher number of components have always been the major concern about these topologies. Furthermore, the topologies proposed in [21], [22], [24], [25] have a lower value of boosting factor.

Based on the twice boosting gain, several nine-level MLI topologies have input. In [26], a single-stage nine-level topology has been proposed. The topology uses 12 switches for nine levels across the load with twice of voltage gain. An improvement in terms of switches from [26] has been made in [27], which uses 11 switches to achieve nine levels. In [28], a new nine-level boost topology based on SC has been proposed to which the capacitors are charged in the first two levels and then discharged to give the boost feature in the next two states of the output voltage. Furthermore, for the topologies [29]–[38] the switch count for nine levels has been on the higher side. Considering these facts, this paper attempts to synthesize a nine-level voltage using the SC technique to reduce the component count. The main features of the proposed MLI are:

i. A single dc source is used.
ii. Self-voltage balancing is achieved across the capacitors.
iii. The output voltage is twice the input voltage.
iv. Low voltage stress across the switches.
v. The capacitor voltages are independent of the load power factor and modulation index.

The circuit topology and its working will be discussed in Section II. A detailed comparison has been carried out in terms of quantitative and cost analysis and has been resented in Section III. Sections IV gives a detailed explanation of the proposed topology with several simulations and experimental results and the conclusion of the paper has been presented in Section V.

II. PROPOSED TOPOLOGY

A. CONFIGURATION OF THE PROPOSED TOPOLOGY

The configuration of the proposed single-phase SCMLI topology is shown in Fig. 1 along with the maximum voltage stress across each switch as a factor of input dc voltage source, i.e. V_{dc}. The assembly of the proposed topology consists of ten switches. The switches can be either IGBT or MOSFET based on the frequency of operation, voltage, and power rating of the converter. Two capacitors C_1 and C_2 are used to split the dc supply voltage into halves. By systematic and sequential turning ON/OFF of the switches, the capacitor voltages are maintained at half of the supply voltage, i.e., $V_{dc}/2$. The proposed topology generates nine levels across the load with a twice voltage boosting factor. The switching

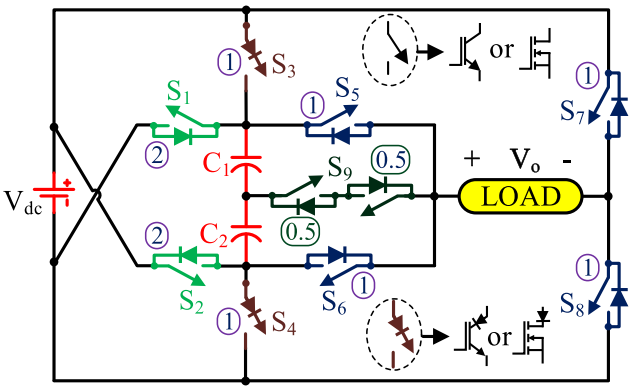

FIGURE 1. Proposed nine level inverter topology.

TABLE 1. Switching states of the proposed topology.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	V_o	V_{C1}	V_{C2}
0	0	1	1	0	1	0	1	0	0	C	C
0	0	1	1	0	0	0	1	1	$V_{dc}/2$	C	C
0	0	1	1	1	0	0	1	0	V_{dc}	C	C
0	1	0	0	0	0	0	1	1	$3V_{dc}/2$	—	D
0	1	0	0	1	0	0	1	0	$2V_{dc}$	D	D
0	0	1	1	1	0	1	0	0	0	C	C
0	0	1	1	0	0	1	0	1	$-V_{dc}/2$	C	C
0	0	1	1	0	1	1	0	0	$-V_{dc}$	C	C
1	0	0	0	0	0	1	0	1	$-3V_{dc}/2$	D	—
1	0	0	0	0	1	1	0	0	$-2V_{dc}$	D	D

Notations: 0 = OFF state of the switch, 1 = ON state of the switch, — = no change in capacitor voltage, C = charging of capacitor, D = discharging of capacitor

table for the proposed topology along with the variation of capacitor voltages V_{C1} and V_{C2} are given in Table 1.

B. DESCRIPTION OF VOLTAGE LEVELS

With the proposed topology, nine levels are generated across the load. In this section, all five levels in the positive half cycle are described with the blocking voltages of all the non-conducting switches and shown in Fig. 2 (a)-(e).

(i) State i (Zero voltage state): In this voltage state, as shown in Fig. 2 (a), the capacitors C_1 and C_2 are made to charge to their peak voltage by connecting them directly across the dc voltage source. This is achieved by turning ON the switches S_3 and S_4. By turning ON the switches S_5 and S_7, the load terminals are shorted and a path is provided for the flow of current in case of an inductive load.

(ii) State ii ($+V_{dc}/2$): As shown in Fig. 2 (b), the first voltage state equal to $V_{dc}/2$ appears across the load by turning ON the switches S_8 and S_9 and turning OFF switches S_5 and S_7. In this state, the capacitor voltage V_{C1} and V_{C2} are maintained at $V_{dc}/2$. The capacitor voltage V_{C1}, equal to $V_{dc}/2$, is subtracted from dc voltage source V_{dc}.

(iii) State iii ($+V_{dc}$): In this voltage state, the full source voltage appears across the load by turning ON switch S_5 and turning OFF switch S_9 as shown in Fig. 2 (c). Both capacitor voltages are further maintained at $V_{dc}/2$. The energy is stored in both capacitors until this voltage state.

(iv) State iv ($+3V_{dc}/2$): In this voltage state, the switches S_3 and S_4 are turned OFF and energy stored in capacitor C_2 is used to create the third voltage state. The voltage V_{C2} is

(v) added to the dc voltage source V_{dc} by turning ON switch S_2. The state of capacitor C_1 remains unchanged and the voltage is held at $V_{dc}/2$. This voltage state is shown in Fig. 2 (d).

(vi) State v ($+2V_{dc}$): The energies stored in both capacitors are released in this voltage state and the voltages of both capacitors are added to the dc voltage source. This boosting of dc voltage source results in $2V_{dc}$ across the load as shown in Fig. 2 (e).

Fig. 3 summarizes the voltage stress across all the switches for each level at the output. The switches S_1 and S_2 are

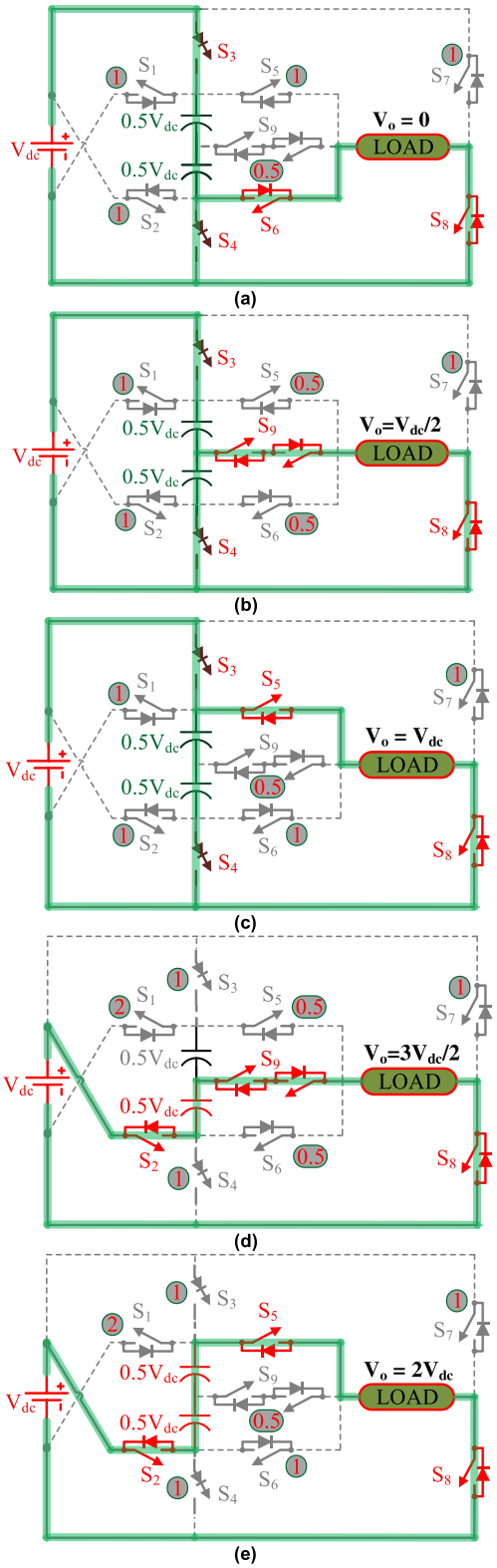

FIGURE 2. Positive voltage states of the proposed nine level topology with (a) $V_o = 0$, (b) $V_o = V_{dc}/2$, (c) $V_o = V_{dc}$, (d) $V_o = 3V_{dc}/2$, and (e) $V_o = 2V_{dc}$.

cross-connected between the dc voltage source and capacitors to obtain the boost feature. These switches need to block the $2V_{dc}$ due to the cross-connection. The switches S_3 and

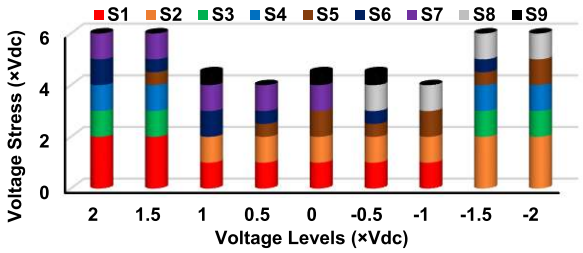

FIGURE 3. Voltage stress across all switches during all voltage levels.

S_4 are connected in series with diodes in order to prevent the conduction of switches S_3 and S_4 in the boost mode of operation. The switches S_3 to S_8 are needed to block the supply voltage V_{dc} and the bidirectional switch S_9 needs to block half of the supply voltage.

C. MODULATION TECHNIQUE

For the proposed topology, phase disposition pulse width modulation (PD-PWM) technique has been used. In PD-PWM, four carrier signals with the same magnitude and high frequency have been compared with the sinusoidal reference signal V_{ref} having a frequency of output voltage. The comparison results in the gate pulses for the switched according to Table 1. The logic for the proposed nine-level topology has been derived using Table 1 and has been implemented using the logic gates as shown in Fig. 4 (a). Based on the logic as shown in Fig. 4 (a), the different signals are shown in Fig. 4 (b) and (c). Fig 4 (b) depicts the four carrier signals V_{cr1} to V_{cr4}, each having a magnitude of V_{cr} along with the reference voltage V_{ref}. The gate signals produced with the comparison and the switching logic has been depicted in Fig. 4 (c). The modulation index for the PWM shown in Fig. 4 (b) can be obtained as

$$MI = \frac{V_{ref}}{4V_{cr}} \tag{1}$$

In order to show a better performance of the PD-PWM, different modulation techniques have been applied to the proposed nine-level topology. Apart from PD-PWM, phase opposition disposition PWM (POD-PWM), alternate phase opposition disposition PWM (APOD-PWM) and nearest level control PWM (NLC-PWM) techniques have been used for the comparison. With a carrier frequency of 2.5kHz and input voltage source, $V_{dc} = 100$V, Table 2 gives the comparison of different modulation techniques with the different factors. The PD-PWM gives the lower THD and higher output voltage compare to all other modulation techniques.

D. CAPACITOR VOLTAGE BALANCING

The self-voltage balancing of the capacitors C_1 and C_2 is one of the essential features of the proposed topology. Both voltages must be balanced with the voltage equal to half of the input voltage. From Table 1, the capacitor C_1 and C_2 have the same behavior in terms of charging and discharging pattern over a fundamental cycle. The capacitors C_1 and

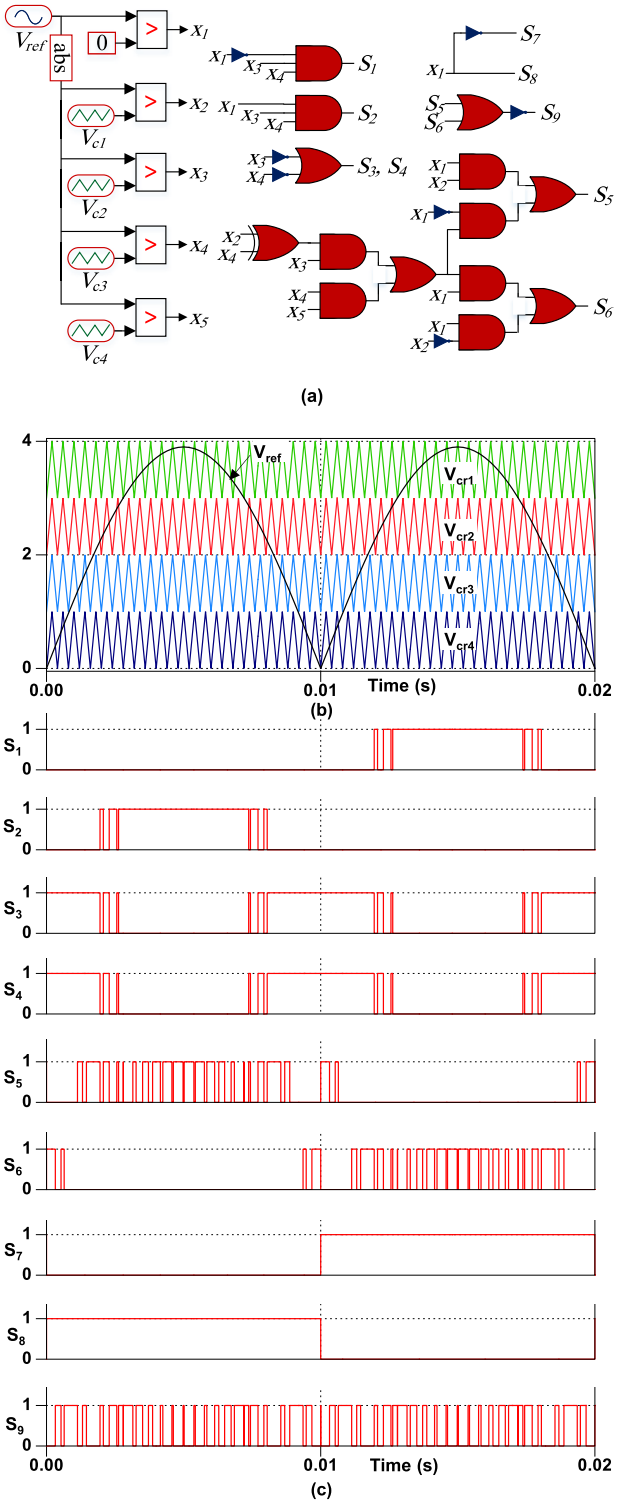

FIGURE 4. PD-PWM technique with (a) logic for the gate pulse generation, (b) carrier and reference signal and (c) generated gate pulses for all switches.

C_2 get charged during the voltage levels of zero, $\pm V_{dc}/2$, and $\pm V_{dc}$. The equivalent circuit during the charging od the capacitors is depicted in Fig. 5 (a). In the charing loop, the parasitic resistance of diodes, switches and equivalent series resistance (ESR) of capacitors are present. The lower

TABLE 2. Comparison of different PWM techniques.

Load	Modulation Techniques	THD %						V_{rms}	I_{rms}
		V_{THD}	3rd	5th	I_{THD}	3rd	5th		
R=20Ω, L=50mH	PD-PWM	9.57	0.98	0.37	0.72	0.49	0.12	139.7	5.5
	POD-PWM	9.89	1.14	0.39	0.75	0.54	0.13	139.1	5.37
	APOD-PWM	9.71	1.06	0.37	0.74	0.52	0.12	139.5	5.43
	NLC-PWM	9.82	1.36	0.67	0.97	0.57	0.22	139.3	5.35

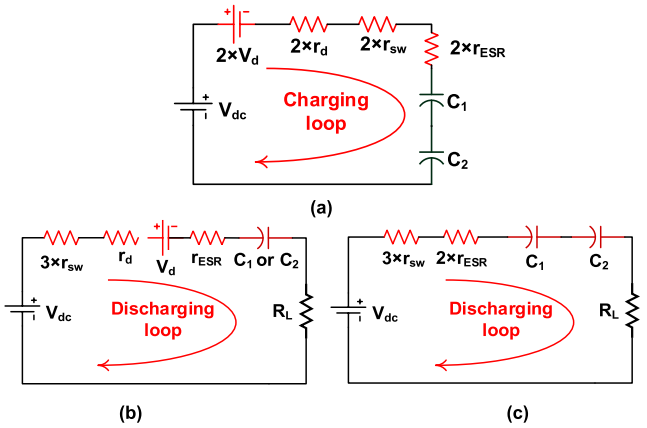

FIGURE 5. Equivalent circuit for the proposed nine level inverter for (a) charging of capacitors, (b) discharging of capacitor during voltage level of $\pm 3V_{dc}/2$ and (c) discharging of capacitors during the voltage voltage of $\pm 2V_{dc}$ [V_d = Forward voltage drop of diode, r_d = forward resistance of diode, r_{sw} = forward resistance of switch and r_{ESR} = ESR of capacitor].

value of these elements results in a meager value of time constant RC in the charing loop. By neglecting the voltage drops of the switches and diodes, the capacitor voltages will be half of the input voltage, i.e.,

$$V_{C1} = V_{C2} = \frac{V_{dc}}{2} \tag{2}$$

The capacitors get discharged by connecting them in series with the input source during the boost mode of operation, i.e., during the voltage levels of $\pm 3V_{dc}/2$, and $\pm 2V_{dc}$ as shown in Fig. 5 (b) and (c) respectively. the fully charged capacitors start to discharge and their voltage drops from $V_{dc}/2$. However, during the discharging of capacitors as shown in Fig. 5 (b) and (c), the time constant RC is very much high compared to the charging of the capacitors. This results in the slow discharging of the capacitors. When the next charging state comes, the voltage across the capacitors again rises to $V_{dc}/2$. Therefore, over a complete fundamental cycle, both capacitors charge and discharge for several duration, and each capacitor voltage can be maintained at the $V_{dc}/2$ with some ripple voltage.

III. COMPARATIVE STUDY

To show the merits of the proposed nine-level topology, a comparison has been carried out in terms of different component counts, total voltage stress, and gain of different topologies. Table 3 gives a quantitative comparison between the proposed topology and recently introduced SC-based topologies. The proposed topology requires ten switches for the nine-level generation, which is lower than the topologies proposed in [26], [27], [30], [33], and [35]. Furthermore, the proposed topology uses only two capacitors for the gain of two. However, the topologies proposed in [22] and [24] gives a voltage gain of 1.5 by using three capacitors. Another noticeable benefit of the proposed topology has been in terms of reduced voltage stress. The TSV_{pu} for the proposed topology has a lower value compared to topologies of [28], [30], [33], [34], and [36].

Apart from the quantitative analysis, a cost comparison of the proposed topology is given in Table 4. The rating of components has been selected based on the structure of the topologies. From Table 4, the proposed topology gives the minimum cost among all the topologies under consideration. The lower cost, along with the lower number of components gives an additional edge of the proposed topology for low and medium voltage applications as compared to other nine-level topologies with a single dc input voltage source. The reduced switch count implies reduced conduction losses. In theory, the maximum switch blocking voltage dictates the switching losses in addition to switching frequency. Furthermore, two of the total switches operate at the fundamental switching frequency. These factors supplement the fact of reduced switching losses. All these factors help in concluding that the proposed MLI has improved efficiency in comparison to similar counterpart topologies

For a power electronic converter, efficiency has been one of the leading performance parameters. The efficiency of a converter depends on the losses of the converter. With power electronic switches, conduction and switching losses contribute to the overall losses in addition to the ripple losses of the switched capacitor unit. The conduction losses occur due to the power loss of the equivalent resistance of switch or diode. PLECS software has been used for the accurate estimation of efficiency through thermal modeling. Fig. 6 illustrates the curves of efficiencies with output power for different similar topologies. As can be seen from these curves that the proposed topology along with topologies of [26] and [27] has almost similar curves. However, the proposed topology has a slightly higher value of efficiency compared to all other topologies. The topologies proposed in [30] and [36] have lower efficiencies due to their higher number of components and the number of capacitors.

IV. RESULTS AND DISCUSSION

In this section, different simulation and experimental results have been illustrated and discussed in detail. The PD-PWM technique as shown in Fig. 4 has been used to demonstrate the performance of the proposed nine-level topology. For the simulation, two capacitors with 2200μF have been used. The rating of the capacitor has been chosen based on the following

TABLE 3. Quantitative comparison of the proposed topology with other topologies.

Topology	N_L	N_{sw}	N_d	N_{dc}	N_{cap}	Variety of capacitor	TSV_{pu}	Gain	Voltage Boosting	Negative Level
[10], [11], and [12]	9	8	0	2	2	1	4.5	1	No	Inherent
[15], and [16]	7	16	0	1	2	1	5.3	3	Yes	Inherent
[17]	7	12	0	1	2	1	5.3	3	Yes	Inherent
[22]	7	10	0	1	3	2	5.3	1.5	Yes	Inherent
[24]	7	9	1	1	3	2	5.3	1.5	Yes	Inherent
[26]	9	12	0	1	2	1	5.5	2	Yes	Inherent
[27]	9	11	0	1	2	1	5	2	Yes	Inherent
[28]	9	10	1	1	2	1	7.5	2	Yes	Inherent
[30]	9	17	0	1	4	1	7.25	1	No	Inherent
[33]	9	12	0	1	3	2	6	4	Yes	Inherent
[34]	9	9	0	1	2	2	6.25	4	Yes	H-Bridge
[35]	9	12	0	2	1	1	5	1	No	Inherent
[36]	9	8	3	1	3	2	6.5	4	Yes	Inherent
[P]	**9**	**10**	**0**	**1**	**2**	**1**	**5.5**	**2**	**Yes**	**Inherent**

N_L=number of levels, N_{sw}= number of switches, N_d=number of diodes (including antiparallel and series connected to a MOSFET), N_{dc}=number of dc voltage sources, N_{cap}= Number of capacitors, TSV_{pu}= Total standing voltage (in per unit), [P] = Proposed

TABLE 4. Cost comparison between proposed topology and recently introduced topologies with single source nine level configuration.

Component	Part Number	Rating	Unit Price ($)	Topology							
				[26]	[27]	[28]	[30]	[33]	[34]	[36]	**[P]**
MOSFET*	IRFP9140NPBF	100V, 23A	2.2	2	2	2	-	-	-	2	**2**
	IRFP240PBF	200V, 20A	2.68	10	9	2	7	4	2	3	**6**
	AUIRFSL6535	300V, 19A	3.32	-	-	2	-	-	-	-	**-**
	IRFP350PBF	400V, 16A	3.48	-	-	4	7	6	3	-	**2**
	IXFH15N80	800V, 20A	13.492	-	-	-	2	2	4	4	**-**
Diode*	V20PWM10HM3/I	100V, 20A	1.11	-	-	-	-	-	1	2	**-**
	20ETF64PBF	200V, 20A	1.81	-	-	1	-	-	-	-	**-**
Capacitor#	23A252F100BB1H1	100V, 2500 µF	14.23	2	2	2	4	1	1	2	**2**
	23M252F200BH1H1	200V, 2500 µF	23.61	-	-	-	-	2	1	-	**-**
Total Cost ($)				56.99	56.98	60.59	127.024	120.034	108.718	97.088	**55.9**

*www.digikey.com, #www.galco.com

equation:

$$C_1 = C_2 = \frac{I_{pk}}{(\Delta V_C \times f_o)} \tag{3}$$

where, I_{pk}, ΔV_C, and f_o are the peak load current, capacitor voltage ripple, and frequency of the output voltage, respectively [27]. The different parameters used for the validation of the proposed topology has been given in Table 5.

A. SIMULATION RESULTS

The proposed nine-level topology has been simulated using PLECS software. Fig. 7 shows the different simulated waveforms for the proposed topology. The ac output voltage has a peak of 200V, which has been fed to a series-connected the resistive-inductive load (Z = 50mH + 20 Ω), results in an output current of a peak value of 7.5A. The voltage across both capacitors varies around 50V with a minimum and maximum value of 45V and 51V, respectively. Furthermore, the FFT of the output voltage has also been shown in Fig. 7 (b), which has a THD of 9.41% with the elimination of all lower-order harmonics.

Some of the performance parameters have also been shown for the proposed topology. Fig. 8 shows the variation of capacitor ripple voltage along with THD. The capacitor ripple

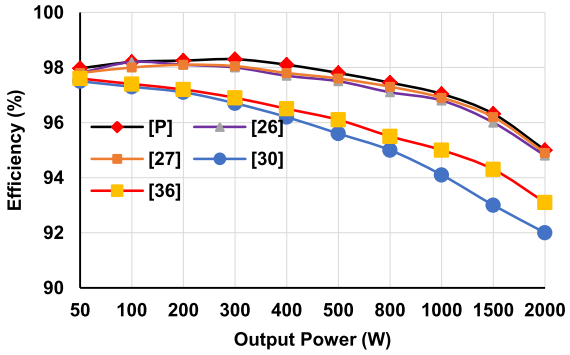

FIGURE 6. Efficiency comparison of different topologies.

TABLE 5. Simulation and experimental parameters.

Parameter	Simulation	Experimental
Input voltage source	100V	100V
Output frequency	50Hz	50Hz
Carrier frequency	2.5 kHz	2.5 kHz
Capacitor	2200 μF	2200 μF
Load Parameters	Different combinations of resistive-inductive load	Different combinations of resistive-inductive load

TABLE 6. Power loss distribution of the proposed topology with $P_o = 800W$.

Power Loss of	P_{sw} (W)	P_c (W)	P_{loss} (W)
Switch S_1	0.0256	0.826	0.8516
Switch S_2	0.0256	0.826	0.8516
Switch S_3	0.0541	3.838	3.8921
Switch S_4	0.0612	3.848	3.9092
Switch S_5	0.0506	0.649	0.6996
Switch S_6	0.0537	0.652	0.7057
Switch S_7	0.041	1.018	1.059
Switch S_8	0.044	1.015	1.059
Switch S_9	0.0579	1.487	1.5449
Total switch losses	0.4137	14.159	14.5727
Capacitor C_1			3.15
Capacitor C_2			3.17

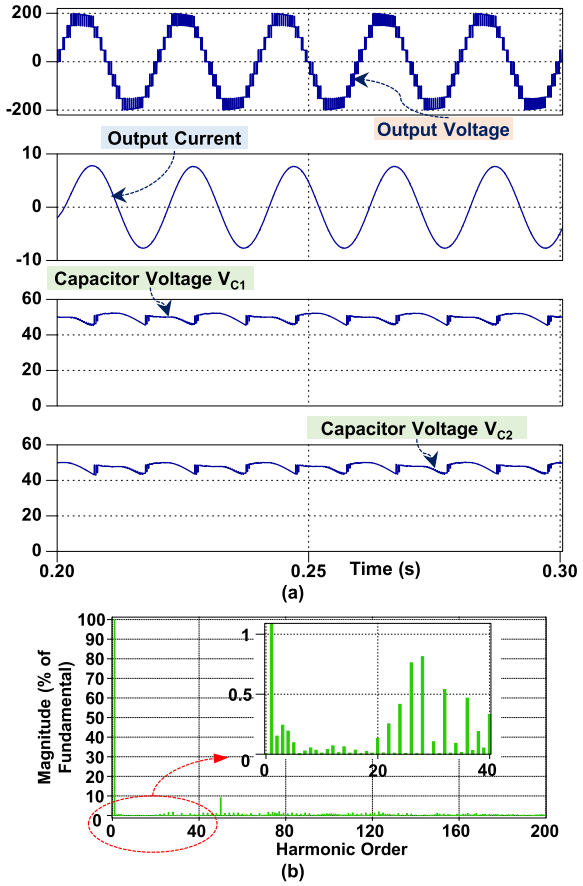

FIGURE 7. Simulation results of (a) output voltage, output current and capacitor voltage with Z = 50mH + 20 Ω and (b) FFT of output voltage.

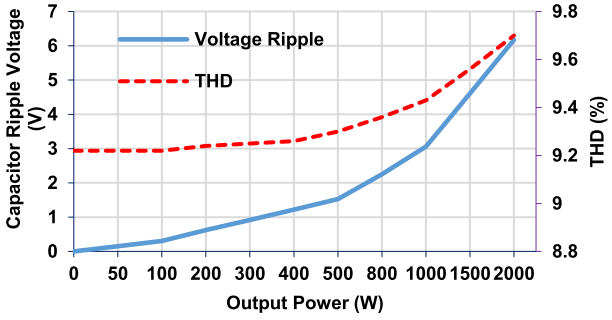

FIGURE 8. Variation of capacitor ripple voltage along with THD.

voltage increases as the output power increase. The increase in capacitor ripple voltage slightly deteriorates the output voltage waveform and this change results in a slight increase in the THD. At no load, the THD has a value of 9.2% which increases to 9.7% at an output power of 2kW.

Furthermore, the performance of the proposed topology has been tested with a dynamic change of load and modulation index (MI). Fig. 9 (a) illustrates the output voltage, current and capacitor voltages with a load change of purely resistive load of Z = 50 Ω to a series-connected resistive-inductive load with Z = 50mH + 50 Ω. With the change of load type, both capacitor voltages are balanced and it shows that the load type does not affect the balancing of capacitor voltages. In addition, a dynamic change of modulation index has been illustrated in Fig. 9 (b). The MI has been changed from 1.0 to 0.6 and from 0.6 to 0.4. With a modulation index of 0.6, the number of levels is reduced to seven and with a modulation index of 0.4, the number of levels becomes 5. However, both capacitor voltages remain balanced.

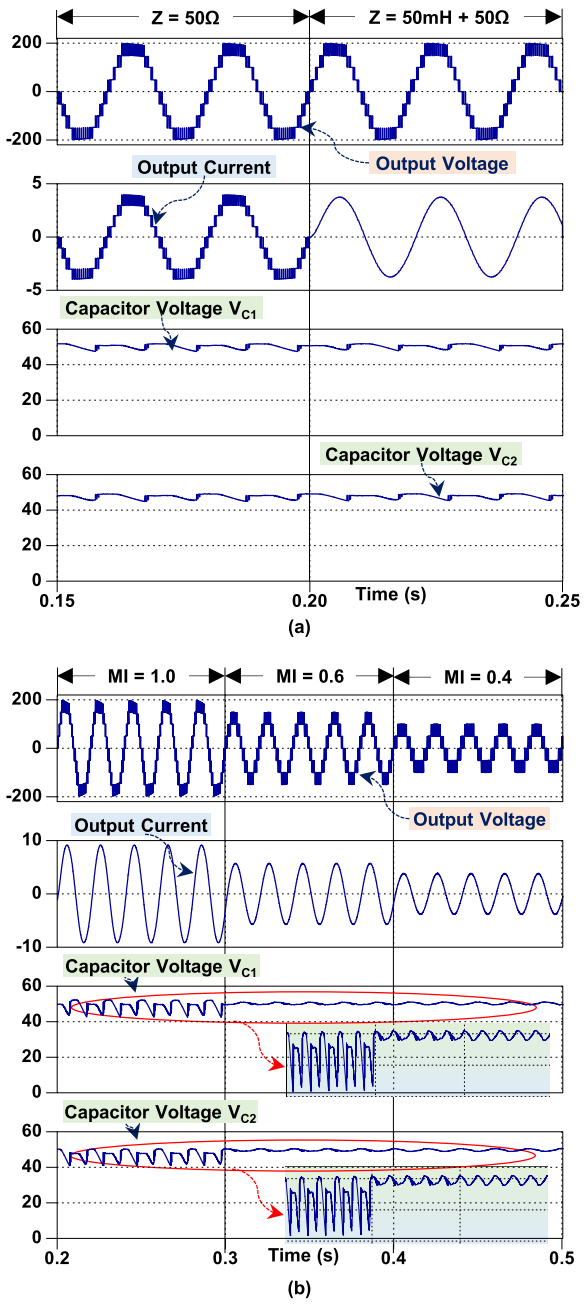

FIGURE 9. Simulation results of output voltage, output current and capacitor voltage with (a) change of load from Z = 50 Ω to Z = 50mH + 50 Ω and (b) change of modulation index with Z = 20mH + 20 Ω.

In addition, the efficiency of the proposed topology against the output power has been shown in Fig. 10. The maximum efficiency of the proposed topology has been estimated as 98.25% at the output power of 200W. At the output power of 2kW, the efficiency of the proposed topology comes out to be 95%. The proposed topology gives adequate efficiency at a higher power rating. Furthermore, the power loss distribution among different switches and capacitors for a power rating of 800W has been given in VI. The switch pair S_3 and S_4 have the maximum power loss as both switches are involved in the charging and discharging of capacitors. With 800W output power, the total losses of the converter become 20.9W. This results in the efficiency of the proposed topology as 97.5%.

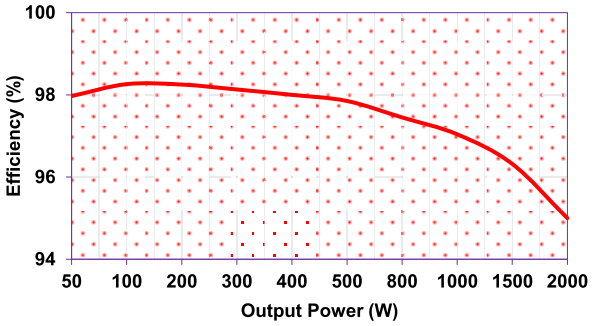

FIGURE 10. Efficiency vs output power curve of the proposed topology.

B. EXPERIMENTAL RESULTS

To verify the feasibility of the proposed nine-level topology, a laboratory prototype was developed to carry out the experimental work. The switching frequency of 2.5 kHz has been selected for the PD-PWM with a dead time of 2μs provided by the delay circuit. The gate pulses have been generated using dSPACE. The experimental setup has been shown in Fig. 11. For the experimental results, the magnitude of the dc input voltage source was fixed to 100V. Fig. 12 (a) shows the output voltage and current waveform for series-connected resistive-inductive load with R=10Ω and L=100mH. One of the main features of the proposed topology has been the twice voltage gain and this has been confirmed by the output voltage, which has a 200V peak resulting from a 100V dc input voltage. In addition, both capacitor voltages are depicted in Fig. 12 (b). Both capacitor voltages, i.e., V_{c1} and V_{c2} are well balanced and are equal to half of the dc voltage source, i.e., 50V as shown in Fig. 12 (b). Fig. 12 (c) depicts the FFT spectrum of the output voltage with a THD value of 9.5% which is analogous to the simulation value of THD.

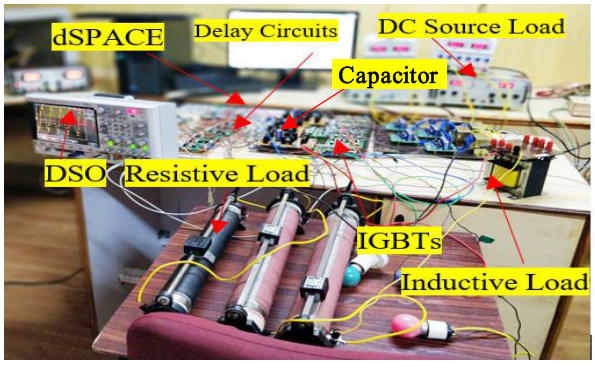

FIGURE 11. Experimental setup for the proposed nine level topology.

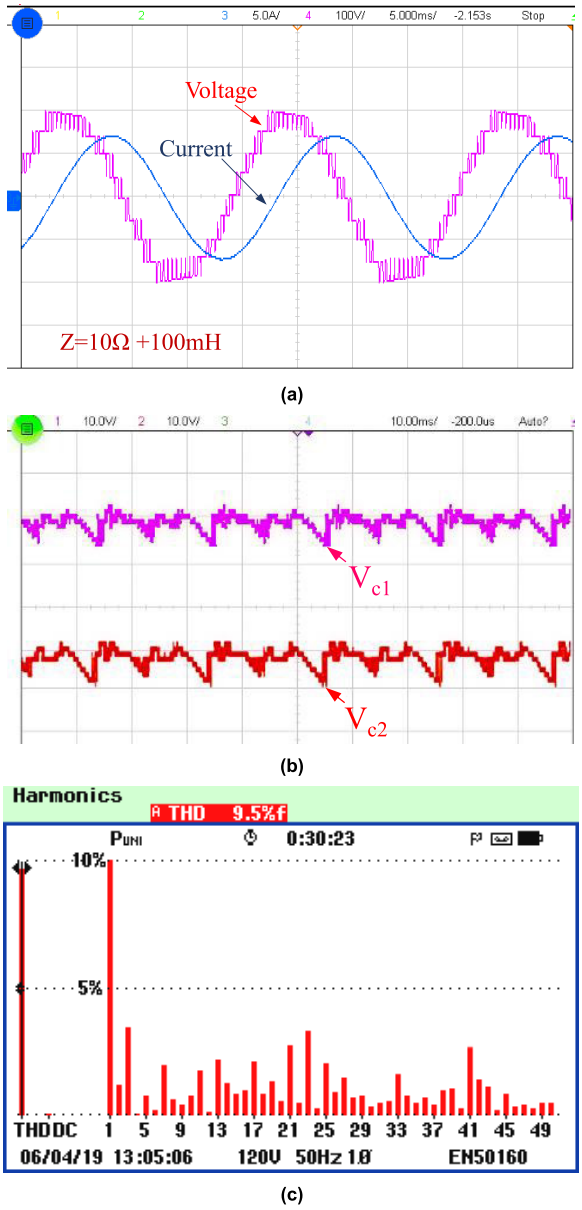

FIGURE 12. Experimental results of (a) output voltage, output current waveform [v = 100v/div, i = 5A/div] (b) capacitor voltages [$V_{c1} = V_{c2}$ = 10V/div] and (c) FFT of output voltage with Z = 100mH + 10 Ω.

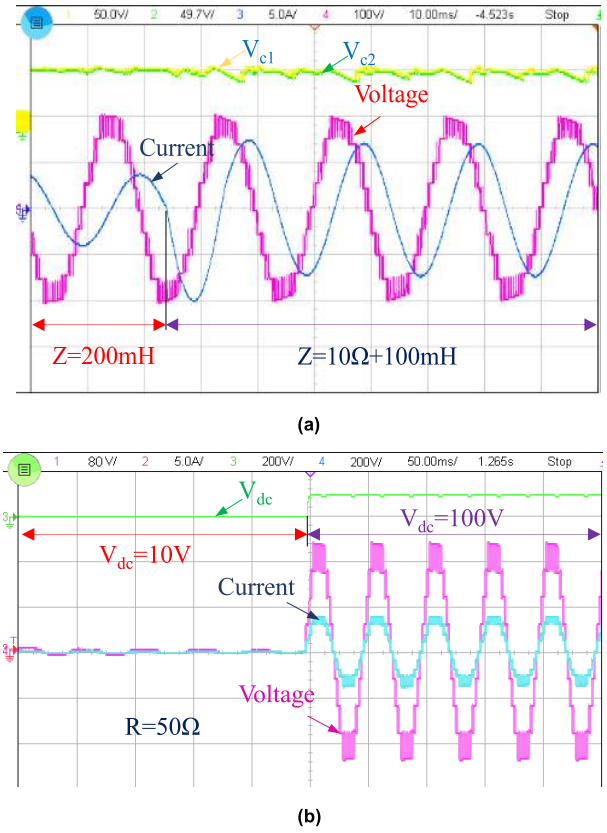

FIGURE 13. Experimental results for the proposed nine level MLI with (a) change of load from purely inductive to resistive-inductive load [v = 100v/div, i = 5A/div, $V_{c1} = V_{c2}$ = 50V/div] and (b) step change in input dc voltage source from 10V to 100V [v = 80V/div, i = 5A/div, V_{dc} = 200V/div.

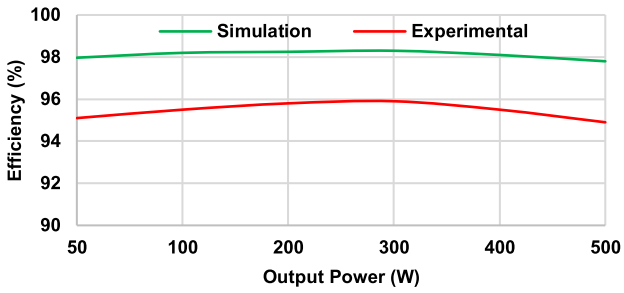

FIGURE 14. Simulation and experimental efficiency of the proposed topology.

Moreover, a change in the type of load has also been considered during the experimental results. Fig. 13 (a) shows the waveforms as the load changes from resistive-inductive load to a purely inductive load. Furthermore, the proposed topology has been tested with a step-change in input dc voltage while feeding the resistive load. The input dc voltage V_{dc} is changed to 100V from 10V and the corresponding voltage and current waveforms are shown in Fig. 13 (b). All these results prove the suitability and feasibility of the proposed nine-level boost inverter topology for varying operating conditions.

Fig. 14 shows the variation of efficiency of the proposed topology with simulation and hardware results. As the maximum efficiency of the proposed topology in simulation is 98.25%, however, with the experimental setup, the measured efficiency is about 96%.

V. CONCLUSION

A new single-phase nine-level MLI topology has been proposed in this paper. The proposed nine-level boost inverter topology has been based on switched capacitors with a reduced number of switches. A detailed comparative study highlights the proposed topology potential in terms of reduced requirements of components for the same number of voltage levels. The cost comparison supplements the lower

price of the proposed topology with a single dc voltage source for nine-level and proves it to be cost-beneficial. The efficiency comparison also gives the additional edge of the proposed topology compare to other topologies. The reduction in the number of components, cost, and higher efficiency makes the proposed topology suitable for low and medium voltage applications. The workability of the proposed topology has been proved by the different results with various loading conditions. The different simulation and hardware results verify the improved performance of the proposed topology.

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