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A Single-Event Burnout Hardened Super-Junction Trench SOI LDMOS with Additional Hole Leakage Paths

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Abstract: In this paper, a novel super-junction trench silicon-on-insulator laterally-diffused metal-oxide-semiconductor (SJT SOI LDMOS) power device with additional hole leakage paths to improve single-event burnout (SEB) performance under high liner energy transfer (LET) is proposed for the first time. The electrical characteristics and SEB performance of the proposed SJT SOI LDMOS are both enhanced effectively. The replacement of a lightly doped N drift region with a heavily doped P pillar and N pillar considerably improves the tradeoff between breakdown voltage (BV_{DS}) and specific on-resistance ($R_{on,sp}$). Compared with the conventional trench SOI LDMOS (CT SOI LDMOS), the static figures of merit (FOM, ${BV_{DS}}^2/R_{on,sp}$) of the SJT SOI LDMOS increases by 239%. The SEB performance of the SJT SOI LDMOS is significantly improved as the holes induced by the heavy ion can be quickly absorbed to the trench source metal through the heavily doped P+ region and P buried region rather than the base resistor of the parasitic bipolar junction transistor (BJT). The SEB threshold voltage (V_{SEB}) of the CT SOI LDMOS is 58 V (39% of the BV_{DS}) and that of the SJT SOI LDMOS is up to 173 V (87% of the BV_{DS}) at high LET of 1 pC/μm.

Keywords: additional hole leakage paths; sensitive region; single-event burnout (SEB); SOI LDMOS; super-junction; trench source

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1. Introduction

As essential components of power switching systems, power MOSFETs require surviving from the energetic particle incidence in a space radiation environment [1–3]. It is usually ions with significant linear energy transfer (LET) that produce enough charge injection to cause destructive single-event burnout (SEB) which will degrade the reliability of satellites [4–6]. SEB is attributed to a feedback mechanism that, once the parasitic bipolar junction transistor (BJT) is turned on, when a heavy ion strikes at the device in the OFF state, the ensuing high currents can cause catastrophic damage [7,8].

A large number of SEB hardening solutions in a power vertical double-diffused metal-oxide-semiconductor (VDMOS) have been extensively proposed, including adding a buffer layer [9], P+ plug enlargement [10], carrier lifetime reduction [11], Schottky diode source [12], and high-k dielectric materials for gate oxide [13]. Traditional VDMOS devices suffer from high gate charge and high switching losses with the increase of switching frequencies, failing to satisfy the requirements for space power electronics systems to operate at a higher switching frequency. With the rapid development of the silicon-on-insulator (SOI) technology, SOI LDMOS devices have been widely applied in various power ICs for power conversion owing to prominent isolation, low parasitic capacitances, high switching speed, and ideal compatibility with advanced very-large-scale integration (VLSI) technologies [14]. However, very limited studies focused on the SEB effect and mitigation techniques of the SOI LDMOS devices. Shea and Shen [15] investigated the SEB and single-event gate rupture (SEGR) effects in 150 V SOI LDMOS for radiation hardness both experimentally and using a Sentaurus simulator. Wang et al. [8] researched the SEB

failure mechanism of a 60 V radiation-hardened SOI LDMOS, and the results showed that the action of the parasitic BJT is the key to SEB tolerance of the device. Shu et al. [16] studied the SEB in SOI LDMOS by pulsed laser irradiation, but the results were not directly correlated with the SEB induced by heavy ions. Moreover, SOI LDMOS devices based on surface conduction are susceptible to permanent damage when exposed to energetic heavy ions. Therefore, it is essential to design a SEB-hardened SOI LDMOS power device to meet the requirements for applications in the extreme environment.

In addition, the electrical properties of the existing radiation- hardened MOSFET devices are worse than that of the common commercial MOSFET devices, no longer meeting the demand for power systems in the space radiation environment. As the most important electrical characteristics, breakdown voltage (BV_{DS}) and specific on-resistance ($R_{on,sp}$) have a contradiction relation which limits the performance improvement of the MOSFET [17]. Trench and super-junction technologies can effectively relieve the contradiction relation between BV_{DS} and $R_{on,sp}$. The planar MOSFET is not area efficient, and its $R_{on,sp}$ is physically limited due to the confinement of drift region near the surface. The trench technology is desirable to improve the tradeoff between BV_{DS} and $R_{on,sp}$ by spreading the current into the bulk of the device and enhancing the reduced surface field (RESURF) [18–20]. Super-junction technology is also widely adopted to enhance the bulk electric field of the drift region by charge compensation, breaking through the relationship between BV_{DS} and $R_{on,sp}$ [21–23]. It is worth noting that the super-junction MOSFET devices have better SEB tolerance because of effective modulation of the two-dimensional electric field by P and N pillars [24].

In this paper, a novel super-junction trench SOI LDMOS (SJT SOI LDMOS) with additional hole leakage paths to improve SEB performance is proposed. The electrical characteristics and SEB performances of the CT SOI LDMOS and the proposed SJT SOI LDMOS are studied through 2D simulations. As an ion's strike position can affect the SEB performance, sensitive regions for SEB in the SJT SOI LDMOS and CT SOI LDMOS are analyzed. The SEB threshold voltage (V_{SEB}) of the SJT SOI LDMOS and CT SOI LDMOS after heavy ions with a high LET of 1 pC/μm (96 MeV·cm^2/mg) are extracted, and the influence of different LETs on V_{SEB} is explored. Time evolutions of the distributions of the hole current density and electric field are discussed to study the turn-on and run-away of the parasitic BJT, exploring the SEB hardening mechanism of the proposed SJT SOI LDMOS in detail.

2. Device Structure and Simulation Setup

The cross-section schematic of the SJT SOI LDMOS and CT SOI LDMOS are shown in Figure 1a,b, respectively. The thickness of the buried oxide (BOX) layer and the drift region are 1.26 μm and 0.88 μm, respectively. In the SJT SOI LDMOS, the drift region is formed by a heavily doped N pillar and P pillar, replacing the lightly doped N drift region in the CT SOI LDMOS. The thickness and doping concentration of the N pillar and P pillar are optimized to achieve charge balance, improving the tradeoff of the BV_{DS} and $R_{on,sp}$. The N pillar concentration is 7×10^{16} cm^{-3} with a thickness of 0.46 μm, and the P pillar concentration is 6×10^{16} cm^{-3} with a thickness of 0.42 μm. The trench gate is introduced into the drift region of which only one side forms the source and P well region. On the other side of the trench gate, the heavily doped P buried region is formed by Boron implantation and diffused until the surface of the BOX layer, and the trench source depth of the P buried region is 0.7 μm. With a P buried region integrated between two trenches, an additional 3.8% of area is needed compared with the CT SOI LDMOS. In addition, a heavily doped P+ region is inserted beside the source region, covering the partial P well region without impacting the threshold voltage. The depth of trench source metal between the source and P+ region is 0.13 μm. The P buried region and P+ region present low-resistance paths for the collection of holes generated by heavy ions, reducing the potential in the P well region. The shallow trench isolation (STI) region is inserted into the drift region near the drain region, effectively modulating the electric field distribution and preventing the high electric

field from gathering near the drain. Table 1 details the key structure parameters used for design simulation.

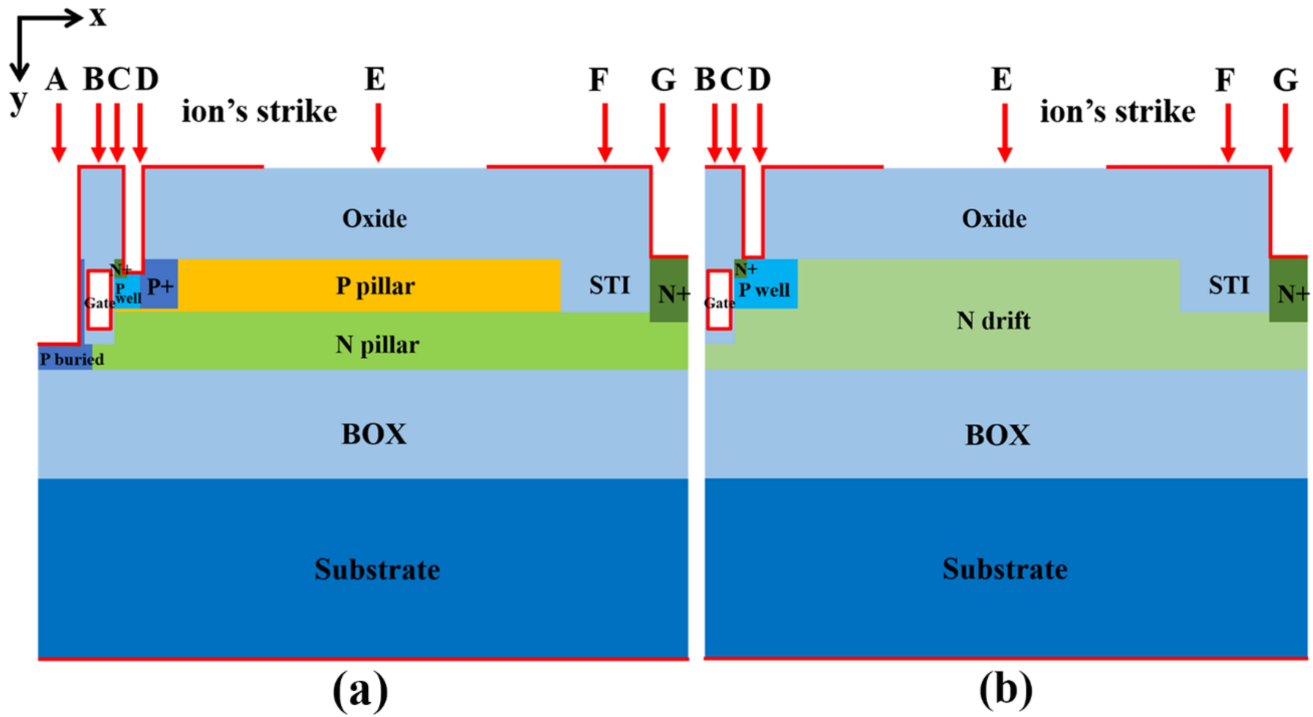

Figure 1. The cross-section schematic of (**a**) the SJT SOI LDMOS and (**b**) the CT SOI LDMOS.

Table 1. Device parameters for simulations.

Device Parameter	CT SOI LDMOS	SJT SOI LDMOS
Cell pitch	10 μm	10.4 μm
Trench width	0.15 μm	0.15 μm
Trench depth	0.48 μm	0.48 μm
Gate oxide wall thickness	30 nm	30 nm
Gate oxide bottom thickness	0.1 μm	0.1 μm
P pillar thickness	-	0.42 μm
N pillar thickness	-	0.46 μm
Buried oxide (BOX) layer thickness	1.26 μm	1.26 μm
P pillar doping	-	6×10^{16} cm^{-3}
N pillar doping	-	7×10^{16} cm^{-3}
N drift region doping	1.7×10^{16} cm^{-3}	-
P+ region doping	-	4×10^{17} cm^{-3}
P+ region width	-	0.3 μm
P+ region depth	-	0.4 μm
P+ region trench source depth	-	0.13 μm
P buried region doping	-	4×10^{17} cm^{-3}
P buried region depth	-	0.88 μm
P buried region width	-	0.43 μm
P buried region trench source depth	-	0.7 μm
N+ source doping	1.8×10^{18} cm^{-3}	1.8×10^{18} cm^{-3}
P well region doping	2×10^{17} cm^{-3}	2×10^{17} cm^{-3}
N+ drain doping	6×10^{17} cm^{-3}	6×10^{17} cm^{-3}
Substrate doping	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}

As shown in Figure 2a, the proposed SJT SOI LDMOS device is fabricated by starting with 1 µm oxide deposited on the heavily doped substrate. Then, the N pillar and P pillar are formed by depositing (Figure 2b). The trench is formed by ion etching, and the thick oxide is deposited on the bottom of the trench (Figure 2c). The gate oxide wall is thermally grown on the trench surface, and the polysilicon is deposited to fill the trench (Figure 2d). Subsequently, the p+ and n+ ions are implanted for the source region, drain region, P+ region, and P buried region (Figure 2e). The STI region is formed by etching and depositing, the trench sources are formed by etching, and the device fabrication is then completed by the deposition of the metal layer (Figure 2f). The fabrication process of the CT SOI LDMOS is similar to that of the SJT SOI LDMOS. There are no redundant and complicated manufacturing processes; thus, the cost for fabricating the proposed device is low.

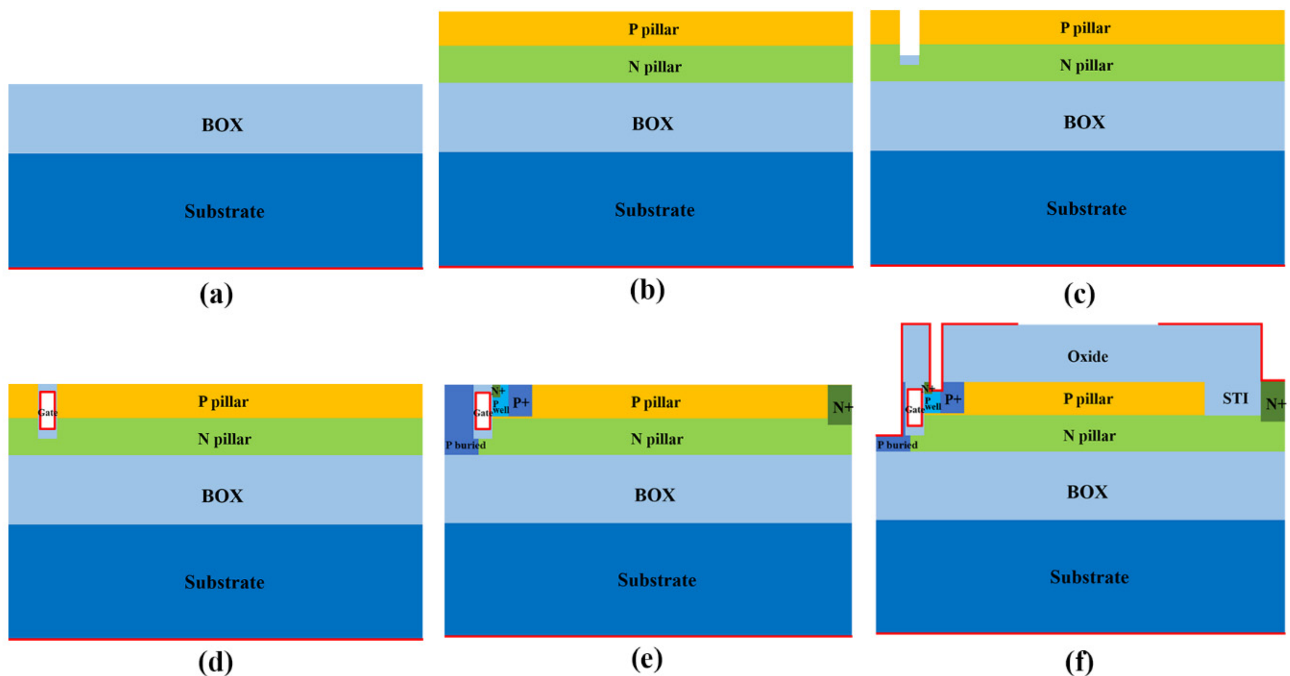

Figure 2. Fabrication process steps for the SJT SOI LDMOS, (**a**) deposit oxide on the substrate; (**b**) N pillar and P pillar are formed by depositing; (**c**) trench is formed by ion etching and the thick oxide is deposited on the bottom of the trench; (**d**) gate oxide wall is thermally grown and polysilicon is deposited; (**e**) the p+ and n+ ions are implanted; (**f**) STI region is formed by etching and depositing and the metal is deposited.

In this paper, the basic electrical characteristics and SEB performance of the SJT SOI LDMOS and CT SOI LDMOS are studied. In the simulations, the physics models employed are recombination models including Auger recombination, Shockley–Read–Hall recombination; carrier statistic models, including Fermi–Dirac statistics and bandgap narrowing models; mobility models considering the effects of carrier concentration, including field-dependent mobility (FLDMOB), concentration dependent mobility (CONMOB); and an impact ionization model accounts for ionization rates [25].

The SEB performances of the SJT SOI LDMOS and CT SOI LDMOS are investigated using the built-in heavy ion radiation model in Sentaurus TCAD simulator. The TCAD models are validated against basic measured device parameters before being used for single event simulation [15]. Good agreement has been reported between 2D and 3D TCAD in predicting SEB thresholds [5]. The coordinates used for defining a heavy ion's track are expressed as the x- and y- directions shown in Figure 1. Heavy ions are assumed to penetrate vertically through the surface of silicon layer into the BOX layer. A function allowing generation of electron–hole pairs to remain constant in a vertical direction in a specific area of the device is defined to simulate the ionizing impact, as shown in Equation (1) [26]:

For $y_0 \leq y \leq y_1$:

$$rate\ (x, y) = \frac{\text{LET}}{q\pi\omega_0 T_C} \exp\left(-\frac{(x - x_0)^2}{\omega_0{}^2}\right) \times \exp\left(-\frac{(t - T_0)^2}{T_C{}^2}\right) \tag{1}$$

where ω_0 is the ion track radius, T_C is the temporal Gaussian function width, T_0 is the initial charge generation time, which are set to 0.05 µm, 2 ps, and 0.1 ps, respectively. The linear energy transfer (LET) is defined as the charge deposited per unit of track length and given in pC/µm [27]. As the LET is unchanged in a certain range, constant LET along the ionizing track is chosen to facilitate the research [28]. The distribution of the generated electron–hole pair concentration can be calculated according to the LET, track radius, and ion penetrating range. No SEB occurs when hit by an ion with larger LET, and even less for ions with smaller LET values. A large LET value of 1 pC/µm (96 MeV·cm^2/mg) and a range of 2.14 µm to penetrate through the device are selected to simulate the worst possible ionizing track condition that triggers SEB. The corresponding parameters for SEB simulations are listed in Table 2.

Table 2. Parameters for SEB simulations.

Parameter	Value
Track radius ω_0	0.05 µm
Temporal Gaussian function width T_c	2 ps
Initial charge generation time T_0	0.1 ps
Track length l_0	2.14 µm
Linear energy transfer (LET)	1 pC/µm (96 MeV·cm^2/mg)

In the SEB test, the devices are in the OFF-state with a gate voltage of 0 V before irradiation. To assess the SEB sensitivity, SEB threshold voltage (V_{SEB}) is defined as the critical applied drain voltage at which the burnout occurs for a given LET value. It is verified that the ion strike position can affect the SEB performance [29]. Thus, seven typical strike positions along the device structure are selected to investigate the most sensitive region for SEB, as shown in Figure 1: the P buried region (Position A, x = −0.23 µm), the middle of the trench gate (Position B, x = 0.09 µm), the source region (Position C, x = 0.22 µm), the P well/P+ region (Position D, x = 0.4 µm), the drift region (Position E, x = 5 µm), the STI region (Position F, x = 8.5 µm), and the drain region (Position G, x = 9.8 µm). To compare the SEB performance, the V_{SEB} of the devices after heavy ions with LET of 1 pC/µm vertically striking at different positions in both CT SOI LDMOS and SJT SOI LDMOS are extracted. In order to investigate the influence of various LETs on V_{SEB} for the SJT SOI LDMOS, heavy ions with discrete LETs strike at different positions, respectively. In addition, time evolutions of the distributions of the hole current density and electric field are studied to understand the SEB triggering mechanism.

3. Simulation Results and Discussion

3.1. Basic Electrical Characteristics

Figures 3–5 show the breakdown, transfer, and I–V characteristics of the CT SOI LDMOS and SJT SOI LDMOS, respectively. Compared with the CT SOI LDMOS, the basic electrical characteristics of the SJT SOI LDMOS proposed in our work are significantly improved.

As Figure 3a shows, the BV_{DS} of the CT SOI LDMOS and SJT SOI LDMOS are 150 V and 198 V, respectively, increasing by 32%. It is attributed to the replacement of lightly-doped N drift region in the CT SOI LDMOS with the P pillar and N pillar in the SJT SOI LDMOS, making depletion region extend in two dimensions. Therefore, instead of obtaining a triangular electric field profile with a maximum field at the P well and N drift junction like the CT SOI LDMOS, a rectangular electric field profile with a uniform field can be achieved in the SJT SOI LDMOS (as shown in Figure 3b). In addition, the leakage

current of the SJT SOI LDMOS is higher than that of the CT SOI LDMOS because the barrier height of the P buried/N pillar junction is higher than that of the P well/N drift junction.

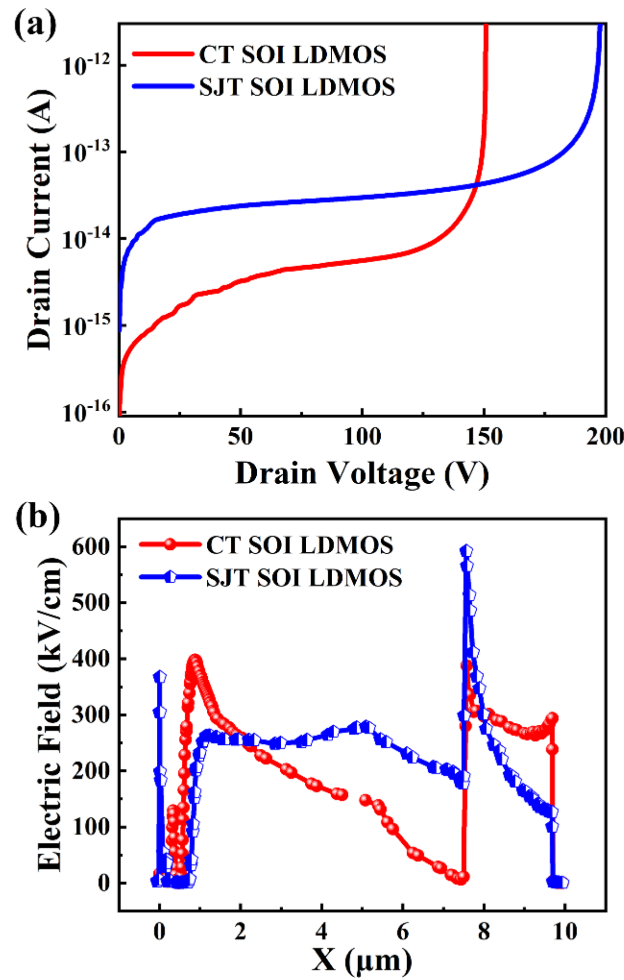

Figure 3. (**a**) Breakdown characteristics, and (**b**) electric field distributions of the CT SOI LDMOS and SJT SOI LDMOS.

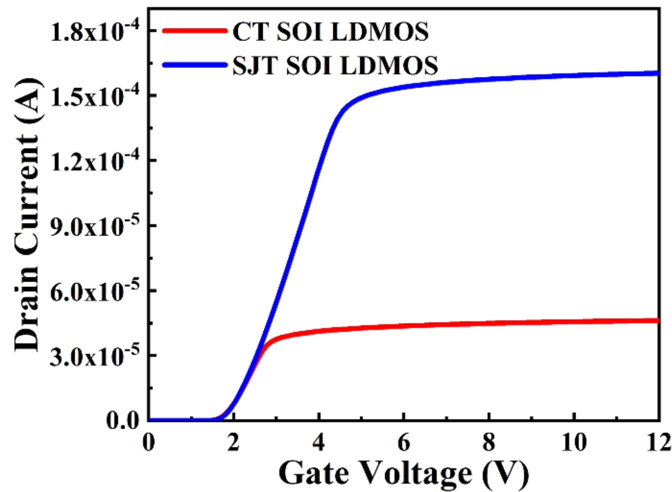

Figure 4. Transfer characteristics of the CT SOI LDMOS and SJT SOI LDMOS.

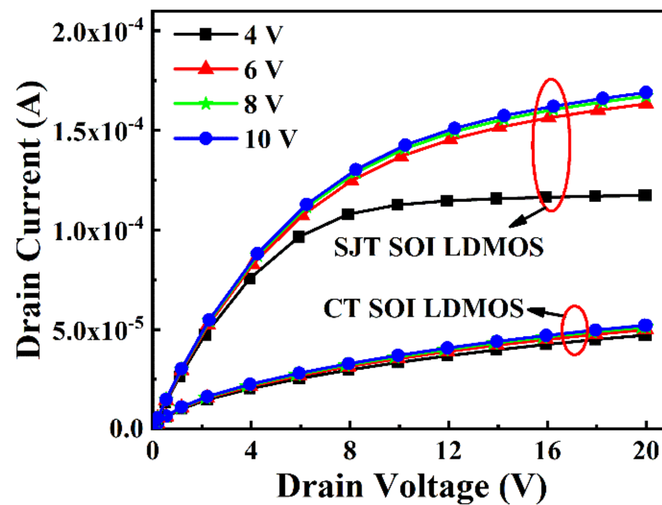

Figure 5. I–V characteristic curves of the CT SOI LDMOS and SJT SOI LDMOS.

It can be seen from Figure 4 that the threshold voltages of the SJT SOI LDMOS and CT SOI LDMOS are almost the same. Furthermore, the SJT SOI LDMOS exhibits a higher drive current because of the smaller resistance of the drift region, which is four times higher than that of the CT SOI LDMOS.

Figure 5 shows the I–V characteristic curves of the CT SOI LDMOS and SJT SOI LDMOS for V_{GS} = 4 V, 6 V, 8 V, and 10 V. It is shown that the SJT SOI LDMOS exhibits better current handling capability than CT SOI LDMOS because a high doping concentration of the drift region reduces the total resistance of the device. The specific on-state resistance ($R_{on,sp}$) of the CT SOI LDMOS and SJT SOI LDMOS are 38 mΩ·cm^2 and 74 mΩ·cm^2, respectively. Actually, the SJT SOI LDMOS has a 239% increment of the static FOM ($BV_{DS}{}^2/R_{on,sp}$) compared with the CT SOI LDMOS.

3.2. Single-Event Burnout Performance

The changes of device structure can affect the most sensitive position for SEB [30]; therefore, seven typical ions' strike positions are chosen to investigate the most sensitive position of the SJT SOI LDMOS and CT SOI LDMOS. In the SEB simulations, the devices are biased in the OFF-state and the applied V_{DS} increases from zero to the V_{SEB}, which are extracted to evaluate the SEB sensitivities. Table 3 shows the V_{SEB} of the CT SOI LDMOS and SJT SOI LDMOS after heavy ions with LET of 1 pC/µm vertically striking at different positions. V_{SEB} is the index to estimate the device's SEB performance [7], and the device with lower V_{SEB} is considered to be more vulnerable to SEB failure. Although the V_{SEB} of other positions in the CT SOI LDMOS are not low, that of the drift region (Position E) is only 58 V (39% of the BV_{DS}), whereas the minimum V_{SEB} of the SJT SOI LDMOS when heavy ions strike at the STI region (Position F) is still up to 173 V (87% of the BV_{DS}). Therefore, we conclude that the SJT SOI LDMOS has a remarkable improvement of SEB performance compared with the CT SOI LDMOS. Furthermore, the most sensitive region for SEB in the CT SOI LDMOS is the drift region (Position E), whereas that in the SJT SOI LDMOS is the STI region (Position F).

Figure 6 shows the evolutions of drain current versus time after heavy ions with LET of 1 pC/µm strike at different positions of the CT SOI LDMOS and SJT SOI LDMOS. The initial transient currents keep close to each other when time is less than 40 ps. Then, a different trend of the transient drain current can be seen at 200 ps, including an upward trend or a descending trend. SEB occurrence is indicated by the drain current remaining a stable high value at 10 ns. On the contrary, the induced drain current reduces to a very low level over time, which indicates no burnout. Figure 6 shows that SEB triggers when heavy ions strike at the drift region (Position E), whereas no SEB occurs at other positions of the CT SOI LDMOS at V_{DS} of 58 V, indicating that the most sensitive position of the CT

SOI LDMOS is the drift region. Similarly, it can be obtained that the STI region (Position F) is the most sensitive region of the SJT SOI LDMOS, consistent with the results of Table 3. In addition, the SEB triggering mechanism is related to the activation of the parasitic BJT and impact ionization in the high field region [31,32]. This may because changes of device structure affect the distribution of the high field region which can effectively accelerate the holes and electrons to ionize more carriers, causing the activation of the parasitic BJT and triggering SEB. Maximum SEB currents of the CT SOI LDMOS and SJT SOI LDMOS are about 0.34 A and 1.73 A, respectively, which is mainly determined by the doping concentration of the drift region and the distribution of the electric field.

Table 3. The V_{SEB} at different strike positions.

Strike Positions	CT SOI LDMOS (V)	SJT SOI LDMOS (V)
Position A	-	192
Position B	132	189
Position C	129	183
Position D	142	176
Position E	58	186
Position F	129	173
Position G	129	178

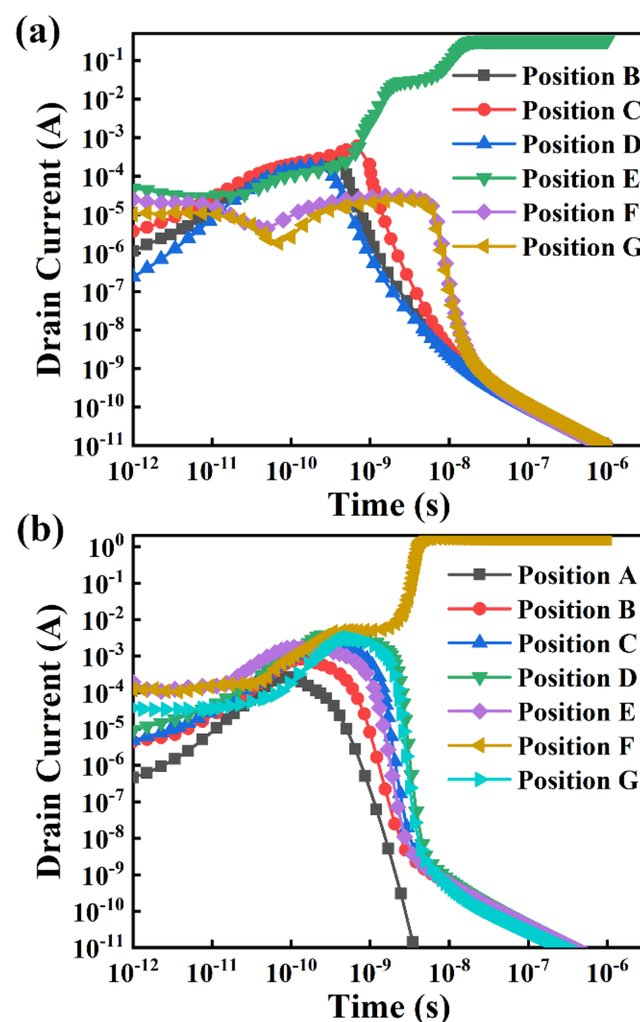

Figure 6. Drain current versus time after heavy ions with LET of 1 pC/μm strike at different positions of (**a**) the CT SOI LDMOS at V_{DS} = 58 V and (**b**) the SJT SOI LDMOS at V_{DS} = 173 V.

The number of electron–hole pairs generated by heavy ions is proportional to the LET [33], affecting the time evolution of the drain current induced by heavy ions, which is related to V_{SEB}. Thus, in order to investigate the influence of various LETs on SEB tolerance of the device, the V_{SEB} are extracted after heavy ions with different LETs strikes at different positions of the SJT SOI LDMOS, as shown in Figure 7. The results indicate that the V_{SEB} increases with decreasing LET. The SJT SOI LDMOS can survive at V_{DS} of 190 V (96% of the BV_{DS}) for heavy ions with LET of 0.1 pC/μm incidence. Furthermore, the V_{SEB} when heavy ions strike at the most sensitive region (Position F) increases the most, increasing from 173 V to 190 V.

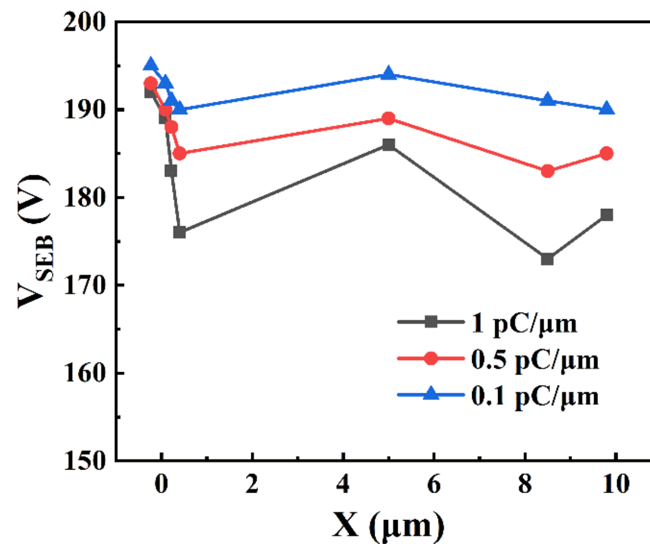

Figure 7. The V_{SEB} for heavy ions with different LETs vertically striking at different positions along the SJT SOI LDMOS device structure.

As SEB occurrence is related to the amplification bipolar effect and impact ionization in the high field region, time evolutions of the distributions of hole current density and electric field after heavy ion incidence are investigated to understand the SEB failure mechanism. Figure 8 reveals the distribution variations of hole current density with time in the CT SOI LDMOS and SJT SOI LDMOS after heavy ions with LET of 1 pC/μm strike at the drift region (Position E) when V_{DS} is set as 58 V. At a time of 1 ps, the number of electron–hole pairs generated by heavy ion is small and hole currents are relatively concentrated around the ion striking path in the SJT SOI LDMOS and CT SOI LDMOS. Then, more and more electron–hole pairs generated by impact ionization under the electrical field. At a time of 0.5 ns, in the CT SOI LDMOS, the holes spread to most of the drift region and the adjacent area of the source, which mainly pass through the P well region to the N+ source contact, leading to the activation of the parasitic BJT. However, in the SJT SOI LDMOS, the heavily doped P+ region and P buried region in direct contact with the trench source metal provide the low resistance paths for holes generated by heavy ions to leak off, effectively reducing the hole current density flowing into the P well region below the source and suppressing the triggering of the parasitic BJT [34]. The vertical electric field caused by the N pillar and P pillar drives most of the hole current to flow toward the P pillar and then leaking off toward the P+ region trench source. Then, the hole current density in the CT SOI LDMOS keeps increasing, and the holes will obtain enough energy to impact more electron–hole pairs as they flow to the high field region between the gate and the drain [35], eventually resulting in SEB, as shown in Figure 8a. On the contrary, at a time of 10 ns, almost all of the holes leak off toward the trench source contact through the P+ region and P buried region in time, and the current density decreases to a very low level in the SJT SOI LDMOS, the parasitic BJT failing to reach the opening threshold, as shown in Figure 8b. We can see that SEB occurs in the CT SOI LDMOS rather than the SJT SOI LDMOS, indicating that

the SJT SOI LDMOS can well suppress the operating of the parasitic BJT and improve SEB performance in the case of heavy ion incidence.

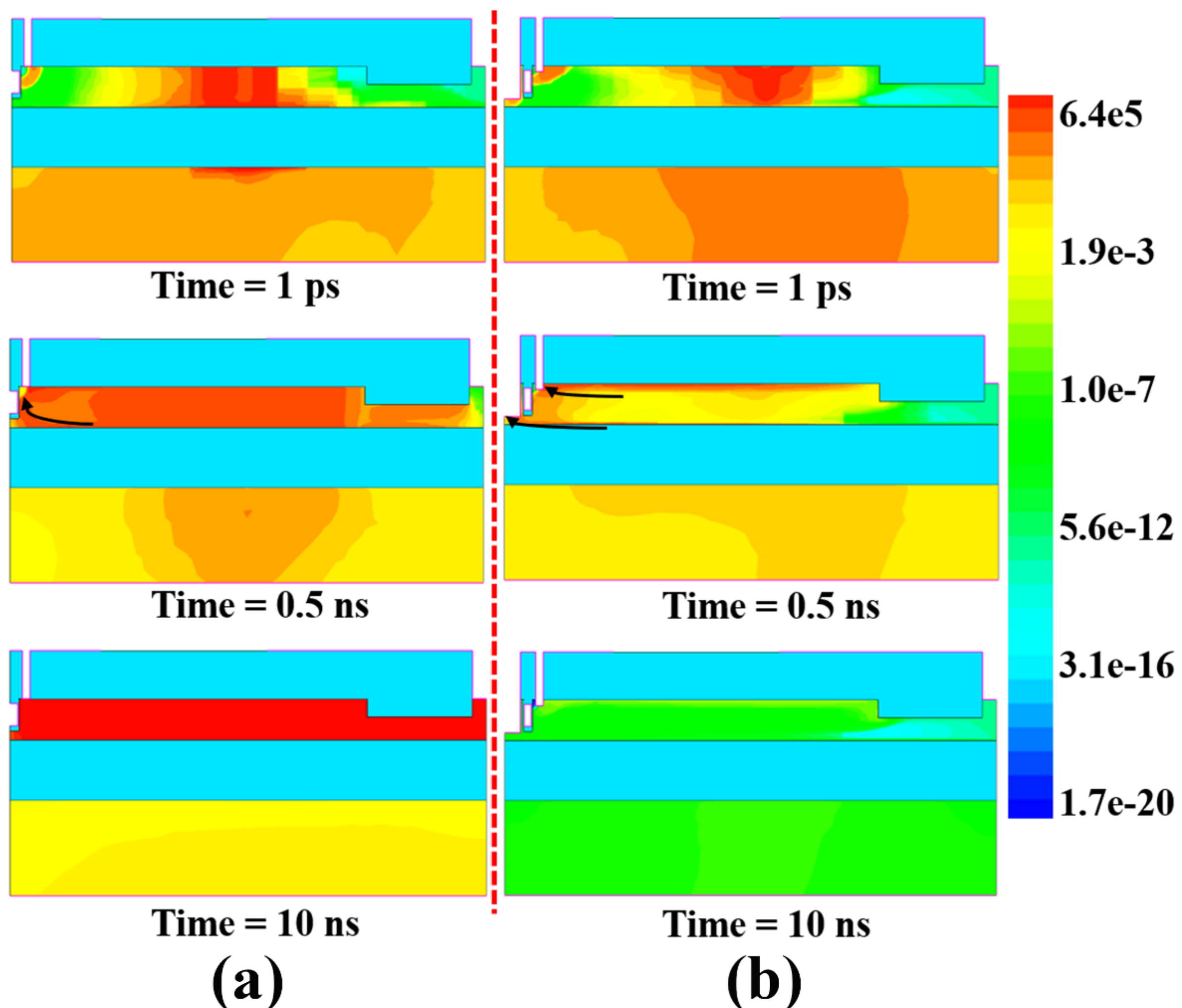

Figure 8. The distribution variations of hole current density with time in (**a**) the CT SOI LDMOS and (**b**) the SJT SOI LDMOS after heavy ions with LET of 1 pC/μm strike at Position E when V_{DS} is set as 58 V.

Figure 9 exhibits the electric field distributions of the CT SOI LDMOS and SJT SOI LDMOS at different times after heavy ions with LET of 1 pC/μm strike at Position E when V_{DS} is set as 58 V. At the time of 1 ps, a partial depletion region is formed near the striking path in the drift region due to a large number of electron–hole pairs generated by heavy ion incidence. Furthermore, the electric field peaks are located at the interface of the P well/drift region in the CT SOI LDMOS and the interface of P pillar/STI region in the SJT SOI LDMOS, respectively. As the depletion region keeps collapsing, the electric field peaks inside the SJT SOI LDMOS and CT SOI LDMOS are gradually transferred to the left of the drift region between 1 ps and 0.5 ns. At a time of 10 ns, the electric field peaks are transferred to the source region in the CT SOI LDMOS so that the avalanche multiplication effect is further enhanced, leading to the triggering of the parasitic BJT and the failure of the electric field reconstruction, as shown in Figure 9a, whereas the electric field in the SJT SOI LDMOS is reconstructed and restored to the initial distribution state gradually, attributing to quick leakage off of the generated holes through the P+ region and P buried region. The parasitic BJT fails to reach the opening threshold, and no SEB occurs in the SJT SOI LDMOS, as shown in Figure 9b. In addition, as the impact ionization coefficient which is related to SEB sensitivity is exponentially related to the electric field, reducing the electric field peak

can greatly improve the SEB performance. At time of 0.5 ns, the peak of the electric field in the CT SOI LDMOS reaches 373 kV/cm, whereas that of the SJT SOI LDMOS reduces to 213 kV/cm, which represents a decrease of about 43%, so that the ionization coefficient is relatively low and SEB survivability increases significantly, as shown in Figure 9c. The above changes are consistent with the evolution of the hole current density distribution in Figure 8a,b.

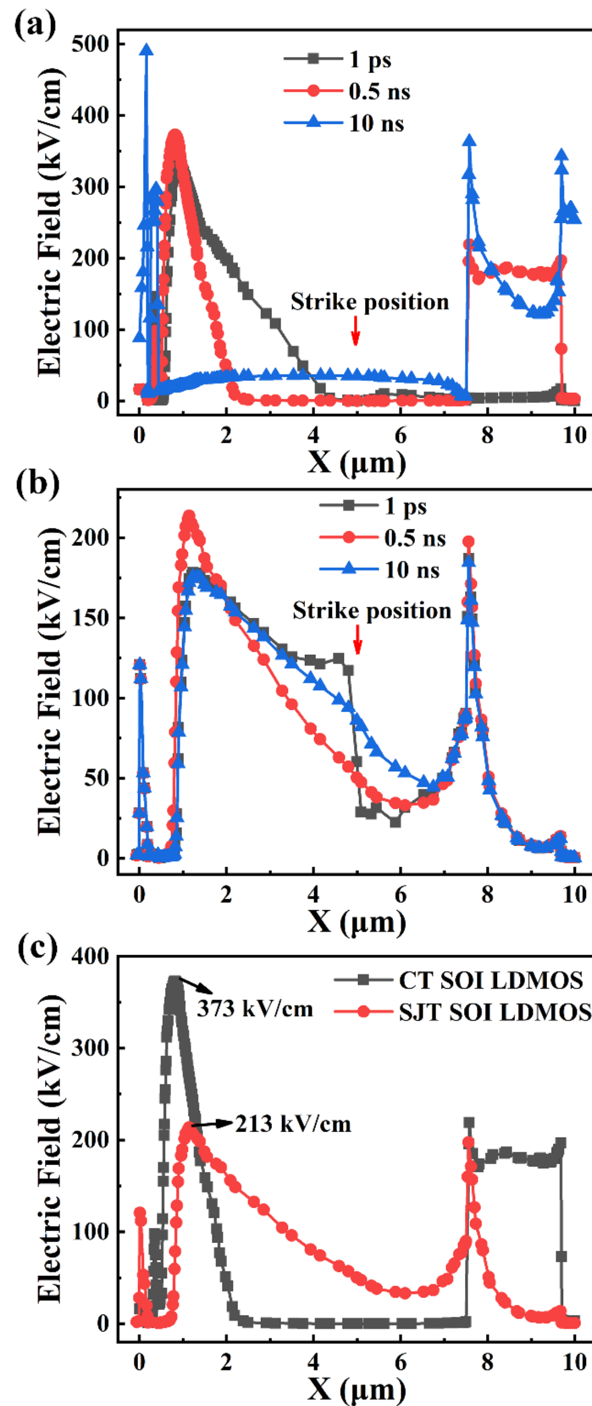

Figure 9. The electric field distributions of (**a**) the CT SOI LDMOS and (**b**) the SJT SOI LDMOS at different times after heavy ions with LET of 1 pC/μm strike at Position E when V_{DS} is set as 58 V, (**c**) the electric field distributions of the SJT SOI LDMOS and CT SOI LDMOS at time of 0.5 ns after heavy ion incidence.

The SEB performance is also improved when heavy ions strike at other positions of the SJT SOI LDMOS, since most of the hole currents flow into the trench source contact through the heavily doped P+ region and P buried region, as shown in Figure 10. The most sensitive position for SEB in the SJT SOI LDMOS is Position F. This may be because no conductive paths are formed in the oxide layer (STI region) so that a large number of generated electron–hole pairs accumulate on the oxide surface and move toward the source contact under the action of the electric field, resulting in a narrow channel for carrier movement. Therefore, a high current density is formed under the STI region near the drain, which can induce more impact ionization and in turn strengthen the parasitic BJT operation [36], resulting in catastrophic SEB failure, as shown in Figure 10.

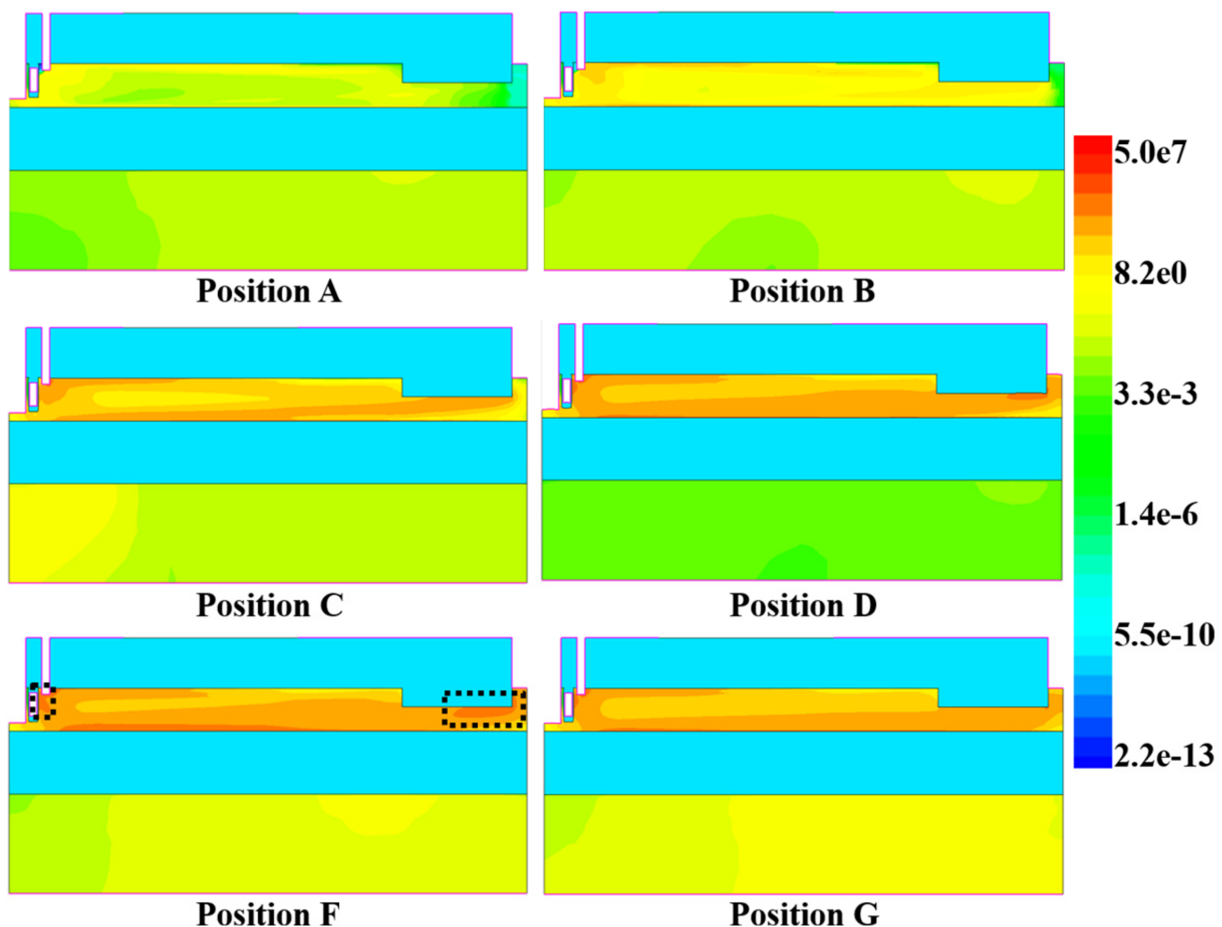

Figure 10. The hole current density distributions of the SJT SOI LDMOS at 0.5 ns after heavy ions with LET of 1 pC/µm strike at Position A, Position B, Position C, Position D, Position F, and Position G when V_{DS} is set as 173 V.

4. Conclusions

Power MOSFET devices in space systems are subject to be permanently damaged by the SEB effect. This work presents a novel SJT SOI LDMOS with additional hole leakage paths intended to be SEB resistant in harsh-environment space applications. The electrical characteristics and SEB performances of the SJT SOI LDMOS and CT SOI LDMOS are investigated by simulation. The results demonstrate that the SJT SOI LDMOS can significantly improve SEB tolerance while maintaining great electrical performances. Compared with the CT SOI LDMOS, the static FOM ($BV_{DS}{}^2/R_{on,sp}$) of the SJT SOI LDMOS increases by 239%, and the SJT SOI LDMOS exhibits a higher drive current because of smaller resistance of the drift region. A sensitive region for SEB is analyzed by heavy ions with LET of 1 pC/µm striking at different positions and the most sensitive region of the CT SOI LDMOS and SJT

SOI LDMOS are the drift region and STI region, respectively. SEB tolerance of the SJT SOI LDMOS is obviously improved since the holes can be quickly attracted to trench source contact through the heavily doped P+ region and P buried region to weaken the effect of parasitic BJT, suppressing the premature burnout. The V_{SEB} of the SJT SOI LDMOS is 173 V even for a highly-energetic ion with LET of 1 pC/µm, increased to 87% of the BV_{DS}. The influence of different LETs on V_{SEB} is explored, and the SJT SOI LDMOS is shown to be SEB resistant at the high V_{DS} of 190 V (96% of the BV_{DS}) for a LET of 0.1 pC/µm.

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