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A single-event transient hardened LDO regulator with built-in filter

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Abstract: A single-event transient (SET) hardened LDO using novel structure is proposed to enhance the single-event effect tolerance. The novel LDO with built-in filter can mitigate the response of the sensitive nodes of circuit. If the SET pulse current flows through the sensitive nodes, the maximum variation of the output voltage is only 15.5 mV. In addition, the transient performance is slightly dropped back as a tradeoff for the built-in filter. When the workload changes transiently between 100 µA and 100 mA in 100 ns, the undershoot is 28.4 mV and the overshoot is nearly 20 mV with imperceptible peak.

Keywords: SET, built-in filter, hardened LDO

Classification: Integrated circuits

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1 Introduction

As the rapid development of space exploration, the ICs which are widely used in artificial satellites, space shuttle etc. need to be hardened for working in radiation environment. Space radiation may cause soft errors which change the states of the circuits and don't damage the devices in circuits, for example SEU (single-event upset) and SET. Generally, the SEUs cause the data upset in logic circuits, and SETs cause unstable states in mixed-signal circuits. Researches on SET hardening can be implemented in process level, device level, circuit level and system level. The process and device with strong SET robustness usually need special materials or technology which maybe expensive. Therefore, designing strong topological structure in circuit level for SET hardening is efficient and practical.

There are among of works on circuits SET hardening. In common CMOS process, the radiation hardened by design (RHBD) layout methods have been proposed to enhance the SET tolerance [1, 2, 3, 4, 5, 6, 7]. Charge sharing techniques and SETs model are used to mitigate SET effects [8, 9]. In addition, the power management unit (LDO) that plays an important role in ICs also needs to be hardened [10, 11, 12]. According to the previous researches, the RHBD for LDO need to consider the SET harden methods for layout, amplifier, reference circuit etc. There are numerous SET sensitive points especially in amplifier and reference [8, 9], and it's hard to be hardened. Therefore, the hardened LDO should be a simply topological structure and enough robustness.

In this letter, a novel structure LDO with built-in filter has been proposed. The LDO without amplifier and reference implements a simply structure, and mitigates the SET effect on circuit.

2 Design and SET sensitivity analysis

SETs are a type of radiation effects coming from a single energetic particle such as a heavy ions striking semiconductor material. Particle striking is random and may happen at any location in semiconductor circuits. When a particle strikes the lattice structure of a semiconductor material, its energy is transferred to the lattice, and

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amount of free electron-hole pairs are ionized. The ionized electron-hole pairs may recombine before they affect circuits if the ion passes through the bulk. However, the sensitive part of semiconductor material is the p-n junctions, for example the drain–substrate of an nMOS (or pMOS) transistor which is reverse-biased. Under the electric field, the electron-hole pairs will be separated and collected that may change the voltage level or logic state.

The parasitic p-n junction under CMOS device is paramount to describing the response of the circuit to heavy ion strikes. When a particle strikes an nMOS transistor, a mount of electron hole pairs are generated by ionization. If the hit point is the source of the transistor, the electron hole pairs may recombine or be transferred by GND network (or VDD network in pMOS). If the striking location is the drain of the transistor, a part of the electron-hole pairs will be separated by the electric field before recombination. That is shown as the Fig. 1.

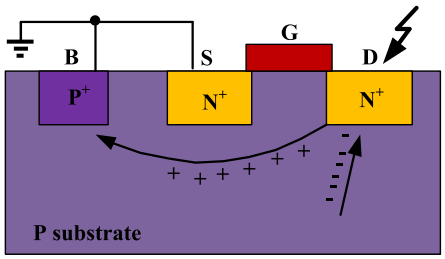

Fig. 1. The electron-hole pairs are generated by ionization and separated by electric field.

According to the Fig. 1, the electrons are collected by the drain of nMOS, and holes are collected by the GND network. In this way, the transport of the carrier forms current pulse by drift and diffusion that is shown as the Fig. 2. According to the Fig. 2, the peak of the current pulse may reach hundreds of microampere. The transient response of the source is mitigated by GND network. However, the voltage of the drain will change transiently. Therefore, the sensitive node of transistor is the drain terminal.

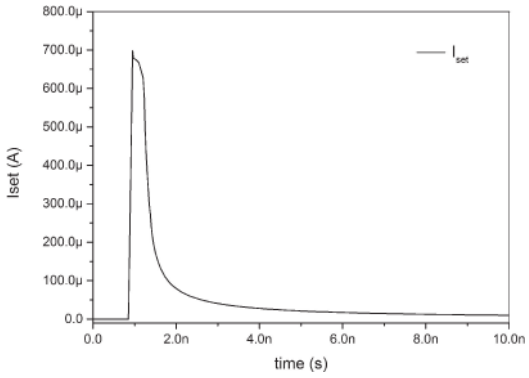

Fig. 2. The current pulse introduced by a high energy particle striking CMOS device.

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The structure of the proposed LDO: As we discussed previously, the RHBD for LDO should harden the drain terminal, simplify the topological structure and mitigate the effect of the current pulse. Basing on the characteristics of the RHBD for LDO, the typical LDO that generally includes error amplifier and reference generation circuit has too many sensitive nodes to space application. Therefore, we propose a simply LDO without reference voltage and error amplifier. The proposed LDO adopts feedback loop and feedforward loop to establish an equilibrium point that is shown in the Fig. 3a. The equilibrium point is the output voltage of the LDO. In this way, the error amplifier and reference can be removed which are generally sensitive to SET.

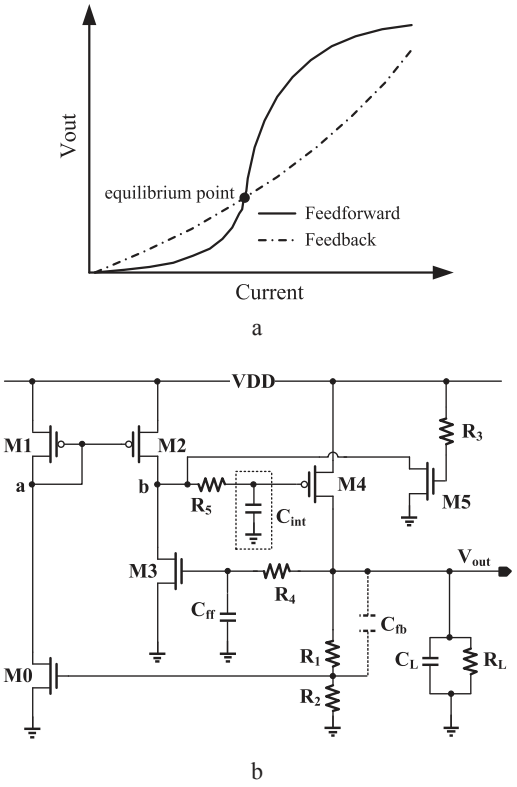

Fig. 3. a. The working principle of the proposed LDO; b. The schematic of the proposed LDO.

According to the Fig. 3b, the feedback loop is comprised of R_1, R_2, M0~M2, R_5 and C_{int}; and the feedforward loop includes R_4, C_{ff} and M3. The proposed LDO establish an equilibrium point by feedforward loop and feedback loop. When the output voltage deviate the equilibrium point, the feedback loop plays a dominated role in regulating output voltage. The role of the feedforward loop is establishing equilibrium point. Therefore, the feedforward loop should have a slower response speed and less sensitive to the variation of Vout than the feedback loop for a better transient response performance. The devices C_{ff} and C_4 are inserted in feedforward loop to filter the transient variation of the output voltage in some way.

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The transistors (M0~M2) work as a feedback transconductance that converts the feedback voltage to feedback current. The feedback current is compared with the feedforward current generated by the transistor M3. The startup circuit is composed of the transistor M5 and resistor R_3. In addition, C_L is the decoupling capacitor and R_L is the workload.

The output voltage can be expressed as the Eq. (1)

$$V_{out} = \frac{V_{th}(\sqrt{k_2 k_3} - 1)}{\sqrt{k_2 k_3} k_1 - 1} \tag{1}$$

In which,

$$k_1 = \frac{R_2}{R_1 + R_2}, \quad k_2 = \frac{(W/L)_{M2}}{(W/L)_{M1}}, \quad k_3 = \frac{(W/L)_{M0}}{(W/L)_{M3}}$$

The sensitive nodes hardening: The proposed LDO has more simple structure and fewer nodes than typical LDO. There are three main nodes in the proposed circuit which are a, b and V_{out}. The node 'a' is the drain of M1 and M0 which affect the feedback current through current mirror structure. The node 'b' is the intersection point of feedback and feedforward. The SET response of a high energy particle striking on 'a', can propagate through current mirror and reach 'b' node. Therefore, a SET mitigation filter should implement at 'b', which is comprised of R_5 and C_{int}. C_{int} is the integrated capacitor at the gate of the power MOSFET (M4). The node 'V_{out}' is the drain of power MOSFET and the output of the LDO. The output of LDO connects with large decoupling capacitor. Therefore, the node 'V_{out}' doesn't need extra protection. In addition, the capacitor C_{fb} works as a low impedance path for transient response.

3 Simulation results and evaluation

The space application requires the power supply unit not only working stably but also being tolerant to particles striking. Therefore, the performance of the proposed LDO can be divided into SET response and normal transient response. The performance of the proposed LDO is simulated in 0.18 µm CMOS technology.

The SET response of the proposed LDO: The current pulse generated by a particle striking the sensitive nodes may cause the output voltage deviating from the steady-state value. Inserting internal filter can mitigate SET affection and reduce the performance imperceptibly. The SET response of the proposed circuit is described as the Fig. 4.

The three nodes are struck by SET current pulse, and the responses of the output are shown respectively. According to the Fig. 4a, when the SET current pulse striking node 'a', the affection diffuses through the circuit and changes output voltage value. The peak-peak ΔV_{out} is 9.6 mV without inserting internal filter, 3.4 mV with internal filter. When striking node 'b', the peak-peak ΔV_{out} is 12.3 mV and 1.3 mV respectively. If the striking location is node 'V_{out}' which is the drain of the power MOSFET, the SET response can be limited by decoupling capacitor and workload.

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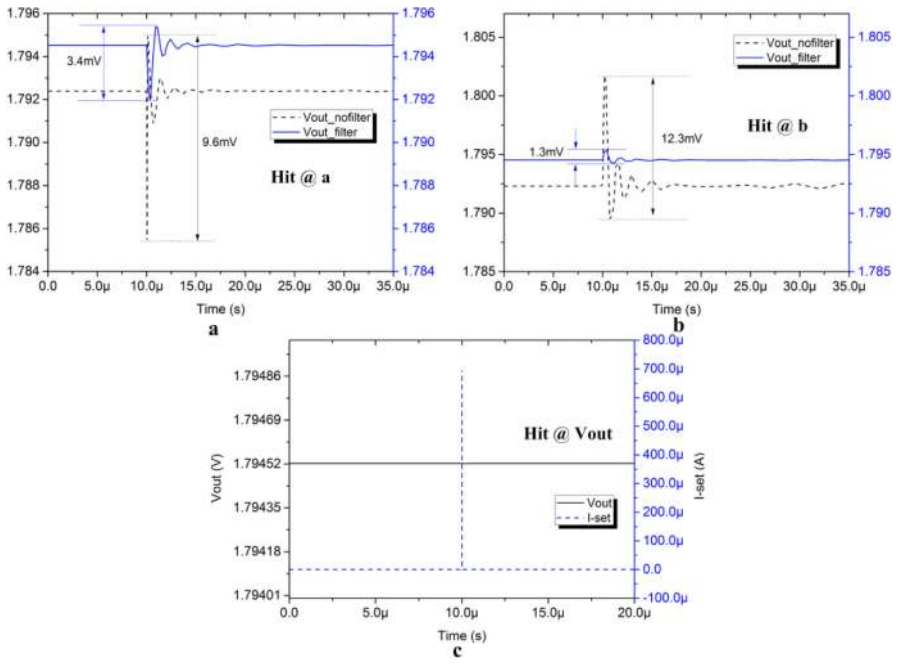

Fig. 4. The SET response of the proposed LDO

According to the SET striking results, the proposed LDO has the advantage of simply structure that has a few nodes and internal filter. Therefore, the SET interruption can be mitigated significantly.

Table I. SET performance comparison between previous works and this work

	[11]	[12]	This work
Output voltage (V)	5.5	1.5	1.8
Workload (mA)	<50	50	50
Capacitor C_L	1 µF	47 µF	1 µF
SET ΔV_{out}	>100 mV	>70 mV	<4 mV

The performance of the proposed LDO is compared with other works in recent years. The works [11] and [12] are latest works which are related to harden power units. According to Table I, the proposed circuit has a better SET response performance, and the variation range of the output voltage is less than 4 mV.

The transient response of the proposed LDO: As a power supply unit, the proposed LDO should maintain the output when the workload changes transiently. The output voltage V_{out} is 1.8 V, and the range of the workload is 50 µA~50 mA with 100 ns hopping time. The transient response of the proposed LDO is described in the Fig. 5.

According to the Fig. 5, the post-layout simulation result shows that the workload changes at the ratio of ±60 dB in 100 ns. The dropout is 12.5 mV, the peak undershoot is 17.1 mV with 1.687 µs settling time. The peak overshoot is imperceptible.

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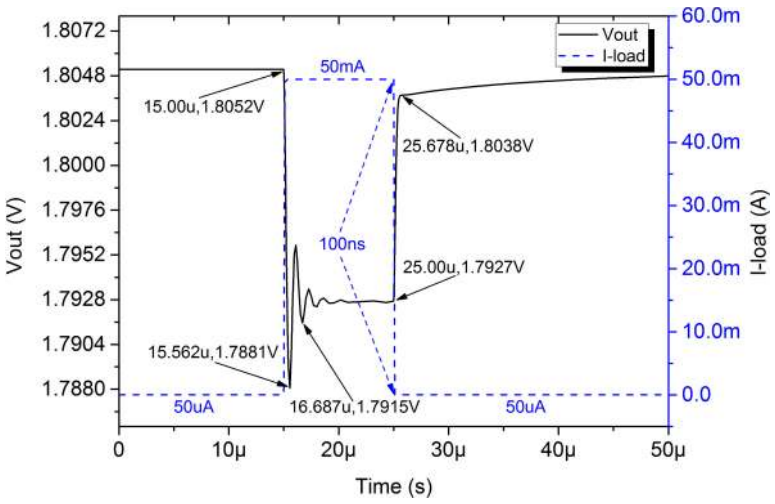

Fig. 5. The transient performance of the proposed LDO.

Table II. Normal performance comparison between previous works and this work

	[13]	[14]	[15]	This work
Process (µm)	0.13	0.18	0.18	0.18
De-capacitor (µF)	2	0.1	1	1
V_{out} (V)	1	1	1.2	1.8
Max. load (mA)	25	100	50	50
Overshoot (mV)	15	~120	70	11.1
Undershoot (mV)	10	277	50	17.1
Settling time O (µs)	N.A.	~2	1	0.687
Settling time U (µs)	N.A.	N.A.	1.5	1.687

The normal performance of the proposed LDO is compared with recent works. According to the Table II, the proposed circuit has a better transient performance than [14, 15], and has a slightly bigger undershoot than [13] for the difference in load.

4 Conclusion

In this paper, a SET hardened LDO is presented. The proposed LDO is different from the typical LDO; it removes reference circuit and amplifier which are generally sensitive to SET. Taking advantage of simply structure and inserting internal filter, the proposed circuit mitigates SET significantly. The output voltage changes less than 16 mV when the SET current pulse strikes the sensitive node, making it suitable for high-reliability applications. In addition, the transient response performance of the proposed LDO is still excellent, because the poles of the inserting filters are far away from the main pole.

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