7.4 A Single-Inductor Step-Up DC-DC Switching Converter with Bipolar Outputs for Active Matrix OLED Mobile Display Panels

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Of the different flat panel displays that can meet the increasing requirements of customers, the active matrix OLED (AMOLED) display is a strong candidate for mobile applications owing to its high resolution, low power consumption and low cost. AMOLED panels, however, usually require multiple power supplies with different regulated voltages. Therefore, step-up switching converters that can supply multiple outputs for this application are important.

A single inductor bipolar output (SIBO) converter, shown in Fig. 7.4.1, is presented in this paper to power an AMOLED display for TDMA (GSM) mobile sets, which requires both positive and negative voltages with a gap of 10 to 12V. This converter reduces the overall size and cost of a mobile set. The most critical specification for this application is the line transient response of the positive supply, V_{OP}, which can seriously affect the display by changing V_{gs} of M_{p4} if it is not fast enough, thus changing the current I_{OP} through the AMOLED. Based on experimentally verified data, the average variation of V_{OP} should be strictly less than 4mV within 51.2μs of a 0.5V fluctuation in the battery voltage, V_g, to avoid visible flicker on the display as illustrated in Fig. 7.4.1. Its switching ripple should also be under 30mV for a clean image. However, for the negative output V_{ON}, its variation only affects V_{ds} of M_{p4}, and hence, its line transient and ripple specifications are not as severe. Because of the stringent requirements for V_{OP}, some chipmakers have attempted to obtain the V_{OP} with an LDO [1] regulator, which creates a trade-off between reduced efficiency and increased cost and area.

The converter in Fig. 7.4.1 is a combination of two converters: V_{OP} is obtained from a boost operation employing modified comparator control (MCC) and V_{ON} from a charge-pump circuit with PI-control. The control of the power switches is simplified compared to the topologies reported in [2] by delivering charge to all outputs at every switching cycle with priority given to V_{OP}. The charge remaining after transferring charge to V_{OP} is used to control the PWM signal for M_{n1}. Therefore, the effect of battery voltage fluctuations can be seen on V_{ON} but is very small on V_{OP} since V_{OP} is controlled by a comparator while V_{ON} is controlled by a PI loop. An additional high voltage output V_H (= $|V_{ON}| + V_{D1}$) is intentionally generated to supply all gate drivers and to bias the bodies of the power PMOS transistors to reduce the sizes of the switches. The freewheeling switch M_{p3} is active in the discontinuous-conduction mode (DCM) with the zero-inductor-current detection technique reported in [3]. Consequently, the size and the conduction loss of M_{p3} are smaller than those of the one in the converter of [4].

Figure 7.4.2 shows the timing diagram for SIBO operation. In DCM, during D_1T, the NMOS switch M_{n1} is conducting and the inductor current I_L increases. During D_2T, M_{n1} is off and the PMOS switch M_{p1} is on to divert I_L into C_{OP}. During D_3T, the NMOS switch M_{n2} and the PMOS switch M_{p2} are conducting at the same time to divert the rest of I_L into the output capacitor C_{OH} and the capacitor C_F until I_L is zero. During D_4T, M_{p3} is conducting and I_L remains at zero until the end of the cycle. The negative output capacitor C_{ON} is negatively charged through D_1 from C_F during the next D_1T in the charge-pump operation. In continuous-conduction mode (CCM) operation, the switching sequence is the same as in DCM except for M_{p3}. In this mode, the switches M_{n2} and M_{p2} are turned off at the end of a cycle and M_{p3} is inactivated since I_L does not go to zero.

Figure 7.4.3 shows the peak current sensing method used in this converter. The circuit can accurately sense the peak inductor current I_{peak} both in DCM and CCM. Normally, I_{peak} is obtained from the on-voltage across M_{n1} (in Fig. 7.4.1). However, in this SIBO, the current in M_{n1} is $I_{MN1} = I_{peak} + I_{neg}$, where I_{neg} models the negative-charge-transfer current during D_1T. Therefore, I_{neg} should be removed from I_{MN1} to obtain I_{peak}. In this circuit, I_{neg} is generated from the current trimming block by modeling the charge and discharge currents in the charge-pump operation producing V_{ON} using the real inductor current shape I_{ac}, capacitor C_{eq} and resistor R_{eq}. In this modeling, C_{eq} and R_{eq} act like C_F and the on-resistance of M_{n1}, respectively. I_{ac} is derived from V_{ac} by the AC_current sense block, which senses the exact shape of I_L as reported in [3]. I_{neg} is obtained using I_{CFM}, which models the charge current of C_F during D_3T, as illustrated in Fig. 7.4.3. In D_3T, since S_{MN} is low and S_{VP} and S_{VN} are high, I_{CFM} flows through M_1, M_2, C_{eq} and M_3 to store charge in C_{eq}, modeling I_L diverting charge to C_F. During D_1T when S_{VN} is low and S_{MN} and S_{VP} are high, the discharge current of C_{eq} flows through M_4, M_6, C_{eq}, R_{eq} and M_8 to AC_gnd, which is a constant voltage, modeling the negative-charge current from C_{ON} through D_1 to C_F. This current is I_{neg}, converted from I_{CFM} by the equivalent time constant $R_{eq}{\cdot}C_{eq}$ of $R_{on}(M_{n1}){\cdot}C_F$. M_8 is used to reset the charge across C_{eq} during D_2T to make I_{neg} accurate.

Using the information contained in I_{MN1} and I_{neg} from this circuit, I_{peak} through the inductor is obtained. The capacitor C_C is used with switches M_{11} and M_{12} to sample a voltage proportional to the peak inductor current, I_{sense}, during D_1T. Offset and clock feedthrough cancellation techniques are used.

Figure 7.4.4 shows the MCC structure used to generate a robust V_{OP}. The structure is necessary because a simple comparator cannot maintain a regular duty cycle for M_{p1} since it is seriously affected by output noise. The noise would cause M_{p1} to switch unpredictably and produce a large switching ripple at V_{OP}. Whereas, the MCC senses the average of V_{OP}, rather than output ripple, by adding some triangular signals at the inputs of the comparator. This enables the PWM channel control to switch every cycle and generate a new PWM signal (X_1). The duty-cycle of X_1 is controlled by OTA A_1, A_2 and the G_m-C_i integrator. Abrupt errors in the feedback voltage FB_P of V_{OP} are quickly corrected by OTA A_1. Steady-state errors are corrected by the G_m-C_i integrator with OTA A_2. Therefore, the input offset voltage of the comparator is also corrected because the integrator only controls the difference between the band-gap voltage (BGV) and FB_P. The operation of the MCC is illustrated by the timing diagram in Fig. 7.4.4.

This converter was fabricated in a 0.5μm power BiCMOS process and occupies a die area of 4.1mm^2. It operates at a switching frequency of 1MHz with an inductor of 4.7μH having an ESR of 320mΩ. The input battery voltage varies from 2.7 to 4.5V, and V_{OP} and V_{ON} are regulated to 4.58V and -6.24V with ripple voltages of 15mV and 5mV, respectively. Figures 7.4.5 and 7.4.6 show experimental results. Figure 7.4.5 shows CCM and DCM operations and Fig. 7.4.6 shows the line transient response of V_{OP}. The maximum output power is 1.1W, and the maximum efficiency is 82.3% at an output power of 330mW.

Acknowledgement:
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References:
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[4] D. Ma, W. H. Ki, C. Y. Tsui and P. Mok, "A Pseudo-CCM/DCM SIMO Switching Converter With Freewheel Switching," *IEEE J. Solid-State Circuits*, pp.1007-1014, June, 2003.

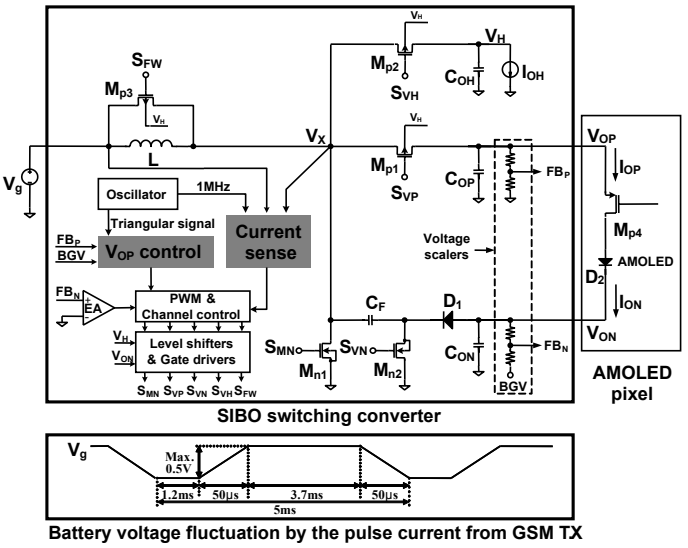

Figure 7.4.1: Block diagram of SIBO converter (I_{OP}=I_{ON}).

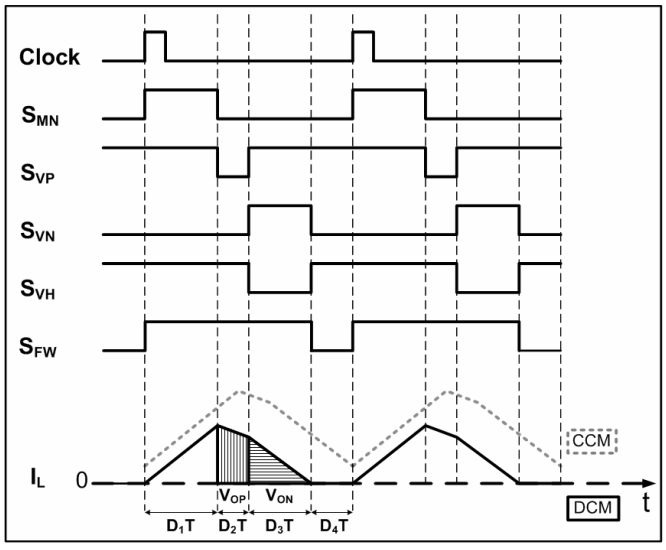

Figure 7.4.2: Timing diagram of the SIBO converter.

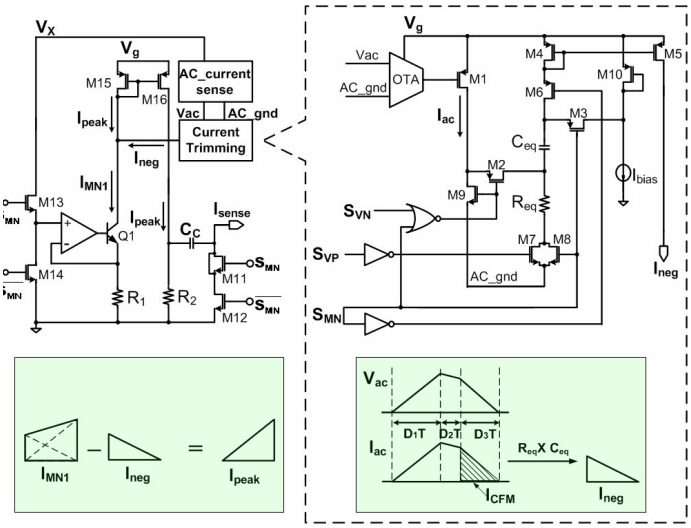

Figure 7.4.3: Current sense method for the SIBO converter.

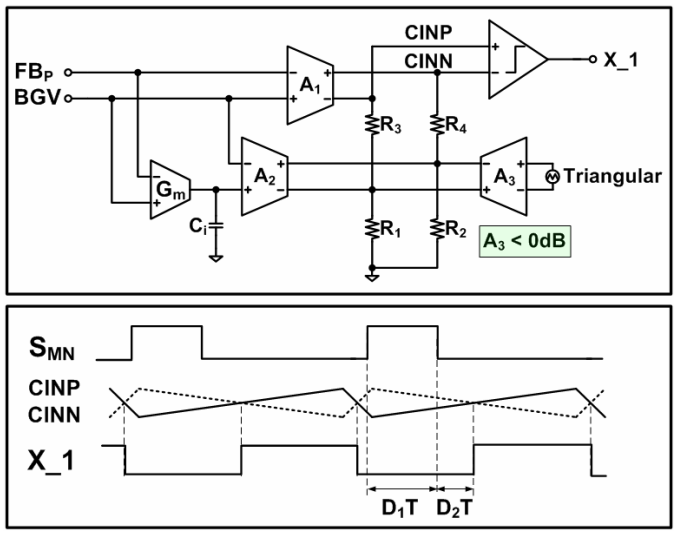

Figure 7.4.4: Block and timing diagrams for the MCC.

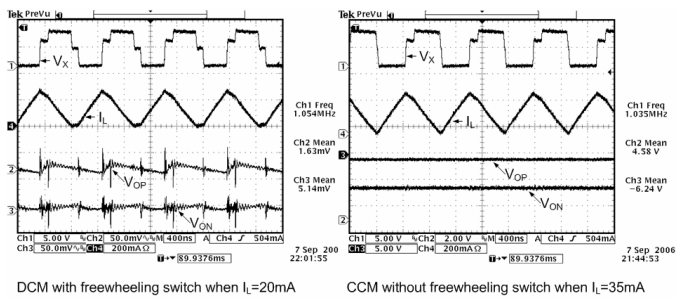

Figure 7.4.5: Measured waveforms with the SIBO converter both in DCM and CCM.

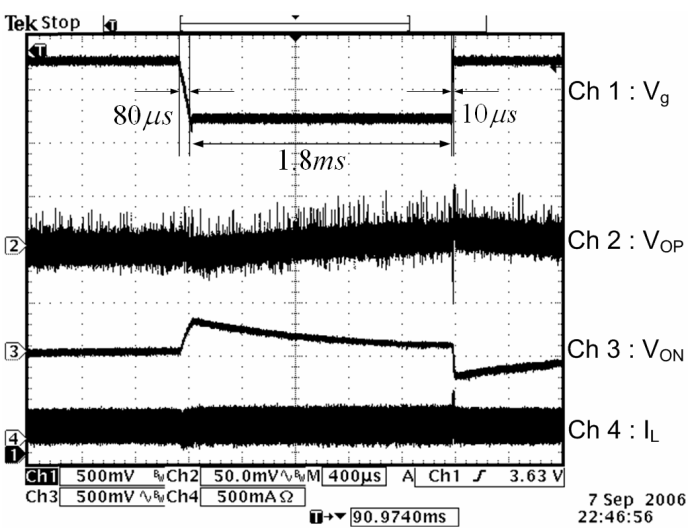

Figure 7.4.6: Measured line transient response when I_{OP} = I_{ON} = 20mA.

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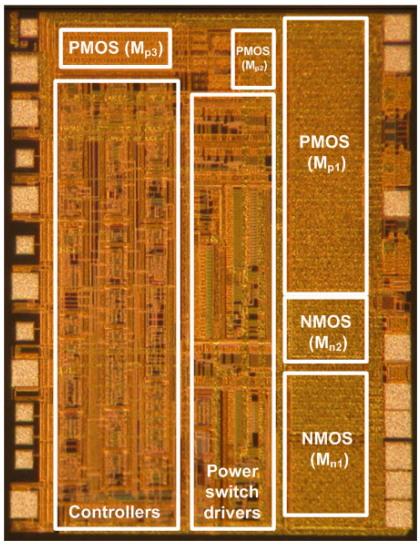

Figure 7.4.7: Chip micrograph.

