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# A Single MEMS Resonator for Reconfigurable Multifunctional Logic Gates

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**Abstract.**

Despite recent efforts toward true electromechanical resonator-based computing, achieving complex logics functions through cascading micro resonators has been deterred by challenges involved in their interconnections and the large required array of resonators. In this work we present a single micro electromechanical resonator with two outputs that enables the realization of multifunctional logic gates as well as other complex logic operations. As examples, we demonstrate the realization of the fundamental 2-bit logic gates of OR, XOR, AND, NOR, and a half adder. The device is based on a compound resonator consisting of a clamped-guided electrostatically actuated arch beam that is attached to another resonant beam from the side, which serves as an additional actuation electrode for the arch. The structure is also provided with an additional electrothermal tuning capability. The logic operations are based on the linear frequency modulations of the arch resonator and side microbeam. The device is compatible with CMOS fabrication process and works at room temperature.

## 1. Introduction

The past two decades have seen increasing interest to explore micro/nano-electromechanical systems (MEMS/NEMS) for various applications, such as filters [1–5], switches [6–9], memory devices [10–12], and logic gates [13–18]. MEMS/NEMS devices can be based on their static behavior, such as switches, or on their dynamic behavior, such as resonators and resonant sensors [19]. Due to their simplicity and high efficiency, MEMS switches have been excellent candidates to perform multifunctional switching operations, and more recently were proposed for logic and memory applications [12, 20-21]. However, they suffer major drawbacks due to the contact and stiction problems. Thus, non-contact dynamic-based logic devices have received increasing attention the past few years [14, 18, 22-23].

MEMS resonators are commonly operated in the linear regime. However, due to the geometric and electrostatic force nonlinearities, they can exhibit nonlinear behavior [24–26], which has been exploited recently for memory devices [20, 27]. Halg [28] demonstrated an integrated nonvolatile memory based on the bi-stable states of a micromechanical bridge. Yao et al. [20] demonstrated both logic and memory unit from a single MEMS resonator integrated with a closed loop control to fix the output signal at a single frequency.

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There is an increasing interest in alternative computing architectures that can overcome the limitations of complementary-metal-oxide-semiconductor (CMOS) transistors-based computing, such as their inability to operate at high temperatures and their high off-state power consumption. Hence, there are demands for an alternative approach that will provide run time re-configurability to improve their functionality and energy efficiency. These demands have revitalized the objective of seeking for a scalable mechanical computation that can be traced back to the work of Charles Babbage in 1822 on calculating engines [29]. In addition, subsequent improvements in micro-/nano- fabrication and measurement techniques have revived research interest in mechanical computation and stimulate the use of MEMS/NEMS resonators for different logic and memory applications. Dynamic-based resonant structures have been particularly under increasing interest for logic applications, where their on-resonance large response is considered a "High" state and their off-resonance response is taken as "Low" state. The fact these are non-contact devices make them especially attractive compared to MEMS and NEMS switch-based logic devices. The first attempt in this domain was presented by Masmanidis et al. [17] who demonstrated a scalable dynamic mechanical logic gate (XOR) using an L-shaped nano-cantilever [30]. AND/NAND and OR/NOR logic gates were demonstrated using doubly clamped nano-beams operating in the nonlinear regime. A universal logic gate was demonstrated with multi-bit logic functions using a single parametrically excited resonator in [31]. Mita et al. [32] demonstrated XNOR and XOR logic gates based on a single cantilever beam. Mahboob et al. [33] reported 2-bit and multi-bit logic operations using a single electromechanical parametric resonator by encoding binary information as different oscillation frequencies. In [15], several basic 2-bit and 3-bit logic operations have been demonstrated using an electrothermally actuated arch resonator.

Thus far, the realization of complex combinational logic gates has posed a great challenge. Toward this, Hafiz et al. [34] reported an alternative approach to realize complex logic gates by cascading multiple electrothermally actuated resonators demonstrating a single bit binary comparator, a single bit 4-to-2 encoder, parallel XOR/XNOR and AND/NOT gates, and a 2:1 MUX [35]. However, cascading multiple MEMS resonators to perform complex logic operations introduces major challenges, such as the required interconnections between the resonators, the increase in the device complexity, and more fabrication restrictions.

The development of fundamental and complex logic circuits with a single conceptual framework is key to realize a complete mechanical computing machine with run-time programmability. Motivated by the challenges involved in cascading resonators to develop complex logic circuits, we demonstrate an alternative approach to realize both fundamental and complex logic circuits from a single MEMS microstructure. The microstructure is composed of a compliant shallow arch, which can be actuated electrostatically across its length and through its side near the anchor [36]. In addition, it can be actuated electrothermally. On the arch guided side is another resonant beam that can be actuated electrostatically and can modulate the stiffness of the arch. Therefore, this structure offers various possibilities to control stiffness, and hence, leads to various possible logic outputs. This enables programmability of the device to give different multifunctional logic operations depending on the combination of the inputs and outputs. With this concept, two different logic operations can be obtained simultaneously from the two outputs. In this paper, we demonstrate basic 2-bit logic operations, mainly OR/NOR, AND/XOR/NOR, and complex combinational logic half adder operation from the single MEMS structure. The proposed device will be shown as a promising platform for performing other complex logic circuits.

## 2. Device Operations and Experimental Set-up

An image of the fabricated device and its schematic are shown in Figures 1(a) and (b), respectively. The device has been fabricated by MEMSCAP [37] based on (100) a highly conductive Silicon layer (n-

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Si) of Silicon on insulator (SOI) wafer and a two-mask lithography. The device consists of a clamped-guided arch microbeam of a half-wave sine (beam 1), two flexure beams, and a movable beam (beam 2). Beam 1 is sandwiched between two electrodes and is anchored at one side while the other side is guided by beam 2. Beam 2 is also sandwiched between two electrodes. These electrodes can be used for electrostatic actuation (input) and also for sensing (output). The actuation of beam 2 applies compressive or tensile axial forces on beam 1, the arch, thereby controlling the arch curvature and stiffness. Also, near the guided end of beam 1, two flexure beams are added, which prevent rotation of beam 1. Additionally, the two flexure beams can be actuated electrothermally, by passing a current through them, which adds another input to control the curvature and stiffness of beam 1 and beam 2. The flexure beams have 460 µm length, 10 µm width, and 25 µm depth. The dimensions of the other two beams composing the device are listed in Table 1. The device is designed with electrostatic and electrothermal actuators for the application of tensile and compressive axial loads. In our previous work, which is based on the same structure [36], the measurement results of the resonant frequency of several beams with different dimensions and under electrostatic voltage showed that the axial stress dominates the reduction in stiffness due to the decrease in curvature, and thus results in increasing the resonant frequency. This dominant effect can be attributed to the low initial curvature of the arches compared to their length. Also in [25], we studied the competing effects among the design parameters on the resonance frequencies and the mid-point deflections of an arch beam. Based on the results and analyses in [25], we selected a shallow arch beam that gives required frequency shifts necessary to perform the logic operations.

| ***Description*** | ***Beam 1 (Arch beam)*** | | ***Beam 2 (Straight beam)*** | |
|---|---|---|---|---|
| Length (µm) | $L_1$ | 600 | $L_2$ | 1000 |
| Width (µm) | $h_1$ | 2 | $h_2$ | 50 |
| Depth (µm) | $b_1$ | 25 | $b_2$ | 25 |
| Initial curvature (µm) | $b_{o1}$ | 1.7 | | |
| Gap between the microbeams and the electrodes (µm) | $D$ | 10.6 | $g$ | 2 |

**Table 1:** Dimensions of the beams composing the device.



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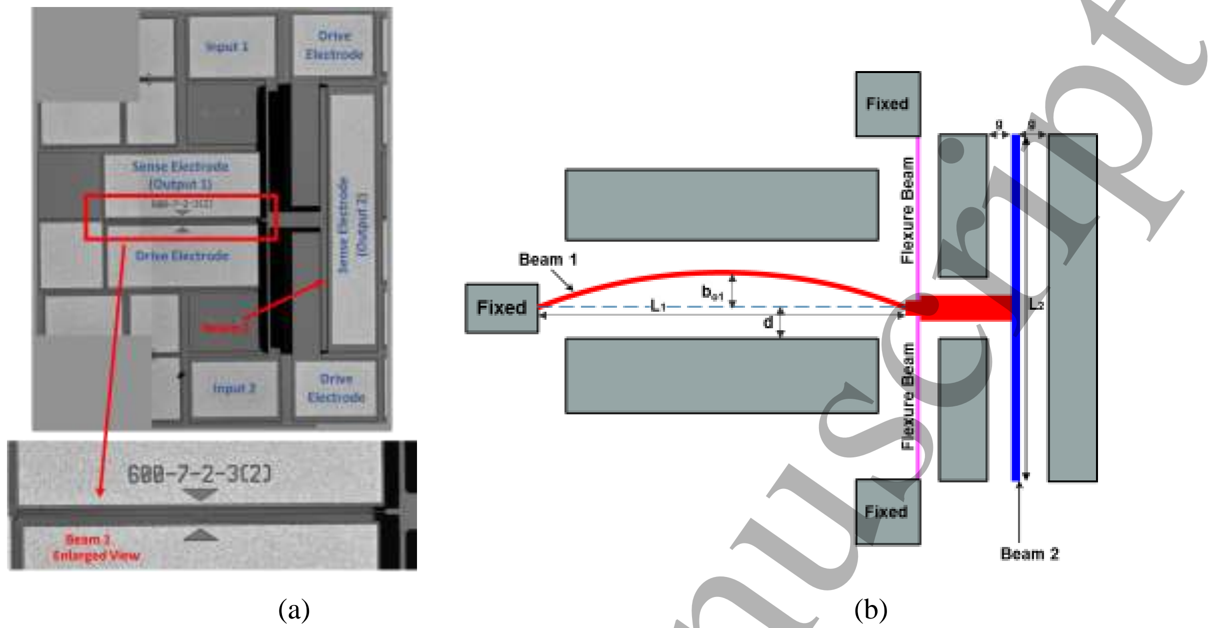


**Figure 1**: (a) A scanning electron microscope SEM image. (b) Schematic of the device (not-to-scale).

To experimentally characterize the device, we utilize a network Analyze (E5071C) and the setup shown in Figure 2. The two flexure beams are used as logic inputs and are electrothermally actuated to control the resonance frequencies of both beam 1 and beam 2. For the outputs, the sense electrodes of beam 1 and beam 2 are used as output 1 and output 2, respectively. The lower electrode of beam 1 and the compressive electrode (to the left side) of beam 2 are used as the driving electrodes to excite the structure into the required mode of vibration. The electrical actuation signal for the driving electrodes is composed of an AC signal from the network analyzer superimposed to a DC voltage. When the structure is driven into vibration using the driving electrodes, its motion induces AC currents in the sense electrodes, which form the outputs (output 1 and output 2). The output currents are then amplified using low noise amplifiers (LNA). The LNA outputs are connected to the input port of the network analyzer for S21 transmission measurement. For all the logic operations demonstrated in this paper, the beams are biased with DC of 40V and superimposed with an AC signal of 20mV (RMS) at room temperature and pressure of 2 Torr.

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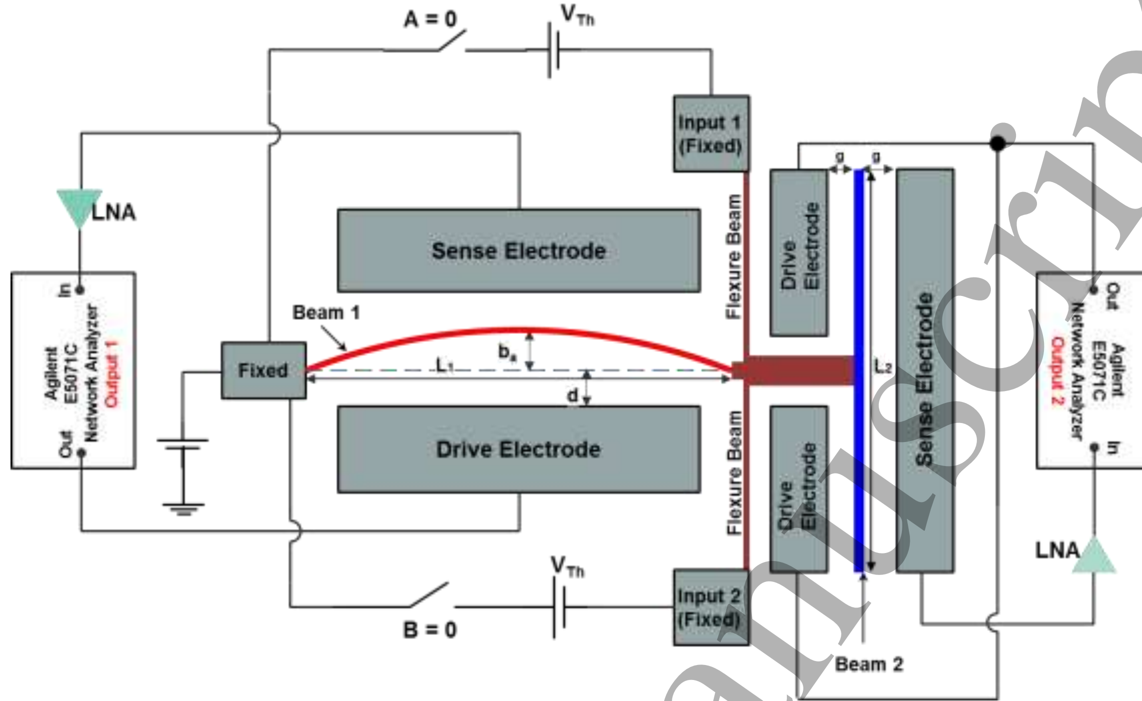


**Figure 2**: Schematic of the experimental setup. The beams are biased with a DC load of 40V superimposed with an AC signal of 20mV (RMS), operating at room temperature and a pressure of 2 Torr.

## 3. Modeling the Resonator Vibration Modes

A finite element (FE) model of the device was developed with the software COMSOL to design and simulate the natural frequencies and mode shapes of the device. To compute the natural frequencies, the solid mechanics physics under structural mechanics module was used to carry out the eigen-frequency study. Polysilicon was used as the material for the device and free tetrahedral mesh with custom element size were used to mesh the device for accurate results.

While the whole device with its two straight and arch beams can be considered as a single integrated structure, the FE simulation indicates that there are two distinct localized modes, where the individual beams 1 and 2 can locally vibrate with minimum effect on each other. Figure 3(a) shows a mode in which the local motion of beam 1 dominates and Figure 3(b) shows a mode in which the local motion of beam 2 dominates. These two dominating modes will be utilized and excited to realize the logic functions that are demonstrated in this paper. For simplicity, we will call the mode of Figure 3(a) as beam 1 mode and that of Figure 3(b) as beam 2 mode.

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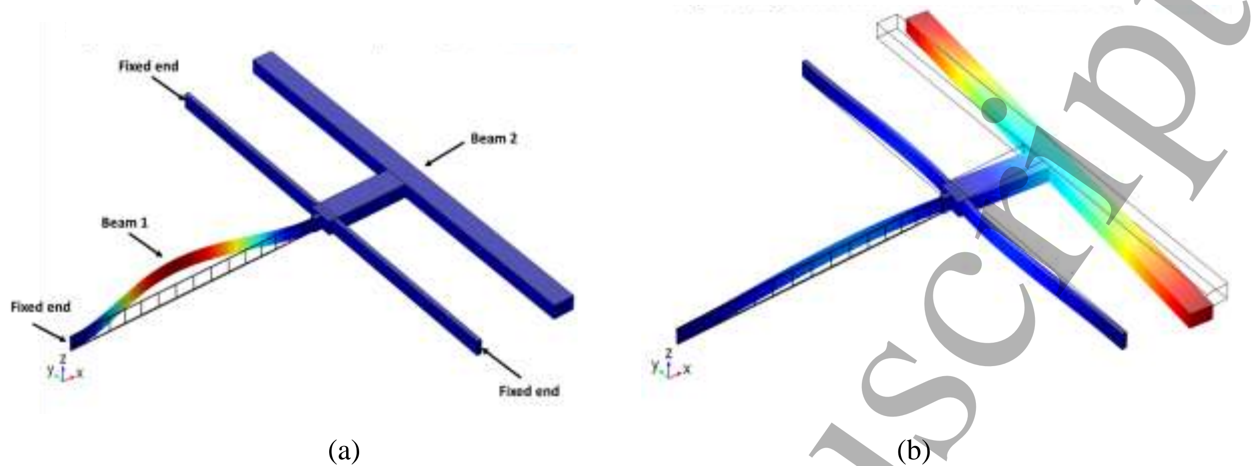


(a) (b)

**Figure 3**: (a) The modeshape with dominant motion of beam 1 of a natural frequency near 41.978 kHz. (b) The modeshape with dominant motion of beam 2 of a natural frequency near 22.113 kHz.

## 4. The Tunability of Modes

Before implementing the device for logic operations, the tunability of both modes of beam 1 and beam 2 are experimentally obtained, Figure 4, while varying the electrothermal voltage on the flexure beams. When the flexure beams are powered, the elastic stiffness of the beams changes depending on the applied voltage and the amount of the current passing through the microbeam. As shown in Figure 4(a), the resonance frequency of beam 1 with one electrothermal input (switch A on) decreases until it reaches a critical point ($V_{th}$ = 4 V) after which it increases as $V_{th}$ increases. The resonance frequency however keeps decreasing when both electrothermal inputs (switch A and B are on) are applied on the flexure beam. The decrease/increase in the resonance frequency of beam 1 is due to the competing effects among its initial curvature, the induced axial stress due to the electrothermal voltage from the inputs, and the axial displacement [25]. The tunability results of beam 1 show that there are significant effect of axial stress in the case with one electrothermal input (switch A on). In this case the amount of current is divided between the arch beam and the second flexure beams. Hence, it is concluded that the axial displacement in the case when both electrothermal inputs (switch A and B are on) are applied is higher than the case when one input is applied (switch A on). Also, it can be observed from the tunability that the resonance frequency of beam 1 for either one or both electrothermal inputs follows the same trend for low electrothermal voltages until it reaches $V_{th}$ = 3 V. This response of beam 1 at low $V_{th}$ will be utilized to implement the multifunctional logic gates.

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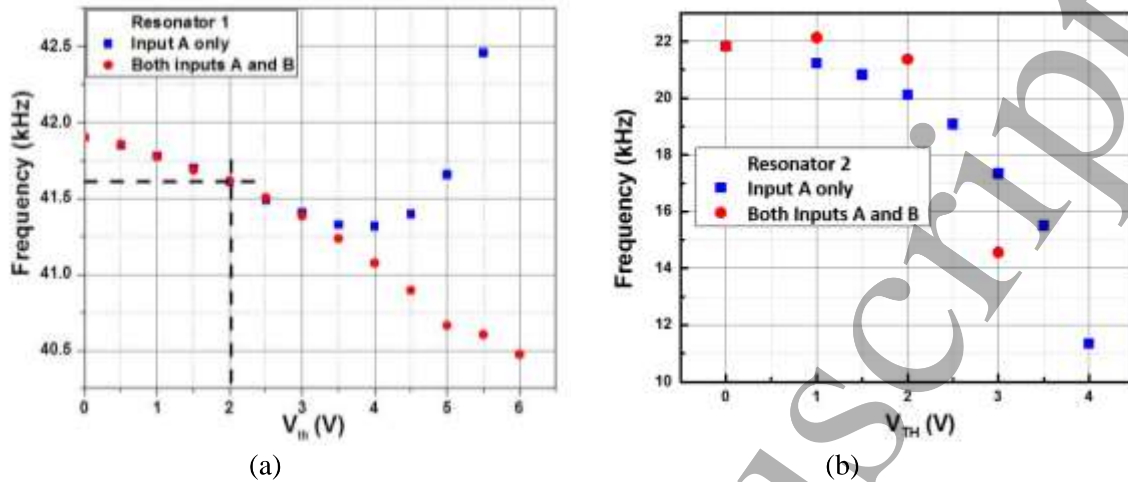
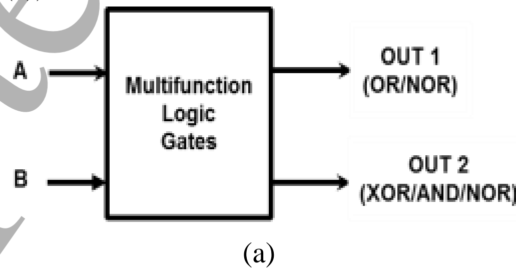


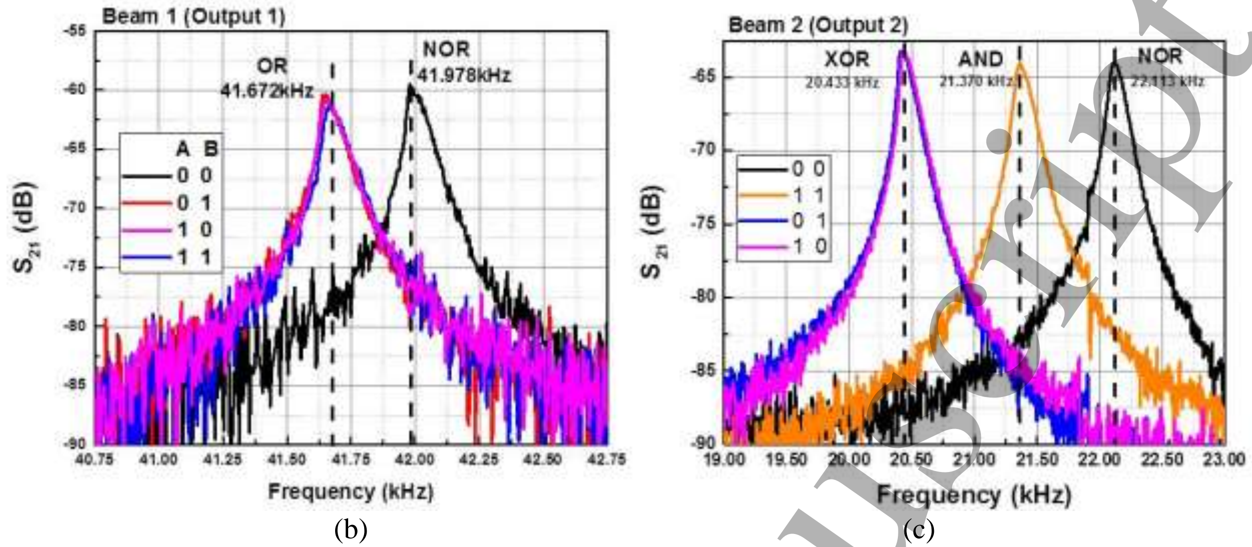

**Figure 4**: Variation of resonance frequency (a) of mode 1 of beam 1 when one or two electrothermal inputs are applied and (b) of mode 1 of beam 2 when one input is applied.

## 5. Fundamental 2-bits logic operations

To perform the OR, NOR, XOR, AND, and NOR logic operations, the resonators are operated in the linear regime and their resonance frequency are controlled by the electrothermal voltages on the anchors of the flexures, which act as the logic inputs. The two logic inputs are provided with two DC sources $V_A$ and $V_B$ and they are used to switch between low and high states of the $S_{21}$ transmission signal corresponding to the logic outputs “0” and “1”, respectively. The logic input 0(1) represents the disconnection (connection) of the DC sources. For logic inputs condition $V_A = V_B = 0$ V, the natural frequencies of the beams are measured as 41.978 kHz and 22.113 kHz for beam 1 and beam 2, respectively. Upon changing the logic inputs condition to 1 ($V_A = V_B = 2$V), a DC current flows through the flexures and induces a compressive stress, which results in increase or decrease of the resonance frequencies of beam 1 depending on the initial curvature and the boundary conditions, as shown in Figure 4. By a proper selection of the input voltage, different logic operations can be demonstrated and obtained from the two outputs (Figure 5 (a)).




(a)




(b) (c)

**Figure 5**: (a) Schematic for 2-bits logic operations in which OR/NOR can be obtained from the output 1 and XOR/AND/NOR from the output 2. (b) Frequency response of output 1 showing the operating frequencies (dashed vertical lines) for OR and NOR gates. (c) Frequency response of output 2 showing the operating frequencies (dashed vertical lines) for AND, XOR, and NOR gates.

The frequency responses for beam 1 and beam 2 are shown in Figures 5(b) and (c). To demonstrate NOR gates, the natural frequencies of the resonators at $V_A = V_B = 0$ V are selected as the operating frequency of both beams (41.968 kHz for beam 1 and 22.113 kHz for beam 2). An OR logic operation can be realized by tunning beam 1 as follows. As shown in Figure 4 (a), the frequency tunability of beam 1 indicates that for low electrothermal voltages (below 3 V), the natural frequency of the beam remains the same when activating one or two inputs. Accordingly, 41.672 kHz is selected as the operating frequency for electrothermal input voltage of 2 V. When one or both inputs are activated, the resonance frequency of the resonator is shifted to the same lower value, and hence shows a high state “1” for logic input conditions (0, 1), (1, 0) and (1, 1) and a low state “0” only at its natural frequency (0, 0). The time responses showing the binary inputs and the logic output are depicted in Figure 6 (a). For NOR logic operation of beam 1, the frequency of operation 41.968kHz is selected for the AC input signal and the two inputs A and B were triggered as shown in blue and black, respectively. The switching between 0V and 2V correspond to the 0/1 logic input conditions, respectively, and the $S_{21}$ (dB) transmission signal in brown is the logic output and it fulfills the NOR truth table. The same principle is used to demonstrate the time response for all other logic operations. With the same inputs from A and B; an XOR and AND gates can be realized from beam 2 by selecting its operating frequencies to be, respectively, as 20.433 kHz and 21.37 kHz.

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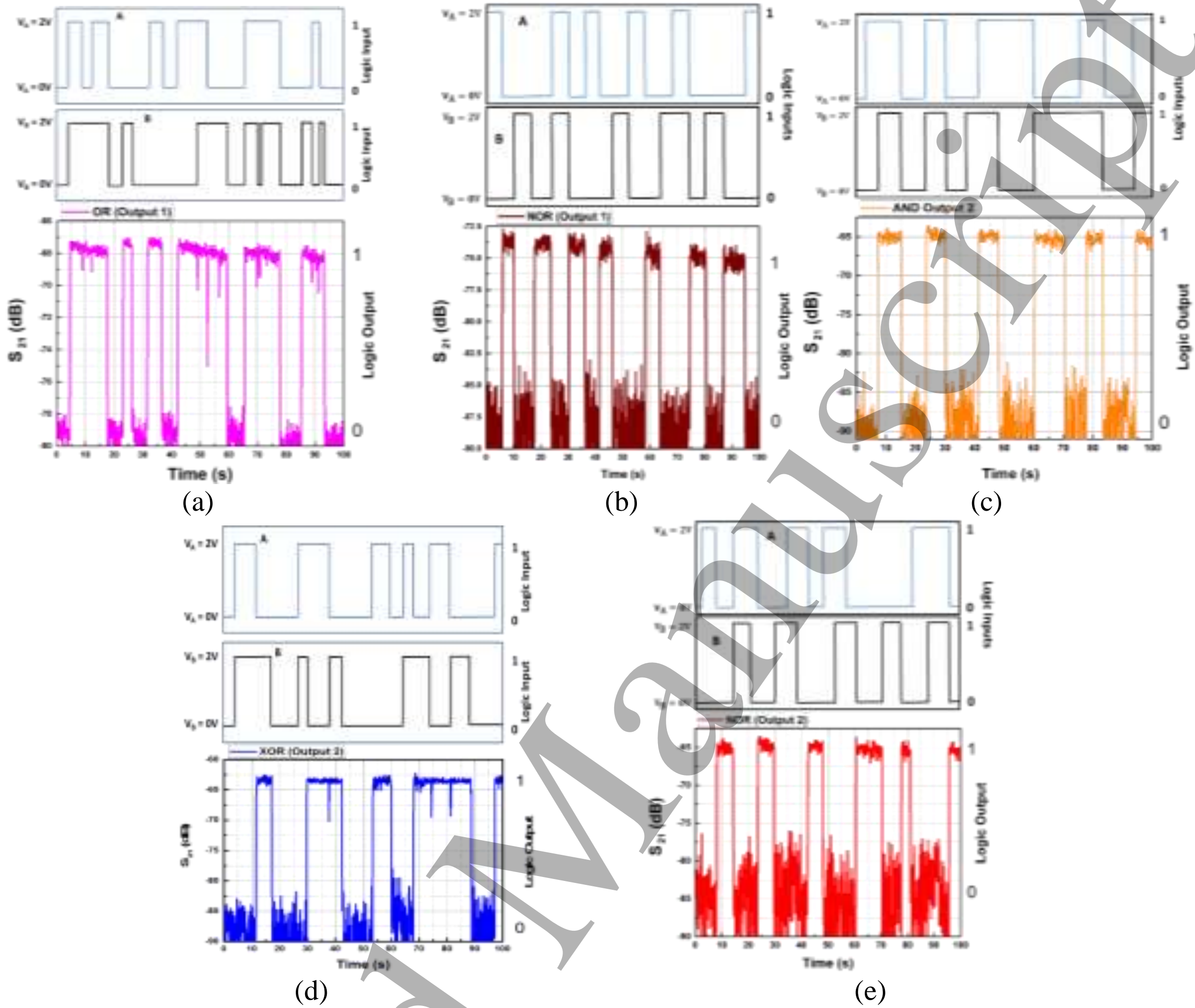


**Figure 6:** (a) OR gate real time response from output 1. (b) NOR gate real time response from output 1. (c) AND real gate time response from output 2. (d) XOR real gate time response from output 2. (e) NOR real gate time response from output 2.

## 6. Half Adder

A half adder is built from two basic logic gates: XOR and AND gates, see Table 2. It takes two binary digit inputs to give two binary digit outputs (Sum and Carry bit). The two inputs have to be the same for both logic gates. The Sum bit is the XOR gate of the two inputs while the Carry bit is the AND gate as shown in Figure 7(a).

| ***Inputs*** | | ***Outputs*** | |
|---|---|---|---|
| **A** | **B** | **OUT 1 (C)** | **OUT 2 (S)** |
| **0** | **0** | **0** | **0** |
| **0** | **1** | **0** | **1** |
| **1** | **0** | **0** | **1** |
| **1** | **1** | **1** | **0** |

**Table 2:** Half adder truth table.



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The AND logic operation is obtained from output 1, while the XOR logic operation is obtained from output 2. To realize an AND gate from beam 1, an electrothermal voltage of 3.7 V is selected. At this voltage, Figure4 (a), the resonance frequency from a single input (0, 1) differs from that from two inputs (1, 1); a must requirement for the realization of logic gate AND. Hence, selecting the operating frequency to be 41.081 kHz for beam 1, the resonator shows high state "1" for only logic input conditions (1, 1), while it shows low state for all other logic input conditions, Figure 7 (b). Hence, this is used as the Carry bit. In implementing an XOR gate for the Sum bit from output 2, the selected frequency is 14.505 kHz. As shown in Figure 7 (c), the resonator shows high state "1" for logic input conditions (0, 1) and (1, 0), while it shows low state for logic input conditions (0, 0) and (1, 1).

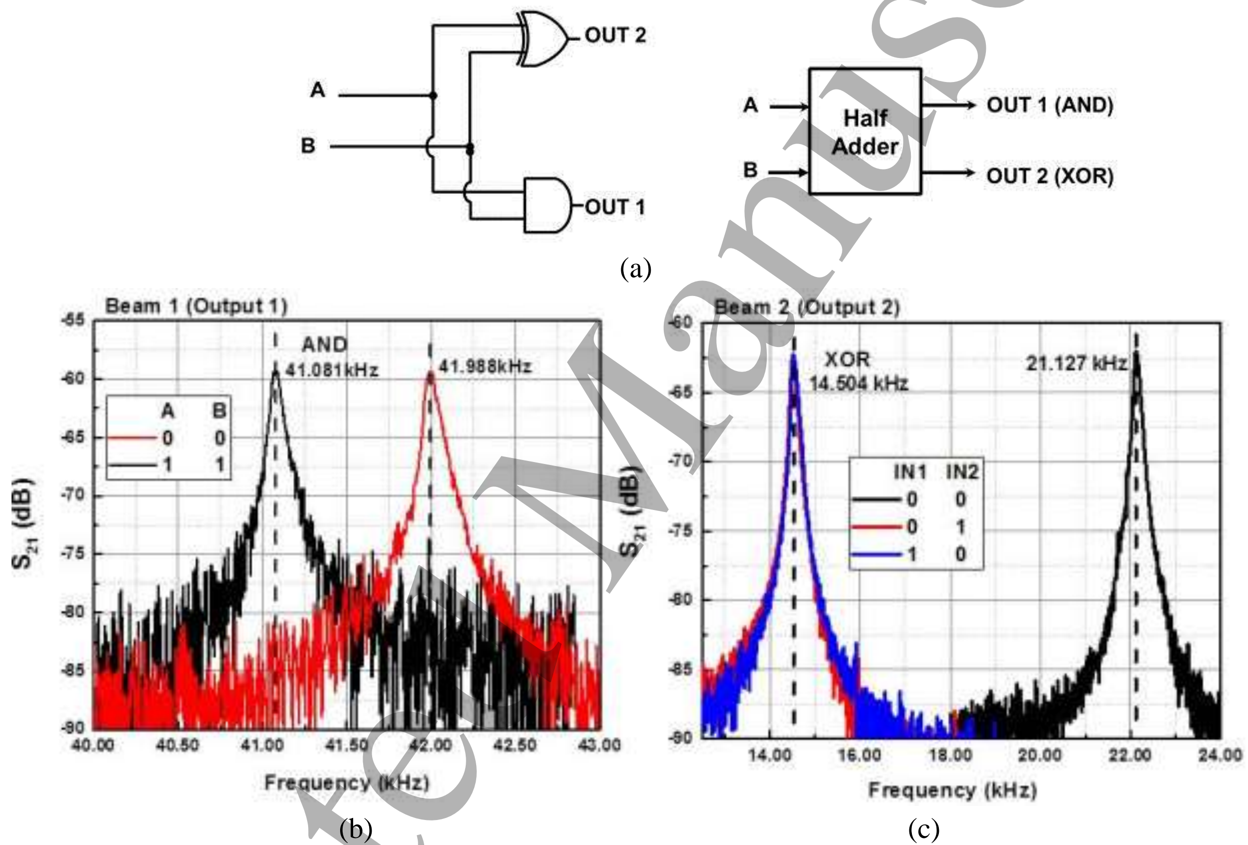


**Figure 7**: (a) Half adder logic diagram and schematic diagram. (b) Frequency response from output 1 showing AND gates for a Carry bit. (c) Frequency response from output 2 showing an XOR gate for a Sum bit.

## 7. Performance Evaluation per Logic Operation

The performance of the electromechanical resonator as a potential computing device needs to be evaluated in terms of operating speed and switching energy [15]. The operating speed of MEMS resonators can be estimated as *f/Q*, where *f* is the resonance frequency and *Q* is the quality factor. The *Q* factors of beam 1 and beam 2 are estimated to be 518 and 139, respectively. Thus, the switching speed for beam 1 is 81Hz and beam 2 is 159Hz and these correspond to the switching time of 12.345ms and 6.27ms respectively. The switching time of the proposed device can be significantly decreased by scaling the



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device to the nanoscale. Such switching speeds indicate that such a device can be potentially used for applications that do not require high computational speed, such as for processors in sensors applications.

Another important measure is the switching energy per logic operation. Since the switching operation in this proposed device is based on electrothermal actuation, the switching energy is estimated based on resistive heating of the microbeam $\left(\frac{V_A^2}{R_{MB}}+\frac{V_B^2}{R_{MB}}\right)t_s$ where $V_A$ and $V_B$ are the voltage inputs and $R_{MB}$ is the resistance of the microbeam, which is estimated to be 1.84 kΩ. It is worth noting the high resistance value of the microbeam, which is due to the dimensions of the flexures. Thus, the maximum switching energy per logic operation is estimated to be 53.67 μJ and 27.27 μJ for beam 1 and beam 2, respectively. It is observed that the switching energy is high compared relatively to the case in which electrostatic actuation is used for the switching operation. It is well established that electrothermal actuation is not energy friendly compared to other forms of actuation as most of the energy is lost in form of heat during operation. However, since the logic inputs are integral parts of the proposed architecture, the proposed scheme saves some energy in comparison to other electrothermally actuated microstructures.

Although MEMS logic devices are slower compared to CMOS devices, there are applications where power consumptions are more important than speed, such as keyless auto entry system, traffic lights controller, and sensors networks. In such applications, MEMS logic devices when scaled down to the Nano regime can offer an attractive option.

## 8. Conclusions

This paper presented a single MEMS resonator with two inputs and two outputs. The design relies on in-plane arch clamped-guided microbeam attached to another resonant beam from the side, in which the two beams are excited electrostatically. In addition, the design is provided with two electrothermally actuated flexures beams that are used for tunning the resonance frequencies of the beams. We demonstrated that this configuration allows to realize fundamental 2-bit logic operations, such as (OR/XOR/AND/NOR), and complex logic operations, for example a half adder. The experimental results showed that the resonance frequencies of the arch microbeam and the side beam with electrothermal actuation can be very useful and helpful for selecting the frequency of operations for different logic gates. This device can be reconfigured to enable different multifunctional logic operations depending on the combination of the logic inputs and the two logic outputs. With this concept, different logic operations can be obtained simultaneously from the two logic outputs with the same logic inputs. The same microstructure can be used to demonstrate more complex logic circuits, especially for cases that require two logic outputs. Such a device provides the prospect to realize a mechanical computing machine with run-time configurability.

## Acknowledgement

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