A SINGLE-PHASE HYBRID SWITCHED-CAPACITOR INVERTER FOR HIGH STEP-DOWN APPLICATIONS

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Abstract – **In this paper, a novel single-phase inverter topology is proposed, which was derived from the integration of the conventional voltage source inverter with switched-capacitor dc-dc converters. The inverter circuit can provide a low ac output voltage from a high dc input voltage, using low-voltage devices (switches and capacitors). The modulation scheme is the same employed in conventional inverters and the capacitor voltages are self-balanced. The proposed topology is suitable for applications with high conversion ratios. A 2.5 kW prototype (800 V/220 V), which achieved a peak efficiency of 97.8%, was built to show the feasibility of the novel inverter.**

Keywords – **High Step-Down Applications, Hybrid Switched-Capacitor, Inverter, Pulse Width Modulated Inverters, Switched-Capacitor.**

I. INTRODUCTION

In single-phase non-isolated applications, voltage source inverters (VSI) are the topologies most commonly used in dc-ac conversion, an example being the full-bridge (FB) inverter [1], which can only synthesize an output voltage lower than the input voltage. However, when the difference between the input and output voltages is high (i.e., high step-down conversion ratio), FB inverter will operate with low performance due to the high voltage stress on the semiconductors. Furthermore, it will operate with a lower modulation index, resulting in a poor switch utilization ratio [2] and an increase in the output voltage total harmonic distortion (THD).

Multilevel converters, such as the neutral point clamped (NPC) inverter [3], reduce the voltage stress on the semiconductors. However, additional control loops are required for the capacitor voltage balancing [4], which increases the costs (due to voltage sensors) and becomes a potential cause of failures at voltage imbalance conditions [5].

Two-stage conversion architectures consisting of a front-end step-down dc-dc converter with a back-end topology can also be employed in high step-down specifications, such as dc-dc topologies for power supply applications [6]. However, multiple-stage solutions can present a high component count, high control complexity and low efficiency, because all of the energy is processed more than once [7]. These architectures [6], [7] use a front-end switched-capacitor (SC) dc-dc converter, which presents a high conversion ratio, low semiconductor voltage stresses and suitability for integrated

circuits implementation. In contrast, SC converters cannot regulate the output voltage with high efficiency [6].

To provide a solution for the aforementioned issues, a single-stage single-phase high step-down hybrid switched-capacitor (HSC) inverter is proposed. The novel topology was generated through the integration of dc-dc SC converters with the FB inverter, hence the term 'hybrid'. Consequently, the advantages of SC converters can be exploited in dc-ac conversion and their drawbacks can be reduced or even eliminated.

Several HSC topologies have been proposed in low power dc-dc [8], [9], ac-dc [10] and dc-ac [11]–[15] conversion. Except for [11], [12], these inverters are not suitable for step-down applications, because they use the SC circuit to generate a multilevel staircase waveform.

Some similar topologies have been proposed as isolated high-frequency inverters for low power dc-dc conversion [7], [8], [16]. However, the inverter proposed in this paper was developed to be applied at higher power levels, for application in, for instance, grid-connected inverters for renewable systems, interruptible power supplies, ac drives, interfaces between high voltage dc and low voltage ac grids and, auxiliary power supplies. Moreover, rather than use a fixed duty-cycle as in [8], the proposed inverter employs a sinusoidal pulse width modulation (SPWM), as reported herein.

The aim of this study was to investigate and evaluate the proposed inverter performance. A detailed study, design issues, comparative analysis, and experimental results are reported herein.

II. PROPOSED TOPOLOGY

A generalized version of the proposed topology, named the full-bridge hybrid switched-capacitor (FBHSC) inverter, can be seen in Figure 1. A half-bridge version was proposed in [12]. The FBHSC is composed of 'n' SC cells ($n \in \mathbb{N}_{\geq 1}$), and controls the power flow between the dc input voltage V_{pn} and an ac load. Table I shows the FBHSC component count.

Regardless of the number of SC cells, all switching states

TABLE I
Component Count for the FBHSC Generalized Version

Description	Value*
Power Switches	$4(n+1)$
Floating Capacitors (Capacitors with even index)	$2n$
Link Capacitors (Capacitors with odd index)	$n+1$

*n is the number of SC cells.

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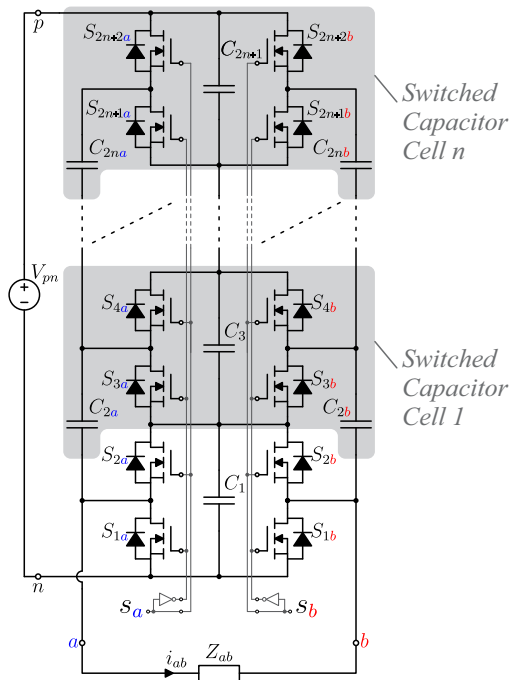
Fig. 1. Proposed single-phase inverter: generalized version with 'n' SC cells.

Fig. 3. FBHSC inverter with a single SC cell ($n = 1$).

can be defined by only two switching functions: s_a (for leg 'a') and s_b (for leg 'b') as follows

$$s_k = \begin{cases} 1, & \text{if } S_{xk} \text{ on and } S_{yk} \text{ off} \\ 0, & \text{if } S_{yk} \text{ on and } S_{xk} \text{ off} \end{cases} \quad (1)$$

where $k \in \{a, b\}$, $x \in \{2, 4, 6 \dots 2n - 2\}$ and $y = x - 1$.

The FBHSC can operate with sinusoidal pulse width modulation (SPWM) with a symmetrical triangular carrier v_{cr}. Both unipolar (Figure 2(a)) and bipolar (Figure 2(b)) SPWM schemes can be employed. A dead time t_d between switches with subsequent index (e.g., S_{1a} and S_{2a}) is required to avoid a short circuit. As in FB inverters, the averaged switching functions d_a and d_b are given by

$$d_a = \langle s_a \rangle = 1 - d_b = 1 - \langle s_b \rangle = \frac{1}{2} + \frac{M}{2} \sin(\omega t) \quad (2)$$

where $\omega = 2\pi f_g$ (f_g in Hertz), t is the time in seconds and M is the modulation index, which can vary from 0 to 1.
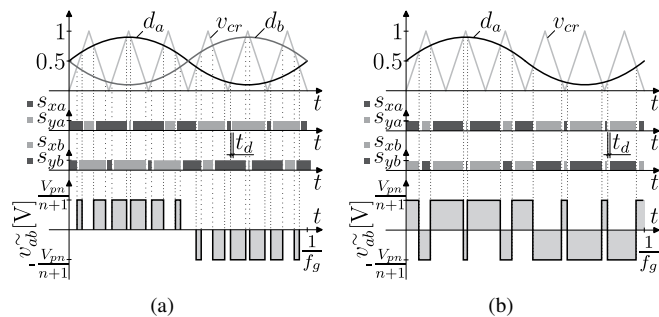

Fig. 2. (a) Unipolar and (b) bipolar SPWM schemes for the FBHSC inverter, where x is an odd index and y is an even index.
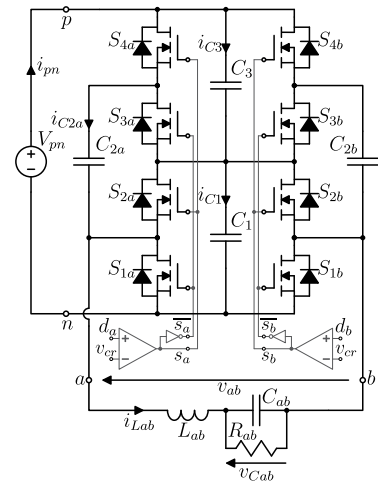
Figure 2 also shows the expected output voltage $v_{ab}^{\sim}$, which is dependent on the input voltage V_{pn} and the number of SC cells n. However, for the sake of simplicity, the topology with one SC cell (shown in Figure 3) will be the focus of this paper. Moreover, the inverter operation of the proposed topology will be focused in this paper, even though the FBHSC can operate as a bidirectional rectifier, a reactive compensator or a active power filter.

III. THEORETICAL ANALYSIS

This section presents the theoretical analysis for the FBHSC (Figure 3). The analysis was performed, unless specified, under the following conditions:

- All components are considered ideal, except for the MOSFETs. These are represented by their on-state resistance while conducting (R_{DSon}). Without parasitic resistances, it is impossible to obtain the model [17];
- High-frequency ripple is neglected for all components;
- The current through the MOSFET, regardless of the direction, will always be conducted by the MOSFET channel instead of the body diode;
- The switching frequency f_{sw} is much higher than the output frequency f_g;
- The low-frequency variables (e.g., i_{Lab}, v_{Cab}) are assumed constant within the switching period T_{sw}; and
- The proposed converter operates in the no-charge (NC) mode (see section IV).

The topology presented in Figure 3 has two linearly dependent states: v_{C1} and v_{C3}. Thus, to obtain a system without redundant states, capacitors C_1 and C_3 will be replaced with an equivalent capacitor C_{1e}, as shown in Figure 4. The relations among these capacitors are defined by

$$\begin{cases} C_{1e} = C_1 + C_3 \\ v_{C1e} = V_{pn} - v_{C3} = v_{C1} \\ \frac{i_{C1}}{C_1} = -\frac{i_{C3}}{C_3} \\ i_{C1e} = i_{C1} - i_{C3} \end{cases} \quad (3)$$

Inverter legs can be analyzed separately. In leg 'a', the FBHSC operation can be described using two modes as follows:
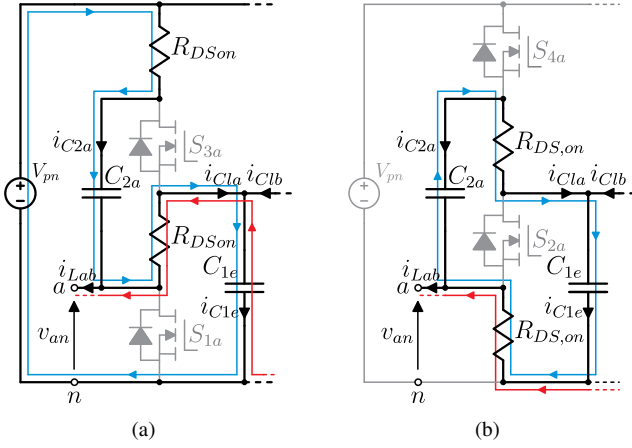
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Fig. 4. FBHSC switching states. (a) $s_a = 1$. (b) $s_a = 0$.

Mode 1 (Figure 4(a)): capacitor C_{1e} is connected to the output port v_{an} supplying the load while capacitor C_{2a} is connected between the voltage source V_{pn} and the capacitor C_{1e}. Assuming a positive output current i_{Lab}, C_{2a} is charging and C_{1e} is discharging. This switching state, which has a duration of $d_a T_{sw}$, can be represented as

$$\begin{cases} i_{C2a} = & \frac{i_{Lab}R_{DSon}-v_{C1e}-v_{C2a}+V_{pn}}{2R_{DSon}} \\ i_{Cla} = & -\frac{i_{Lab}R_{DSon}+v_{C1e}+v_{C2a}-V_{pn}}{2R_{DSon}} \quad , \ 0 < t < d_a T_{sw}. \\ v_{an} = & \frac{(-i_{Lab}R_{DSon}+v_{C1e}-v_{C2a}+V_{pn})}{2} \end{cases} \quad (4)$$

Mode 2 (Figure 4(b)): inductor current i_{Lab} is in the freewheeling state through S_{1a}. The energy stored in C_{2a}, in the previous switching state, is transferred directly to C_{1e}. The instantaneous current through C_{1e} and C_{2a} is limited by R_{DSon}. This switching state, which has a duration of $(1-d_a)T_{sw}$, can be represented as

$$\begin{cases} i_{C2a} = & \frac{i_{Lab}R_{DSon}+v_{C1e}-v_{C2a}}{2R_{DSon}} \\ i_{Cla} = & -\frac{i_{Lab}R_{DSon}+v_{C1e}-v_{C2a}}{2R_{DSon}} \quad , \ d_a T_{sw} < t < T_{sw}. \\ v_{an} = & \frac{(-i_{Lab}R_{DSon}+v_{C1e}-v_{C2a})}{2} \end{cases} \quad (5)$$

The same procedure must be applied to leg 'b'. Furthermore, to obtain the complete system, it is necessary to include equations of the output filter (Figure 5), defined as

$$\begin{cases} L_{ab}\frac{dv_{Lab}}{dt} = & v_{an} - v_{bn} - v_{Cab} \\ C_{ab}\frac{di_{Cab}}{dt} = & i_{Lab} - i_{Load} \end{cases} . \quad (6)$$

To attain a compact representation of the system, all equations will be written in state-space form [18], as follows

$$\dot{\mathbf{x}} = [\mathbf{A_1}d_a + \mathbf{A_2}(1-d_a) + \mathbf{A_3}d_b + \mathbf{A_4}(1-d_b) + \mathbf{F}]\mathbf{x} + \\ [\mathbf{B_1}d_a + \mathbf{B_2}(1-d_a) + \mathbf{B_3}d_b + \mathbf{B_4}(1-d_b) + \mathbf{G}]\mathbf{u} \quad (7)$$
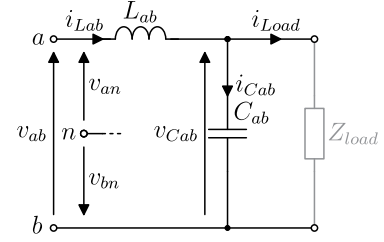

Fig. 5. LC output filter.

where the state and the input vectors[*] ($\mathbf{x}$ and $\mathbf{u}$) are

$$\begin{aligned} \mathbf{x} &= \begin{bmatrix} \langle v_{C1e} \rangle & \langle v_{C2a} \rangle & \langle v_{C2b} \rangle & \langle i_{Lab} \rangle & \langle v_{Cab} \rangle \end{bmatrix}^T \\ \mathbf{u} &= \begin{bmatrix} V_{pn} & \langle i_{Load} \rangle \end{bmatrix}^T \end{aligned} . \quad (8)$$

In the state-space averaged model presented in (7), $\mathbf{A_1}$ is the matrix representation of (4). Likewise, $\mathbf{A_2}$ is the matrix representation of (5). Matrices $\mathbf{A_3}$ and $\mathbf{A_4}$ are the representations of equivalent leg 'b' switching states. Matrices $\mathbf{F}$ and $\mathbf{G}$ represent the output filter, presented in (6). All matrices are presented in the Appendix A.

A. Steady-State Analysis

All steady-state values ("$\rightarrow$") can be found by setting all derivative terms to zero [19], as follows

$$0 = [\mathbf{A_1}d_a + \mathbf{A_2}(1-d_a) + \mathbf{A_3}d_b + \mathbf{A_4}(1-d_b) + \mathbf{F}]\bar{\mathbf{x}} + \\ [\mathbf{B_1}d_a + \mathbf{B_2}(1-d_a) + \mathbf{B_3}d_b + \mathbf{B_4}(1-d_b) + \mathbf{G}]\bar{\mathbf{u}} \quad (9)$$

where the vectors $\bar{\mathbf{x}}$ and $\bar{\mathbf{u}}$ are given by

$$\begin{aligned} \bar{\mathbf{x}} &= \begin{bmatrix} \overline{\langle v_{C1e} \rangle} & \overline{\langle v_{C2a} \rangle} & \overline{\langle v_{C2b} \rangle} & \overline{\langle i_{Lab} \rangle} & \overline{\langle v_{Cab} \rangle} \end{bmatrix}^T \\ \bar{\mathbf{u}} &= \begin{bmatrix} V_{pn} & \overline{\langle i_{Load} \rangle} \end{bmatrix}^T \end{aligned} . \quad (10)$$

From (9) and performing algebraic manipulation, the steady-state values for all capacitor voltages can be found, as follows

$$\begin{cases} \overline{\langle v_{C1e} \rangle} = & \frac{V_{pn}}{2} - \frac{\overline{\langle i_{Load} \rangle}R_{DSon}}{2}\frac{d_a - d_b}{d_a(1-d_a)+d_b(1-d_b)} \\ \overline{\langle v_{C2a} \rangle} = & \frac{V_{pn}}{2} - \frac{\overline{\langle i_{Load} \rangle}R_{DSon}}{2}\frac{d_a(2d_b-1)+(2d_b-3)d_b}{d_a(1-d_a)+d_b(1-d_b)} \\ \overline{\langle v_{C2b} \rangle} = & \frac{V_{pn}}{2} - \frac{\overline{\langle i_{Load} \rangle}R_{DSon}}{2}\frac{d_a(3-2d_b)-2d_a^2+d_b}{d_a(1-d_a)+d_b(1-d_b)} \end{cases} . \quad (11)$$

All capacitor voltages have a constant value ($V_{pn}/2$) plus a term dependent on the output current i_{Load} and the MOSFET on-resistance R_{DSon}. Therefore, by neglecting R_{DSon}, all capacitor voltages are simplified to

$$\langle V_{C1e} \rangle \approx \langle V_{C1} \rangle \approx \langle V_{C3} \rangle \approx \langle V_{C2a} \rangle \approx \langle V_{C2b} \rangle \approx 0.5 V_{pn}. \quad (12)$$

From (12), all capacitor voltages are a half of the input voltage, regardless of the duty-cycle or output current, as in the regular SC converters. Moreover, all voltage across the semiconductors are also given by (12).

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[*]For the sake of simplicity and to avoid the average-value notation "$\langle \rangle$", the input voltage V_{pn} will be assumed constant (i.e., $\langle v_{pn} \rangle = V_{pn}$).
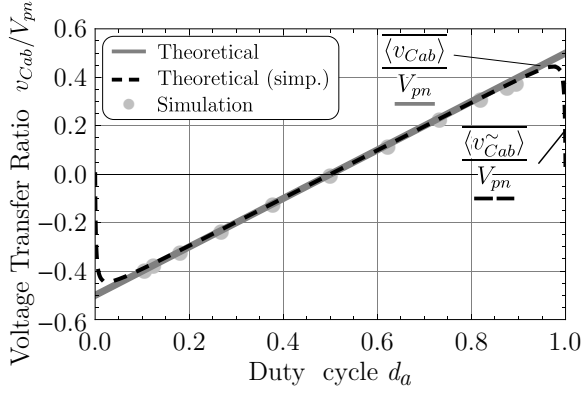
Fig. 6. FBHSC voltage transfer ratio as a function of the duty cycle: analytical model (full and simplified) and numerical simulation.

The steady-state value of the output voltage is given by

$$\overline{\langle v_{Cab}\rangle} = \frac{V_{pn}d_{ab}}{2} - \overline{\langle i_{Load}\rangle}r_{eq} \tag{13}$$

where $d_{ab} = d_a - d_b$ and r_{eq} is defined by

$$r_{eq} = \underbrace{d_{ab}{}^2 \frac{R_{DSon}}{2\left(d_a\left(1-d_a\right)+d_b\left(1-d_b\right)\right)}}_{r_{eq,p}} + \underbrace{2R_{DSon}}_{R_{eq,s}}. \tag{14}$$

The equivalent resistance r_{eq} represents the total conduction loss and its evaluation can be useful to compare the FBHSC performance with other solutions. It can be divided into two terms: $R_{eq,s}$ represents the losses of an equivalent FB inverter whereas $r_{eq,p}$ represents the capacitor balancing losses.

Neglecting R_{DSon}, and recalling that $d_b = 1 - d_a$, the simplified output voltage can be defined as

$$\overline{\langle v_{\widetilde{Cab}}\rangle} = \overline{\langle v_{Cab}\rangle}\big|_{R_{DSon}=0} = \frac{V_{pn}(2d_a - 1)}{2}. \tag{15}$$

Figure 6 shows the voltage transfer ratio of (13) and (15). For the non-simplified result, a resistive load (i.e. $\overline{\langle i_{Load}\rangle} = \overline{\langle v_{Cab}\rangle}/R_{ab}$) was assumed. Also, a set of computational simulations performed in PSIM® was added to the results. All parameters used are shown in Table II.

The FBHSC voltage transfer ratio is almost linear, as shown in Figure 6. Simulation and theoretical results are in excellent agreement. Divergences between the complete and simplified results increase at the duty cycle extremes, where the converter rarely operates. Therefore, considering the whole duty cycle variation, the difference can be neglected. However, if a precise prediction of the output voltage is required (e.g., for deadbeat control), (13) can be used.

B. Dynamic Analysis

To obtain the dynamic model, small-signal analysis will be performed. In the system presented in (7), a small ac perturbation ("^") is summed to the steady-state values, as follows:

$$\begin{aligned}
\overline{\mathbf{x}}+\hat{\mathbf{x}} = &\left[\mathbf{A_1}(d_a+\hat{d}_a)+\mathbf{A_2}(1-d_a-\hat{d}_a)+\mathbf{F}+\right.\\
&+\mathbf{A_3}(d_b+\hat{d}_b)+\mathbf{A_4}(1-d_b-\hat{d}_b)\big](\overline{\mathbf{x}}+\hat{\mathbf{x}})+\\
&\left[\mathbf{B_1}(d_a+\hat{d}_a)+\mathbf{B_2}(1-d_a-\hat{d}_a)+\right.\\
&+\mathbf{B_3}(d_b+\hat{d}_b)+\mathbf{B_4}(1-d_b-\hat{d}_b)+\mathbf{G}\big](\overline{\mathbf{u}}+\hat{\mathbf{u}})
\end{aligned} \tag{16}$$

TABLE II
Components Used in the Prototype and Main Specifications

Description	Symbol	Value
Input Voltage	V_{pn}	800 V
RMS Output Voltage	$V_{Cab,RMS}$	220 V
Output Power	P_o	2500 W
Output frequency	f_g	60 Hz
Power MOSFET	$S_{1a...4b}$	SCT2120AF ($R_{DSon} = 120\ \text{m}\Omega$/ $V_{DS,max} = 650$ V)
Switching Frequency	f_{sw}	30 kHz
Floating Capacitor	C_{2a}, C_{2b}	B32778 (60 µF × 800 V)
Link Capacitor	C_1, C_3	MKP1848 (200 µF × 450 V)
Output Inductor	L_{ab}	900 µH
Output Capacitor	C_{ab}	*2 × B32656S (1 µF × 1000 V)
Output Resistor	R_{ab}	19.36 Ω

* Two capacitors in parallel.

where $\hat{\mathbf{x}}$ and $\hat{\mathbf{u}}$ are the small-signal ac variation vectors of the variables presented in (8). For the sake of simplicity, the small-signal perturbation of the input vector $\hat{\mathbf{u}}$ will be neglected.

After extracting the steady-state values and the second-order nonlinear terms [18] and applying the Laplace transform, a linear model can be found, as follows:

$$\begin{aligned}
\hat{\mathbf{x}} = &\left[s\mathbf{I_5} - \left[\mathbf{A_1}d_a + \mathbf{A_2}(1-d_a) + \mathbf{A_3}d_b + \mathbf{A_4}(1-d_b) + \mathbf{F}\right]\right]^{-1} \cdot\\
&\cdot \left[\hat{d}_a\left[(\mathbf{A_1}-\mathbf{A_2})\overline{\mathbf{x}}+(\mathbf{B_1}-\mathbf{B_2})\overline{\mathbf{u}}\right]\right.\\
&\left.+\hat{d}_b\left[(\mathbf{A_3}-\mathbf{A_4})\overline{\mathbf{x}}+(\mathbf{B_3}-\mathbf{B_4})\overline{\mathbf{u}}\right]\right]
\end{aligned} \tag{17}$$

where $\mathbf{I_5}$ is a 5×5 identity matrix.

After substituting the steady-state values of (9) in (17), solving and performing some algebraic manipulation, the FBHSC transfer functions can be found. The small-signal control-to-output transfer function $G_{vc}(s)$ is defined by

$$G_{vc}(s) = \frac{\langle v\hat{C}ab\rangle}{\hat{d}_{ab}} = \frac{a_2s^2 + a_1s + a_0}{b_4s^4 + b_3s^3 + b_2s^2 + b_1s + b_0} \tag{18}$$

where $C_f = C_{2a} = C_{2b}$ and the coefficients are given by

$$\left\{\begin{aligned}
a_2 &= 4C_{1e}C_f(d_a-1)d_aR_{DSon}^2V_{pn}\\
a_1 &= R_{DSon}\begin{pmatrix}2(d_a-1)d_a(C_{1e}+2C_f)V_{pn}+\\+C_{1e}\overline{\langle i_{Load}\rangle}(2d_a-1)R_{DSon}\end{pmatrix}\\
a_0 &= -8d_b{}^2d_a^2V_{pn}+2\overline{\langle i_{Load}\rangle}(2d_a-1)R_{DSon}\\
b_4 &= 8C_{1e}C_f(d_a-1)d_aC_{ab}L_{ab}R_{DSon}^2\\
b_3 &= 4(d_a-1)d_aC_{ab}R_{DSon}\begin{pmatrix}L_{ab}(C_{1e}+2C_f)+\\+2C_{1e}C_fR_{DSon}^2\end{pmatrix}\\
b_2 &= -8d_bd_a\begin{pmatrix}R_{DSon}^2\left(C_{ab}(C_{1e}+C_f)+C_{1e}C_f\right)+\\+2d_bd_aC_{ab}L_{ab}\end{pmatrix}\\
b_1 &= 4(d_a-1)d_aR_{DSon}\begin{pmatrix}(1+4d_bd_a)C_{ab}+\\+C_{1e}+2C_f\end{pmatrix}\\
b_0 &= -16(d_a-1)^2d_a^2
\end{aligned}\right. \cdot \tag{19}$$

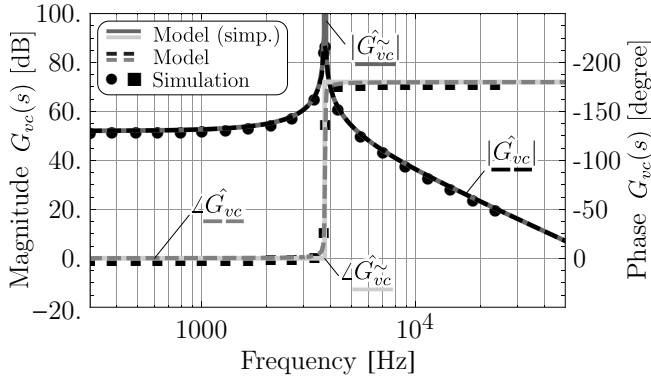The 4$^{\text{th}}$ order system obtained in (18) can be simplified by

Fig. 7. Frequency responses of the control-to-output transfer function $G_{vc}(s)$: analytical model (full and simplified) and numerical simulation.

neglecting the MOSFET on-resistance R_{DSon}, as follows

$$G_{vc}^{\sim}(s) = G_{vc}(s)|_{R_{DSon}=0} = \frac{\frac{V_{pn}}{2}}{s^2 C_{ab} L_{ab} + 1}. \tag{20}$$

Apart from the numerator $V_{pn}/2$, the transfer function (20) is the same as that of a FB inverter with an LC output filter. Therefore, conventional compensator design can be applied in the proposed topology to perform the output voltage control.

To validate the simplified model, a set of numerical simulations was performed in PLECS$^\circledR$ with the parameters shown in Table II. The frequency responses of the simulated and theoretical results are given in Figure 7.

The frequency responses presented in Figure 7 show excellent agreement between the theoretical and simulation results. Therefore, it can be concluded that the switching capacitor dynamics can be neglected without loss of generality, as presented in [10], [20]. As a consequence, a simplified state-space system can be proposed, as follows

$$\dot{\mathbf{x}} = \begin{bmatrix} 0 & \frac{-1}{L_{ab}} \\ \frac{1}{C_{ab}} & 0 \end{bmatrix} \underbrace{\begin{bmatrix} \langle i_{Lab} \rangle \\ \langle v_{Cab} \rangle \end{bmatrix}}_{\mathbf{x}} + \begin{bmatrix} \frac{1}{L_{ab}} & 0 \\ 0 & \frac{-1}{C_{ab}} \end{bmatrix} \begin{bmatrix} \langle v_{ab} \rangle \\ \langle i_{Load} \rangle \end{bmatrix} \tag{21}$$

where the voltage v_{ab} is defined by

$$\langle v_{ab} \rangle = \frac{M V_{pn}}{2} \sin(\omega t). \tag{22}$$

The model detailed in (21) is a large signal model, as used in conventional inverter modelling. Since the simplified model is the matrix representation of the output filter, the dynamic model for other output filter topologies (e.g., L, LCL filters) can be easily deduced.

IV. DESIGN CONSIDERATIONS FOR THE FLOATING CAPACITORS

Apart from the well-known design criteria (e.g. current stress, voltage ripple), FBHSC floating capacitors must also be designed considering the charge/discharge in the switching period, as in SC design [21]. Otherwise, a high peak current will flow through the components, increasing FBHSC losses.
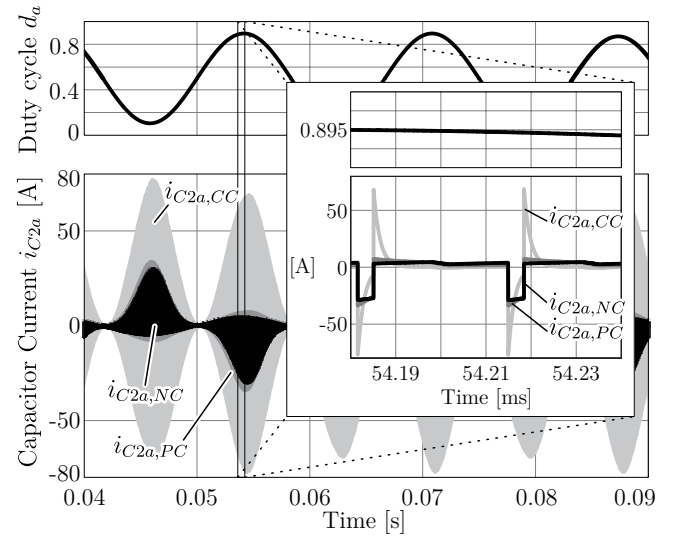

Fig. 8. Simulation results for τ_f effect on the capacitor current i_{C2a} for all SC operation modes: CC, PC and NC.

Maximum instantaneous peak current in the capacitors is dependent on the floating capacitor value, the MOSFET on-resistance value, the modulation index M and the switching period T_{sw}. Depending on these values, the converter can operate in three modes: complete charge (CC), partial charge (PC) and no charge (NC) [21].

As stated in section III, theoretical analysis was performed assuming NC mode. However, NC mode operation requires a high switching frequency or a high capacitance value, resulting in a difficult design process. Thus, the PC mode was selected because it ensures low peak current in capacitors, avoids large capacitance values and provides a small error compared to the NC mode [20], [22]. The PC operation mode, assuming unipolar SPWM, is guaranteed when

$$2R_{DSon}C_f \approx \tau_f > \frac{M T_{sw}}{2} \tag{23}$$

where $C_{2a} = C_{2b} = C_f$, and assuming $C_1 \gg C_f$.

An example of the floating capacitor design is shown in Figure 8. All parameters are given in Table III, except for the floating capacitors. The operation in the other operation modes was obtained with $C_{2a} = C_{2b} = 6\,\mu F$ (CC mode) and $C_{2a} = C_{2b} = 400\,\mu F$ (NC mode). The PC operation mode was obtained with $C_{2a} = C_{2b} = 60\,\mu F$, resulting in a time constant $\tau_f \approx 14.4\,\mu s$.

Even though the peak current through C_{2a} in the NC mode (29.26 A) is lower than that in the PC mode (34.12 A), the PC mode capacitance is six times lower. In addition, the i_{C2a} RMS values in the two modes ($I_{C2a,NC,RMS} = 5.69$ A, $I_{C2a,PC,RMS} = 5.83$ A) are similar. However, the CC mode must be avoided due to its high peak current (78.56 A) and high RMS value (9.27 A).

As shown in Table II, it was employed capacitors of 60 μF to the floating capacitors (C_{2a} and C_{2b}), which fulfills the current stress criteria and ensure the PC mode operation. On the other hand, the link capacitors (C_1 and C_3) should be greater than the floating capacitors and fulfill the current stress criteria. Moreover, the link capacitors should limit the well-known low-frequency voltage ripple present in single-phase
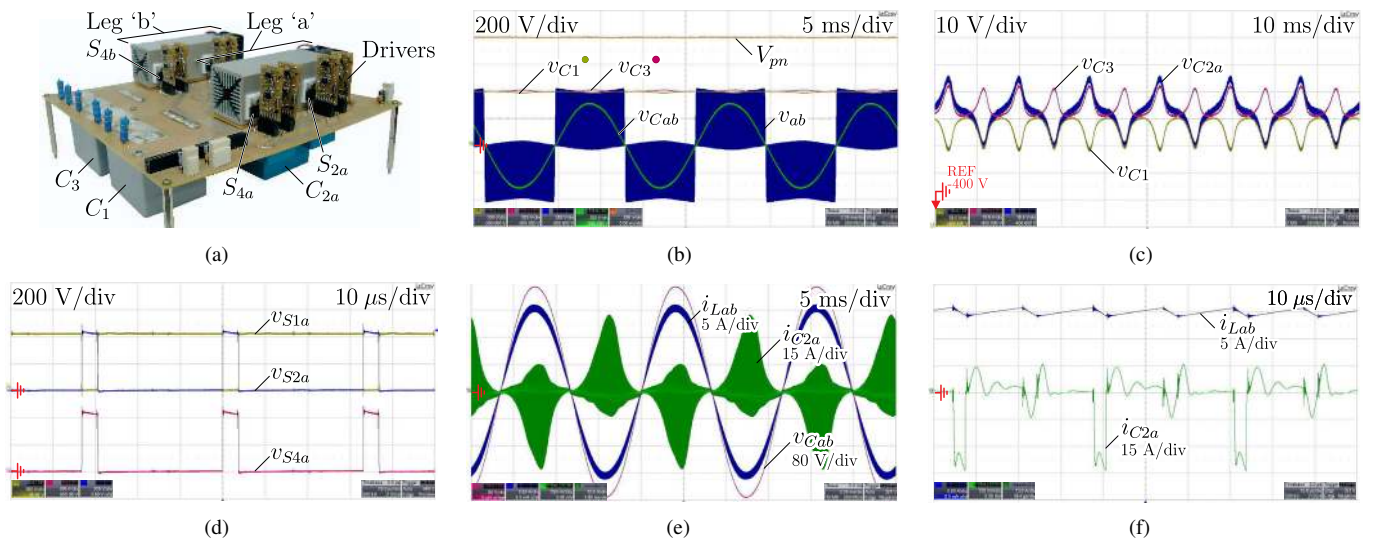
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Fig. 9. Picture of the prototype and experimental results for the converter at nominal output power (2.5 kW). (a) Implemented 2.5-kW FBHSC hardware prototype (mechanical dimensions: 238 mm x 246 mm x 115 mm). (b) Input voltage V_{pn}, capacitor voltages v_{C1}, v_{C3} and v_{C2a} and output voltage v_{Cab}. (c) Detailed view of v_{C1}, v_{C3} and v_{C2a}. (d) Semiconductor voltages v_{S1a}, v_{S2a} and v_{S4a}. (e) Inductor current i_{Lab}, floating capacitor current i_{C2a} and output voltage v_{Cab}. (f) Detailed view of i_{Lab} and i_{C2a}.

systems [23], which is defined by

$$\Delta V_\% = \frac{P_o}{4\pi f_g V_{pn}^2 C_{link}} \qquad (24)$$

where $\Delta V_\%$ is the percentage of ripple on the input voltage.

Assuming $\Delta V_\% = 4\%$, a capacitance of approximately 130 μF is obtained by (24). Therefore, the dc-link was implemented with two capacitors of 200 μF connected in series, which complemented with the floating capacitors [22] fulfills the required voltage ripple.

V. EXPERIMENTAL RESULTS

A single-SC-cell 2.5-kW FBHSC prototype, as shown in Figure 9(a), was built to evaluate and verify the concepts introduced above. All tests were carried out in open loop, with a modulation index of approximately 0.79 using unipolar SPWM, and with a resistive load, as seen in Figure 3. FBHSC gating signal generation was performed by a microcontroller TMS320F28027, developed by Texas Instruments. All components used in the prototype and the specifications can be found in Table II.

As the converter operates in open loop, the input voltage V_{pn} was generated by a regulated dc source. However, any control structure applied to VSI inverters (e.g., current control in the inner loop and dc-link control in the outer loop) can be employed.

Due to the low semiconductor voltage stress, silicon carbide (SiC) low-voltage (e.g., 650 V) devices could be used. SiC was also chosen due to its better performance and lower switching losses. With regard to the capacitors, only polypropylene film capacitors were employed in the prototype, due to their high current capability and better reliability, when compared to the aluminum electrolytic capacitors. On the other hand, film capacitors have a higher cost and lower

energy density, leading to a large volume to obtain the needed capacitance [24]. However, due to its low equivalent series resistance (ESR) and the high current stresses common in SC converters, film capacitors can achieve a higher lifetime than the aluminum electrolytic capacitors.

The waveforms in Figures 9(b)-9(f) show the operation at nominal output power. The high step-down inverter operation can be seen in Figure 9(b), which shows all voltages in the same scale, including the switched (v_{ab}) and filtered (v_{Cab}) output voltage. All capacitor voltages are equal to half of the input voltage plus a small ripple (less than 7% of $V_{pn}/2$), as shown in Figure 9(c). Consequently, it is expected that the voltages across the semiconductors are limited to the same value, as seen in Figure 9(d), which shows the voltages v_{S1a}, v_{S2a} and v_{S4a}.

Figure 9(e) shows the inductor current, the output voltage and the current through the floating capacitor C_{2a}. As expected, the inductor current and the output voltage are sinusoidal, with a negligible displacement angle. Even though the peak current in the capacitor C_{2a} is less than 3 times the peak current at the output, the RMS value is less than 60% (6.68 A) of the inductor current.

A detailed view of the current i_{C2a} (Figure 9(f)) shows the behavior within the switching period, where it can be observed that the converter operates in the PC mode. However, the exponential behavior cannot be clearly seen due to the switching transition resonances, which were probably caused by the parasitic inductances and the PCB layout.

The FBHSC was also tested as a inverter with different types of loads (inductive and nonlinear) and as a rectifier. The parameters are the same presented in Table II, except for the output filter ($L_{ab} = 470$ μH and $C_{ab} = 8$ μF) in all cases, and the switching frequency (50 kHz) at the rectifier and nonlinear load tests. The experimental results are presented in Figure 10.

Figure 10(a) presents the output voltage v_{Cab} and the output load current i_{Load} for a 2245 VA inductive load with
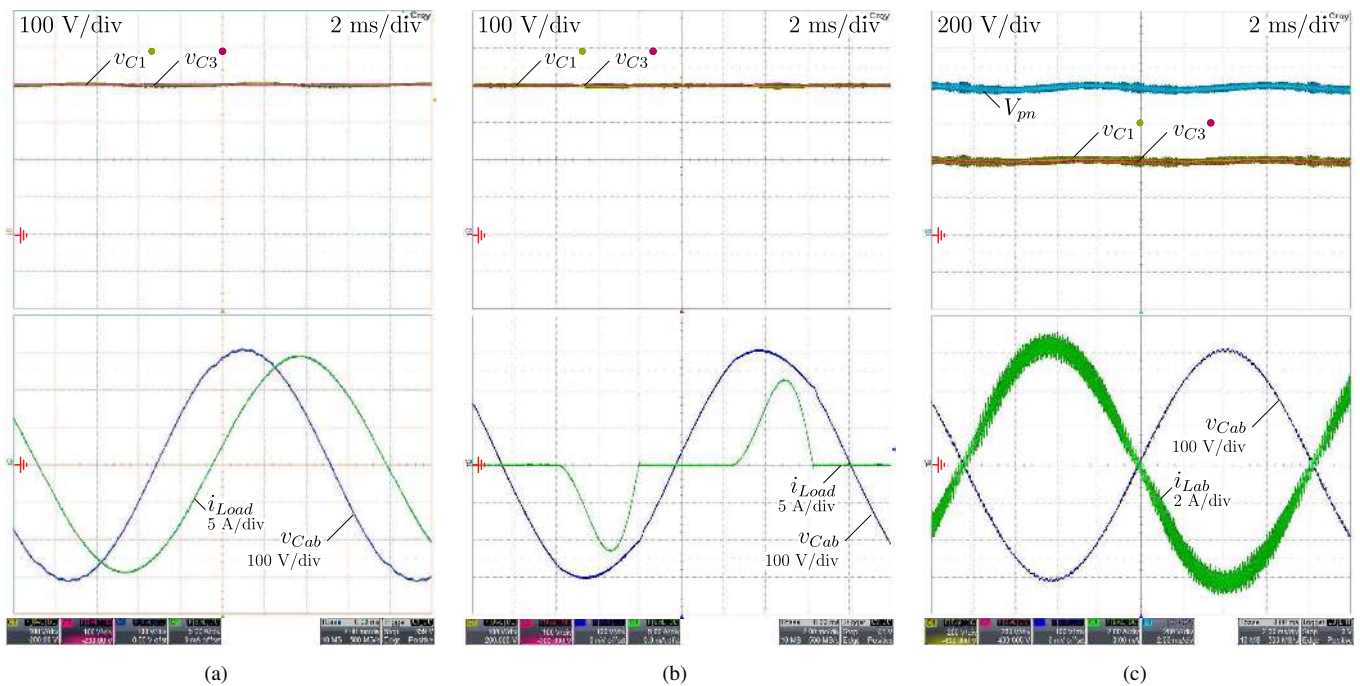
Fig. 10. Experimental results of the proposed converter operating with different loads. (a) Inductive load operation: capacitor voltages v_{C1} and v_{C3}, output voltage v_{Cab}, and load current i_{Load}. (b) Nonlinear load operation: capacitor voltages v_{C1} and v_{C3}, output voltage v_{Cab}, and load current i_{Load}. (c) Rectifer operation: input voltage V_{pn}, capacitor voltages v_{C1} and v_{C3}, output voltage v_{Cab} and output inductor current i_{Lab}.

a power factor of 0.504. The nonlinear load test, presented in Figure 10(b), was performed with a 1100 VA load with a crest factor of 2.25. At the nonlinear load operation, it is important to analyze the maximum peak current at the semiconductors, since the semiconductor currents is higher than the output current. In both tests, the converter operates properly with low output voltage distortion and maintaining the self-balancing in the capacitors.

Figure 10(c) presents the results with the converter operating as a rectifier. The rectifier operation was achieved by a self-control strategy [25], [26], adapted to the single-phase full-bridge rectifier. The converter was supplied by an ac power source (Agilent 6813B) in order to supply a 970 W resistive load. The self-control constant was adjusted to keep the nominal input (800 V) and output voltage (220 V), as shown in Figure 10(c). As the previously results, the FBHSC operates properly, validating the four-quadrant operation.

The capacitor voltage balancing was evaluated under load variation conditions. The response for a resistive load step from 15% to 100% is shown in the waveform of Figure 11, and the capacitor voltages v_{C1}, v_{C3} and v_{C2a} are also shown. Even with a step from a light load to a full load condition, all capacitor voltages remain balanced.

Figure 12 shows the converter efficiency experimentally obtained using the power analyzer WT-1800 (Yokogawa Electric) with resistive load and excluding the output filter losses. The prototype was tested under different switching frequencies in order to verify the best operation point, which was observed to be at 30 kHz. An efficiency of 96.03% at full load (peak of 97.8% for a load of $0.403P_o$) was obtained, which is in good agreement with similar results reported in the literature [27].

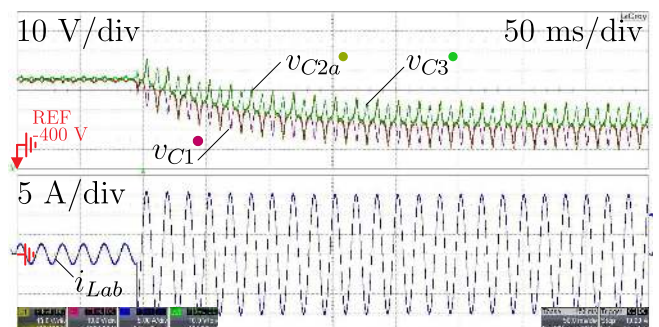Fig. 11. Experimental step response of the output current i_{Lab} after a load step from 15% to 100% of the output power. Capacitor voltages (v_{C1}, v_{C3} and v_{C2a}) are also shown.
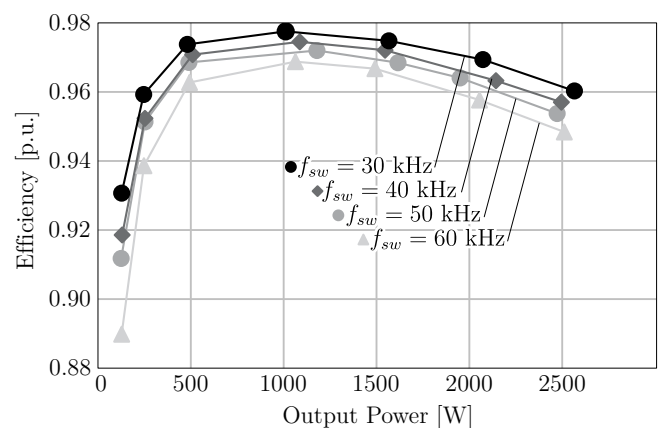

Fig. 12. Efficiency curve for the converter as a function of the output power obtained experimentally (excluding output filter losses).

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VI. TOPOLOGY COMPARISON

This section presents a comparison between the proposed topology and some of the well-known solutions available in the literature: FB, HB (half-bridge), HB-NPC, FB-NPC inverters, and a two-stage architecture (dc-dc bidirectional buck converter plus a FB inverter). Table III presents the results of the comparison, in relation to the specifications given in Table II.

The comparison was performed through some simple metrics. The number of switches (n_s), diodes (n_d), and capacitors (n_{cap}) were analyzed and grouped according to the blocking voltage. For the topologies with a capacitor divider, it is important to analyze the low-frequency harmonics of the current injected at the midpoint '$i_{mid,LF}$', because this can require a high capacitance value for the capacitor divider [28]. The requirement of an additional control loop for the capacitor voltages and the inverter modulation index M are also considered. The output filter components are excluded from this analysis.

Both HB and FB inverters have the lowest component count. However, all switches are subjected to the full input voltage. Apart from the increase in switching losses, the use of high-voltage switches can yield an increase in conduction losses. For silicon high-voltage MOSFETs ($V_{DS,max} \geq 600$ V), R_{DSon} is approximately proportional to the square of the breakdown voltage [29]. On the other hand, FBHSC uses only low-voltage devices, leading to low switching losses and low conduction losses. However, a high semiconductor count, as is the case for the FBHSC inverter, result in a high number of isolated gate-driver circuits, increasing the PCB area and the costs. To alleviate this drawback, some bootstrap techniques can be employed at the FBHSC to reduce the number of gate drive circuits [30].

Based on Table III, HB-NPC can be considered a notable candidate, due to its low component count with low voltage devices. However, HB-NPC has a low-frequency current in the midpoint (worst case in the HB inverter), leading to a high capacitance value. Although the FB-NPC solves the midpoint current issue, both NPC solutions require a voltage control loop for the capacitor voltage balancing, resulting in additional sensors. Although FBHSC has more capacitors, the midpoint current is negligible and the voltages across the capacitors are self-balanced. However, FBHSC achieves self-balancing with

the drawback of additional losses (see section III-A).

Low-modulation-index operation, as occurs in FB and FB-NPC, must be avoided because it leads to a higher THD on the output voltage. FB-NPC, for example, when operating with $M \approx 0.38$ will synthesize only a 3-level voltage, rather than a 5-level voltage. This issue can be resolved through the addition of an output low-frequency step-down autotransformer, which increases the converter volume and weight. FBHSC avoids the need for the use of auto-transformers, since it can synthesize a low ac voltage with a high modulation index. The SC circuit can be seen as an electronic dc-dc autotransformer integrated to an inverter in the proposed topology.

FBHSC can be considered a strong candidate in high step-down applications. Even though FBHSC has a high component count, its features such as low-voltage devices and capacitors with self voltage balancing provide some compensation for its drawbacks. The additional losses, due to capacitor balancing, have a minimal effect on the overall FBHSC losses, reaching a maximum efficiency of 97.08% with the built prototype.

VII. CONCLUSIONS

In this paper, a novel single-phase inverter topology (FBHSC) was proposed. With the use of low-voltage devices and no additional voltage control loop, the FBHSC can synthesize a low ac voltage from a high dc input voltage. Hence, the FBHSC is suitable for high step-down applications, where the conventional topologies (e.g., FB inverter) cannot operate properly. The FBHSC inverter also includes the following features:

- Single-stage topology with bidirectional power flow;
- Operation in high step-down applications with a high modulation index;
- All switches and capacitors are subjected to half of the input voltage (for one SC cell), leading to low switching and conduction losses;
- The capacitor voltages are naturally self-balanced through the switching states. In addition, the voltage ripple is negligible and the output current control does not provoke imbalance in the capacitors.
- The topology can be generalized by the addition of more SC cells;
- Regardless of the number of SC cells, FBHSC has a low-order dynamic model, resulting in a conventional compensator design;
- FBHSC has a simple modulation strategy, the same as that used in the conventional FB Inverter;

With the built prototype, an efficiency of 96.08% (peak of 97.8%) in a high-conversion-ratio specification was achieved. Although other solutions could be applied to high step-down applications, the FBHSC overall performance makes the solution proposed herein a noteworthy candidate.

ACKNOWLEDGEMENTS

TABLE III
Comparison of Topologies for High Step-Down Applications

Topology	Component count					Midpoint current $i_{mid,LF}$	Capacitor balance Loop?	Modul. Index M
	n_s @ V_{pn}	n_s @ $\frac{V_{pn}}{2}$	n_d @ $\frac{V_{pn}}{2}$	n_c @ V_{pn}	n_c @ $\frac{V_{pn}}{2}$			
FBHSC	0	8	0	0	4	≈ 0	no	≈ 0.78
FB	4	0	0	1	0	-	no	≈ 0.39
HB	2	0	0	0	2	i_{Load}	no	≈ 0.78
HB-NPC	0	4	2	0	2	$Ki_{Load}{}^a$	no	≈ 0.78
FB-NPC	0	8	4	0	2	≈ 0	yes	≈ 0.39
Buck[b] +FB	2	4	0	1	1	-	no	≈ 0.78

[a] Where $K = 1 - |M\sin(\omega t)|$.
[b] The dc-dc buck converter operates with a duty-cycle of 0.5.

APPENDIX

A. State-Space Matrices

The matrices in (7) are defined in (25) to (31).

$$\mathbf{A_1} = \begin{bmatrix} \frac{-1}{2C_{1e}R_{DSon}} & \frac{-1}{2C_{1e}R_{DSon}} & 0 & -\frac{1}{2C_{1e}} & 0 \\ \frac{-1}{2C_{2a}R_{DSon}} & \frac{-1}{2C_{2a}R_{DSon}} & 0 & \frac{1}{2C_{2a}} & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{1}{2L_{ab}} & -\frac{1}{2L_{ab}} & 0 & \frac{R_{DSon}}{-2L_{ab}} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (25)$$

$$\mathbf{A_2} = \begin{bmatrix} \frac{-1}{2C_{1e}R_{DSon}} & \frac{1}{2C_{1e}R_{DSon}} & 0 & \frac{-1}{2C_{1e}} & 0 \\ \frac{1}{2C_{2a}R_{DSon}} & \frac{-1}{2C_{2a}R_{DSon}} & 0 & \frac{1}{2C_{2a}} & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{1}{2L_{ab}} & -\frac{1}{2L_{ab}} & 0 & \frac{R_{DSon}}{-2L_{ab}} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (26)$$

$$\mathbf{A_3} = \begin{bmatrix} \frac{-1}{2C_{1e}R_{DSon}} & 0 & \frac{-1}{2C_{1e}R_{DSon}} & \frac{1}{2C_{1e}} & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{-1}{2C_{2b}R_{DSon}} & 0 & \frac{-1}{2C_{2b}R_{DSon}} & \frac{-1}{2C_{2b}} & 0 \\ \frac{-1}{2L_{ab}} & 0 & \frac{1}{2L_{ab}} & \frac{R_{DSon}}{-2L_{ab}} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (27)$$

$$\mathbf{A_4} = \begin{bmatrix} \frac{-1}{2C_{1e}R_{DSon}} & 0 & \frac{1}{2C_{1e}R_{DSon}} & \frac{1}{2C_{1e}} & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{1}{2C_{2b}R_{DSon}} & 0 & \frac{-1}{2C_{2b}R_{DSon}} & \frac{-1}{2C_{2b}} & 0 \\ \frac{-1}{2L_{ab}} & 0 & \frac{1}{2L_{ab}} & \frac{R_{DSon}}{-2L_{ab}} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (28)$$

$$\mathbf{B_1}^T = \begin{bmatrix} \frac{1}{2C_{1e}R_{DSon}} & \frac{1}{2C_{2a}R_{DSon}} & 0 & \frac{1}{2L_{ab}} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \mathbf{B_2} = 0\mathbf{I}_{5\times2} \quad (29)$$

$$\mathbf{B_3}^T = \begin{bmatrix} \frac{1}{2C_{1e}R_{DSon}} & 0 & \frac{1}{2C_{2b}R_{DSon}} & \frac{-1}{2L_{ab}} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \mathbf{B_4} = 0\mathbf{I}_{5\times2} \quad (30)$$

$$\mathbf{F} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{L_{ab}} \\ 0 & 0 & 0 & \frac{1}{C_{ab}} & 0 \end{bmatrix}, \mathbf{G}^T = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{C_{ab}} \end{bmatrix} \quad (31)$$

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