A SINGLE–PHASE INVERTER BASED ON FULL–BRIDGE MODULES WITH INPUTS IN SERIES–CONNECTION AND OUTPUTS COUPLED BY A MULTIPLE–WINDING TRANSFORMER

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***Abstract* – This paper proposes an isolated modular single–phase inverter for high–input voltage applications. The topology is composed of conventional and modular full–bridge inverters with series–connected inputs and magnetically–connected outputs. All input bus capacitors are connected in series and thus the dc voltage is divided among the inverter modules. The full–bridge outputs are connected by a multiple–winding low–frequency transformer, the inverters employ a typical three–level modulation with phase–shift carriers and when an appropriate modulation is used a multilevel output voltage is supplied for the load. The auto–balance of the input capacitor voltages is verified and a harmonic analysis is performed in order to investigate the exchange of active and reactive power between the inverter modules at low and high frequency. An 8 kW prototype with three modules, a multiple–winding transformer with a transform ratio of 1:1:1:1, 1200 V dc input source and 220 V/ 60 Hz ac output voltage was built and tested in order to verify the proposed topology.**

***Keywords* – High–input Voltage, Magnetically–connected Outputs, Multilevel Inverter, Multiple–winding Transformer, Series–connected Inputs.**

I. INTRODUCTION

In recent years, the use of applications that employ high voltage, dc voltage and a power converter has been increasing, which has encouraged new solutions in the field of power electronics. In this context, a class of high–input low–output voltage converters with low voltage stress, high output current capacity and modular construction has been researched for application to distributed power generation, energy storage, traction systems and electrical vehicles [1], [2].

Solutions based on traditional multilevel converters such as the neutral point clamped (NPC) inverter, flying capacitor (FC) converter, cascaded H–bridge (CHB) inverter and modular multilevel converter (MMC) [3], [4] have been used in these applications. However, there is still considerable opportunity for new contributions and, recently, novel topologies have been proposed for drives [5], single–phase structures [6], electrical vehicles [7] and modular systems [8]. Modular solutions are well received by researchers in academia and industry due to their design, reliability and cost [9].

On the other hand, in the case of high voltage, a common solution is the use of multiple standardized power modules with the inputs connected in series in order to divide the voltage stress. The outputs can be connected in parallel or in series according to the application [10]–[12]. This architecture has been used in a rectifier [11], inverters [13] and other applications, in which the main challenge is to ensure an appropriate voltage division among the converters [11], [13], [14].

In this context, this paper proposes a multilevel modular isolated single–phase inverter for powering a load at low voltage from a high dc voltage source. The inverter is based on the series connection of a single–phase H–bridge modular converter that divides the voltage stress. The structure allows the auto–balancing of the input voltage in each module, which makes this a very attractive option. The architecture employs a multiple–winding transformer, which connects the outputs of the H–bridge modular converters via a magnetic connection. Magnetic elements such as multiple–winding transformers or electric machines with open–end winding as well as split windings present interesting characteristics [15]–[17] which can be used in UPS systems [18], [19] and drives. The inverter can also provide multilevel output voltage and fault tolerance when an appropriate modulation is used [20]. An 8 kW–prototype was built and tested for 1200 V in dc voltage and 220 V RMS in output voltage. The prototype is comprised of three sub–modules with series–connected inputs and the outputs are magnetically connected by a multiple–winding transformer. A detailed analysis of the proposed converter and experimental results are reported herein.

II. PROPOSED CONVERTER

A single-phase version of the proposed converter with three full–bridge inverters is presented in Figure 1a. The proposed converter is based on the input–series connection of low voltage full–bridge inverters and output–magnetic connection. Full–bridge inverters with in–series inputs reduce the voltage stress on the switches, providing a characteristic associated with a multilevel converter which is appropriate for application with high dc voltage and has a modular structure (one full–bridge is designed as a sub–module). The output connection based on magnetic coupling is the key factor of the proposed converter and it acts as an interface between the full–bridge modules and the load. The magnetic connection allows

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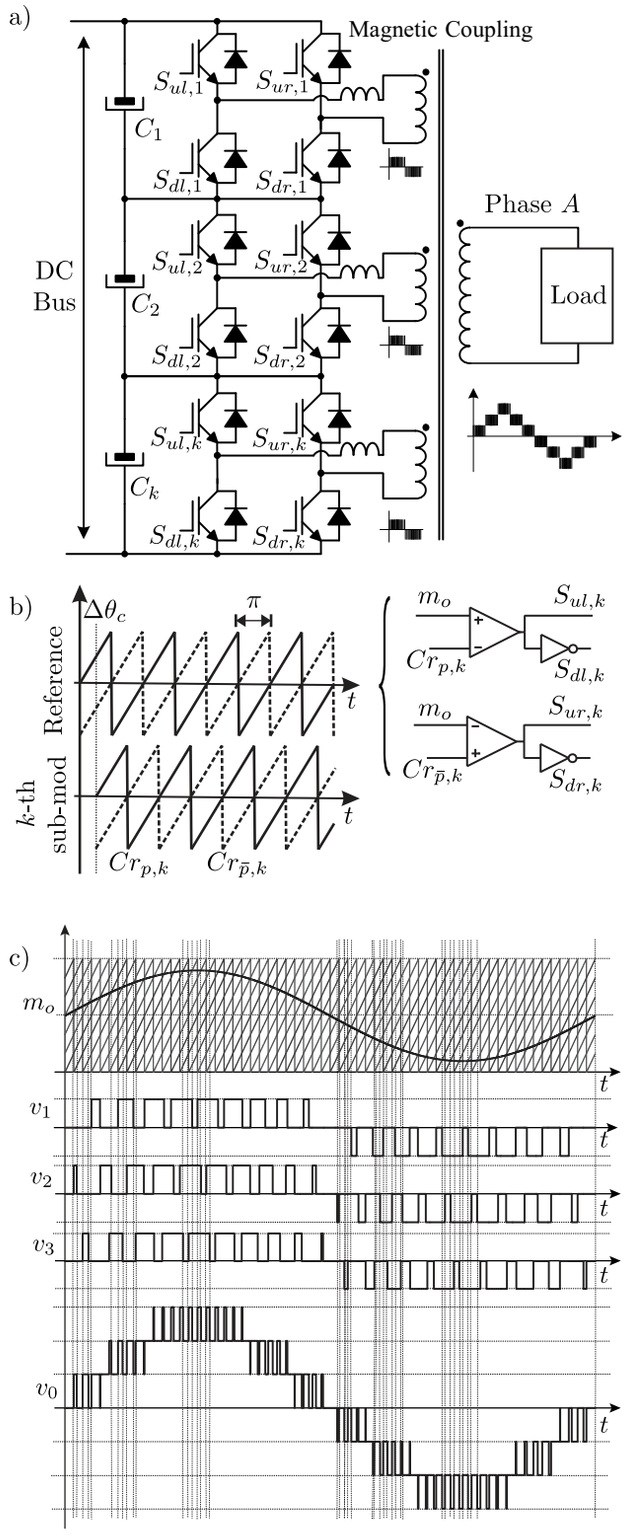

Fig. 1. a) Proposed converter with three sub–modules (*u = upper; d = down; l = left; r = right; k = k–th cell;*). b) PWM generation logic (for each sub–module) with sine–sawtooth modulation and carrier phase delay (p and $\bar{p} = p + \pi$) schematic. c) Output waveform v_0 generated with the combination of inverter voltages (v_1, v_2 and v_3) and sine–sawtooth modulation with carrier phase delay.

the load–current sharing among the modules (as a parallel connection) and it also provides the output voltages of the full–bridge modules. If the output voltages of full–bridge modules are appropriately lagged, the voltage applied on the load will present multilevels (some harmonics are canceled), which represents another characteristic of a multilevel converter (as illustrated in Figure 1a).

The output voltage in each sub–module is a traditional three–level voltage that can be obtained by one reference wave and two carrier signals (triangular or sawtooth). Figure 1c shows the operation of the modulator, the generation of the three–level output voltage in each sub–module and, most importantly, the composition of the output voltage on the load due to magnetic coupling for three sub–modules. This figure demonstrates that an adequate modulation can provide multilevel output voltage through the canceling of harmonics. This characteristic is obtained when the carrier waveforms of the modules are appropriately lagged in relation to each other (for three modules the phase–shift is 120°, as shown in Figure 1c), which causes the canceling of harmonics in the transformer.

Figure 1b illustrates the circuit employed to generate the sinusoidal PWM signals using as a reference a waveform with fundamental frequency f_o (rad/sec) and phase θ_o. This reference is then compared with a sawtooth carrier with frequency f_c (rad/sec) and phase θ_c generating the sinusoidal phase–shifted PWM modulation signals. The carrier phase shift between modules is given by $\Delta\theta_c = (k-1)\frac{\pi}{m}$ rad, where k is the inverter index. This index should be determined in order to obtain the desired number of levels in the output voltage.

The main challenges associated with the proper operation of the proposed converter are to:

- Equate the converter operation point in order to specify the design requirements;
- Ensure voltage balance in the input capacitors that are series–connected;
- Avoid the exchange of active and reactive average power between the sub–modules;
- Obtain the canceling of harmonics through magnetic coupling, which provides multilevel output voltage.

All of these challenges will be discussed in this paper.

III. COMPARISON WITH OTHER FULL–BRIDGE CONFIGURATIONS

A brief comparison of four configurations based on a full–bridge structure is presented in this section. The configurations are shown in Figure 2, where Figure 2a presents a multiple isolated dc input source with a non–isolated ac output connected in series (cascaded), Figure 2b shows a single dc source with full–bridge inputs in parallel connection and isolated ac output with three transformers, Figure 2c illustrates a single dc source with full–bridge inputs in parallel connection and an isolated ac output with a single (coupled output connection) transformer and Figure 2d shows the single dc source with full–bridge inputs in series connection and an isolated ac output with a single (coupled output connection) transformer.

With the use of the same device technology and switching frequency, the losses can be associated with voltage and

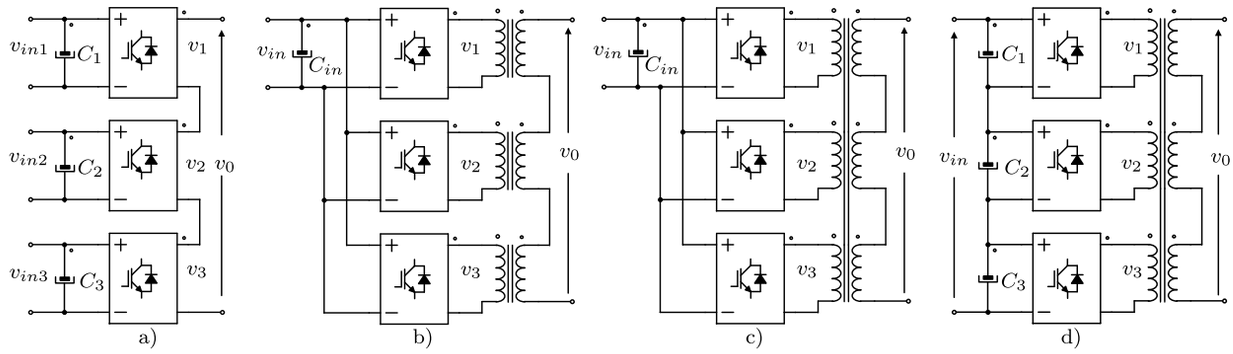

Fig. 2. a) Multiple isolated dc input sources with non–isolated ac series–connected output (cascaded). b) Single dc source with H–bridge inputs in parallel connection and isolated ac output with three transformers. c) Single dc source with H–bridge inputs in parallel connection and isolated ac output with single (coupled output connection) transformer. d) Single dc source with H–bridge inputs in series connection and isolated ac output with single (coupled output connection) transformer.

current levels. Series association distributes the voltage between submodules, while the combination in parallel distributes the current. A high current leads to conduction losses, while a high voltage results in switching losses.

Having a single DC source at the input (Figures 2b, 2c and 2d) appears to be a great advantage over the cascade (Figure 2a), but it requires galvanic isolation at the output of the modules, for some applications. The need for galvanic isolation is not necessarily a disadvantage, since in most applications as a cascade converter (Figure 2a), low–frequency transformers are used to obtain multiple dc sources at the entrance.

The topology has the same number of levels (voltages and symmetrical transformation ratio), but the harmonic content or total harmonic distortion (THD) is directly linked to modulation strategy employed.

A critical aspect of the structure shown is the number of capacitors used, and in this regard topologies with input parallel association (Figure 2b and 2c) offer advantages.

Input voltage division with the association of sub–modules in series enables the use of this structure in high–voltage direct current (HVDC) and its auto assessment since the magnetic coupling present at the output of the inverters can be considered as the main characteristics of the proposed topology (Figure 2d).

IV. STEADY STATE ANALYSIS FOR THREE MODULES AT THE FUNDAMENTAL FREQUENCY

This subsection presents a method for solving the system in order to obtain inverter output currents and voltages for analysis and design. In the case studied, three inverters with an ideal transformer (transform ratio of n_1, n_2 and n_3), as shown in Figure 3, were analyzed. A system of equations can be obtained, as shown in (1), for each inverter voltage with the same angle ($\varphi_1 = \varphi_2 = \varphi_3 = 0$) and applying a resistive load R_0, where R_k is the conductor resistance and L_k is the output series inductance for each inverter ($k = 1, 2, 3, \ldots, m$).

$$-n_1 V_1 + R_1 i_1 + L_1 \frac{di_1}{dt} + (i_1 + i_2 + i_3) R_0 = 0 \qquad (1a)$$

$$-n_2 V_2 + R_2 i_2 + L_2 \frac{di_2}{dt} + (i_1 + i_2 + i_3) R_0 = 0 \qquad (1b)$$

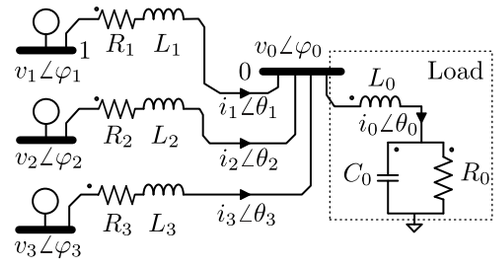

Fig. 3. Equivalent circuit with three inverters and ideal multiple windings transformer.

$$-n_3 V_3 + R_3 i_3 + L_3 \frac{di_3}{dt} + (i_1 + i_2 + i_3) R_0 = 0 \qquad (1c)$$

These equations can be represented in the form of a matrix $\mathbf{B}_3 = \mathbf{A}_3 \mathbf{x}_3$ as shown in (2), where $i_R = \mathrm{Re}\{i_k\}$ and $i_{kX} = \mathrm{Im}\{i_k\}$. Note the placement of an arbitrary load ($R_0 + jX_0$). In order to separate the real and imaginary parts and considering that the real parts are equal (as will be shown in the expression (16)), one can solve the system in the form of $\mathbf{x}_3 = \mathbf{A}_3^{-1}\mathbf{B}_3$ with the help of system (3). Other parameters can be obtained from $i_k = i_R + j i_{kX}$, $I_k = |i_k|$ and $\theta_k = \arg(i_k)$.

V. VOLTAGE BALANCE BEHAVIOR

Due to the series connection at the dc side of the inverters, unbalanced energy stored in each bus capacitor must be analyzed in order to guarantee the proper operation of the converter. Figure 4 shows the nomenclature used to achieve this goal.

The output current i_k considering only the fundamental frequency f_o, is evaluated by

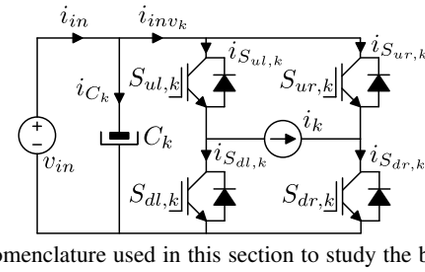

Fig. 4. Nomenclature used in this section to study the bus capacitor voltage behavior.

$$\begin{bmatrix} n_1V_1 \\ n_2V_2 \\ n_3V_3 \end{bmatrix} = \begin{bmatrix} jX_1+jX_0+(R_1+R_0) & jX_0+R_0 & jX_0+R_0 \\ jX_0+R_0 & jX_2+jX_0+(R_2+R_0) & jX_0+R_0 \\ jX_0+R_0 & jX_0+R_0 & jX_3+jX_0+(R_3+R_0) \end{bmatrix} \begin{bmatrix} i_R+ji_{1X} \\ i_R+ji_{2X} \\ i_R+ji_{3X} \end{bmatrix} \tag{2}$$

$$\underbrace{\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ m_oV_{in} \end{bmatrix}}_{\mathbf{B_3}} = \underbrace{\begin{bmatrix} (3R_0+R_1) & -(X_0+X_1) & -X_0 & -X_0 & -n_1 & 0 & 0 \\ (3X_0+X_1) & (R_0+R_1) & R_0 & R_0 & 0 & 0 & 0 \\ (3R_0+R_2) & -X_0 & -(X_2+X_0) & -X_0 & 0 & -n_2 & 0 \\ (3X_0+X_2) & R_0 & (R_0+R_2) & R_0 & 0 & 0 & 0 \\ (3R_0+R_3) & -X_0 & -X_0 & -(X_3+X_0) & 0 & 0 & -n_3 \\ (3X_0+X_3) & R_0 & R_0 & (R_0+R_3) & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & n_1 & n_2 & n_3 \end{bmatrix}}_{\mathbf{A_3}} \underbrace{\begin{bmatrix} i_R \\ i_{1X} \\ i_{2X} \\ i_{3X} \\ V_1 \\ V_2 \\ V_3 \end{bmatrix}}_{\mathbf{x_3}} \tag{3}$$

$$i_k(\theta) = I_k \sin(\theta+\theta_k). \tag{4}$$

The inverter duty cycle d_o is evaluated as:

$$d_o(\theta) = \frac{1}{2} + \frac{1}{2} m_o \sin(\theta). \tag{5}$$

Applying (4) and (5) with respect to Figure 4, the average steady–state currents for each switch are given by

$$\langle i_{\text{Sul,k}}(\theta)\rangle_{Ts} = d_o(\theta)\, i_k(\theta) \tag{6a}$$
$$\langle i_{\text{Sdr,k}}(\theta)\rangle_{Ts} = d_o(\theta)\, i_k(\theta) \tag{6b}$$
$$\langle i_{\text{Sur,k}}(\theta)\rangle_{Ts} = -[1-d_o(\theta)]\, i_k(\theta) \tag{6c}$$
$$\langle i_{\text{Sdl,k}}(\theta)\rangle_{Ts} = -[1-d_o(\theta)]\, i_k(\theta). \tag{6d}$$

The average input steady–state inverter current i_{inv_k} is determined as follows:

$$i_{inv_k}(\theta) = \langle i_{\text{Sul,k}}(\theta)\rangle_{Ts} + \langle i_{\text{Sur,k}}(\theta)\rangle_{Ts} \tag{7a}$$
$$= d_o(\theta)\, i_k(\theta) - [1-d_o(\theta)]\, i_k(\theta) \tag{7b}$$
$$= [2d_o(\theta)-1]\, i_k(\theta) \tag{7c}$$
$$= I_k m_o \sin(\theta)\sin(\theta+\theta_k). \tag{7d}$$

Equation (7d) can be rewritten as a dc and an ac component,

$$i_{inv_k}(\theta) = \frac{m_oI_k}{2}\cos(\theta_k) - \frac{m_oI_k}{2}\cos(2\theta+\theta_k). \tag{8}$$

For steady–state operation, it can be considered that the high frequency ac component of the inverter current i_{inv_k} passes through the capacitor C_k, and the dc component is the input current i_{in}.

$$i_{in}(\theta) - i_{Ck}(\theta) = \underbrace{\frac{m_oI_k}{2}\cos(\theta_k)}_{i_{in}(\theta)} - \underbrace{\frac{m_oI_k}{2}\cos(2\theta+\theta_k)}_{i_{Ck}(\theta)} \tag{9}$$

The expressions for the input current i_{in} and capacitor C_k current i_{C_k} are given respectively by:

$$i_{in}(\theta) = \frac{m_oI_k}{2}\cos(\theta_k) \tag{10}$$

$$i_{Ck}(\theta) = \frac{m_oI_k}{2}\cos(2\theta+\theta_k). \tag{11}$$

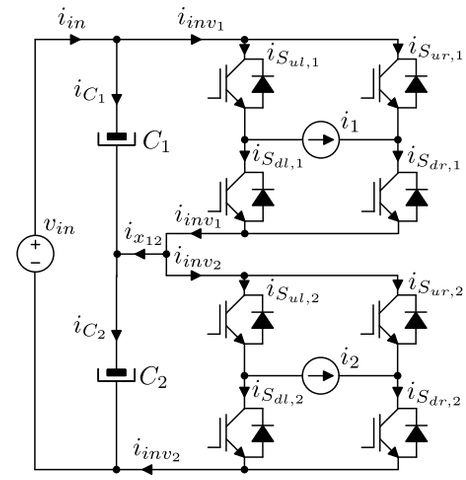

Fig. 5. Equivalent circuit used to analyze the capacitor voltage for two sub–modules.

The dc bus capacitor voltage balance between two adjacent inverters can be analyzed considering Figure 5. In order to monitor the current which is responsible for charging and discharging the capacitors C_1 and C_2 it is defined as $i_{x_{12}}$ in (12). The objective here is to show that the voltage achieves a stable operation point under a small parametric variation.

$$i_{x_{12}}(\theta) = i_{inv_1}(\theta) - i_{inv_2}(\theta) \tag{12}$$

Substituting expression (8), which defines the current in the inverter k, in (12) gives

$$i_{x_{12}}(\theta) = \frac{m_o}{2}[I_1\cos(\theta_1) - I_2\cos(\theta_2)] + \underbrace{\frac{m_oI_2}{2}\cos(2\theta+\theta_2)}_{i_{C2}} - \underbrace{\frac{m_oI_1}{2}\cos(2\theta+\theta_1)}_{i_{C1}}. \tag{13}$$

The average value for the difference between the steady-state currents of two adjacent capacitors (C_1, C_2) is calculated using the following expression

$$I_{x_{12},\text{dc}} = \frac{m_o}{2}[I_1\cos(\theta_1) - I_2\cos(\theta_2)]. \tag{14}$$

The real part of the inverter current output is $\text{Re}\{i_k\} = I_k\cos(\theta_k)$, thus the dc component becomes

$$I_{x_{12},\text{dc}} = \frac{m_o}{2}(\text{Re}\{i_1\} - \text{Re}\{i_2\}). \tag{15}$$

As a result, if the real parts of the complex current value are the same for each inverter (16), the steady–state capacitor current dc component is null and the voltage reaches a stable value.

$$\mathrm{Re}\{i_1\} = \mathrm{Re}\{i_2\} = \cdots = \mathrm{Re}\{i_k\} \tag{16}$$

The real part of the current i_k is determined by considering only its fundamental component, the active power, as follows:

$$P_k = \frac{V_k I_k}{2}\cos(\theta_k). \tag{17}$$

For 100% efficiency, the active power can be considered as,

$$P_k = \frac{V_k I_k}{2}\cos(\theta_k) = I_{in} V_{Ck}. \tag{18}$$

The peak output voltage of the inverter is related to the capacitor voltage and the modulation index as $V_k = m_o V_{Ck}$. Applying this in (18) results in

$$\frac{m_o V_{Ck} I_k}{2}\cos(\theta_k) = I_{in} V_{Ck}. \tag{19}$$

The capacitor voltage can be eliminated from (19), and the real component of i_k is found through

$$I_k \cos(\theta_k) = \frac{2I_{in}}{m_o} = \mathrm{Re}\{i_k(\theta_k)\}. \tag{20}$$

Thus, the equality (16) is proved. The current i_{x12} does not present dc components in steady–state operation, thereby ensuring the stability of the capacitor energy.

To verify the auto balance behavior, a simulation is carried out starting with unbalanced bus capacitors voltages (450 V, 400 V and 350 V). As shown in Figure 6 the capacitor bus voltage reaches is equilibrium point after 25 ms without any control strategy.

The losses in the dc–link capacitors can be evaluated using (11). In order to obtain the RMS value, θ_k can be considered to be zero,

$$I_{Ck,\mathrm{RMS}} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left(\frac{m_o I_k}{2}\cos(2\theta)\right)^2} = m_o I_k \frac{\sqrt{2}}{4} \tag{21}$$

and considering that $P = RI^2$, the losses in each dc–link capacitor are given by:

$$P_{Ck,\mathrm{Losses}} = R_{Ck}\left(m_o I_k \frac{\sqrt{2}}{4}\right)^2 = \frac{R_{Ck} m_o^2 I_k^2}{8}. \tag{22}$$

VI. ACTIVE AND REACTIVE POWER

A. Restrictions Based on Active and Reactive Power Exchange Between Inverters

Some considerations are made regarding the power flow between two inverters a and b in steady–state operation at the fundamental frequency f_o. The apparent power transfer from inverter a to b is calculated using (23). Similarly, the apparent

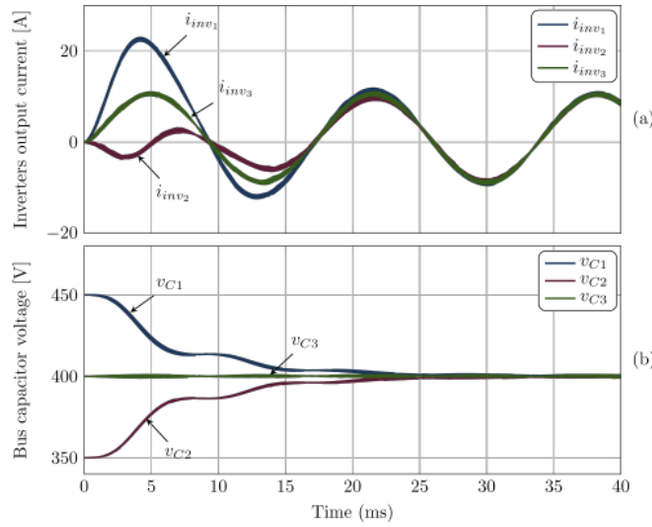

Fig. 6. Simulation result for unbalanced bus capacitor voltages. (a) Output current in each inverter; (b) Capacitor voltage.

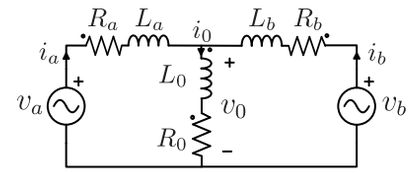

Fig. 7. Equivalent circuit for two inverters connected to a *RL* load.

power transfer from inverter b to a is obtained from (24).

$$S_{ab} = P_{ab} + jQ_{ab} = \frac{V_a V_b sen\theta_{ab}}{X_{ab}} + j\frac{V_a^2 - V_a V_b \cos\theta_{ab}}{X_{ab}} \tag{23}$$

$$S_{ba} = P_{ba} + jQ_{ba} = \frac{V_b V_a sen\theta_{ba}}{X_{ba}} + j\frac{V_b^2 - V_b V_a \cos\theta_{ba}}{X_{ba}} \tag{24}$$

One goal is to avoid active power flow between two adjacent modules. Therefore, $P_{ab} = P_{ba} = 0$, which implies that $\theta_{ab} = \theta_{ba} = 0$. Thus, the signal applied to the modulator has to be the same for all inverters in order to avoid active power flow between the inverter modules. Note that this is valid when the losses are neglected. This procedure does not restrict the power flow at the harmonics level.

B. Analysis of Harmonics and Power Flow at Higher Frequencies

Analysis of the harmonics is performed in order to investigate the active and reactive power flow between inverters. Tables I and II show, respectively, the harmonic spectrum using a sawtooth and a triangular carrier waveform with a frequency of $f_c = 333 \cdot f_o$. It can be observed that the power exchanges are more intense near the double carrier frequency $2f_c$ (typical in three–level modulation) and a more detailed analysis is carried out at this level. Table I shows that there are harmonics at close to $2f_c$ in v_1, v_2, v_3, however they are canceled in v_0 (where they are null). Table II shows that the harmonics are canceled in $2f_c$ and also $3f_c$ for a sine–triangular modulation. In both tables, the canceling of harmonics occurs when there is a phase–shift between the signals. This characteristic is provided by the appropriate phase–shift proposed for the carrier signals.

TABLE I
Harmonics for Sine–Sawtooth Modulation (THD = 76.8661)

Harmonics	Magnitude %		Phase (rad)			
Order	v_0	v_{123}	v_0	v_1	v_2	v_3
1	100.0	100.0	$\pi/2$	$\pi/2$	$\pi/2$	$\pi/2$
661	-	10.5	-	$\pi/2$	$-\pi/6$	$-5\pi/6$
662	-	15.6	-	$-\pi$	$\pi/3$	$-\pi/3$
663	-	14.3	-	$-\pi/2$	$5\pi/6$	$\pi/6$
665	-	13.1	-	$-\pi/2$	$5\pi/6$	$\pi/6$
666	-	46.5	-	0	$-2\pi/3$	$2\pi/3$
667	-	13.1	-	$-\pi/2$	$5\pi/6$	$\pi/6$
669	-	14.3	-	$-\pi/2$	$5\pi/6$	$\pi/6$
670	-	15.6	-	$-\pi$	$\pi/3$	$-\pi/3$
671	-	10.5	-	$\pi/2$	$-\pi/6$	$-5\pi/6$
1332	-	24.8	-	0	$2\pi/3$	$-2\pi/3$
1998	13.7	13.7	0	0	0	0

TABLE II
Harmonics for Sine–Triangular Modulation (THD = 76.8551)

Harmonics	Magnitude %		Phase (rad)			
Order	v_0	v_{123}	v_0	v_1	v_2	v_3
1	100.0	100.0	$\pi/2$	$\pi/2$	$\pi/2$	$\pi/2$
663	-	17.4	-	$\pi/2$	$-\pi/6$	$-5\pi/6$
665	-	39.3	-	$-\pi/2$	$5\pi/6$	$\pi/6$
667	-	39.3	-	$-\pi/2$	$5\pi/6$	$\pi/6$
669	-	17.4	-	$\pi/2$	$-\pi/6$	$-5\pi/6$
1327	-	10.5	-	$\pi/2$	$-5\pi/6$	$-\pi/6$
1329	-	14.3	-	$-\pi/2$	$\pi/6$	$5\pi/6$
1331	-	13.1	-	$-\pi/2$	$\pi/6$	$5\pi/6$
1333	-	13.1	-	$-\pi/2$	$\pi/6$	$5\pi/6$
1335	-	14.3	-	$-\pi/2$	$\pi/6$	$5\pi/6$
1337	-	10.5	-	$\pi/2$	$-5\pi/6$	$-\pi/6$

Considering Figure 7, the equivalent resistance between two inverters can be defined as $R_{ab} = R_a + R_b$, and the equivalent inductance as $L_{ab} = L_a + L_b$. The equivalent impedance is defined as $Z_{ab} = R_{ab} + jX_{ab}$. The apparent power flow, S_{ab}, between inverters a and b is given by

$$S_{ab}\angle\psi_{ab} = V_a\angle\varphi_a\left(\frac{V_a\angle-\varphi_a - V_b\angle-\varphi_b}{Z_{ab}\angle-\delta_{ab}}\right) \quad (25a)$$

$$= \frac{V_a^2 - V_bV_a\angle\varphi_{ab}}{Z_{ab}\angle-\delta_{ab}} \quad (25b)$$

$$= \frac{V_a^2\angle\delta_{ab} - V_bV_a\angle(\varphi_{ab}+\delta_{ab})}{Z_{ab}}. \quad (25c)$$

Thus, the active power is calculated through

$$P_{ab} = \frac{V_a^2\cos(\delta_{ab}) - V_bV_a\cos(\varphi_{ab}+\delta_{ab})}{Z_{ab}} \quad (26)$$

and the reactive power flow as

$$Q_{ab} = \frac{V_a^2 sin(\delta_{ab}) - V_bV_a sin(\varphi_{ab}+\delta_{ab})}{Z_{ab}}. \quad (27)$$

Considering an ideal condition where all harmonics of the same order have the same amplitude, and having defined the phase–shifts, the active and reactive power flows are given, respectively, by

$$P_{ab} = \frac{V_k^2}{Z_{ab}}\{\cos(\delta_{ab})[1-\cos(\varphi_{ab})] + \sin(\delta_{ab})\sin(\varphi_{ab})\} \quad (28)$$

$$Q_{ab} = \frac{V_k^2}{Z_{ab}}\{\sin(\delta_{ab})[1-\cos(\varphi_{ab})] - \cos(\delta_{ab})\sin(\varphi_{ab})\} \quad (29)$$

where:

$$Z_{ab} = \sqrt{R_{ab}^2 + X_{ab}^2} \quad (30a)$$

$$\cos(\delta_{ab}) = \frac{R_{ab}}{\sqrt{R_{ab}^2 + X_{ab}^2}} \quad (30b)$$

$$\sin(\delta_{ab}) = \frac{X_{ab}}{\sqrt{R_{ab}^2 + X_{ab}^2}}. \quad (30c)$$

For the case where three inverters and sawtooth carrier waveforms are used, φ_{ab} varies between $\pm 2\pi/3$. Therefore, applying this phase in (28) and (29), the expressions for the active and reactive power flow between the inverters are given, respectively, by

$$P_{ab} = \frac{V_k^2}{R_{ab}^2 + X_{ab}^2}\left\{\frac{3}{2}R_{ab} + \frac{\sqrt{3}}{2}X_{ab}\right\} \quad (31)$$

$$Q_{ab} = \frac{V_k^2}{R_{ab}^2 + X_{ab}^2}\left\{\frac{3}{2}X_{ab} + \frac{\sqrt{3}}{2}R_{ab}\right\}. \quad (32)$$

As (31) and (32) show, the active and reactive power exchange at high frequencies can be reduced by changing the impedance Z_{ab}. In this study, the inductance L_k is used for this purpose.

VII. PROTOTYPE AND EXPERIMENTAL RESULTS

A prototype was designed (see Figure11) based on the equations presented in Section IV and built in order to verify the proposed converter. Figure 8 shows the structure of the 18–pulse series–type diode rectifier implemented together with the inverters, the multiple–winding transformer and the load. Table III provides further details on the setup used.

A. Sub-modules Communication Setup

As Section II describes, all of the full–bridge inverters (SM–k) must communicate with each other in order to achieve the synchronization of the carrier and modulation signals.

Figure 9 outlines the communication setup. The pulse–width–modulation (PWM) carriers synchronization of the inverters is obtained by synchronization pulses PWM_{sync} generated in the master micro–controller device. Each secondary micro–controller receives the PWM_{sync} pulse as an event interrupt, which is used to synchronize the PWM modules. This timing is critical for the generation of a multilevel output voltage waveform.

The synchronization of the modulation signal is performed using a look–up table that provides a sine wave and an index table. The modulation index is delivered through a CAN

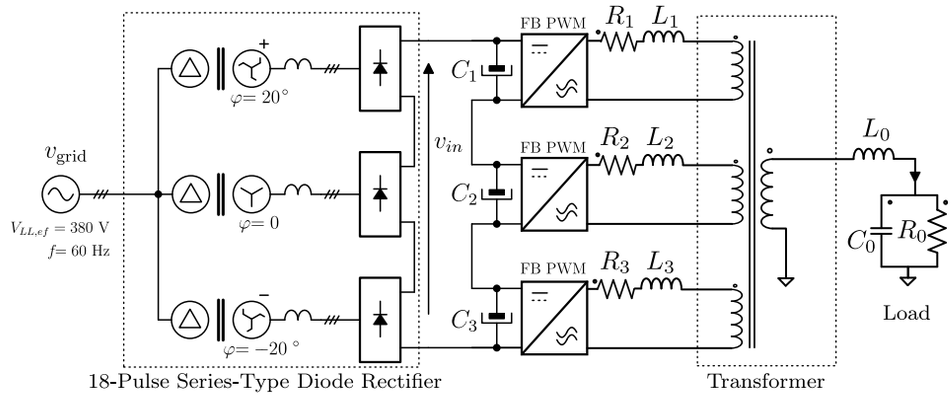

Fig. 8. Laboratory setup containing the 18–pulse series–type diode rectifier implemented together with the inverters, the multiple–winding transformer and the load.

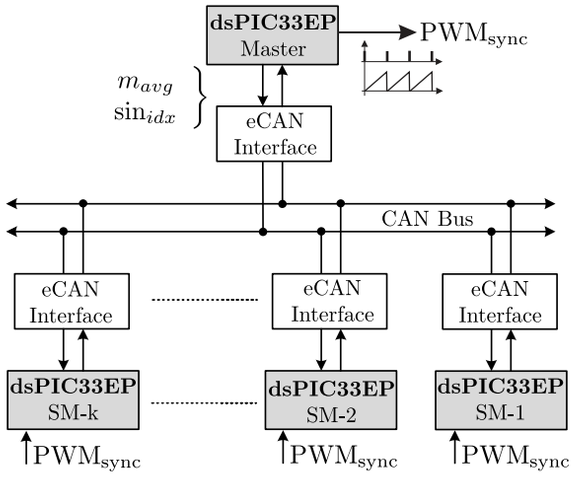

Fig. 9. Communication structure powered by CAN protocol.

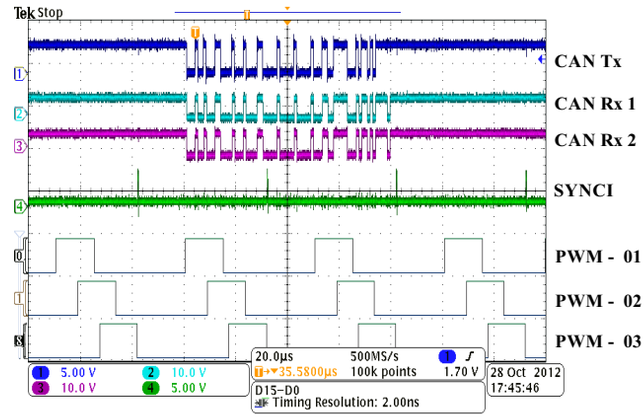

Fig. 10. CAN signals, interrupt pulse for synchronization and synced PWM signals.

protocol communication, as seen in Figures 9 and 10. The signal CAN Tx is transmitted by the master micro–controller to all secondary micro–controllers, and CAN Rx is the signal received.

B. Power System Setup Description

The 18–pulse series–type diode rectifier was built in order to obtain a 1200 V dc source. It is composed of three three–phase transformers connected in delta–zigzag and delta–star winding configurations. It eliminates four dominant harmonics by applying a 20° phase displacement between any two adjacent secondary windings.

The multiple–winding transformer with a rated power of 15 kVA and 220 V windings voltage is connected to the *RLC* load.

C. Experimental Results

Some voltages of the system are shown in Figure 12 (see spectra in Figure 14), where the voltages in each sub-module (V_1, V_2 and V_3) present three levels, their PWM signals are phase shifted by 120° (as seen in Figure 10), the sum of V_1, V_2 and V_3 (V_{ab}) exhibit seven levels and the output voltage (V_o) is a sinusoidal waveform (these results are as expected). The inverters and load currents at rated power are shown in Figure 13 (see spectra in Figure 15). The waveforms verify the balance of currents in each sub–module (i_1, i_2, i_3) and that the load current is the sum of the module currents. The RMS voltages, RMS currents and average power in each inverter are shown in Tables IV and V. These data demonstrate the balance of the voltage, current and power between the sub–modules.

TABLE III
Prototype Values

Parameter	Value	Description
P_0	5 kW	Output rated power
V_0	220 V	Output rated voltage
V_{in}	1200 V	Input voltage
f_s	20 kHz	Switching frequency
f_o	60 Hz	Fundamental frequency
C_k	1020 µF	Bus capacitor capacitance
R_0	32 Ω	Load resistance
C_0	15 µF	Load capacitance
L_0	5 mH	Load inductance
L_k	1 mH	Filtering inductance
n_k	1:1:1:1	Transformer transformation ratio
k	3	Number of inverters (sub–modules)

VIII. CONCLUSIONS

This paper presented a topology suitable for high input voltage applications. A prototype with 8 kW, 1200 V dc and 220 V at 60 Hz was tested in order to validate all of the analysis presented.

Fig. 11. Photograph of the prototype.

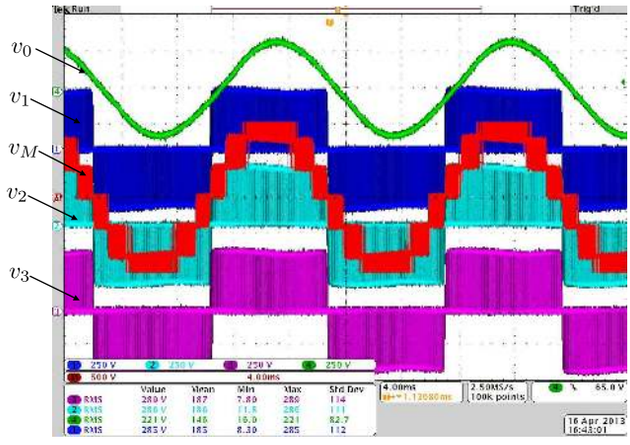

Fig. 12. Inverters and load output voltages at rated power.

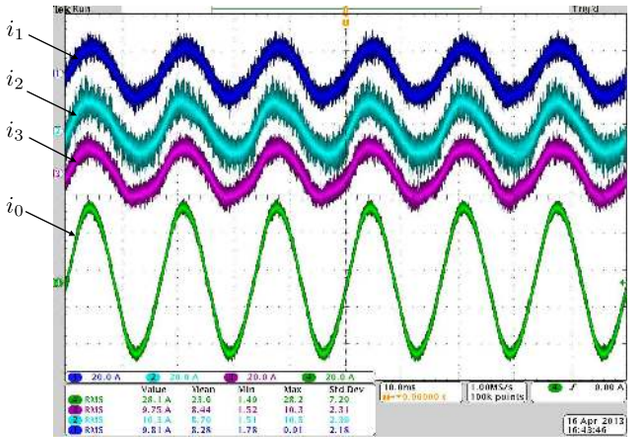

Fig. 13. Inverters and load output currents with the inclusion of the filtering inductance.

TABLE IV
Voltage, current and inverters power at rated power

	Output			Input		
	INV 01	INV 02	INV 03	INV 01	INV 02	INV 03
Vrms [V]	287.65	288.51	288.96	399.39	399.48	398.51
Irms [A]	9.92	9.91	10.20	7.18	7.18	7.18
P [kW]	−2.26	−2.28	−2.28	−2.37	−2.38	−2.36
S [kVA]	2.34	2.30	2.43	2.95	2.96	2.93
Q [kvar]	−0.63	−0.31	−0.86	−1.76	−1.76	−1.75

TABLE V
Voltage, current and inverter power with input voltage of 600 V

	Output			Input		
	INV 01	INV 02	INV 03	INV 01	INV 02	INV 03
Vrms [V]	143.84	144.59	144.62	199.79	200.61	198.79
Irms [A]	4.82	4.90	5.13	3.06	3.06	3.06
P [kW]	−0.57	−0.57	−0.57	−0.60	−0.60	−0.60
S [kVA]	0.56	0.57	0.60	0.74	0.75	0.74
Q [kvar]	0.00	0.00	−0.19	−0.44	−0.44	−0.43

The experimental results show the balance of voltages in the dc bus without the need for local or individual converter control under normal operation of the converter.

In order to prevent the exchange of active and reactive power at high frequency an inductance L_k must be included.

The magnetic coupling can be used in three–phase systems and electric machine configurations with open–windings or with split–windings.

It should be noted that different transform ratios can be applied but only those symmetrically distributed between the primary or secondary side (1:2:2:2 or 2:1:1:1) are suitable. An asymmetrical transform ratio (1:1:2:4 or 1:1:3:9) leads to asymmetrical voltage stress over the switches and power being processed in each submodule.

The proposed structure was verified in a single–phase inverter and at low voltage. However, it can be extended to multiphase systems and high voltage, which increases its field of application. The structure has the potential for application in UPS, drives, distributed power generation and traction.

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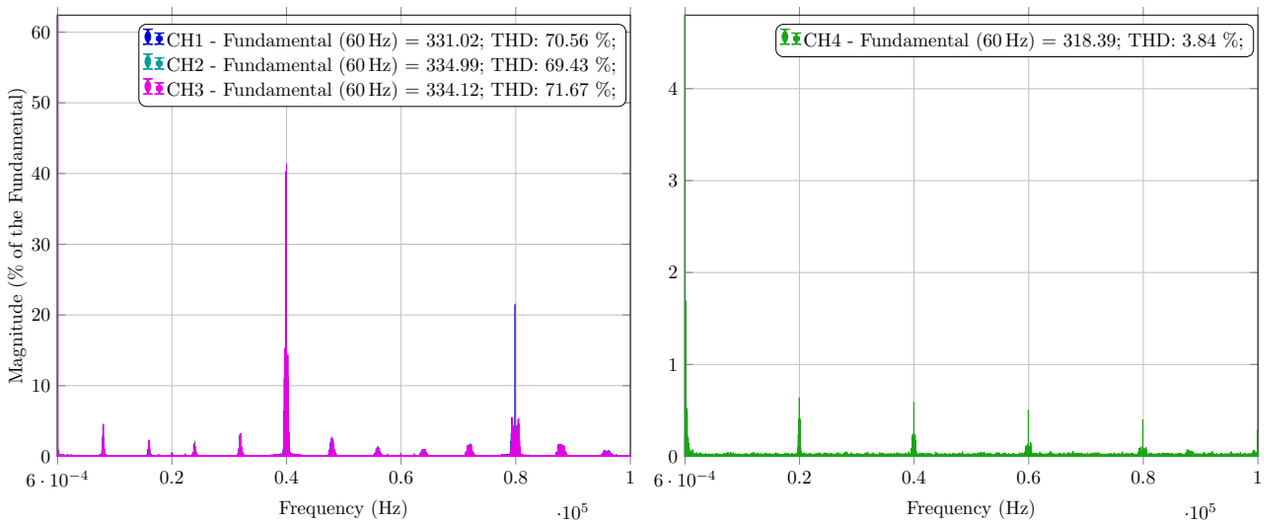

Fig. 14. Spectra for the inverter output voltages (CH1 $\rightarrow v_1$, CH2 $\rightarrow v_2$ and CH3 $\rightarrow v_3$) and load voltage (CH4 $\rightarrow v_0$).

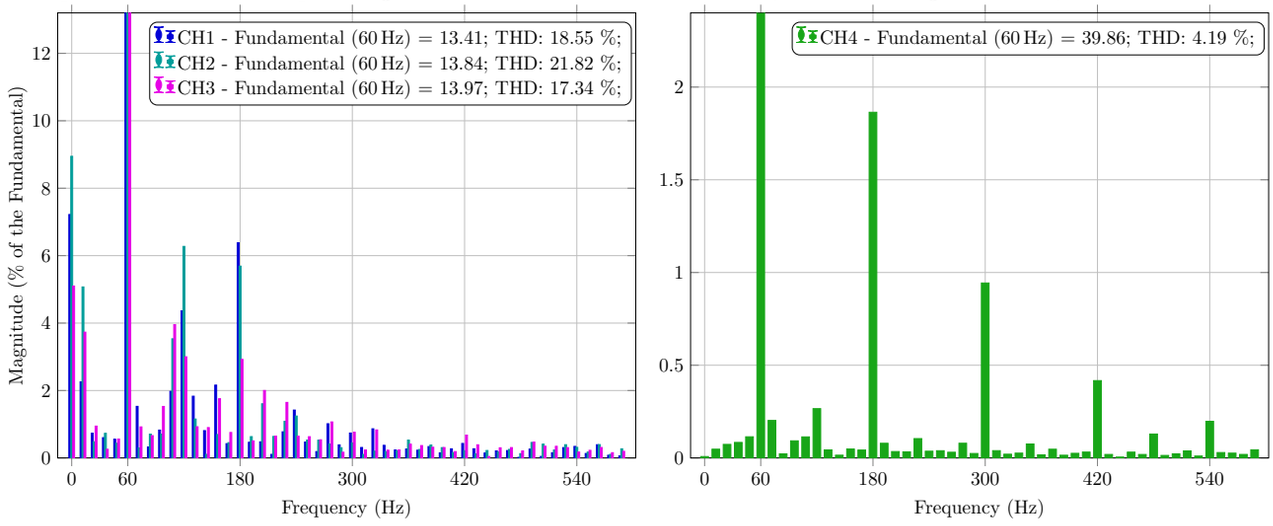

Fig. 15. Spectra for the inverter output currents (CH1 $\rightarrow i_1$, CH2 $\rightarrow i_2$ and CH3 $\rightarrow i_3$) and load current (CH4 $\rightarrow i_0$).

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