A Single Photon Avalanche Diode Array Fabricated in 0.35μm CMOS and based on an Event-Driven Readout for TCSPC Experiments

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ABSTRACT[1]

The design and characterization of an imaging sensor based on single photon avalanche diodes is presented. The sensor was fully integrated in a 0.35μm CMOS technology. The core of the imager is an array of 4x112 pixels that independently and simultaneously detect the arrival time of photons with picosecond accuracy. A novel event-driven readout scheme allows parallel column-wise and non-sequential, on-demand row-wise operation. Both time-correlated and time-uncorrelated measurements are supported in the sensor. The readout scheme is scalable and requires only 11 transistors per pixel with a pitch of 25μm. A number of standard performance measurements for the imager are presented in the paper. An average dark count rate of 6Hz and 750Hz are reported at room temperature respectively for an active area diameter of 4μm and 10μm, while the dead time is 40ns with negligible crosstalk. A timing resolution better than 80ps over the entire integrated array makes this technique ideal for a fully integrated high resolution streak camera, thus enabling fast TCSPC experiments. Applications requiring low noise, picosecond timing accuracies, and measurement parallelism are prime candidates for this technology. Examples of such applications include bioimaging at cellular and molecular level based on fluorescence lifetime imaging and/or, fluorescence correlation spectroscopy, as well as fast optical imaging, optical rangefinders, LIDAR, and low light level imagers.

Keywords: Avalanche photodiodes, CMOS single photon detectors, TCSPC, event-driven readout, time-correlated measurements.

1. INTRODUCTION

Advances in neuro- and medical imaging are placing an increasing burden on optical sensor technology. Time-correlated imaging and other high precision solutions are currently the preferred techniques, where timing accuracy and sensitivity is critical. Some of these methods help enable new fundamental scientific discoveries almost daily.

A number of techniques have been proposed to achieve high speed in conventional charge-coupled devices (CCDs) and CMOS active pixel sensor (APS) architectures [1,2,3,4]. Among some of the most successful techniques are ultra-fast low-noise electronic readout circuitries, on-pixel A/D conversion, and local analog electrical storage. However, in general, a significant design effort and considerable experience is needed to achieve satisfactory results. As an alternative to conventional CCDs and CMOS APS sensors, single photon counters (SPCs) have been proposed.

SPCs have been known for decades and among the most successful devices in this class are microchannel plates (MCPs) and photomultiplier tubes (PMTs) [5]. Even though they have been studied since the 1960s [6], avalanche photodiodes (APDs) have begun to compete with MCPs and PMTs only recently. In APDs operating in linear mode, carriers generated by the absorption of a photon in the p-n junction, are multiplied by impact ionization thus producing an avalanche. The resulting optical gain is usually in the tens to hundreds and thus it does not allow single photon detection. In addition, these devices require relatively accurate monitoring and biasing circuits and, often, specific technological requirements.

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When biased *above* breakdown, an APD is said to operate in so-called Geiger mode and it is known as single photon avalanche diode (SPAD). When a photon is absorbed in the multiplication region of the device, an avalanche may be triggered. By proper design techniques, the avalanche can be quenched in a few nanoseconds and the avalanche current may be converted onto a digital voltage pulse for further processing.

Recently, SPADs have been integrated in CMOS achieving timing resolutions comparable to PMTs [7]. Possible SPAD applications in the bio-sciences and physics include fluorescence-based imaging, such as Förster Resonance Energy Transfer (FRET), fluorescence lifetime imaging microscopy (FLIM) [8], fluorescence correlation spectroscopy (FCS) [9,10,11], voltage sensitive dye (VSD) based imaging [12,13], particle image velocimetry (PIV) [14], instantaneous gas imaging, [15,16], LIDARs and 3D vision systems [17,18], etc.

In this paper we discuss SPAD technology implemented in CMOS focusing on time-resolved imaging techniques and in particular time-correlated single photon counting (TCSPC). We also look at specific architectural solutions that are especially effective detecting photon arrivals in conditions of low and ultra-low illumination conditions. As an illustration, Fig. 1 shows an imager that performs both TCSPC and spectrum analysis of light emissions coming, for example, from a biological sample. A light source, e.g. a laser, generates pulses of coherent light of pico- or femtosecond width. The light reflected by the sample is optically processed and applied to a prism or a grating device where dispersion occurs.

To simultaneously perform TCSPC and spectral analysis, one has to design a sensor capable of detecting photons in parallel and with high timing accuracy in both the x-axis (spatial domain) and y-axis (spectral domain). This technique has been introduced by a number of authors. In [19], for example, sixteen PMTs were used in parallel through optical coupling to a polychromator (grating). Though its applicability has already being shown, this setup still presents some limitations and it could be improved. As it is usual in such microscope setups, this method requires a full scanning of the image in the direction of x and y axis. Since the photon counting rate in such experiments is limited due to practical issues, the acquisition time of a full image is in the range of several minutes at best. Very often it takes several hours, depending on the image resolution. For many research activities, such a lengthy acquisition is not acceptable. The cost and size of the apparatus required in this approach could be an issue in some cases. In addition, a large number of detectors is not feasible, thus limiting the spectral resolution of the approach.

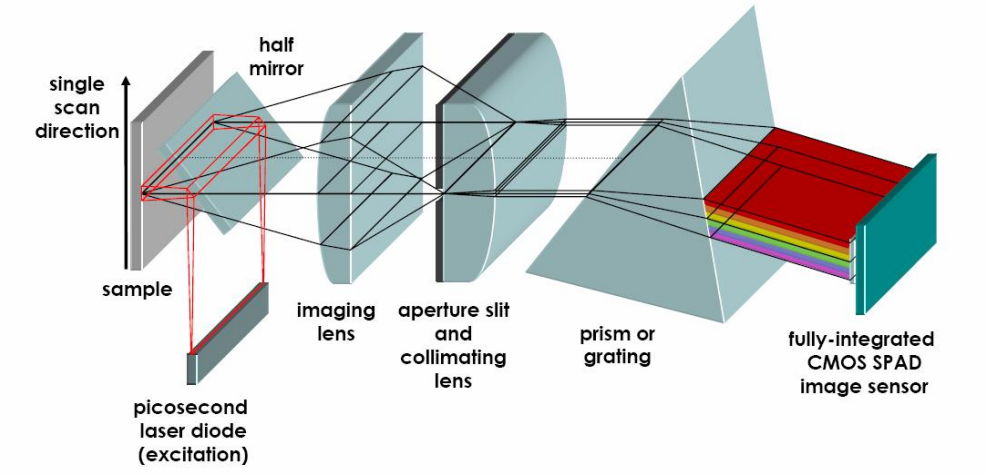

Fig. 1. Principle of an optical setup for simultaneous TCSPC and spectrum analysis based on SPAD array and on event-driven readout architecture.

In the paper, we focus on an *integrated* approach where every detector, implemented in CMOS by a SPAD, is a few tens of micrometers in size. Thus, large arrays can be implemented without compromising timing accuracy. In particular, we

propose sensor architectures that allow for *fully parallel* photon detection in the space domain and *non-sequential* event-driven detection in the spectral domain. It should be noted that the proposed event-driven architecture does not use any time-gating, wavelength scanning, or detector multiplexing. Even though it is not truly parallel, this non-sequential readout architecture is adequate, due to the low probability that two or more photons at different wavelengths impinge the detector simultaneously. Due to the level of miniaturization attained in this design, high spatial and spectral resolutions can be simultaneously achieved. In addition, imaging scanning is reduced to a single direction, thus speeding up considerably the acquisition time of a full image. The paper also discusses the trade-offs that designers need to account for to adapt the architecture to a specific application in this context.

The paper is organized as follows. Section 2 introduces the SPAD imaging technology. Section 3 illustrates the principles and implementation of novel readout techniques, while Section 4 presents results obtained with these techniques.

2. SINGLE PHOTON AVALANCHE DIODES IMPLEMENTED IN CMOS

SPADs have been known for decades [20], but only recently fully integrated CMOS implementations have appeared [7,21,22,23]. Since the introduction of SPADs fabricated in 0.8μm CMOS, circuit designers have had to cope with the limitations of an obsolete 2-metal technology. For this reason, there has been a significant push for SPAD technology to migrate to a more advanced process, which recently has resulted in the first successful implementation in a 2P4M 0.35μm CMOS technology [24].

A SPAD consists of a p-n junction, a quenching mechanism, and a recharge circuitry. The voltage in excess of breakdown is known as *excess bias voltage*, V_e. In Geiger mode, a virtually infinite optical gain is achieved, however a quenching mechanism is necessary to stop an avalanche after it is triggered. Quenching techniques include active and passive methods. The simplest approach is the use of a resistance along the avalanche path. The avalanche current causes the diode reverse bias voltage to drop below breakdown, thus pushing the junction to linear avalanching and even below breakdown. After quenching, the device requires a certain recovery time, to return to the initial state. The quenching and recovery times are collectively known as *dead time*. Current developments in more advanced CMOS technologies have demonstrated full scalability of SPAD devices, a 25μm pitch, and dead time as low as 40ns. Fig. 2 shows a typical schematic of a SPAD. Quenching is performed by a PMOS transistor, while a properly designed inverter performs the conversion of the avalanche current onto a digital voltage pulse.

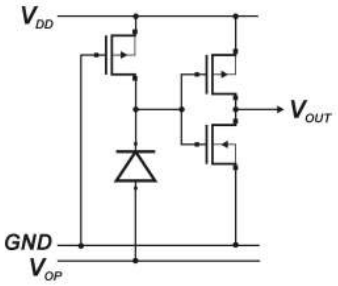

Fig. 2. Typical CMOS SPAD schematic.

A major issue in SPAD designs is represented by edge effects in the p-n junction, where high electric field can produce premature breakdown [7]. This prevents the device to operate in Geiger mode. In order to reduce edge effects and to make a planar multiplication region, usually guard rings of low-doping diffusions are employed [7,20]. The purpose of the diffusion is the reduction of the electric field below the values reached in the planar multiplication region. The cross-section of the proposed implementation, based on [7,24], is shown in Fig. 3. In this case, a p-well guard ring is encircling the p+ diffusion that forms, along with the deep n-well, the multiplication region.

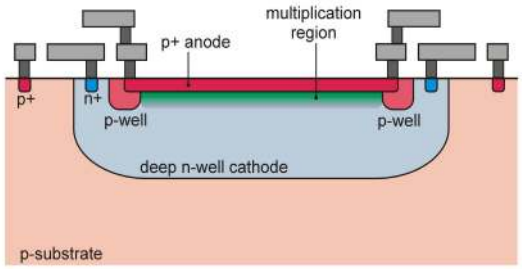

Fig. 3. Cross-section of the SPAD.

The sensitivity in SPADs is characterized by the probability of a single photon to originate an electrical pulse. Such parameter is known as *photon detection probability* (PDP). In most devices it can exceed 25-40% and it is a function of wavelength and excess bias voltage [7,17,21,22]. The PDP is generally dependent of the doping profiles making up the p-n junction, which in turn are determined by geometric and technological parameters.

The noise is measured in SPADs in terms of the rate at which spurious pulses are produced, due to carriers that are not photo-generated, and it is known as *dark count rate* (DCR). DCR is caused by thermal or tunnelling generated carriers [7]. In CMOS SPADs, DCR can be as low as a few Hertz [7,22,24] and it is a strong function of temperature and of excess bias voltage.

The statistical fluctuation of the time interval between the arrival of a photon at the sensor and the output pulse leading edge is defined as the *timing jitter* or timing resolution. Timing jitter mainly depends on the time a photo-generated carrier requires to get into the multiplication region from the absorption point. Typical values of timing jitter in CMOS SPADs vary from a minimum of 40ps up to 80ps [7,17,22,24].

Traps inside the multiplication region tend to capture photo-generated carriers during an avalanche that are released at a random later time, thus potentially re-triggering a subsequent avalanche [7]. Such phenomenon is responsible for causing the so-called *afterpulses*, i.e. spurious pulses correlated to true photon absorption. The parameter characterizing this effect is known as *afterpulse probability*, or probability of afterpulsing, and it is also function of the number of carriers involved in an avalanche, which depends in turn on the SPADs parasitic capacitance. Afterpulse probability may be modulated, for a given parasitic capacitance, by varying the dead time, whether active or passive quenching/recharge is used.

When built in arrays, SPAD devices may be subject to crosstalk. Crosstalk may be of electrical and of optical nature. During an avalanche some photons may be released due to electroluminescence [6]. These photons may cause avalanches in neighbouring pixels, thus generating spurious digital pulses unrelated to a direct photon excitation of that pixel. This probability is much smaller in fully integrated arrays of SPADs in comparison to hybrid versions. This is due to the fact that the diode's parasitic capacitance in the integrated version is orders of magnitude smaller than the hybrid solutions, thus reducing the energy dissipated during a Geiger event. Electrical crosstalk on the contrary, is produced by the fact that photons absorbed beyond the p-n junction, deep in the substrate, generate carriers that can diffuse to neighboring pixels.

3. EVENT-DRIVE READOUT ARCHITECTURE

One of the main issues when it comes to implementing large arrays of SPADs is the readout system. Unlike conventional CMOS APSs, where the photocurrent is integrated independently in every photodiode's or photogate's parasitic capacitance and the resulting voltage is available at the end of the integration process, photon counting is a dynamic process. As a result, an external integrator, counter, or a time-discriminator may be required. Hence, the readout system demands special care. The simplest readout system is a *M*-to-1 digital multiplexer that allows one to

route the output of a selected pixel directly to the global output for all *M* pixels in the array. Using this approach, it is possible to achieve high measuring accuracies per pixel, but it prevents simultaneous detection in all pixels [17,22].

When light illumination on a column is low, an alternative approach is possible. In this approach, known as event-driven readout, a column is transformed into a digital bus, which is accessed by a pixel in an asynchronous fashion based of a well-defined protocol. In the implementation proposed in [24] for the first time, a bus consisting of a high-speed line and a set of *N* addresses, is employed. The high-speed line is used to propagate the digital pulse from the SPAD, where photon detection occurred, to the bottom of the bus, where time-of-arrival (TOA) can be evaluated for TCSPC applications. Time-uncorrelated photon counting or other operations may also be performed outside the pixel array, thus enabling resource sharing and/or better utilization of silicon real estate. The high-speed line is designed so as to limit its timing jitter contribution, thus guaranteeing high timing resolutions. Hence, TOA evaluation can be performed off- or on-chip with picosecond resolution.

The address bus encodes the row where the detection pulse originated, thus enabling to record the TOA in a register associated to a given pixel. The event-driven pixel used in our implementation is shown in Fig. 4. The SPAD's first stage output drives NMOS transistor T_P, which is used to pull down line *nOUT*. This line, usually at logic state H, will propagate a logic L pulse, where the H to L transition is critical for the TOA evaluation. The address corresponding to the appropriate line is sent along address bus *nADDR*, using transistor array T_C as shown in the figure.

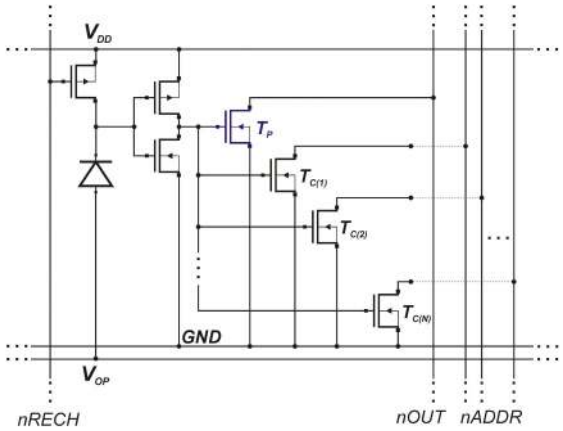

Fig. 4. Event-driven readout principle: the bus structures.

The timing pulse and address propagation assumes that the bus is IDLE, i.e. it is not being utilized by another pixel on the same column. During the time the bus is busy, a column-specific mechanism changes the status of the bus from IDLE to BUSY. This has the effect of preventing all the SPADs on the column from firing. When the timing pulse has successfully propagated and has been detected, the finite state machine releases the bus, which returns to an IDLE state. The time required to complete a full readout cycle is known as *column dead time*.

The address bus may be implemented in a number of ways. In our circuit, the bus is implemented in a parallel fashion. The required number of address lines *N* per pixel is computed as $N = \lceil \log_2 R \rceil$, where *R* is the number of rows in a column. This readout method is scalable and the logarithmic dependence of N from R suggests that it is indicated for large arrays, when it comes to silicon real estate utilization. The scalability of the approach was recently demonstrated in [25]. Larger arrays however have the effect of reducing the maximum photon flux that can be detected before saturating the readout system.

A simplified version of the overall readout system in a column is shown in Fig. 5. The figure shows the pull-up resistors at the extremities of all the lines, that ensure a logic H level while not pulled down by the corresponding transistor.

These resistors, in our implementation can be actually implemented using properly sized transistors. At the bottom of the readout channel, the timing pulse associated with a given pixel is used to latch the address *nADDR* which is transferred into *ADDR*. Once the address *ADDR* is secured, it is ready to be used to address a memory to store the TOA either on- or off-chip. In the mean time, nRECH signals availability of the channel at readout cycle completion. Thus, the recharge of the SPAD pixel that fired can now be completed. The adjustable delay of Fig. 5 is required to avoid setup time violations. The readout scheme has a built-in collision resolution mechanism to avoid bus contention.

Event-driven readout schemes are particularly indicated for applications where there are sparsely arriving photons. This is generally the case in setups such as the one shown in Fig. 1, when event-driven readout is used in the spectral domain and a parallel readout is used in the spatial domain. The scheme is also advantageous in that it provides a simple mechanism to control some of the parameters associated with SPADs, such as dead time and dynamic range, with no or minimal impact on timing accuracy.

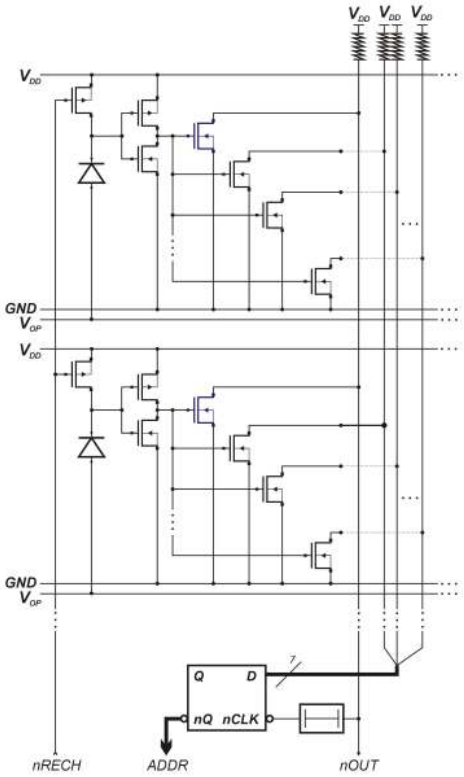

Fig. 5. Complete bus implementation for a single column.

4. EXPERIMENTAL RESULTS

To demonstrate TCSPC applications, a 4x112 SPAD pixel array was fabricated in 0.35µm CMOS. Fig. 10 shows the photomicrograph of the sensor with an inset of the event-driven pixel. The test bed used in our experimentation is based on an Altera Excalibur™ FPGA that includes an ARM processor core. Banks of 16-bit counters were implemented on the FPGA along with a finite state machine to control the interface between the sensor and the outside world. ADDR is used to address a register on the FPGA while the embedded ARM controls all acquisition operations. Volatile and non-volatile memories, communication links, power supply, as well as optional measurement connectors complete the test

bed. A standard C-mount and black plastic casing was placed over the sensor. Fig. 6 shows an image of the prototype including a standard lens.

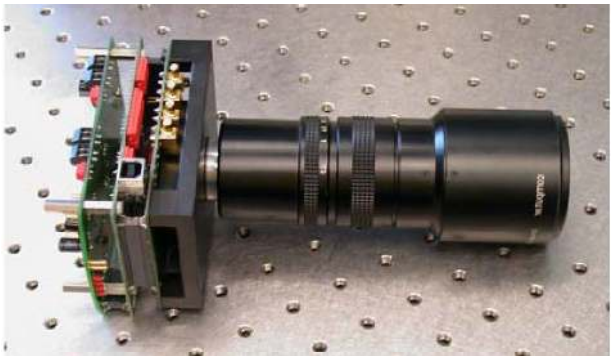

Fig. 6. Test bed implementation.

The DCR over all the array is reported in Fig. 7, while Fig. 8 plots the PDP for the design as a function of the wavelength. In the plot one can see the PDP curves of the original design reported in [24] in comparison to an earlier design implemented in 0.8µm CMOS technology. The plot of Fig. 8 also reports the PDP measured in a more recent design fabricated in 0.35µm CMOS where the polyimide passivation was prevented and where SPADs with slightly larger active area were implemented. In the latter designs a maximum PDP of 40% was reached at 4V excess bias voltage at the expense of higher DCR.

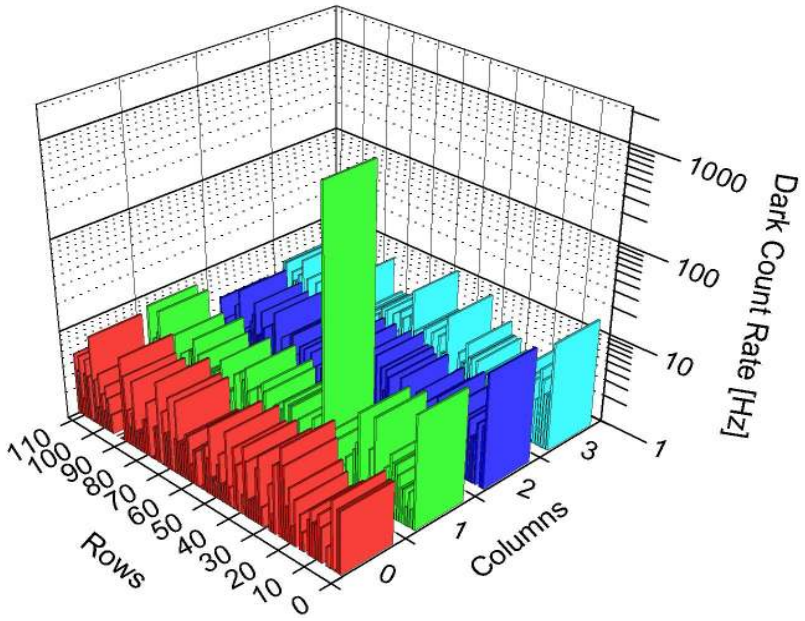

Fig. 7. Dark count rate measured over the whole array.

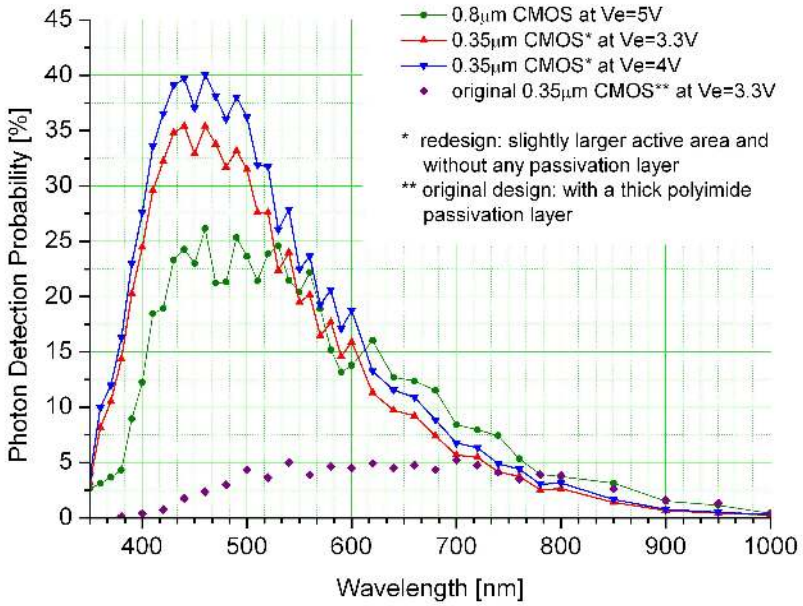

Fig. 8. Photon detection probability as a function of excess bias voltage and wavelength for two implementations in 0.35μm CMOS and an earlier design in 0.8μm CMOS.

The plots of Fig. 9, referred to the redesign, show the temperature behavior of the DCR as a function of excess bias voltage and for various values of temperature.

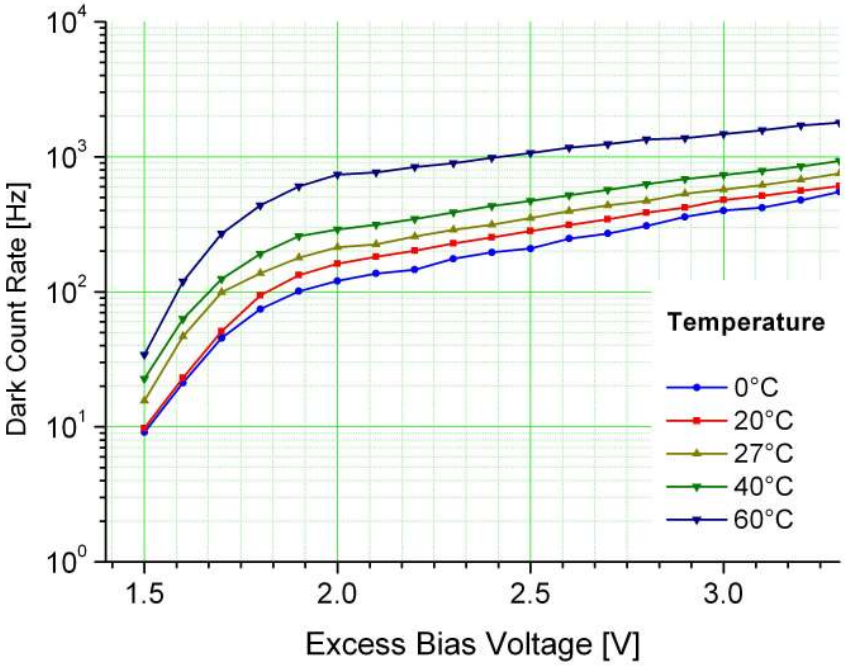

Fig. 9. Temperature behavior of dark count rate as a function of excess bias voltage for an active area diameter of 10μm.

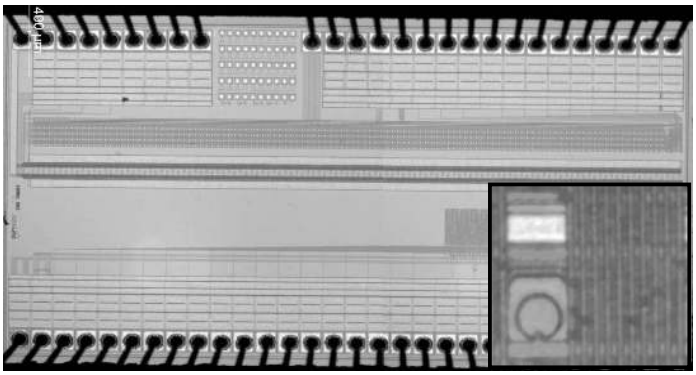

Fig. 10. Photomicrograph of the 4x112 SPAD array fabricated in 0.35um CMOS technology. The inset shows the photomicrograph of a pixel.

The plot of Fig. 11 shows the timing accuracy of the detectors. Finally, Fig. 12 depicts the result of afterpulse probability as a function of dead time. Afterpulsing measurements were carried out by the discrete autocorrelation of the signal from a typical pixel under constant uncorrelated background illumination. The dead time may be varied from a minimum of 20ns to a few hundreds of nanoseconds. The nominal value of 40ns was chosen to trade-off column bandwidth and afterpulse probability.

The FWHM of the jitter and other important parameters of the original design, as well as the redesign, are summarized in Tab. 1. The estimated impact of polyimide onto the PDP is an attenuation factor of approximately 3, mostly in the visible wavelength range. Additional improvements in the PDP came from the modification of the active area size. Though the PDP does not depend directly on the active area, small areas are not desirable, since the electric field in the multiplication region could potentially not be planar. Without a planar and well-defined multiplication region, the area used to determine the PDP suffers from a large uncertainty. Timing accuracy on the other hand, was unaffected. Long time cross-correlation measurements between signals from neighbor pixels, under constant uncorrelated background light, showed crosstalk to be undetectable. We believe that the reason for this is the use of a deep n-well to create the cathode of the diode in the SPAD, thus minimizing electrical interactions between different pixels. Optical crosstalk is negligible due to the relatively small number of carriers involved in each avalanche thanks to the reduced dimensions of the devices.

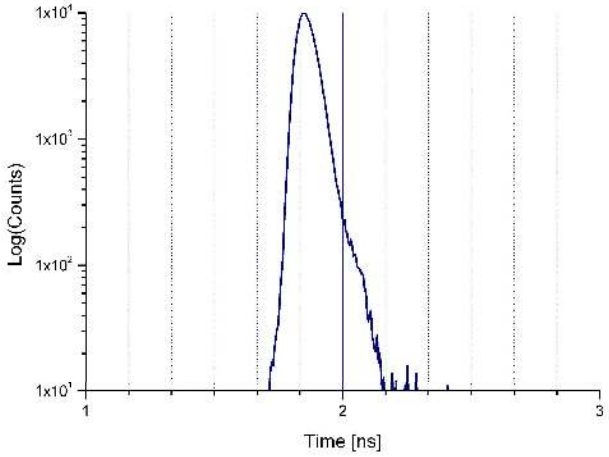

Fig. 11. Timing jitter performance: 80ps FWHM.

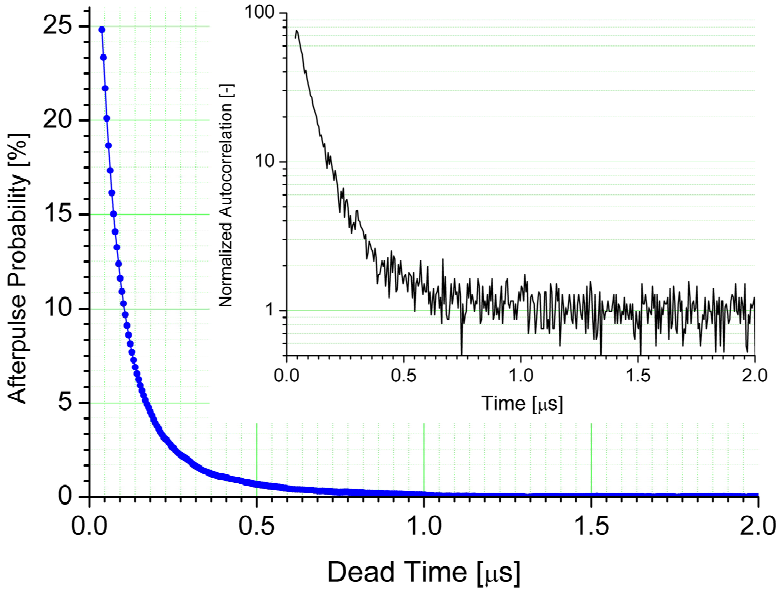

Fig. 12. Afterpulse probability as a function of dead time based on autocorrelation measurement (under uncorrelated background light producing an average count rate of 40 KHz).

Performance	Min.	Typ.	Max.	Unit	Comment
Pitch		25		μm	
Array size		4×112		-	
Avg. dark count rate		6		Hz	Active area diameter: 4μm
Avg. dark count rate		750		Hz	Active area diameter: 10μm
Dead Time			40	ns	
Timing jitter (FWHM)		80		ps	
Column saturation			25	MHz	
Wavelength range	350		1000	nm	
PDP	0.1		5	%	Polyimide passivation
PDP	0.1		40	%	New design, no passivation
Afterpulse probability		23		%	At nominal dead time
Overall crosstalk @ 25μm		negligible		%	

Tab. 1. Performance summary.

CONCLUSIONS

We have reported on the design and characterization of single photon avalanche diode arrays fabricated in 0.35μm CMOS technology. The paper focuses on a 4x112 array where a novel event-driven readout architecture was implemented. The sensor achieves picosecond timing accuracy and low dark count rate while enabling parallel column readout and non-sequential column access. The readout is scalable and has been tested in larger arrays. The pixel consists of 11 transistors and can be miniaturized to achieve a pitch of 25μm. To the best of our knowledge, this is the lowest pitch ever reported for a single photon avalanche diode array in any technology. Applications requiring low noise, high timing accuracies and high measurement parallelism will significantly benefit from this architecture.

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