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Research Article

A Single-Stage Buck-Boost Three-Level Neutral-Point-Clamped Inverter with Two Input Sources for the Grid-Tied Photovoltaic Power Generation

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This paper proposes a novel single-stage buck-boost three-Level neutral-point-clamped (NPC) inverter with two independent dc sources coupled for the grid-tied photovoltaic (PV) application, which can effectively solve the unbalanced operational conditions generally appearing between two independent PV sources. The proposed control scheme can simultaneously guarantee the maximum power point (MPP) operation of both PV sources and maintain the output waveform quality. Compared to the traditional two-stage PV inverter, the proposed NPC inverter could reduce the PV array voltage requirement and the voltage rating of dc-link capacitors; also it shows advantages in operational efficiency. MATLAB simulations and experimental results are presented to examine the performance of the proposed three-level NPC inverter.

1. Introduction

Recently, photovoltaic (PV) power generations are widely applied in the distribution network. The PV power generation system can be classified into two main categories of grid-tied and off-grid systems, and the grid-tied system dominates the PV applications in terms of the generation capacity. To date, most of the applied PV converters are two-level inverter, whose main shortcomings are high operation voltage and low operational efficiency [1, 2]. For the purpose of increasing power conversion efficiency, the multilevel converters are preferably assumed as the interfacing converter between the PV array and the distribution grid due to its inherent operational characteristics [3–7], such as the reduced voltage stress, low harmonic distortion, low electro-magnetic interference (EMI), and reduced current rating. Moreover, the mature 1500V PV panel in commercial allows PV systems to be integrated into the high voltage grid without the galvanic isolation using the multilevel converters [8, 9]. Besides, the common two-level inverter utilizes buck topology, thus a step-up transformer is mandatory at the grid-side, which would increase the size and cost of the PV generation system. At present, the two-stage neutral-point-clamped (NPC) inverter has been widely used in industry as the interfacing converter in dozens of kW PV applications, whose circuit diagram is drawn in Figure 1. Two dc-dc boost converters are directly connected to the upper and lower dc rails of a traditional NPC inverter.

For the effort of making a compact design, this paper proposes a novel single-stage buck-boost three-level NPC inverter as the interfacing circuit to tie separated PV arrays to grid. In addition, the proposed control method can individually track the MPP for each PV array and boost the PV voltages to a higher dc-link voltage. The upper/lower dc-link voltages are also balanced by adjusting the switching states of NPC inverter, which could guarantee the grid-side current quality.

Compared to the two-stage NPC inverter, the proposed inverter saves two diodes and exhibits lower voltage rating of dc-link capacitors as well as lower voltage rating of front-end switches. Moreover, the proposed inverter exhibits higher efficiency under high voltage boosting ratio condition.

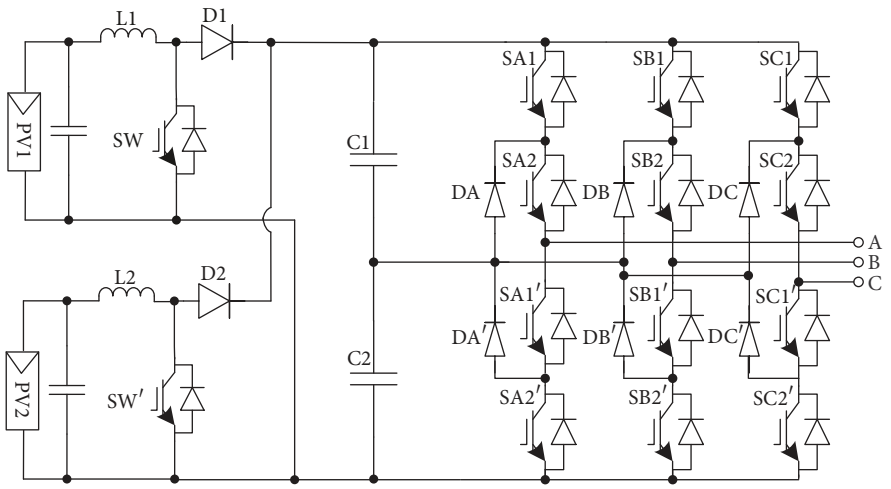


Figure 1: Topology of two-stage three-level NPC inverter.

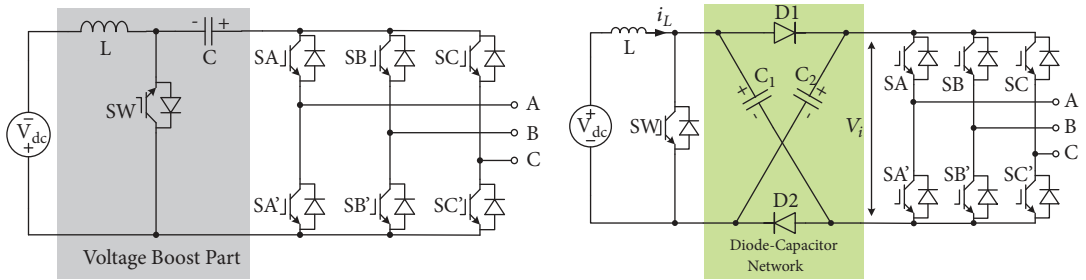


Figure 2: Topologies of (a) Ćuk-derived and (b) diode-assisted buck-boost two-level inverter.

Theoretical analysis has been done in Section 5 to compare the proposed inverter with two-stage NPC inverter in terms of operational efficiency. Finally, MATLAB simulations and experimental prototype verified the performance of the proposed three-level inverter.

2. Review of Single-Stage Buck-Boost Inverters

2.1. Single-Stage Buck-Boost Two-Level Inverters. Figure 2(a) shows the Ćuk-derived buck-boost two-level inverter [10], where capacitor C, switch SW, and inductor L form the voltage boosting part. The voltage boosting part, functioning as the energy storage and delivering intermediate, operates in particular with two distinct states defined by ON and OFF states of SW. The following equation for the Ćuk-derived buck-boost two-level inverter can be obtained:

$$\frac{V_g}{V_{dc}} = \frac{M}{2(1-k)} \tag{1}$$

where V_g refers to the amplitude of grid phase voltage, V_{dc} refers to the DC source input voltage, M refers to the modulation index, and k refers to the duty ratio of switch SW. Specifically, the ratio value (V_g/V_{dc}) is named as voltage boosting ratio, which demonstrates the inverter's voltage boosting capability from DC input voltage to grid voltage amplitude.

Figure 2(b) shows another type of single-stage buck-boost two-level inverter named as the diode-assisted buck-boost inverter [11]. The main difference between the Ćuk-derived inverter and the diode-assisted inverter is that the diode-assisted inverter contains one more diode and capacitor to form the X-shaped diode-capacitor network, which could increase the dc-link voltage doubly. And the voltage boosting ratio of the diode-assisted buck-boost inverter can be derived as:

$$\frac{V_g}{V_{dc}} = \frac{M}{1-k} \tag{2}$$

According to (1) and (2), it is noted that the diode-assisted buck-boost inverter has a higher voltage boosting ratio and it also shows a higher operational efficiency under certain voltage boosting ratio than the traditional two-stage buck-boost inverter [12].

Besides, Figure 3 shows the topology of traditional two-level Z-source inverter [13–15], where the X-shaped capacitor-inductor network couples the rear-end inverter circuit and dc source. The unique shoot-through state of Z-source inverter provides the voltage boosting function. The

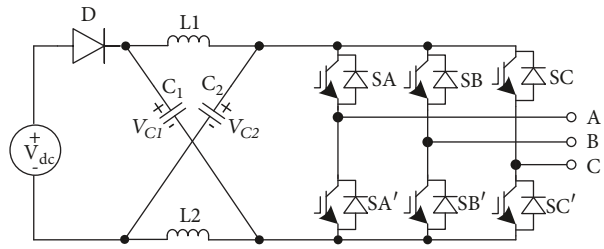


Figure 3: Topology of two-level Z-source inverter.

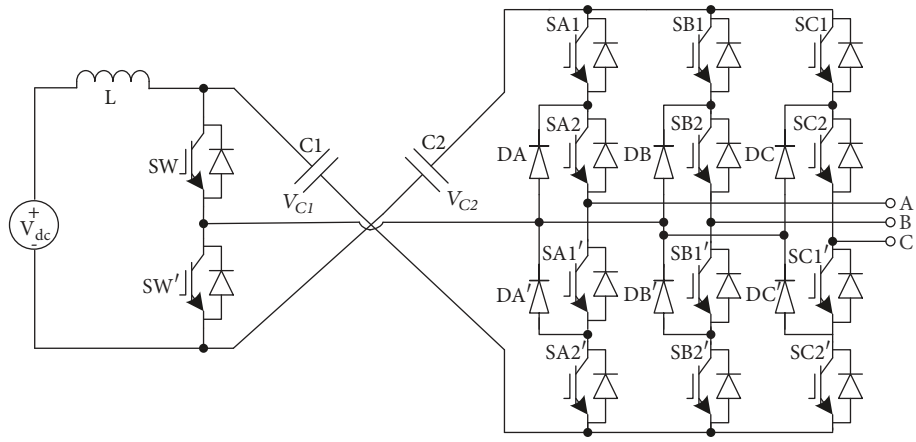


Figure 4: Topology of AE-NPC inverter.

voltage boosting ratio of two-level Z-source inverter can be expressed as

$$\frac{V_g}{V_{dc}} = \frac{M}{2\left(1 - T_0/T\right)} \tag{3}$$

where T refers to the switching cycle of Z-source inverter and T_0 represents the shoot-through duration.

The quasi-Z-source inverter was firstly presented in [16, 17] and the main advantage of the quasi-Z-source converter is lower dc capacitor voltage due to the specific embedded-dc-source circuit. Furthermore, the switched-inductor with the quasi-Z-source converter could increase the boost factor by increasing few elements [18]. The other derive topologies of Z-source converter, consisting of Trans-Z-source, Semi-Z-source [19, 20], are performed with the higher boost factor and lower voltage stress of the devices.

2.2. Single-Stage Buck-Boost Multilevel Inverters. Based on the single-stage buck-boost two-level converters, the buck-boost multilevel inverters were proposed in [21–24] to increase power conversion efficiency. Among them, the amplitude enhanced buck-boost NPC (AE-NPC) inverter presented in [24] is representative. Figure 4 shows the topology of AE-NPC inverter, which can enhance the voltage boosting ratio and balance the dc-link voltages by controlling the front-end switches SW and SW'. The voltage boosting ratio (V_g/V_{dc}) of AE-NPC inverter is the same as (2).

However, the single-stage inverters shown in Figures 2–4 utilize single dc source to power the buck-boost power generation. When implemented in PV generation system, these single-stage inverters cannot effectively handle the power reduction induced by the mismatching of separate PV panels.

To further explore the buck-boost three-level inversion technique in grid-tied PV application, this paper proposes a novel dual-source AE-NPC topology to couple two separate PV sources and a NPC inverter. The corresponding topological and control illustrations of the proposed inverter will be presented in the following sections.

3. Topological Illustration and Operational Principle of Dual-Source AE-NPC Inverter

The proposed dual-source AE-NPC three-level inverter with two input PV arrays is shown in Figure 5, and the voltage boosting part consists of two switches and inductors. Compared with the buck-boost inverter shown in Figure 4, an additional inductor is added in shunt to conduct source current in case of unequal PV currents. Two switches SW and SW' are directly connected to the PV sources, being different from Figure 4 so that two separate PV sources can be controlled independently. Furthermore, the proposed inverter topology could save two diodes when compared with the two-stage NPC inverter.

The equivalent circuits are shown in Figure 6 to describe operating modes of the proposed inverter more specifically. The first operating mode {SW =1 and SW' =0} is shown in Figure 6(a), where the inductor L1 is charged by the source

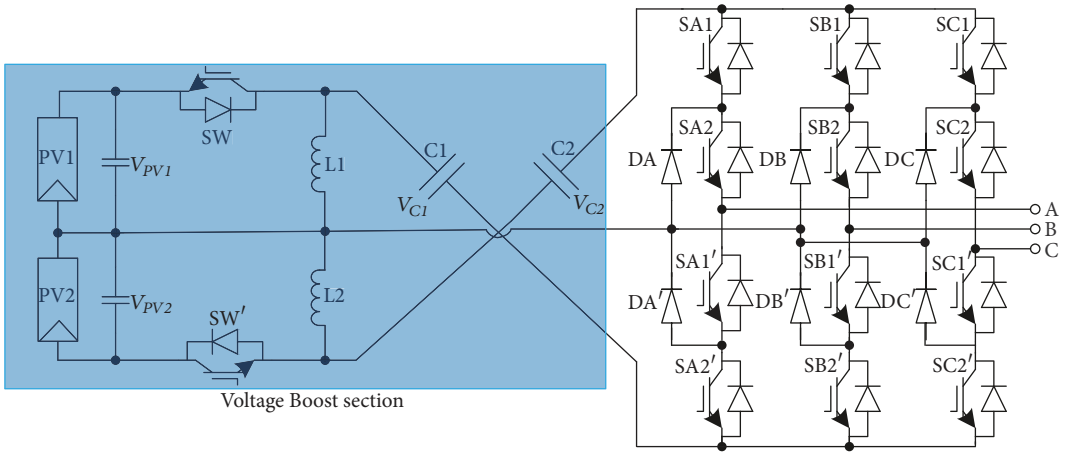
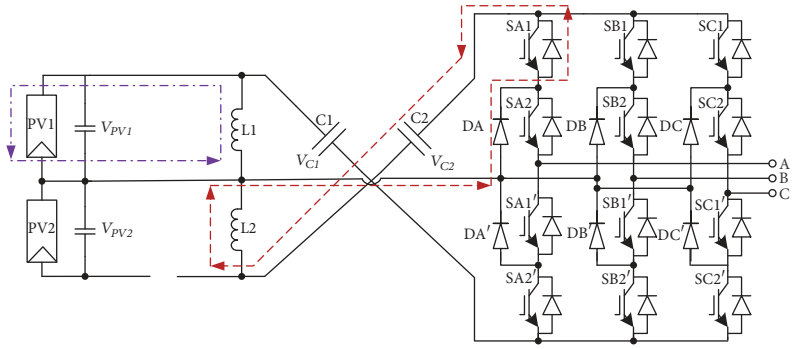
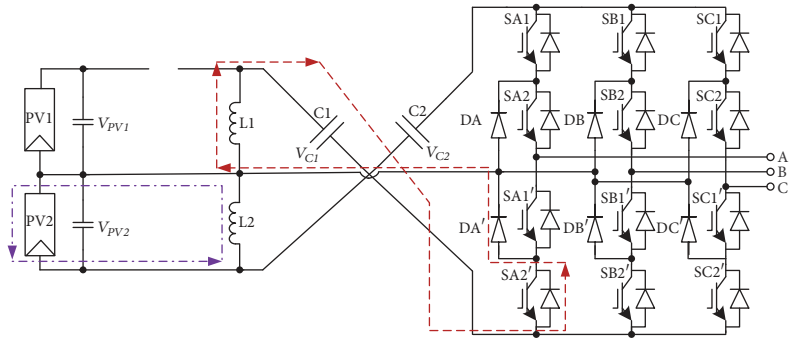


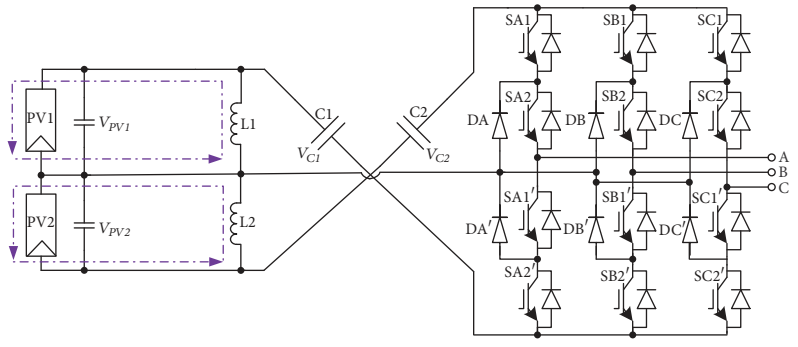
Figure 5: Topology of dual-source AE-NPC inverter.



(a)



(b)



(c)

Figure 6: Equivalent circuits of dual-source AE-NPC inverter when (a) SW = ON and SW' = OFF, (b) SW = OFF and SW' = ON, and (c) SW = SW' = ON.

Table 1: Possible output switching states under different operation modes of dc/dc voltage boosting part.

Operation modes of dc/dc voltage boosting part	SW= SW'=1	SW= 0, SW'=1	SW= 1, SW'=0
Possible output switching states of NPC inverter	all the switching states shown in Figure 8	{1,0,0},{1,1,0},{0,1,0} {0,1,1},{0,0,1},{1,0,1}	{0,-1,-1},{0,0,-1},{-1,0,-1} {-1,0,0},{-1,-1,0},{0,-1,0}

PV1 and the inductor L2 current will flow through DX and SX1 (X = A, B or C) to charge the capacitor C2. Similarly, during the operating mode {SW = 0 and SW' = 1} shown in Figure 6(b), the inductor L2 is charged by the source PV2 and the inductor L1 current will flow through DX' and SX2' to charge the capacitor C1. Figure 6(c) shows the circuit diagram under {SW = 1 and SW' = 1}, where both inductors are charged by the corresponding PV source. And the capacitor voltages V_{C1} and V_{C2} can be expressed as

$$\begin{aligned} \frac{V_{PV1}}{L_1} \times k_1 T = \frac{V_{C1}}{L_1} \times (1 - k_1) T \Longrightarrow V_{C1} = \frac{k_1 V_{PV1}}{1 - k_1} \\ \frac{V_{PV2}}{L_2} \times k_2 T = \frac{V_{C2}}{L_2} \times (1 - k_2) T \Longrightarrow V_{C2} = \frac{k_2 V_{PV2}}{1 - k_2} \end{aligned} \tag{4}$$

where k_1 and k_2 represent the duty ratio of SW and SW', respectively; V_{PVx} refers to the voltage of PVx (x=1, 2). Therefore, the upper dc-link voltage V_{up}, the lower dc-link voltage V_{dn}, and the whole dc-link voltage $V_{dc\text{-}link}$ are calculated as

$$\begin{aligned} V_{up} &= V_{C2} + V_{PV2}, \\ V_{dn} &= V_{C1} + V_{PV1} \\ V_{dc\text{-}link} &= V_{up} + V_{dn} = \frac{V_{PV1}}{1 - k_1} + \frac{V_{PV2}}{1 - k_2} \end{aligned} \tag{5}$$

The dc capacitors together with the PV sources generate the whole dc-link. Compared to the two-stage NPC inverter, the proposed inverter exhibits lower voltage rating of dc-link capacitors as well as lower voltage rating of front-end switches.

Further, if assuming $k_1 = k_2 = k$ and $V_{PV1} = V_{PV2} = V_{PV}$, the voltage boosting ratio can be expressed as

$$BF = \frac{V_{dc-link}}{V_{PV}} = \frac{2}{1 - k} \tag{6}$$

The relationship of the boost factor with the duty ratio could be shown as Figure 7 according to (6). And the proposed inverter exhibits higher voltage boosting ratio.

To smoothly modulate the dual-source AE-NPC inverter, this paper adopts the phase disposition (PD) modulation scheme. As shown in Figure 8, the three-phase sinusoidal reference lines m_A, m_B, and m_C are compared with two carriers to generate the corresponding switching states. Besides, the switching signals of SW' and SW are induced by two additional linear modulation references V_U and V_L, respectively.

Table 1 shows the possible output vectors under different operation modes of voltage boosting part. Take the operation mode {SW = 0 and SW' = 1}, for example, the NPC inverter can still output the switching states of {1,0,0}, {1,1,0}, {0,1,0}, {0,1,1}, {0,0,1}, and {1,0,1} shown in Figure 9. Since C2 and PV2 are connected in series to form the upper dc-link voltage and thus can power the rear-end NPC circuit. Similarly, during the operation mode {SW = 1 and SW' = 0}, the NPC inverter can output the switching states {0,-1,-1}, {0,0,-1}, {-1,0,-1}, {-1,0,0}, {-1,-1,0}, and {0,-1,0}. And during the operation mode {SW = 1 and SW' = 0}, PV1, PV2, C1, and C2 are connected in series to form the whole dc-link voltage. In this mode, the NPC inverter can freely output all the three-level switching states shown in Figure 9.

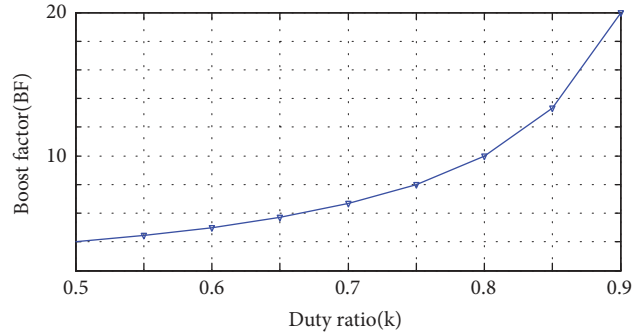


Figure 7: Variation of boost factor (BF) with duty ratio(k).

4. Control Strategy of Dual-Source AE-NPC Inverter with the Front-End PV Sources

The main control destination of the dual-source AE-NPC is to implement the MPP operation of both PV sources and keep the output waveform quality. Figure 10 shows the control block of the overall power generation system. And the two MPPT control blocks induce the modulation signals of the two switches SW and SW', respectively. The calculated total input active power is transferred into the output current reference to accurately regulate the output current utilizing the current feedback control. Besides, to balance the upper and lower dc-link voltages, the capacitor voltages V_{C1}, V_{C2} are controlled individually by modifying the switching states of NPC inverter. The proposed control strategy will be illustrated in the following text.

4.1. Maximum Power Point Control. The perturb and observe MPPT algorithm is assumed to maintain the MPP operation of both PV sources. The PI controller shown in (7) is adopted to precisely track the voltage reference generated by MPPT algorithm. As illustrated in Figure 10, the output of

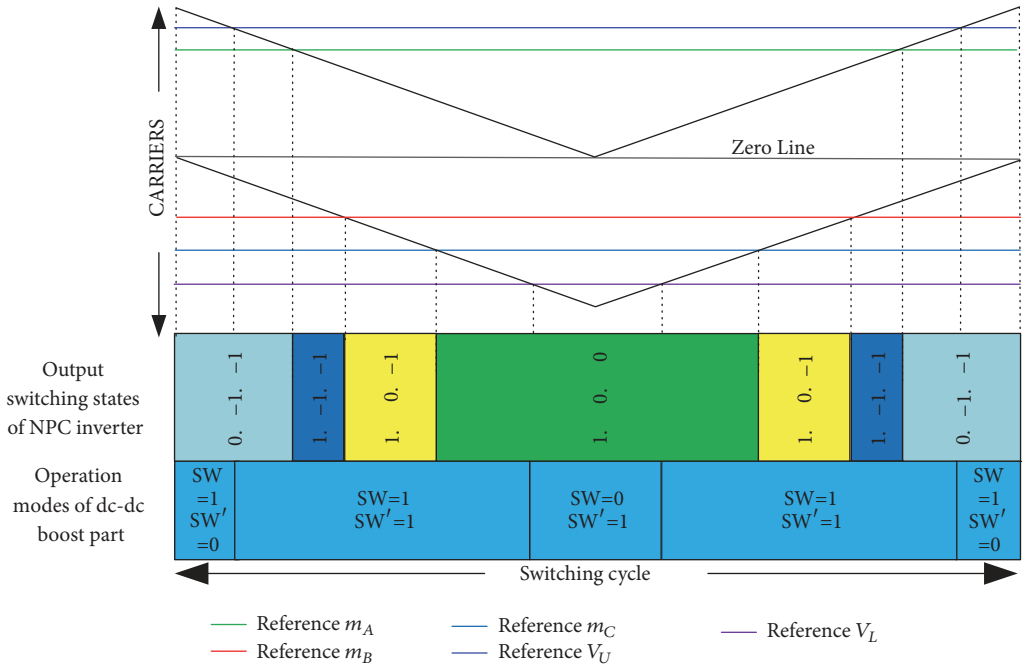


Figure 8: Illustration of PD modulation for dual-source AE-NPC inverter.

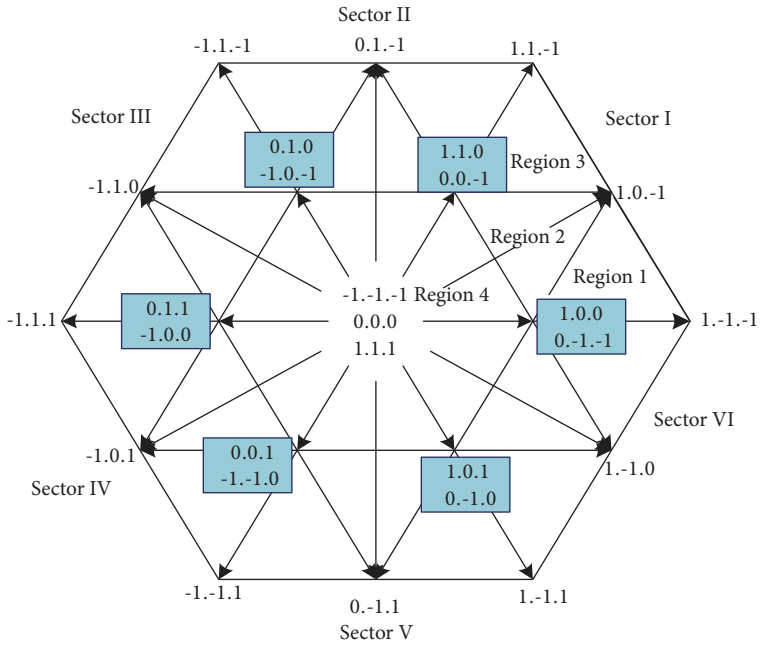


Figure 9: Space vector diagram of three-level inverter.

PI controller will be compared with the triangular carrier to generate the modulation signals for SW and SW', respectively.

$$G_{PI}(s) = k_{p\_pi} + k_{i\_pi}\frac{1}{s} \tag{7}$$

where k_{p_pi} is the proportional gain and k_{i_pi} refers to the integral gain.

4.2. Closed-Loop Output Current Control. The ideal current reference is derived as (8), which assumes the unity power factor condition:

$$I_g^* = \frac{2\left(P_{PV1} + P_{PV2}\right)}{3V_g} \tag{8}$$

where $I^*{}_g$ refers to the ideal current reference and P_{PVx} refers to the output active power of PVx ($x = 1$ or 2).

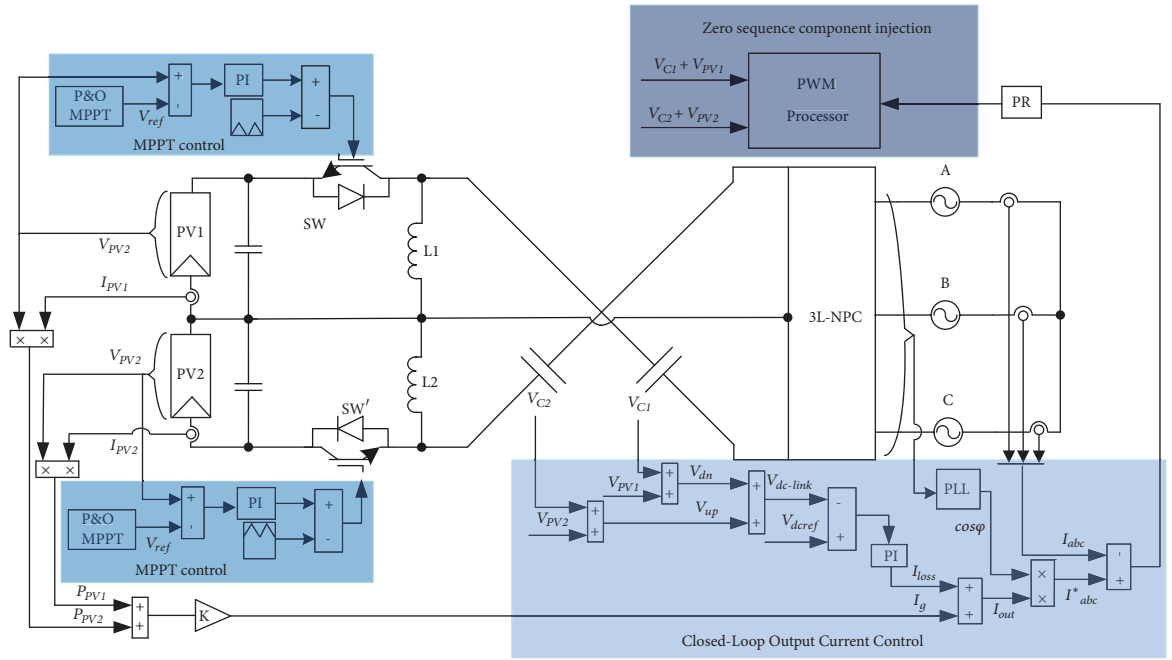


Figure 10: Overall control diagram of dual-source AE-NPC inverter for grid-tied PV application.

Moreover, due to the power losses in the circuit, a current reference compensation I^*_{loss} generated by the dc-link PI controller should be added to the ideal current reference I^*_g, as shown in Figure 10. The dc-link PI controller is identical to (7). Doing so, the overall dc-link voltage ($V_{\text{C1}} + V_{\text{C2}} + V_{\text{PV1}} + V_{\text{PV2}}$) can be regulated as a constant value.

The PR controller expressed in (9) is utilized to precisely track the current reference ($I^*_{\text{g}} + I^*_{\text{loss}}$) without steady state error.

$$G_{PR}(s) = k_{p\_pr} + k_{r\_pr}\frac{s}{s^2 + \omega_0^2} \tag{9}$$

where k_{p_pr} and k_{r_pr} are the control gains and ω_0 is the resonant frequency.

4.3. DC-Link Voltage Balancing Control Method. The PV currents in MPP condition will be different when mismatch appears between the two input PV sources. Consequently, the charging current of dc-link capacitors would be different under the MPP operation, which in turn produces the unbalanced upper and lower dc-link voltages if still utilizing the traditional PD modulation scheme as stated in Section III. The averaged upper and lower dc-link voltages, $V_{\text{up\_ave}}$ and $V_{\text{dn\_ave}}$, can be expressed as (10) when utilizing no dc-link voltage balancing control scheme:

$$\begin{aligned} V_{up\_ave} &= \frac{P_{PV2}V_{dc-link}}{P_{PV1} + P_{PV2}}, \\ V_{dn\_ave} &= \frac{P_{PV1}V_{dc-link}}{P_{PV1} + P_{PV2}} \end{aligned} \tag{10}$$

The unbalanced dc-link voltage would induce low-order harmonics and may damage the switches and capacitors because of the overvoltage condition [25]. And the dc-link balance control is the main issue of the NPC converter. Therefore, the possible solution is either to balance the input power, maintaining $P_{\text{PV1}} = P_{\text{PV2}}$, which is not desirable since the PV sources will deviate from their MPP operation, or to regulate the discharging currents of dc-link capacitors. The discharging current can be modified by controlling the duration of the inner vectors presented in Figure 9 [26]. For example, two equivalent null states (0, -1, -1) and (1, 0, 0) per switching sequence in Figure 10 could output the same line-to-line voltage but the opposite neutral current direction. Therefore, adjusting the duration of equivalent null states can change the discharging current of dc-link capacitors and therefore balance the dc-link voltages [26–32]. Based on the duration modification of the equivalent null states, the three-phase NPC converter with dual PV arrays can simultaneously realize the dc-link balance and MPP operation under different irradiation [32].

In order to balance dc-link voltages and maintain MPP operations, this paper adopts the zero-sequence component injection method to change the discharging duration of the dc-link capacitors. The illustration of the modified PD modulation strategy with zero-sequence component injection is shown in Figure 11, where the previous reference lines are added by the zero-sequence components m_o to achieve dc-link balance, that is, $m_{xo} = m_x + m_o$ (x = A, B or C). And the positive zero-sequence component is injected to increase the duration of state (1, 0, 0) and to decrease the duration of state (0, -1, -1). Doing so, the upper dc-link voltage decreases; meanwhile it will not induce the low-order harmonic distortion to grid-side current.

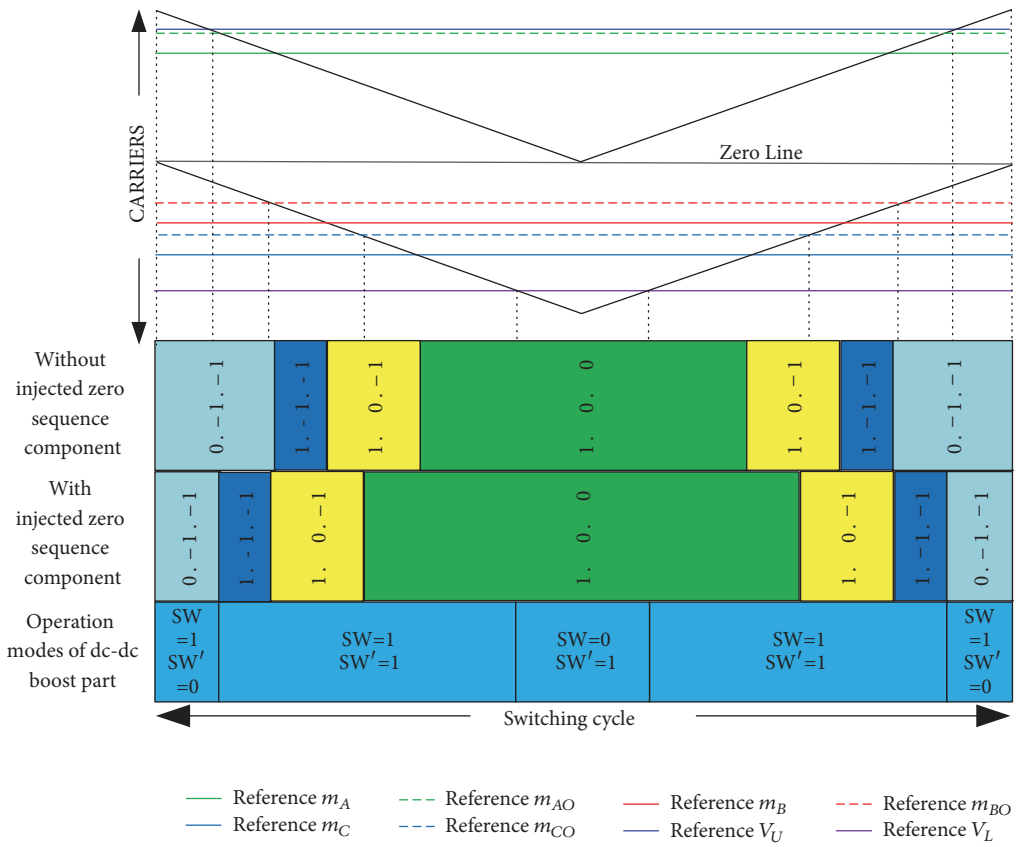


Figure 11: Illustration of the modified PD modulation strategy with zero-sequence component injection.

Under the zero-sequence voltage injection, the neutral current I_0 can be expressed as [26]

$$I_0 = -|m_{AO}| \cdot I_g \cos(\omega t) - |m_{BO}| \cdot I_g \cos\left(\omega t - \frac{2\pi}{3}\right) - |m_{CO}| \cdot I_g \cos\left(\omega t + \frac{2\pi}{3}\right) \quad (11)$$

where I_g refers to the amplitude of output ac current and the zero-sequence component m_o can be written as

$$m_0 = \begin{cases} M - \max(m_A, m_B, m_C) & V_{up} > V_{dn} \\ -M - \min(m_A, m_B, m_C) & V_{up} < V_{dn} \end{cases} \quad (12)$$

where M refers to the modulation index. Figure 12 illustrates the modulation reference with the zero-sequence component. In addition, the averaged neutral current I_{0_ave} can be derived as

$$I_{0\_ave} = \frac{1}{2\pi} \int I_0(wt)\, d(wt) \quad (13)$$

According to (11)–(13), the discharging currents of dc-link capacitors will be regulated unequally by controlling the averaged neutral current. Moreover, the dc-link voltage can

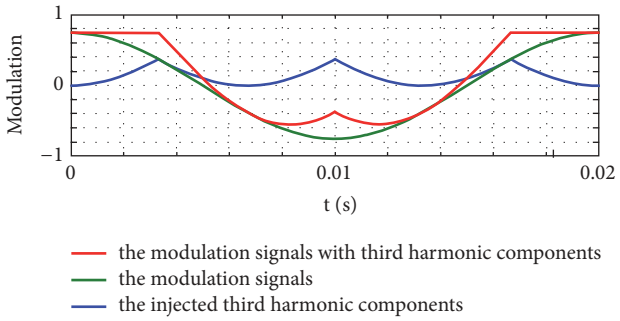


Figure 12: The ideal modulation references of the AE-NPC converter.

be balanced when the averaged output currents of the dc-link capacitors satisfy the following equation:

$$\left.\begin{aligned} \frac{V_{dc-link} I_{up_{ave}}}{2} &= P_{PV2} \\ \frac{V_{dc-link} I_{dn_{ave}}}{2} &= P_{PV1} \end{aligned}\right\} \Longrightarrow I_{up\_ave} - I_{dn\_ave} = \frac{2(P_{PV2} - P_{PV1})}{V_{dc-link}} = -I_{0\_ave} \quad (14)$$

where I_{up_ave} and I_{dn_ave} refer to the averaged discharging currents of dc-link capacitors C2 and C1, respectively. The

zero-sequence component injection can realize the dc-link balance and MPP operation. However, such regulation has a limitation since the range of controlled averaged neutral current is limited. According to (12)-(13), the range of the averaged neutral current I_{0_ave} can be derived as

$$-0.33MI_g \le I_{0\_ave} \le 0.33MI_g \tag{15}$$

Further, according to (14) and (15), the dc-link voltage can be balanced under the following condition:

$$0.64 \le \frac{P_{PV1}}{P_{PV2}} \le 1.56 \tag{16}$$

5. Efficiency Comparison

Compared to the two-level inverter, the NPC inverter exhibits higher efficiency when both switching frequency are greater than 8 kHz [33]. Since the switching frequency in the PV application with rated power < 30kW is 10kHz or more, the two-stage three-level NPC inverter will be more efficient than the two-level converter. On the other hand, along with the mature of 1500V PV panel technology, the PV system can be integrated into a high voltage grid (e.g., 690V grid) to reduce losses. In this case, the NPC inverter could be deemed as a competitive candidate in practice. Therefore, the efficiency comparison in this paper will be focused on the two-stage NPC inverter and the proposed dual-source AE-NPC inverter.

Before analyzing the switching losses, a fair basis for comparison is drawn by tuning the inverters to produce the same input-to-output voltage gain. The duty ratios of front-end switches SW and SW' in dual-source AE-NPC inverter and two-stage NPC inverter can be derived as

$$\frac{M_B}{2\left(1-k_B\right)} = \frac{M_S}{1-k_S}; \quad 0.5 \le k_S,\ k_B \le 1 \tag{17}$$

where the subscripts "B" and "S" indicate the variable of two-stage NPC inverter and the proposed single-stage NPC inverter, respectively. Specifically, M_B and k_B represent the ac modulation index and dc-end transistor duty ratio in two-stage NPC inverter, while M_S and k_S represent the ac modulation index and dc-end transistor duty ratio in the proposed single-stage NPC inverter. As analyzed above, the modulation index M_S of dual-source AE-NPC inverter should be set to k_S to maximize the dc-link voltage utilization, while the modulation index M_B of two-stage NPC inverter is independent on k_B, which can be set to 1. Then the relationship of dc-link voltages of both inverters can be described as

$$V_{dc\text{-}link,B} = k_S V_{dc-link,S} \tag{18}$$

The dual-source AE-NPC inverter suffers a higher dc-link voltage stress and more switching losses in the rear-end NPC circuit. However, the blocking voltage of the front-end switches SW and SW' in dual-source AE-NPC inverter is lower than that of the switches and diodes in two-stage NPC inverter, thus the dual-source AE-NPC inverter suffers lower switching losses in the front-end circuit. Since the conduction currents of both inverters keep equal at any instant, conduction dissipation of the rear-end NPC circuitry will not be discussed in this paper.

The switching and conduction dissipations of the IGBTs used in both topologies can be derived as [34, 35]

$$\begin{aligned} P_{switch} &= \frac{1}{2} V_{OFF} I_{ON} t_{tr} f_{SW} \\ P_{cond} &= V_{CE} I_{ON-ave} \end{aligned} \tag{19}$$

where P_{switch} refers to the total switching dissipation of single-stage or two-stage converter, V_{CE} refers to collector-emitter saturation voltage, and V_{OFF} refers to the turn-on or turn-off voltage of switches. I_{ON} represents the conducting current of the switches, t_{tr} represents the sum of turn-on and turn-off transient duration of switches, and f_{SW} refers to switching frequency. The switching dissipation of both inverters can be derived as follows.

Dual-Source AE-NPC Inverter

$$\begin{aligned} P_{switch\_dc(S)} &= \frac{1}{2} V_{dc-link,S} I_{L,S} t_{tr} f_{SW} \\ P_{switch\_ac(S)} &= \frac{3}{\pi} V_{dc-link,S} I_g t_{tr} f_{SW} \\ P_{switch(S)} &= P_{switch\_dc(S)} + P_{switch\_dc(S)} \\ &= t_{tr} f_{SW} \left(P_{PV1} + P_{PV2}\right)\left(V_g + V_{PV}\right)\left(\frac{4}{\pi V_g} + \frac{1}{2V_{PV}}\right) \end{aligned} \tag{20}$$

Two-Stage NPC Inverter

$$\begin{aligned} P_{switch\_dc(B)} &= V_{dc-link,B} I_{L,B} t_{tr} f_{SW} \\ P_{switch\_ac(B)} &= \frac{3}{\pi} V_{dc-link,B} I_g t_{tr} f_{SW} \\ P_{switch(B)} &= P_{switch\_dc(B)} + P_{switch\_ac(B)} \\ &= t_{tr} f_{SW} \left(P_{PV1} + P_{PV2}\right)\left(\frac{4}{\pi} + \frac{V_g}{V_{PV}}\right) \end{aligned} \tag{21}$$

where $I_{L,X}$ (X= B or S) refers to input inductor current and $P_{switch\_dc(X)}$ and $P_{switch\_ac(X)}$ (X = B or S) represent the dc and ac side switching dissipation. It is calculated from (20)-(21) that the proposed single-stage PV converter suffers lower switching dissipation when the boosting ratio (V_g/V_{PV}) is greater than 2.17. Furthermore, when considering the conduction losses, the forward voltage drops of the diodes and switches are assumed to be equal; therefore the conduction dissipation of the front-end circuit can be calculated as

$$\begin{aligned} P_{cond(S)} &= 2 \times V_{CE} I_{L,S} + 2 \times 2V_{CE}\left(1-k_S\right) I_{L,S} \\ &= \frac{V_{CE}}{V_{PV}}\left(P_{PV1} + P_{PV2}\right)\left(1 + \frac{2V_{PV}}{V_{PV} + V_g}\right) \end{aligned}$$

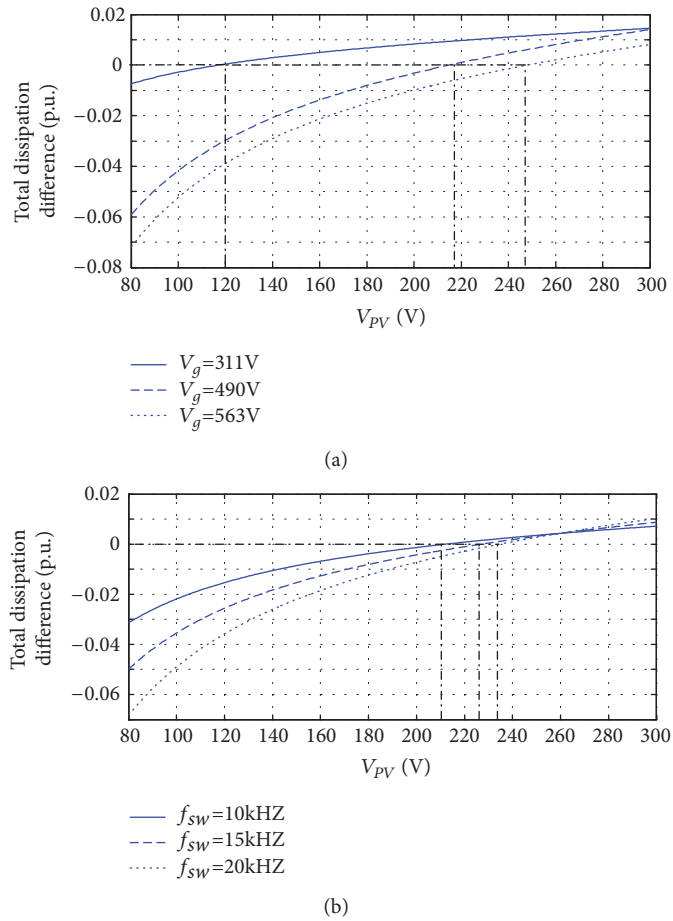


Figure 13: Dissipation comparison under (a) different ac output voltages and (b) different switching frequencies.

$$P_{cond(B)} = 2 \times V_{CE} k_B I_{L,B} + 2 \times V_{CE} (1 - k_B) I_{L,B} = \frac{V_{CE}}{V_{PV}} (P_{PV1} + P_{PV2}) \quad (22)$$

where $2\times V_{CE} I_{L,S}$ and $2\times V_{CE} k_B I_{L,B}$ represent the conduction dissipations during the switch ON period, while $2\times 2V_{CE}(1\text{-}k_S) I_{L,S}$ and $2\times V_{CE}(1\text{-}k_B) I_{L,B}$ represent the conduction dissipations during the switch OFF period. According to (22), the dual-source AE-NPC inverter always suffers a higher conduction loss than the two-stage NPC inverter. However, the conduction loss can be reduced by using the devices with a lower collector-emitter saturation voltage since the blocking voltages of SW and SW' are only half of the dc-link voltage, unlike that of the traditional two-stage NPC inverter. And the total dissipation difference between both converters can be derived from (20)–(22), which is written below:

$$\Delta P_{dis} = \left[t_{tr} f_{SW} \left(\frac{4V_{PV}}{\pi V_g} - \frac{V_g}{2V_{PV}} + \frac{1}{2} \right) + \frac{2V_{CE}}{V_g + V_{PV}} \right] \cdot (P_{PV1} + P_{PV2}) \quad (23)$$

where ΔP_{dis} represents the total dissipation difference. It is noted from (23) that the dissipation comparison between both converters is related to the parameters of switching frequency f_{SW}, input PV voltage V_{PV}, grid voltage V_g, and collector-emitter saturation voltage V_{CE}. In this case, the theoretical calculation assumes the IGBT of FF150R17KE4 produced by Infineon with V_{CE}, t_{tr}, and f_{SW} to be 1.75V, 1300ns, and 20kHz, respectively. The calculation results are drawn in Figure 13. When PV voltage is below the threshold voltages shown in Figure 13(a), the dual-source AE-NPC inverter exhibits lower dissipation than the two-stage inverter ($\Delta P_{dis} < 0$). For the condition V_g = 311V, 490V, and 563V, the threshold voltages equal 120V, 217V, and 246V, respectively. Also, the dissipation comparisons under different PV voltages and switching frequencies are presented in Figure 13(b), where V_g is equal to 563V.

In general, compared to the two-stage NPC inverter, the proposed dual-source AE-NPC inverter saves two diodes and exhibits lower voltage rating for dc-link capacitors and front-end switches. Moreover, the proposed inverter exhibits higher efficiency under high voltage boosting ratio conditions.

6. Simulation and Experimental Verifications

The proposed AE-NPC inverter is built by MATLAB/SIMULINK. And Table 2 shows the parameters of the AE-NPC circuit and two PV sources. In addition, the PV array

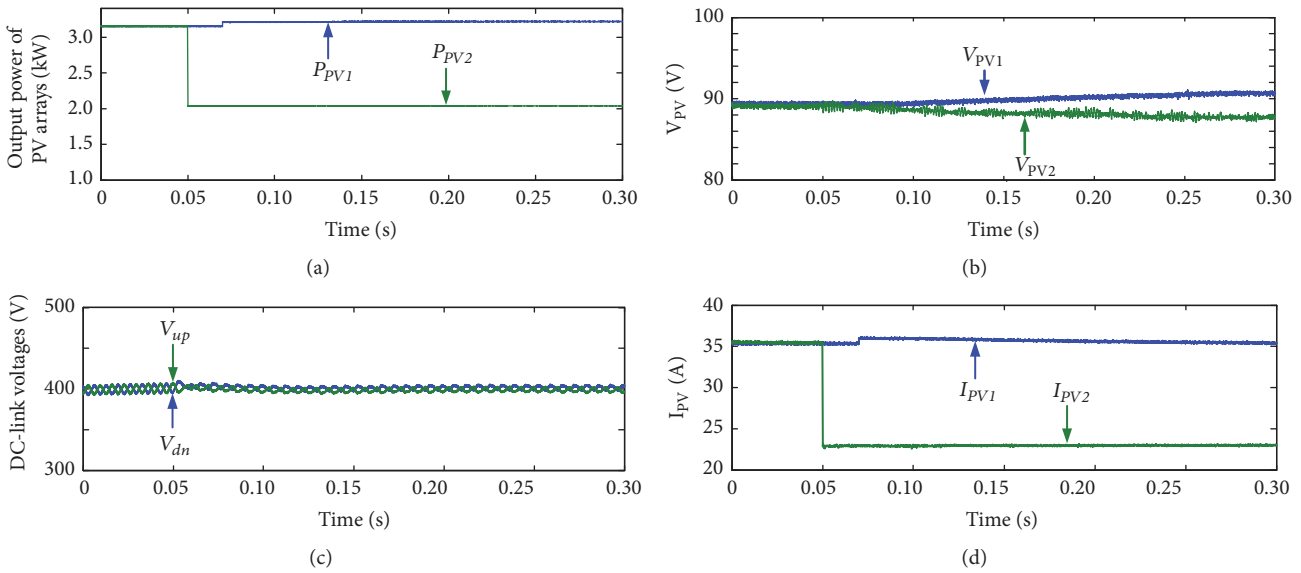


Figure 14: Simulated results of (a) output PV power, (b) PV voltages, (c) upper/lower dc-link voltages, and (d) PV currents.

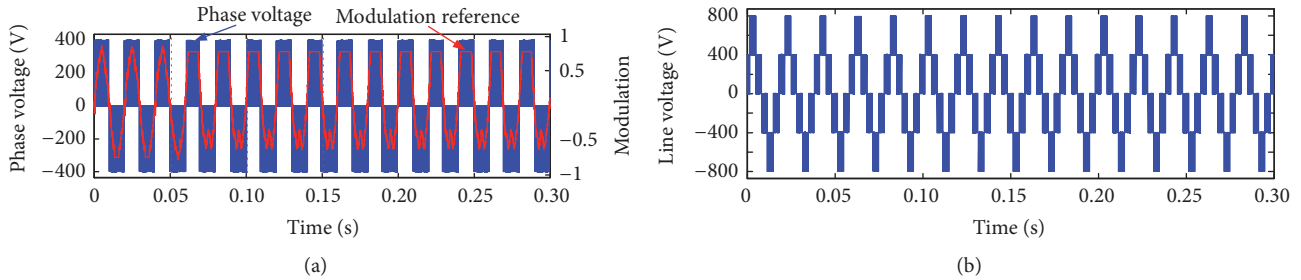


Figure 15: Output waveform of (a) switching phase voltage and its modulation reference and (b) switching line voltage.

Table 2: Simulation parameters.

Parameter	value	Parameter	value
dc-side inductor (L1, L2)	1mH	ac-side filter inductor	5mH
dc-link capacitor (C1, C2)	1000μF	grid phase voltage amplitude (V_g)	311V
overall dc-link voltage (V_{C1}+V_{C2}+V_{PV1}+V_{PV2})	800V	carrier frequency (f_{SW})	10kHZ
PV array short-circuit current (1000W/m^2)	38A	PV array open circuit voltage (0°C)	109V

for the transformer-less PV is connected to the grid without galvanic isolation and the voltage fluctuation between the PV array and the ground would generate leakage current. The leakage current could be eliminated by effectively reducing the fluctuation of the common-mode voltage (CMV). In general, there are two main methods to eliminate the leakage current. Firstly, the variation of the CMV could be reduced by applying the specific vectors utilizing the Space Vector Modulation strategy [36]. Secondly, the common-mode component could be attenuated by the passive filter network presented in [37]. And the passive filter was utilized in this paper to eliminate the leakage current.

Figure 14 shows the simulated PV voltage, PV power, upper/lower dc-link voltages, and PV currents under temperature and irradiation variations, the irradiation of PV1 varies from 1000W/m^2 to 650W/m^2 at 0.05s, and the temperature of PV2 decreases from 15°C to 10°C at 0.07s. Therefore, the output power of PV1 is decreased to about 2000W at 0.05s and PV2 output power increases 70W at 0.07s because of temperature variation. Moreover, the proposed control strategy can fast track the MPP variation, which is shown in Figure 14(a). Figure 14(b) shows the PV voltages under their corresponding MPPs. Figure 14(c) shows that the dc-link voltage can be balanced, and the proposed method could modify the switching states of NPC circuit to compensate the mismatching of upper and lower PV arrays. And the PV currents under the MPP operation condition are shown in Figure 14(d). Moreover, the PV2 current almost keeps unchanged when the PV2 temperature varies to 10°C, and the PV1 current has a sharp decline because of the irradiation variation. However, different PV currents would not affect the whole operational effectiveness due to the novel topological circuit.

Further, the voltage and current of NPC inverter are shown in Figures 15 and 16, respectively. Figure 15 shows one switching phase voltage, one switching line voltage, and its

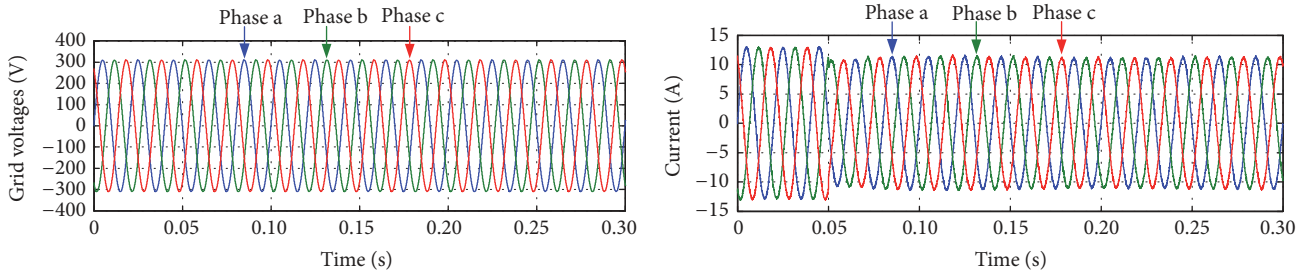


Figure 16: Waveforms of (a) grid voltages and (b) grid currents.

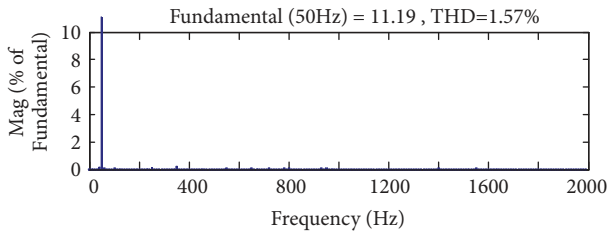


Figure 17: FFT analysis of the output AC current.

Table 3: Experimental parameters.

Parameter	value	Parameter	value
dc-side inductor (L1, L2)	1mH	filter inductor of ac side	5mH
dc-link capacitor (C1, C2)	550μF	grid phase voltage (V_g)	155V
overall dc-link voltage (V_{C1}+V_{C2}+V_{PV1}+V_{PV2})	460V	carrier frequency (f_{SW})	10kHZ
PV array short-circuit current (1000W/m^2)	8A	PV array open circuit voltage (0°C)	58.3V

modulation signal. As shown in Figure 15, after the zero-sequence component injection at 0.05s, the modulation signal and the switching characteristics of phase voltage will be changed. However, such changes will not lead to the normalized volt-sec average change and the three-phase output currents are still purely sinusoidal, as shown in Figure 16. Moreover, the FFT analysis of the grid current is shown in Figure 17 and the total harmonic distortion (THD) of output AC current is 1.57%.

Next, proceeding to the experimental verification, the corresponding experimental parameters are listed in Table 3. Two rooftop installed PV sources were used, whose maximum power points are both 50V and 7.4A. The output power of the whole PV arrays is about 700W, and the amplitude of output ac current is about 3.0A. The picture of experimental prototype is shown in Figure 18. The waveforms of grid voltage and output currents are shown in Figure 19. It is noted that the inverter can output the balanced sinusoidal currents. The harmonic spectrum of phase current is shown in Figure 20. Fortunately, the zero-sequence component injection method

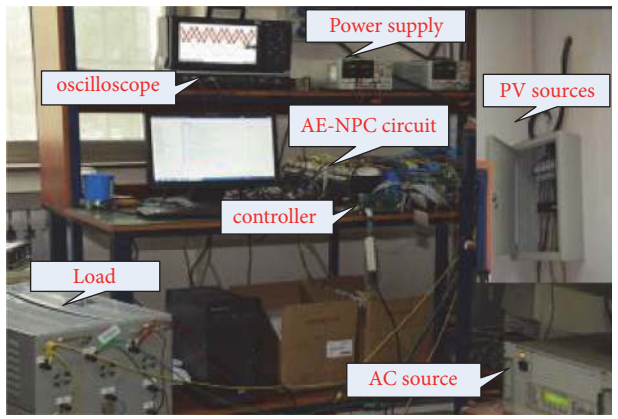


Figure 18: The experimental prototype of dual-source AE-NPC inverter.

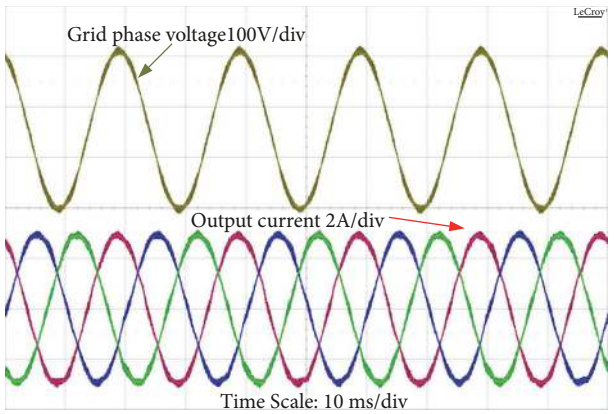


Figure 19: Captured grid voltages and output currents.

did not produce the low-order harmonic distortion and the THD of phase current is 2.56%.

The switching phase voltages and phase B current are shown in Figure 21, and Figure 22 presents the switching line voltages and output currents, where the output current is purely sinusoidal.

Figures 23(a) and 23(b) present the experimental waveforms under the situations where the PV voltage references are suddenly changed to examine the dynamic performance

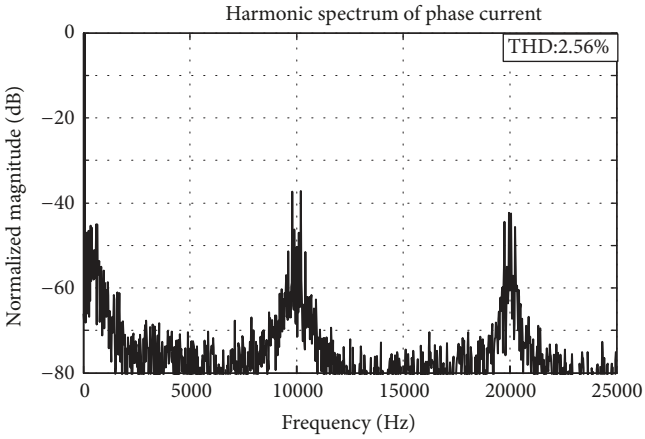


Figure 20: Harmonic spectrum of phase current.

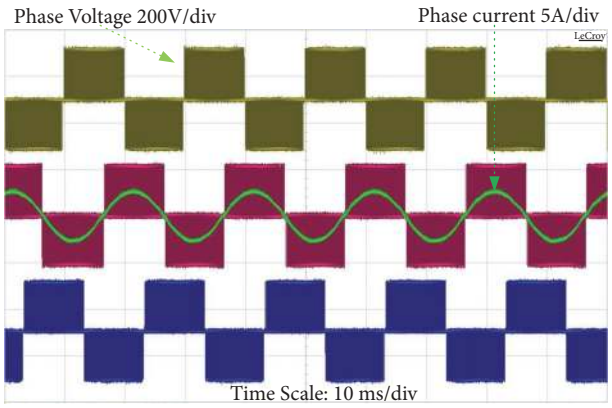


Figure 21: Switching phase voltages and phase B current.

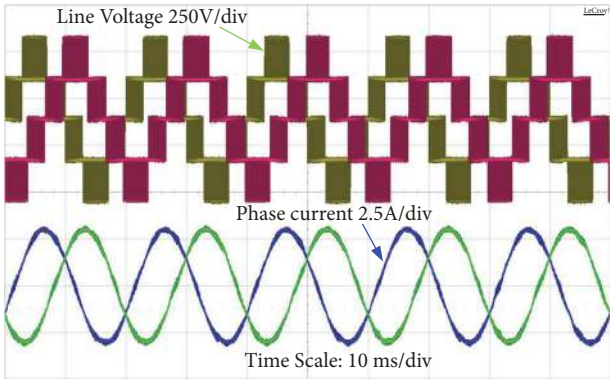


Figure 22: Switching line voltages and phase currents.

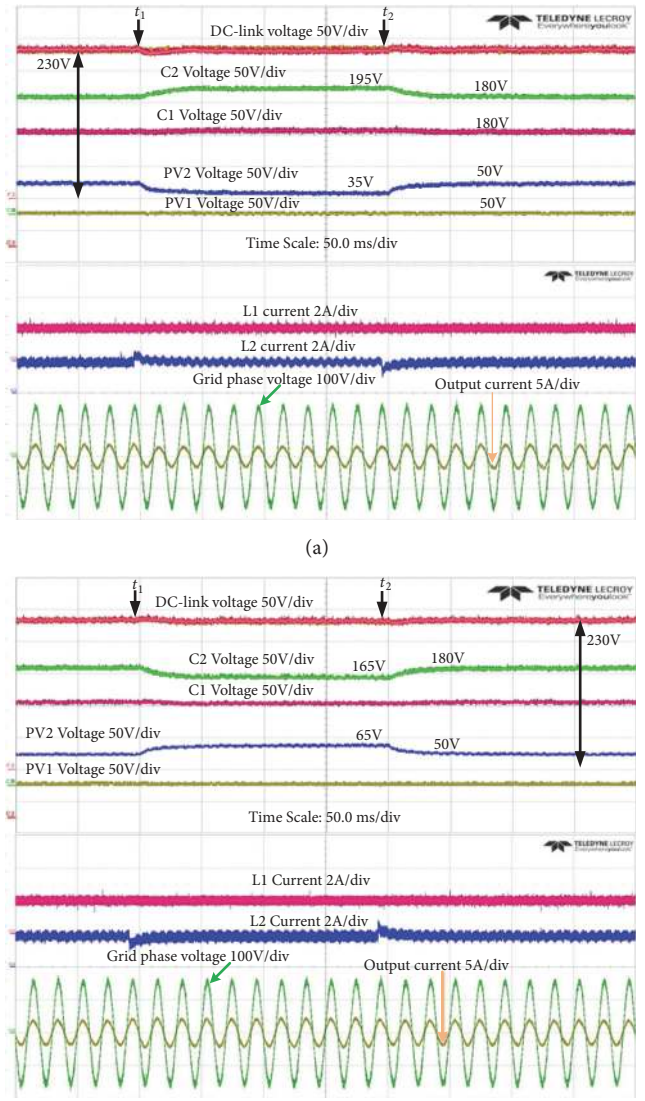


Figure 23: Experimental results of (a) PV2 voltage reference dip and (b) PV2 voltage reference swell.

on PV MPP voltage tracking and dc-link voltage balancing. In Figure 23(a), PV2 voltage reference declines to 35V at instant t_1 and recovers to 50V at instant t_2. Owing to the proposed dc-link balancing control method, the voltage V_{C2} rises up to 195V at instant t_1, so that the upper and lower dc-link voltages could be regulated symmetrically. Similarly, in Figure 23(b), PV2 voltage reference rises up to 65V at instant t_1 and recovers to 50V at instant t_2. The voltage V_{C2} declines to 165V at instant t_1 due to the participation of dc-link balancing control method, therefore the upper and lower dc-link voltages are kept balanced. Meanwhile, since the dc-link voltage is well-balanced, the grid current quality is acceptable during both scenarios presented in Figures 23(a) and 23(b).

Besides, the dynamic performance of dual-source AE-NPC inverter under unsymmetrical irradiation is investigated. Since the irradiation of rooftop installed PV panel cannot be suddenly changed, two programmable dc sources (Chroma 62150H) were used to emulate the PV panels. As shown in Figure 24, one emulated PV current suffers a sudden dip at instant t_0. The dc-dc part still manages to track the dual PV voltage at 50V effectively, while the NPC inverter takes the responsibility to balance the dc-link

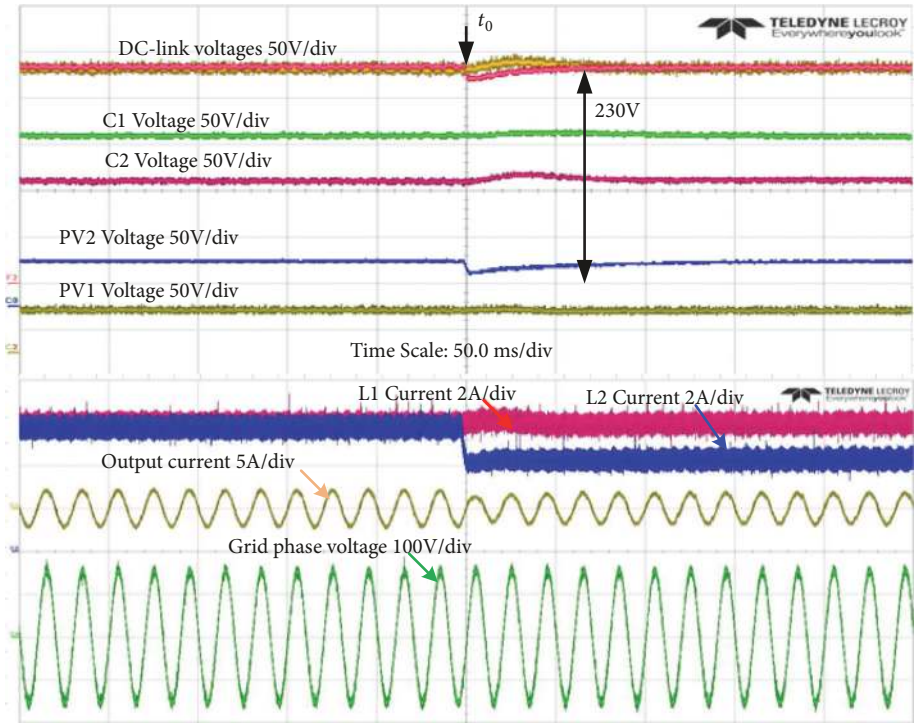


Figure 24: Experimental results of irradiation sudden change of PV2 source.

voltage. Consequently, the upper and lower dc-link voltages (V_{C2}+V_{PV2}) and (V_{C1}+V_{PV1}) can be balanced and stabilized in a short interval; also the grid current quality is acceptable under the unbalanced irradiation condition.

7. Conclusions

This paper proposes a novel single-stage buck-boost three-level NPC inverter, which can couple two separate dc sources in front and balance the upper and lower dc-link voltages. The corresponding operational principles are analyzed. When it is applied as the interfacing circuit between PV arrays and power grid, the zero-sequence component injection method can be employed to balance the dc-link voltage whenever the irradiation and temperature between two PV arrays are different. In addition, this paper illustrates the overall control scheme of the proposed converter for grid-tied PV application and compares the efficiency performance. MATLAB simulations and experimental results verified the performance of the proposed converter.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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