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A Single-Stage Direct-Conversion AC-DC Converter for Inductively Powered Application

Qiong Wei Low, *Student Member, IEEE*, Mi Zhou, *Student Member, IEEE*, Liter Siek, *Member, IEEE*

***Abstract*—An innovative single-stage AC-DC converter for low power, low frequency skin depth wireless power transfer is presented. The power conversion efficiency of a wireless power receiver is limited by the cascaded two-stage design which constitutes a rectifier and a voltage regulator. Owing to the proposed ON-/OFF-mode regulating rectifier, the voltage rectification and regulation are achieved simultaneously in one-stage, thereby improving the power conversion efficiency substantially. The output voltage regulation is accomplished by incorporating the Pulse Skipping Modulation (PSM) and the Pulse Frequency Modulation (PFM) control into the structure. In addition, there is no bulky inductor utilized in the proposed one-stage design. Therefore, the footprint and cost of the receiver can be minimized effectively. The proposed design has been fabricated in 0.18µm standard CMOS process. Measurement results show that a peak power transfer efficiency of 93.48% is achieved at a regulated output voltage of 2V in an output power range of 2mW – 80mW.**

***Index Terms*—Single-stage AC-DC, ON-/OFF-mode controller, power conversion efficiency, inductively powered application**

I. Introduction

Wireless power transfer (WPT) technology is growing rapidly in recent years, which is largely motivated by extensive research work. It is attractive as the power can be transferred through the magnetic coupling between two coils without the usage of any power wires. Owing to the advantages offered by the WPT technology, it has become an appealing approach for the industrial application nowadays. The advancement of the technology has benefited a wide range of applications, such as for RFID smart card, animal tracking control, implantable medical devices (IMD), wireless charging for wearable and portable devices, [1-4]etc.

Fig. 1 shows a generic inductively coupled wireless power transfer system. Two magnetically coupled inductors L1 and L2 are used to transmit the power from the transmitter or reader to a receiver or tag. To maximize the power transfer efficiency between the coils, the resonant tanks at both transmitter and receiver sides are usually designed to resonate at the same frequency. The coupling between the coils induces an AC voltage at the secondary coil L2. The induced AC voltage is required to be converted to a DC voltage to power up the microchip in the receiver for useful operations. For a typical wireless power receiver, the power is usually transferred through two stages, in which a rectifier is used for an AC to DC conversion while a DC-DC converter in the form of switching regulator or LDO would regulate the DC output voltage [5-11]. Thus, the power efficiency of the receiver is mainly dominated by the efficiencies of both of the rectifier and the voltage regulator, which can be expressed as in (1).

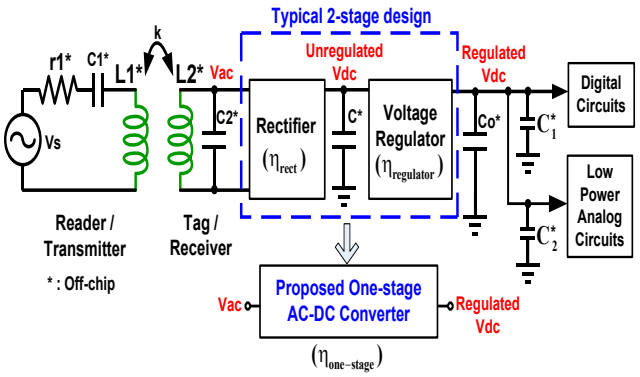

Fig. 1. Inductively coupled WPT system with the proposed one-stage AC-DC converter.

$$\eta_{receiver} \approx \eta_{rect} \times \eta_{regulator} \quad (1)$$

However, the power losses incurred from the cascaded two-stage design often restrict the overall power efficiency of the receiver. The high power losses generated from the cascaded two-stage blocks would cause the thermal emission of the device to increase, which may cause danger to the consumers in certain applications. Besides, greater power losses also imply that more power is required to be transmitted from the transmitter in order to cater for the receiver requirements. This is not desirable as in real life applications; the power transferred from the transmitter may be limited due to the orientation and the distance between the coils. Apart from the power losses issues, the footprint and size of the receiver are of main concern as well. The usual way of cascading an inductive DC-DC converter which utilizes an inductor is undesirable as it increases the footprint and cost of the receiver [5-7]. Even though an LDO is frequently used in [8-11] to regulate the rectified voltage with the aim of extending the power transmission range, but the power efficiency is degraded

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The authors are with VIRTUS lab, School of Electrical & Electronic Engineering, Nanyang Technological University, Singapore 639798. (Emails: qlow002@e.ntu.edu.sg, mzhou004@e.ntu.edu.sg, elsiek@ntu.edu.sg).

greatly due to the losses incurred from the LDO.

Hence, instead of having a two-stage design in the receiver, we propose a one-stage AC-DC converter with embedded regulation capability, which is an energy-efficient solution in a WPT system. The paper is organized as follow: Section II reviews the state-of-the-art work. Section III illustrates the concept and structure of the proposed one-stage AC-DC converter. Section IV describes the implementation of the key circuit blocks. Measurement results are shown in Section V and conclusions are made in Section VI.

II. Reviews on State-of-the-art Work

Various state-of-the-art works have been proposed with the objective of implementing the power conversion in a single-stage. The works in [12-13] achieve the voltage regulation by controlling the transmitter power. However, this would slow down the transient response of the receiver as the feedback has to go through the transmitter to adjust the power transferred in response to a load change in the receiver. The resonant regulating rectifier (3R) in [14] consists of five off-chip diodes and three off-chip capacitors which increase the footprint of the receiver. Moreover, the output voltage is regulated manually with the help of the resonant tanks on both sides. The pulse frequency modulation (PFM) control is used in tandem with the pulse width modulation (PWM) control scheme in [15]. The pulse frequency is increased or decreased based on the upper or lower threshold limit of the pulse-width regulated by the PWM control. However, the efficiency may be degraded due to the varying pulse-width especially when the pulse-width is at its minimum. In [16], a rectifying regulator with PWM and PFM control schemes is proposed. The PFM control utilized in [16] is discontinuous, that is a single short pulse is generated only when the output voltage falls below the reference voltage. By adaptively operating in resonant voltage or current mode (VM or CM) as in [17-18], high voltage conversion efficiency can be achieved in CM while high power conversion efficiency can be obtained in VM for a wide load range. In [19], a one-stage reconfigurable resonant regulating rectifier is used to widen the operation region by avoiding the variation in the system voltage conversion ratio. Besides, the 3-mode reconfigurable resonant regulating rectifier in [20] employs a 3-level configuration that is able to provide for higher power applications at 1 to 2A of output current.

III. Proposed One-stage AC-DC Converter

In this paper, we propose a one-stage AC-DC converter, utilizing a unique controller which consists of the Pulse Skipping Modulation (PSM) and the Pulse Frequency Modulation (PFM) control to produce a regulated output voltage. As compared to the PWM control, the proposed control scheme reduces the complexity of the design. Compared to the work in [15], the on-time of the proposed work is maximized whenever it is in the 'ON' mode in order to optimize the efficiency for the entire load range. Besides, with an adaptive clock, the proposed scheme operates by periodically checking on the loads instead of the discontinuous operation as in [16]. Hence, the regulating operation is more predictable. Moreover, a unique PFM algorithm is proposed in our work, aiming to reduce the switching power losses during light loads and to maximize the transient response during heavy loads. The proposed design retains an active rectifier structure, constituting four power transistors and two comparators. With the proposed ON-/OFF-mode controller, at least 81% of power efficiency is obtained in the range of 2mW-80mW of output power with a 2V output voltage. In addition, switching synchronization is accomplished smoothly without any calibration as in [14] and a good transient response is also observed during measurement. The output voltage has been tested at 1.8V and 2V respectively. The details of the proposed design are discussed in the subsequent sections.

A. Concept and Structure of the proposed design

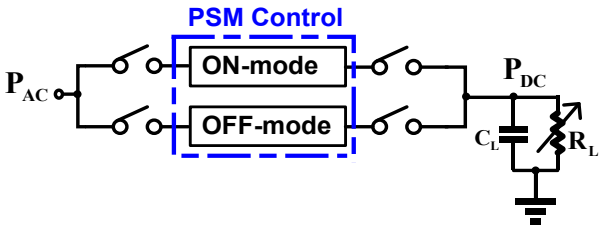

Fig. 2. Basic concept of the ON-/OFF-mode controller.

The basic idea of regulating an output voltage is to have two operations, which are the charging and the discharging operations. When the output load demands for more power, the converter must be able to provide the required output power and thus the occurrence of charging is increased. In contrast, when the system enters light-load conditions, in which lesser power is required by the load, the converter must be able to reduce the power transferred and hence the occurrence of discharging is increased.

Fig.2 illustrates the basic concept of the proposed ON-/OFF-mode controller. PSM control is incorporated in the design in order to cater for the charging and discharging operations. The one-stage converter works in either ON-mode or OFF-mode, in which ON-mode refers to the charging operation while OFF-mode refers to the discharging operation. During ON-mode, the converter works as a normal rectifier, transferring the input power to the output as usual. However, no power is transmitted to the output during OFF-mode and the output voltage is sustained by the charge in the output capacitor.

To gain a better insight of the ON-/OFF-mode operation, the implementation of ON-mode and OFF-mode is described in Fig. 3 (a) and (b). As shown in Fig. 3, the induced AC voltage is represented by the source V_{AC}, where V_{AC} = Vin+ - Vin-. The dc smoothing capacitor is represented by C_L and R_L denotes the load resistor. Fig. 3(a) shows the structure works as a full-wave rectifier in ON-mode operation. When the input node Vin+ is greater than the output voltage VDC, the power transistors MP2 and MN1 will be turned on to charge up the output. On the other hand, the power switches MP1 and MN2 will be turned on when the node Vin- is higher than the output voltage VDC. Fig. 3(b) illustrates the OFF-mode operation. In this mode, both of

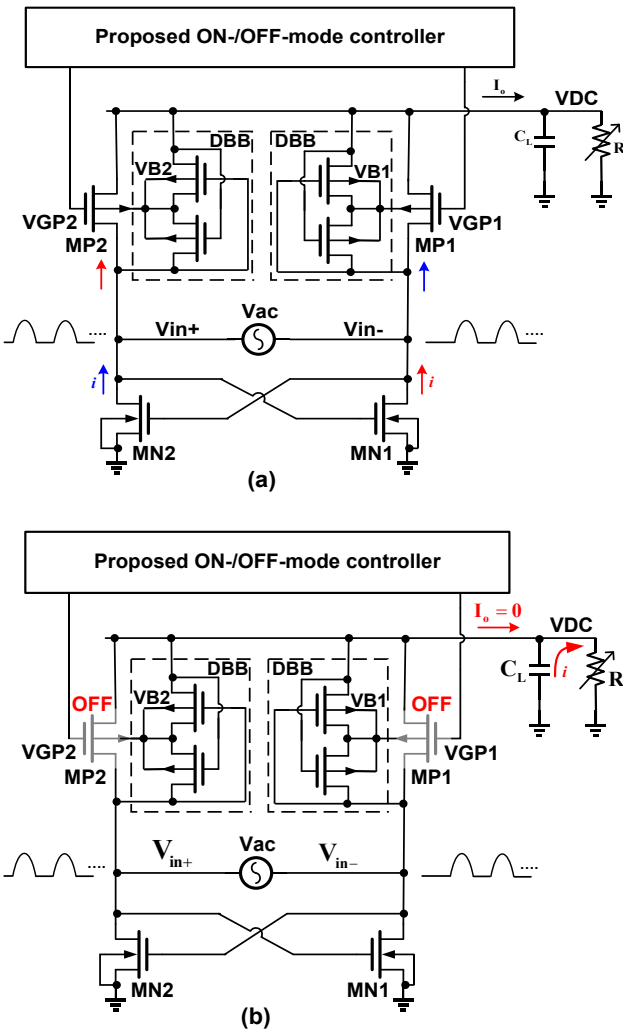

Fig. 3. (a) ON-mode operation and (b) OFF-mode operation of the proposed design.

the high-side switches MP1 and MP2 are turned off. Under this condition, one of the low-side switches (either MN1 or MN2) is turned on, depending on the input nodes Vin+ and Vin-. However, there is no electrical connecting path for the current to flow to the output, so the input current is almost zero. Hence, no power is being transferred to the output and the output capacitor is discharged to the load to maintain the output voltage. As the input node is varying all the time, a dynamic body bias (DBB) circuit is used to tie the body of the high-side power switches, MP1 and MP2 to the highest voltage and therefore to prevent latch-up [21].

The waveforms of the ON-/OFF-mode operation are illustrated in Fig. 4. The system clock is generated from the input voltages Vin+ and Vin-. Therefore, it is synchronized with the input frequency. A feedback comparator is enabled periodically to compare the output voltage with a reference voltage. If the output voltage is below the reference voltage, the converter will operate in ON-mode to charge up the output. In contrast, if the output voltage is detected to be above the reference voltage, the converter will work in OFF-mode to skip the power transmission. As can be seen from Fig. 4, during

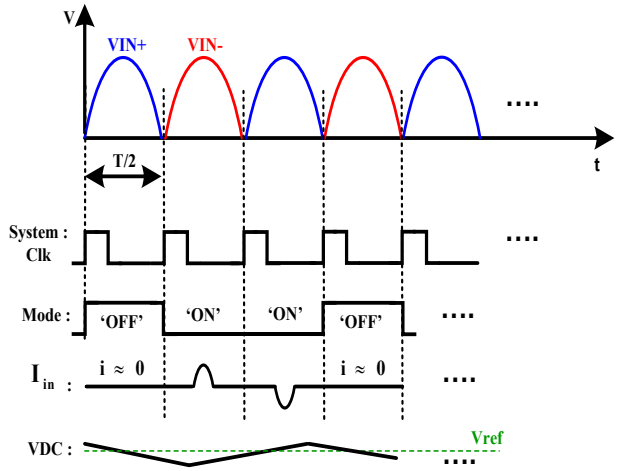

Fig. 4. Illustration of waveforms of the ON-/OFF-mode controller.

OFF-mode, the input current is almost zero, which means no power will be transferred to the output. Besides, the comparator is disabled after each comparison and it will only wake up at the next rising edge of the system clock. Consequently, the overall power consumption of the converter can be minimized. Hence, by utilizing the ON-/OFF-mode controller, the output voltage regulation is achieved over a wide load range with minimal power consumption.

B. PFM Control

To further enhance the performance of the one-stage converter, PFM control is incorporated in the design as well. The system clock frequency can be reduced in order to decrease the switching power losses under light-load conditions. By reducing the system clock frequency, the frequency of turning on the comparator is reduced as well and thus the overall quiescent power can be minimized under light-load conditions.

In order to ensure that the mode transition occurs only at the zero-crossing instant of the input current, the switching frequency is required to be synchronized with the input frequency. Hence, the switching frequency is designed to be in multiple of the input frequency f_{in}. There are two frequencies $2f_{in}$ and f_{in} available to be selected for the system. The selection of the system clock frequency is done based on the load conditions and the PFM algorithm as shown in the Fig. 5. The PFM algorithm is designed such that the transient response of the converter is maximized while at the same time the power consumed is minimized during light-load conditions. When heavy-load condition is detected, the frequency is increased in order to speed up the transient response. On the contrary, when light-load condition is detected, the frequency is decreased to reduce the switching power losses.

As shown in the Fig. 5, if the output voltage is detected to be below the reference voltage for at least once, the system clock frequency will be increased by two times. In contrast, if the output voltage is detected to be above the reference voltage thrice consecutively, indicating that the system enters light-load condition and thus the system clock frequency will

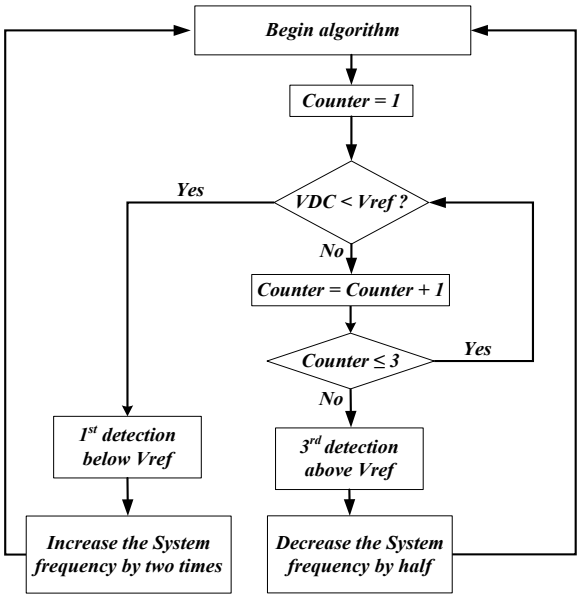

Fig. 5. Flow chart of the proposed PFM algorithm.

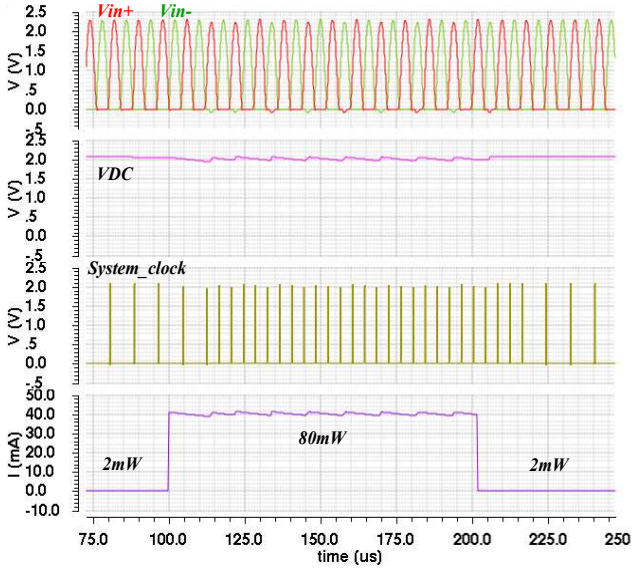

Fig. 6. Simulated waveforms of the converter operating in PFM mode.

be reduced by half.

Fig.6 shows the simulated waveform of the PFM control. As can be observed, the system clock frequency is changing from f_{in} to $2f_{in}$ during the increment of output power from 2mW to 80mW. On the contrary, the system clock frequency is reduced from $2f_{in}$ to f_{in} when the output power is stepped down from 80mW to 2mW.

C. Power Losses and Efficiency

Fig. 7 shows the ON and OFF-mode configurations and their respective input waveforms. For ON-mode configuration as shown in Fig. 7(a), the structure works as a normal rectifier by turning on one high-side and one low-side power switches for each conducting cycle. For example, when VIN+ is greater than VIN-, MN1 is turned on and the node VIN- is limited to

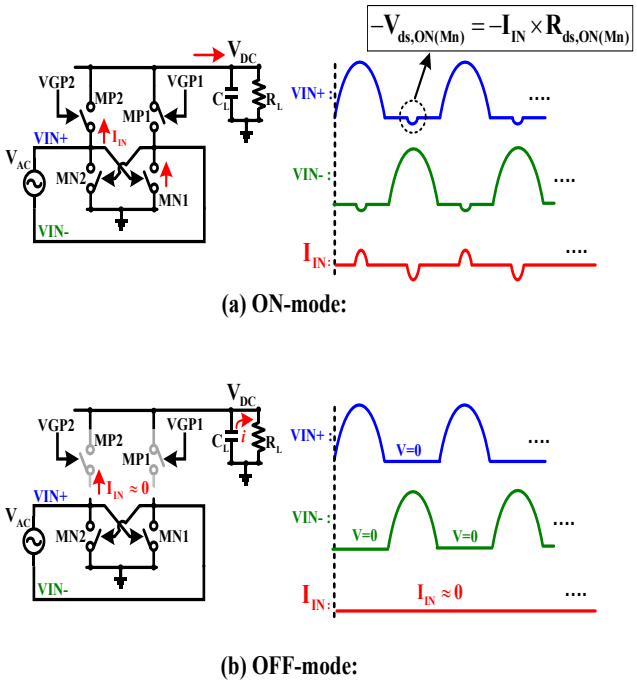

Fig. 7. The configurations and input waveforms of (a) ON-mode and (b) OFF-mode.

$-V_{ds(ON)}$, which is the drain to source voltage drop of MN1. The current flows through MN1 and MP2 to charge up the output. Under this mode, the power losses are the conduction loss and switching loss of both conducting switches (MP2 and MN1) and the leakage power losses which include the reverse current conduction loss and the leakage power loss of the transistors. The total power losses for the ON-mode can be expressed as in (2).

$$P_{losses\,(ON-mode)} = P_{conduction\ loss\,(Mp\&Mn)} + P_{switching\ loss\,(Mp\&Mn)} + P_{leakage} \quad (2)$$

For OFF-mode configuration as shown in Fig. 7(b), the output is isolated from the input source by turning off both high-side power switches. There is no electrical connecting path for the power to flow from the input source to the output. Therefore, the input current is almost zero and the output voltage is sustained by the output charge of the output capacitor C_L. Under this mode, the gates of the low-side switches (MN1 and MN2) are still connected to the input source and hence a small power is used to charge up the gate of any of the switches. For example, when VIN+ is higher than the threshold voltage of MN1, MN1 is turned on and the node VIN- is clamped to ground. On the other hand, when VIN- is greater than the threshold voltage of MN2, MN2 will be turned on and the node VIN+ will be clamped to ground. Hence, the power losses during OFF-mode are the switching power loss of MN1 or MN2 and the leakage power losses which can be expressed as in (3).

$$P_{losses\,(OFF-mode)} = P_{switching\ loss\,(Mn)} + P_{leakage} \quad (3)$$

The total efficiency of the ON-/OFF-mode converter can be expressed as in (4), where P_{Load} is the output power, P_{con} represents the conduction power losses, P_{sw} denotes the total switching power losses, $P_{controller}$ is the power consumption of the controller which includes the active diode comparators and all the control blocks and P_{leak} represents the total leakage power losses. For ideal case, the leakage power losses can be excluded from the expression.

$$\eta_{ON-/OFF-mode} = \frac{P_{Load}}{P_{Load} + P_{con} * (n \cdot T) + P_{sw} + P_{controller} + P_{leak}}, n \geq \frac{1}{2} \quad (4)$$

D. Mathematical Analysis of One-stage Converter

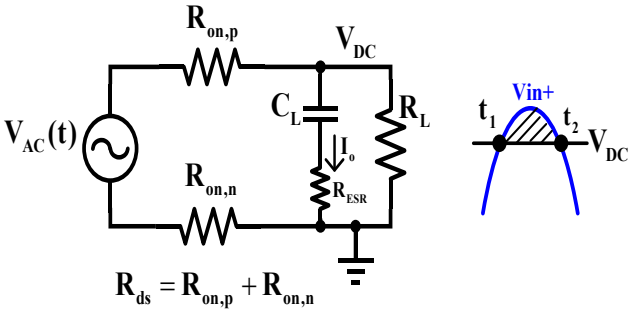

Fig. 8. The equivalent circuit model and the associated half-time period waveform of the converter.

In this section, we develop an analytical model for the ON-/OFF-mode controller of the one-stage converter.

During each conduction cycle, one PMOS switch and one NMOS switch will be turned on and their equivalent on-resistance can be modeled as in Fig. 8. The $V_{AC}(t)$ denotes the AC power source and the total on-resistances of both switches can be simplified as R_{ds}. The smoothing dc capacitor and the output load are represented by C_L and R_L respectively.

The criteria for the converter to function normally is that the input amplitude has to be greater than the voltage drop across the on-resistance of both of the high-side and low-side power switches, as expressed in (5).

$$|V_{AC}| > V_{ds(p)} + V_{ds(n)} \quad (5)$$

Assumed that the positive and negative half cycles are symmetrical and the converter conducts a maximum duration of (t_2-t_1) during each conduction cycle, as illustrated in Fig. 8. During steady-state, the total input charge supplied by the input AC source and the total output charge delivered to the output can be derived as in (6) and (7) respectively.

$$Q_{in} = \int_{t_1}^{t_2} \frac{V_{AC}\, sin\frac{4\pi}{m \cdot T}\, t - V_{DC}}{R_{ds}}\, dt, \qquad m \geq 1 \quad (6)$$

$$Q_{out} = \int_0^{n\cdot\frac{T}{2}} \frac{V_{DC}}{R_L}\, dt = \frac{V_{DC}}{R_L}\left(n \cdot \frac{T}{2}\right), \qquad n \geq 1 \quad (7)$$

By applying the principle of conservation of charge, the output voltage can be expressed in (8) by equating the total input and output charge, where $m \cdot T$ is the rate of charging and $n \cdot \frac{T}{2}$ is the rate of discharging.

$$V_{DC} = \frac{\frac{V_{AC} \cdot m \cdot T}{4\pi}\left(\cos\frac{4\pi}{m \cdot T}t_1 - \cos\frac{4\pi}{m \cdot T}t_2\right)}{(t_2 - t_1) + \frac{R_{ds}}{R_L} \cdot n \cdot \frac{T}{2}}; m,n \geq 1 \quad (8)$$

From the equation (8), it can be inferred that under light-load conditions when R_L increases to conduct lesser load current, the output voltage V_{DC} is maintained by increasing the rate of discharging or reducing the rate of charging. In contrast, during heavy-load condition, the output voltage is regulated by increasing the charging rate or reducing the discharging rate. Hence, by modulating the conduction rate of the converter, the output voltage regulation is accomplished over a wide load range.

E. Output Voltage Ripples

Under steady-state, the voltage drop due to the ESR of the output capacitor C_L and the discharging of C_L into the load R_L contribute to the output voltage ripples. Hence, the output voltage ripples can be approximated as in the equation (9).

$$\Delta V_{ripples} \approx I_o.R_{ESR} + V_{DC} \cdot \left(1 - e^{\frac{-n\cdot T}{R_L \cdot C_L}}\right) \quad (9)$$

As can be inferred from the equation (9), the output voltage ripples can be reduced by increasing the output capacitor value or the operating frequency.

F. Self-startup Mechanism

The proposed structure possesses self-startup ability. During startup, a reset pulse is used to trigger the mode selection to ON-mode, enabling the converter to work as a full-wave rectifier. The parasitic capacitances of the high-side power switch MP2 can be modeled as in the Fig. 9.

During startup, the output voltage VDC is zero and therefore the gate-source voltage V_{sg2} can be approximated as in the Fig. 9, which is a capacitive ratio of the input voltage Vin+. Initially, as MP2 is in the cut-off region, the parasitic capacitances C_{gd} and C_{gs} are almost of the same value and thus the voltage V_{sg2} is roughly half of the voltage Vin+. As Vin+ increases gradually, the voltage V_{sg2} increases as well. Eventually it will exceed the threshold voltage of the transistor MP2 and MP2 will be turned on, acting as a passive diode to slowly charge up the output capacitor. The same applies to the negative cycles as well, the transistor MP1 will act as a passive

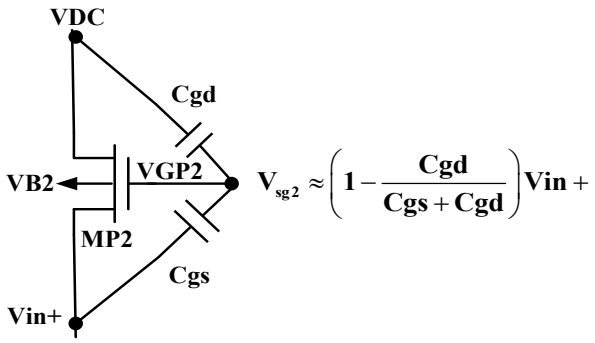

Fig. 9. Parasitic capacitances of power transistor MP2.

diode and the current will flow through the transistors MP1 and MN2 to slowly charge up the output capacitor. After several cycles, the output voltage will reach the minimum supply of the control blocks and thus the structure will start to work in the ON-/OFF-mode operation as described earlier. The simulated waveform during startup is shown in Fig. 10.

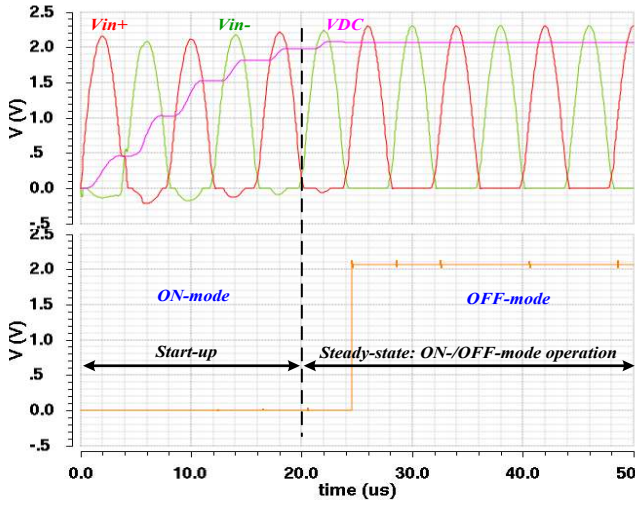

Fig. 10. Simulated waveforms during startup.

IV. Implementation of Key Circuit Blocks

A. Wireless Power Receiver with the proposed Single-stage AC-DC Converter

Fig. 11 shows the block diagram of the wireless power receiver with the proposed single-stage AC-DC converter. It consists of the ON-/OFF-mode reconfigurable topology as the power stage and the controller. The ON-/OFF-mode controller determines the operation modes of the reconfigurable topology based on the load requirements to achieve voltage regulation. In addition, the PFM control is utilized to select the switching frequency of the system in order to maximize the transient response during heavy-load and to minimize the switching power losses during light-load. To cater for different reference voltage values, a non-inverting gain amplifier can be used to tune the reference voltage by manipulating the value of the

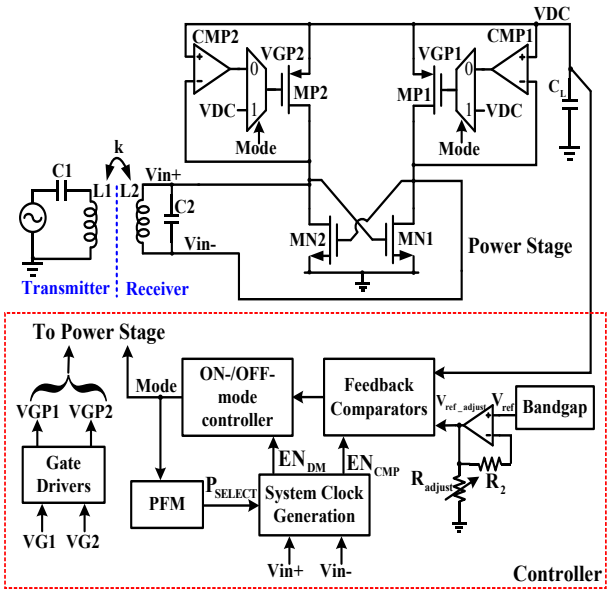

Fig. 11. Block diagram of the wireless power receiver with the proposed single-stage AC-DC converter.

feedback resistor, R_{adjust}. The equation of the tuning is as shown in (10).

$$V_{ref\_adjust} = \left(1 + \frac{R_2}{R_{adjust}}\right) V_{ref} \quad (10)$$

B. Proposed Controller

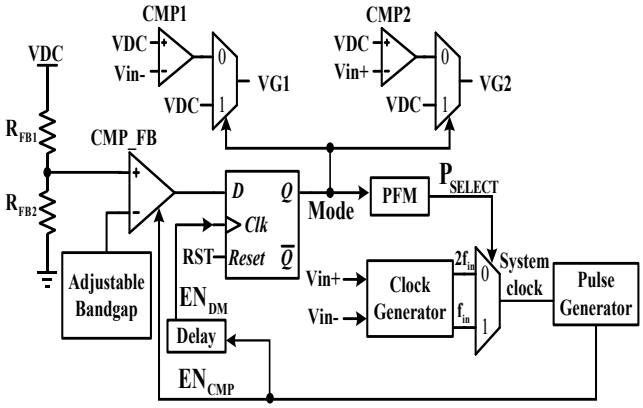

Fig. 12. Implementation of the controller.

The implementation of the controller is illustrated in Fig. 12. A feedback comparator, CMP_FB is utilized to compare a fraction of the output voltage VDC with a reference voltage. The comparison result is stored in a flip-flop which is updated according to the system clock. The system clock will first activate the comparator circuit and after a certain delay only activate the flip-flop. This is to ensure that the correct comparison result is stored as the comparator circuit takes some time to stabilize after the activation. The input voltage, Vin+ and Vin- are used to generate two clocks of different frequencies. The selection of the system clock frequency is

done based on a PFM algorithm as discussed in the Section III. There are two frequencies, which are 250 kHz and 125 kHz available for the selection, depending on the load conditions. The signal 'Mode' is used to determine the mode operation, which is either ON-mode or OFF-mode. The active diodes, MP1 and MP2 of the converter utilizes an unbalanced biasing comparator, CMP1 and CMP2 as in [22], which has been designed to minimize the circuit delay in order to avoid any reverse current from flowing.

V. Measurement Results

The proposed one-stage AC-DC converter was fabricated in a standard 0.18µm CMOS process using 5.5V devices. The chip micrograph photo of the size 1.5 mm × 1.2 mm is as shown in Fig. 13. The total active area is 0.4246 mm^2, in which the power transistors occupy an area of 0.2964 mm^2 and the controller takes up an area of 0.1282 mm^2. The design has been tested at the ISM band of 125 kHz. Fig. 14 shows the transmitter and the receiver boards of the inductively powered system. A power amplifier is used to drive the primary side and the secondary side provides the input to the chip through inductive coupling. The coils of 4.3cm diameter are used for the power transmission. In order to weigh the trade-offs between the voltage ripples and the capacitor value, an off-chip dc filtering capacitor of 4.7µF is used to store the output charge. For safety purpose, zener diodes are connected externally at the input to prevent the voltage from going higher than the breakdown voltage of the 5.5V devices.

As illustrated in Fig. 14, a sense resistor, Rsense is inserted into the input path to measure the input AC current, I_{AC}. The input AC power is obtained by taking the average of the product of the input voltage and the input current over several period cycles. The power conversion efficiency (PCE) of an AC-DC converter can be calculated from the equation in (11).

$$\eta_{AC-DC} = \frac{P_{DC}}{P_{AC}} = \frac{\frac{V_{DC}^2}{R_L}}{\frac{1}{nT}\int_{t_0}^{t_0+nT} V_{AC}(t) * I_{AC}(t)dt} \quad (11)$$

Fig. 15 shows the measured steady-state waveforms of input voltage, input current, output voltage and system clock at 5mA load current. The input voltage V_{AC} denotes (Vin+ - Vin-). As can be observed, the input current is almost zero when no power transfer is required. In order to synchronize with the input frequency, the system clock frequency changes between 125 kHz (f_{in}) and 250 kHz ($2\times f_{in}$) according to the proposed PFM algorithm. Under the conditions that no power transfer is required, the system clock frequency changes to the minimum frequency, as shown in Fig. 15 in order to reduce the switching power losses and enhance the power efficiency. To verify the modulation scheme, the converter has been tested at different load currents, such as 1mA, 5mA, 10mA and 40mA as shown from Fig. 16 to 19. The input voltage, output voltage and the signal 'Mode' waveforms at different load conditions are shown from Fig. 16 to Fig. 19. The signal 'Mode' in the figures

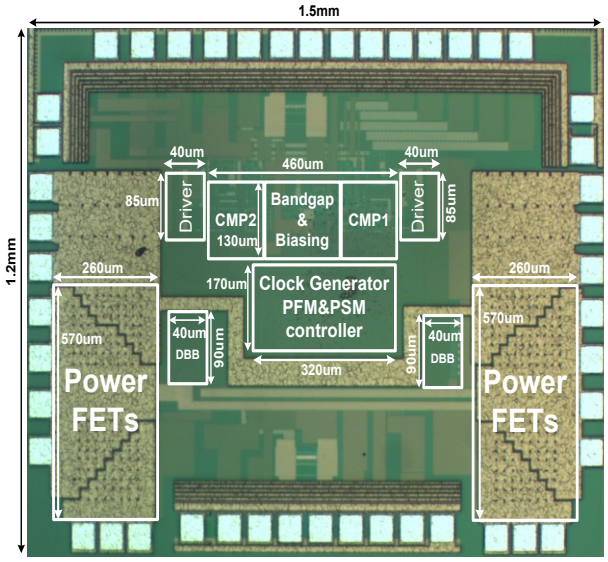

Fig. 13. Chip micrograph photo of the proposed design.

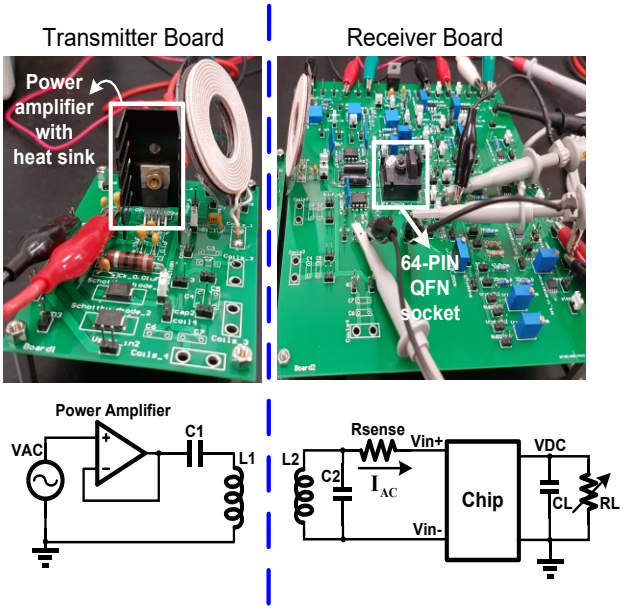

Fig. 14. The test boards for the proposed design.

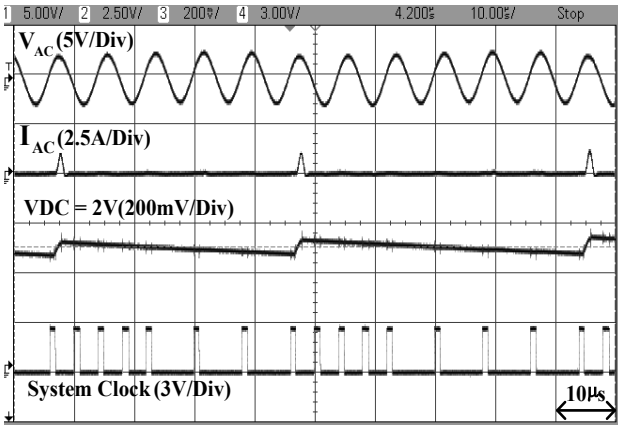

Fig. 15 The measured steady-state waveforms of input voltage, input current, output voltage and system clock.

represents the modulation of the conduction rate of the converter. As discussed earlier, ON-mode denotes the charging operation while OFF-mode represents the discharging operation. The frequency of the mode transition is synchronized with the system clock frequency, which is at the moment when the input current is zero to avoid any power losses. The output voltage and the 'Mode' signal are compared among four different load current scenarios. In the waveforms, ON-mode is indicated by logic '0' while OFF-mode is represented by logic '1'. As can be seen from Fig. 16, OFF-mode is performed more often when the load current is 1mA, implying that the discharging operation is executed more frequently under this light-load condition. However, as the load current increases gradually from 1mA to 40mA as shown from Fig. 16 to Fig. 19, ON-mode operation is executed more frequently, indicating that more power is required to be transferred to the output in order to cater for the increasing load requirements. Hence, by regulating the charging or discharging rate of the converter, the output voltage regulation is achieved successfully.

To further investigate the regulation capability of the proposed one-stage converter, the output load current is stepped from 1mA to 40mA. The regulator is able to track the reference voltage despite a load-step of 40 times is applied to it. Fig. 20(a) shows a voltage undershoot of 200mV during the load-step from 1mA to 40mA while Fig. 20(b) shows a voltage overshoot of 180mV during a load-step from 40mA to 1mA. The regulator takes 68µs to recover from the voltage undershoot and it takes 290µs to recover from the voltage overshoot.

Fig. 21 shows the graph of measured power conversion efficiency (PCE) against the output power. By adjusting the bandgap reference voltage, the output voltage is tested at 1.8V and 2V respectively. When the output voltage is changed from 2V to 1.8V due to the adjustment of reference voltage, the power efficiency degrades. With a lower output voltage, the on-resistance of the power transistor is higher as the gate voltage driving the transistor is lower. Hence, the power losses are higher, causing the efficiency to be lower. Measurement results show that a peak power efficiency of 93.48% is achieved at the output voltage of 2V in an output power range of 2mW-80mW. The maximum output voltage ripples is measured to be around 140mV.

Table I summarizes the performance of the proposed receiver. The line and load regulation are measured to be 60mV/V and 2.56mV/mA respectively. Table II shows the comparison between the proposed work and the relevant state-of-the-art-works. There are different active rectifier designs done at different operating frequency to cater for different load power applications. The proposed design is compared to the reference works that have the nearest possible frequency or output power range. The work in [23] is designed for piezoelectric application, [26-27] are designed for biomedical implantation and [11] and [20] are used for wireless charging for portable devices. The proposed design is suitable for the applications that are working in the ISM band of 125 kHz to 134 kHz, such as for animal tracking control to track the temperature or pressure of the animals.

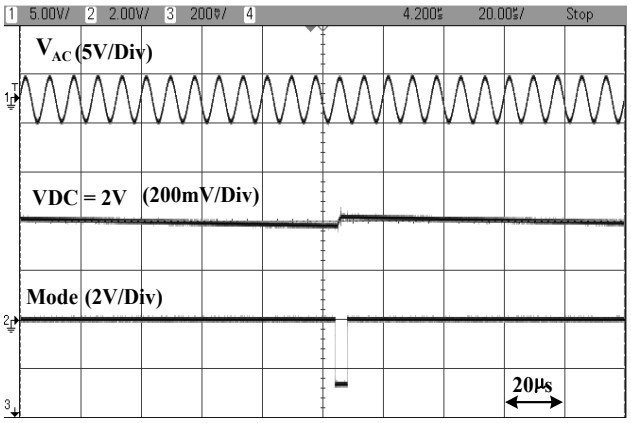

Fig. 16 Measured steady-state waveforms at 1mA.

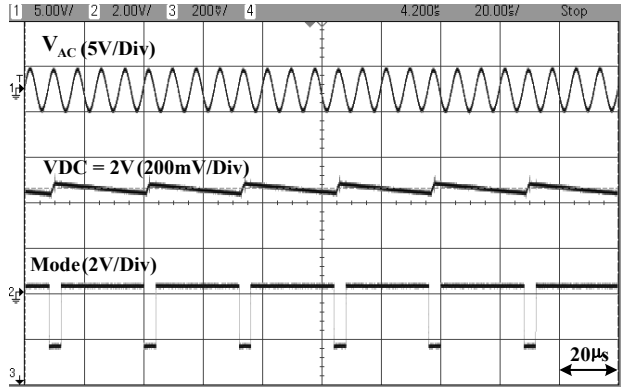

Fig. 17 Measured steady-state waveforms at 5mA.

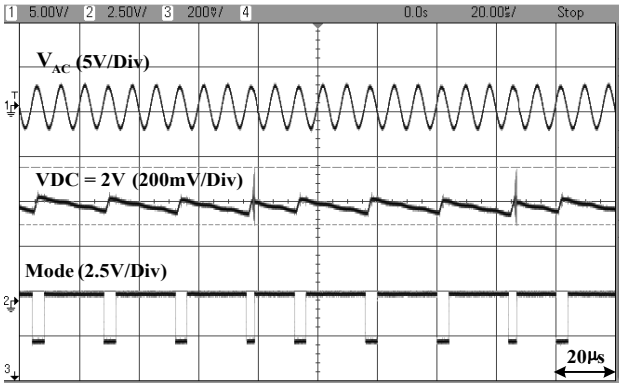

Fig. 18 Measured steady-state waveforms at 10mA.

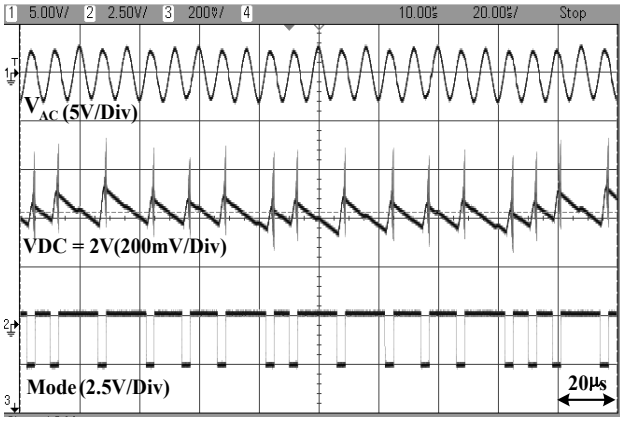

Fig. 19 Measured steady-state waveforms at 40mA.

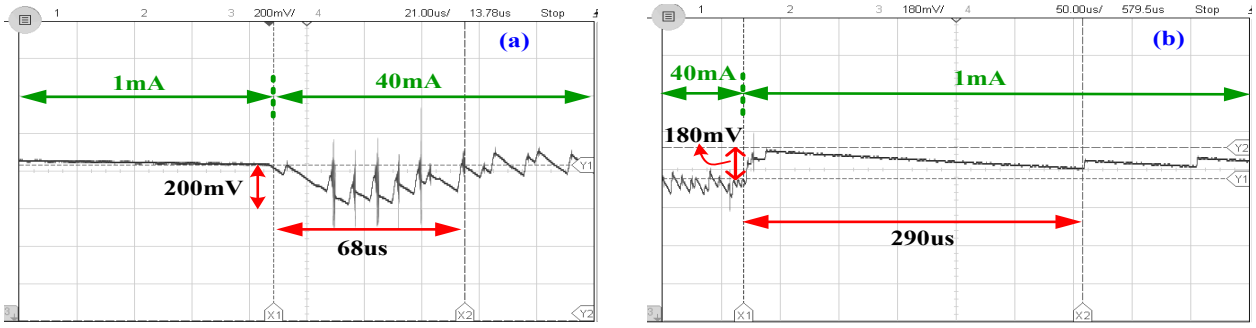

Fig. 20. Measured load transient-response of the proposed converter with load-step of (a) 1mA-40mA, (b) 40mA-1mA.

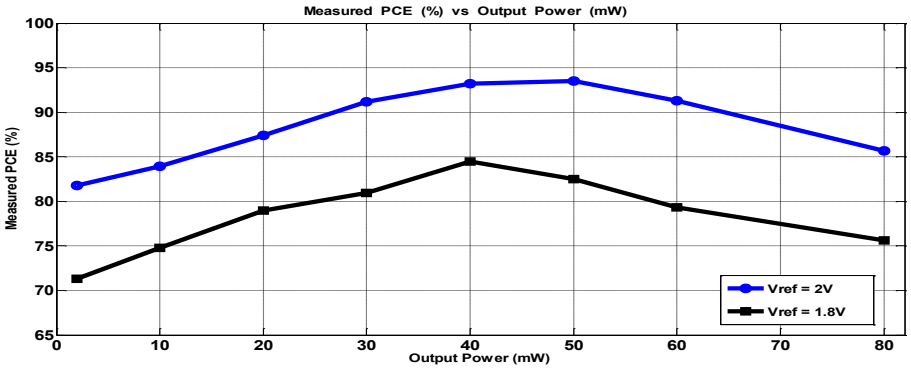

Fig. 21. Measured power conversion efficiency (PCE) versus output power at 2V and 1.8V output voltage.

TABLE I PERFORMANCE SUMMARY

Transmitter and Receiver Coil	24μH/0.1Ω @ 125 kHz
Distance between Transmitter/Receiver	0.5 cm
Output Capacitor C_L	4.7 μH
Active area	0.425 mm^2
Load regulation ($\Delta V_{DC}/\Delta I_{LOAD}$)	2.56 mV/mA
Line regulation ($\Delta V_{DC}/\Delta V_{IN}$)	60 mV/V
Max. link efficiency (Π_{LINK})	11.2%
Max. receiver efficiency ($\Pi_{RECEIVER}$)	93.48%
Total efficiency ($\Pi_{TOTAL}=\Pi_{LINK}\times\Pi_{RECEIVER}$)	10.47%

TABLE II PERORMANCE COMPARISON WITH OTHER ST ATE-OF-THE-ART WORK

References	TBCAS 2008 [25]	JSSC 2009 [24]	ISSCC 2010 [26]	TPEL 2011 [23]	JSSC 2013 [27]	ISSCC 2013 [10]	JSSC 2015 [11]	JSSC 2015 [3]	JSSC 2017 [20]	JSSC 2017 [18]	Proposed Work
Technology	0.5 μm CMOS	0.35 μm CMOS	0.18 μm CMOS	Discrete	0.5 μm CMOS	0.35 μm CMOS	0.35 μm CMOS	0.35 μm CMOS	0.35 μm CMOS	0.35 μm CMOS	0.18 μm CMOS
Structure	Active rectifier	Active rectifier	Timing AC-DC	Active voltage doubler	Adaptive output active rectifier	1X/2X Active rectifier	Rectifier + LDO	R^3 rectifier	3-mode R^3 rectifier	VM-CM rectifier	One-stage AC-DC Converter
Regulation Capability	No	No	Yes	No	Yes	No	Yes	Yes	Yes	Yes	Yes
Chip Area (mm^2)	*0.4	1.03	*0.1	N.A	**2.25	*0.11	4.8	3.06	4.77	1.56	1.8
Frequency	125kHz –1MHz	200kHz –1.5MHz	200kHz –3.3MHz	20Hz	2MHz	13.56 MHz	2MHz	13.56 MHz	6.78MHz	1MHz	125kHz –250kHz
Output Voltage (V)	4.36	1.13-2.28	1.8	2.24	2.5 - 4.6	1.27 - 4	4.5	3.6	5	3.2	1.8-2.0V
Max. P_{OUT}	150mW	42mW	10mW	10mW	~ 13mW	32mW	1.45W	102mW	6W	20mW	80mW
Measured Peak PCE (%)	84.8	87	87.1	83	87	84.2	76	92.6	92.2	77	93.48

*Active area. **Including stimulating system.

The work in [23-25] utilizes a typical active rectifier structure that does not possess regulation capability. In order to regulate the rectified voltage, a LDO is used as in [11] and a buck converter is used in [5-7]. However, due to the two-stage design, the power efficiency is degraded. Even though the work in [26] eliminates the use of an inductor, but the input voltage is rectified before supplying the two converter cores in the design. Thus, the power is still being transferred through two stages.

In order to have an at least 90% of power efficiency for a two-stage design, each stage of the design needs to achieve at least a 95% of power efficiency which is a great challenge. The proposed work has adopted an energy-efficient one-stage design, achieving a peak power efficiency of 93.48% at a regulated output voltage of 2V. In spite of the simplicity of the structure, the proposed design achieves the best power efficiency compared to the other state-of-the-art-works as shown in the Table II. In addition, it possesses a good regulation capability while having a minimal footprint in the receiver.

VI. Conclusion

This paper presents a one-stage AC-DC converter for inductively powered applications, such as in RFID and IMD. The proposed converter has improved the power conversion efficiency from a typical two-stage design to a one-stage design. In addition, it minimizes the cost and footprint of the receiver by omitting the use of an inductor from the design. The unique modulation scheme implemented has successfully regulated the output voltage across a wide load range. Owing to the energy-efficiency modulation technique, a peak power efficiency of 93.48% is achieved in an output power range of 2mW-80mW. The proposed work is suitable for the applications that require minimal footprint while operating in the range of mW power at the ISM band of 125 kHz to 134 kHz, such as for implantable animal tag or biomedical implantation.

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Qiong Wei Low (S'13) received the B. Eng. (Hons.) degree from Nanyang Technological University, Singapore, in 2012, where she is currently working towards the Ph.D. degree in the School of Electrical and Electronic engineering.

Her research interests include mixed-signal/analog integrated circuits design, switching-mode dc-dc converter design, and power management integrated circuits design for wireless power transfer system.

Mi Zhou (S'15) received the B. Eng. (Hons.) degree from Nanyang Technological University, Singapore, in 2014, where she is currently working towards the Ph.D. degree. Her research interests include switching-mode dc-dc converter modeling and design, as well as low power analog IC design.

Liter Siek (M'90) received the B.A.Sc. degree from University of Ottawa, Ottawa, ON, Canada, the M.Eng.Sc. from the University of New South Wales, NSW, Australia, and the Ph.D. degree from Nanyang Technological University (NTU), Singapore.

From 1981 to 1983, he was with a couple of companies in the area of automation and control. From 1983 to 1985, he was an IC Design Engineer with a European semiconductor powerhouse, SGS (now known as ST Microelectronics), situated in Milan, Italy, where he was involved in the central Research and Development Laboratories for Linear IC, designing ICs for cordless telephone and motor regulator. From 1985 to 1987, he was with the same company situated at Singapore's Asia Pacific Design Centre, where he was involved in IC design for monolithic power ICs in bipolar technology. Since 1987, he has been with the School of Electrical and Electronic Engineering at NTU, where he is currently an Associate Professor and the Lead for the Joint NTU-TUM PhD Program. His current research interests include Analog/Mixed Signal ICs especially in the areas of low-voltage low-power circuits, power management ICs, phase-locked loops, and data converters.

Dr. Siek has received numerous Teaching Excellence Awards as well as the Nanyang Award for Excellence in Teaching. He was the Director of VIRTUS - IC Design Centre of Excellence from 2012 to 2015 as well as the Director of the Joint NTU-TUM MSc (IC Design) Program from August 2007 to July 2015. In addition, he has conducted numerous Analog/Mixed Signal IC design short courses as well as providing technical consultancy for the industry. He is actively involved in the IEEE SSCS Singapore Chapter.