A Single-Trim CMOS Bandgap Reference With a 3σ Inaccuracy of $\pm 0.15\%$ From -40°C to 125°C

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***Abstract*—A CMOS bandgap reference with an inaccuracy of $\pm 0.15\%$ (3σ) from -40°C to 125°C is presented. In contrast to prior art, it requires only a single trim to achieve this level of precision. A detailed analysis of the various error sources is provided, and techniques to reduce them are discussed. The prototype bandgap reference draws 55 μA from a 1.8 V supply, and occupies 0.12 mm^2 in a 0.16 μm CMOS process. Experimental results from two runs show that, with the use of chopping and higher-order curvature correction to remove non-PTAT errors, the residual error of a bandgap reference is mainly PTAT, and can be removed by a single room temperature trim.**

***Index Terms*—Chopping, CMOS bandgap reference, curvature correction, room temperature trim.**

I. Introduction

PRECISION bandgap voltage references have been widely used in mixed-signal integrated circuits (ICs). In such a reference, low temperature drift is obtained by adding a proportional-to-absolute-temperature (PTAT) voltage to the base emitter voltage of a bipolar junction transistor (BJT) [1]. However, due to process variations, both the room-temperature bandgap voltage and its temperature coefficient will deviate significantly from their nominal values. In a standard CMOS process, the resulting variation of the reference voltage could be a few percent over temperature [2], [3].

To compensate for process variations, trimming is normally used [2], [3]. In CMOS bandgap references, an operational amplifier (opamp) is used to generate the PTAT voltage. Although the spread of a BJT's base emitter voltage is mainly PTAT, the temperature drift of the offset of a CMOS opamp will usually be non-PTAT. Therefore, a single room temperature trim will be unable to compensate for both these sources of process variations, leading to a bandgap voltage with significant residual temperature drift. To achieve higher precision, multiple temperature trimming has been used [2], [3], but this inevitably increases the production cost.

To achieve high precision with a single room temperature trim, it is necessary to reduce the non-PTAT opamp offset. Low offset can be expected by using BJTs in the input differential pair of the opamp, but this is not always possible in a standard CMOS process. Another possible solution, which utilizes very large MOSFET differential pairs, requires too much chip area. To reduce the offset of CMOS opamps in an area efficient way, dynamic offset cancellation techniques have been used in bandgap references [4]–[6]. In [4], the auto-zeroing technique is used to reduce opamp offset. However, due to the two-phase operation of auto-zeroing, the output voltage is not continuous, and the noise aliasing associated with the sampling leads to increased low frequency noise. In order to obtain a low-noise continuously available bandgap voltage, the chopping technique has also been used in CMOS bandgap references [5], [6]. However, the up-modulated offset generated by chopping results in high frequency ripple at the opamp's output. Reducing this ripple to the noise level typically requires the use of large external capacitors.

In this paper, a CMOS bandgap reference is presented that only requires a single room temperature trim to achieve a 3σ inaccuracy of $\pm 0.15\%$ from -40°C to 125°C [7]. With the use of chopping to cancel the opamp offset and curvature correction to reduce the temperature dependency of the base emitter voltage, the residual errors are mainly PTAT and can be removed by a room temperature trim. The ripple, which would otherwise appear at the bandgap output as a result of chopping, is effectively removed by an on-chip switched-capacitor notch filter.

This paper is organized as follows. Section II presents an error source analysis of CMOS bandgap references, which is then numerically illustrated. Section III describes the circuit techniques used to mitigate these error sources. Experimental results are presented in Section IV, and the paper ends with conclusions.

II. Error Sources in CMOS Bandgap Reference

A typical CMOS bandgap reference is shown in Fig. 1 [1]. The bandgap voltage V_{BG} is given by

$$V_{BG} = V_{BE1} + \alpha \cdot \Delta V_{BE} = V_{BE1} + \frac{R_1}{R_2} V_T \ln N \quad (1)$$

where V_{BE} is the BJT's base emitter voltage, $\alpha = R_1/R_2$ is the resistor ratio between R_1 and R_2, $\Delta V_{BE} = V_T \ln N$ is the base-emitter voltage difference of Q_1 and Q_2, and N is their emitter area ratio. Error sources that degrade the precision of the bandgap reference mainly include the process variation of V_{BE1}, $\alpha \Delta V_{BE}$, the opamp offset, and the nonlinear temperature dependence of V_{BE}. The first two error sources are mainly PTAT, while the last two are non-PTAT. In this section, the influence of these error sources on the precision of bandgap references will be analyzed.

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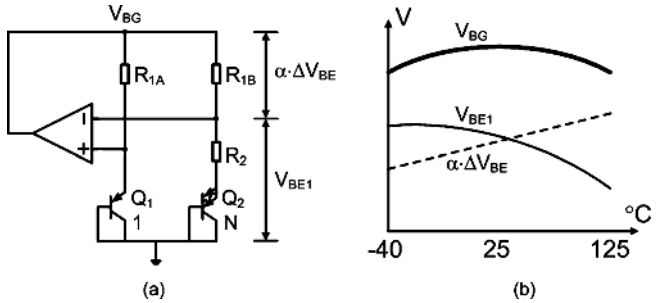

Fig. 1. Typical bandgap reference in CMOS technology.

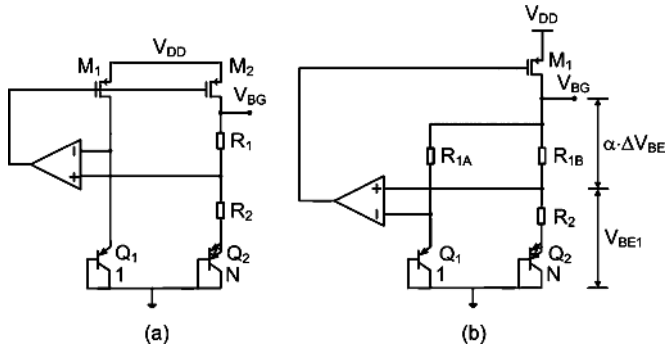

Fig. 2. Determination of the collector current ratio.

A. Process Variations of V_{BE}

In CMOS technology, a bandgap reference can be designed with substrate PNP BJTs [2], [3]. The base-emitter voltage V_{BE} of a BJT is largely determined by its saturation current I_S and its collector current I_C. If I_S deviates from its nominal value, V_{BE} can be written as

$$V_{BE} = V_T \ln \frac{I_C}{I_S + \Delta I_S} \approx V_{BE}|_{\Delta I_S = 0} - V_T \frac{\Delta I_S}{I_S} \tag{2}$$

where ΔI_S represents the deviation of I_S. Since the ΔI_S is mainly introduced by spread of the base doping and spread of the transistor dimension, it can be assumed that $\Delta I_S / I_S$ is mainly temperature independent, which indicates that the spread of V_{BE} as a result of the saturation current spread is PTAT and can be removed by a single PTAT trim.

The resistance variations of R_1 and R_2 can change V_{BE} by altering I_C. By defining the resistance spread as a fractional deviation δ_R, V_{BE} can be reorganized as

$$V_{BE} = V_T \ln \frac{\frac{I_C}{(1+\delta_R)}}{I_S} \approx V_{BE}|_{\delta_R = 0} - V_T \delta_R. \tag{3}$$

Assuming δ_R is temperature independent, (3) indicates that the resulting spread of V_{BE} is also PTAT.

The limited BJT current gain β_F also can affect the precision of V_{BE}, because, while V_{BE} is determined by the collector current I_C, the PTAT current is actually fed to the BJT through the emitter in a bandgap reference [8], [9]. If β_F deviates from its nominal value, V_{BE} can be written as

$$\begin{aligned} V_{BE} &= V_T \ln \left(\frac{I_E}{I_S} \cdot \frac{\beta_F + \Delta\beta_F}{1 + \beta_F + \Delta\beta_F} \right) \\ &\approx V_{BE}|_{\Delta\beta_F = 0} + V_T \cdot \frac{1}{1+\beta_F} \cdot \frac{\Delta\beta_F}{\beta_F} \end{aligned} \tag{4}$$

where I_E is the emitter current of the BJT, and $\Delta\beta_F$ represents the deviation of β_F. After a PTAT trim, the residual error voltage V_{ER} in V_{BE} can then be expressed as

$$V_{ER} = V_T \cdot \frac{\Delta\beta_F}{\beta_F} \cdot \left[\left(\frac{1}{1+\beta_F} \right) \Bigg|_{t=125^\circ\mathrm{C}} - \left(\frac{1}{1+\beta_F} \right) \Bigg|_{t=27^\circ\mathrm{C}} \right] \tag{5}$$

where it is assumed that $\Delta\beta_F / \beta_F$ is temperature independent. With the process data of β_F (≈ 4.7 at room temperature) and an estimated value of $\Delta\beta_F / \beta_F = 40\%$, (5) indicates that the error in V_{BE} after a PTAT trim is around 0.8 mV. Such a non-PTAT error is highly process dependent, and is one of the factors that limit the achievable precision of a single-trimmed CMOS bandgap reference.

B. Process Variations of ΔV_{BE}

In a bandgap reference, a ΔV_{BE} generated by biasing two BJTs at different current densities is added to V_{BE}, to compensate V_{BE}'s negative temperature coefficient. The output V_{BG} can then be written as

$$V_{BG} = V_{BE1} + \frac{R_1}{R_2} V_T \ln \left(\frac{I_{C1}}{I_{C2}} N \right) \tag{6}$$

where I_{C1} and I_{C2} are collector currents of Q_1 and Q_2. The temperature drift of the current ratio I_{C1}/I_{C2} will impact the precision of V_{BG}. In the topology shown in Fig. 2(a), matched current sources are used to set the current ratio. The threshold voltage mismatch between M_1 and M_2, and consequently the variation in I_{C1}/I_{C2} results in non-PTAT error in V_{BG}. To prevent such a non-PTAT error source, a matched resistor based topology shown in Fig. 2(b) was chosen for this design. Since the resistor mismatch is more stable over temperature, according to (6), this results in a PTAT error that can be removed by a single PTAT trim. Similarly, the $R_{1B} - R_2$ and $Q_1 - Q_2$ mismatches also result in PTAT errors.

The parasitic base resistances of the BJTs, however, contribute non-PTAT errors to the PTAT voltage [8], [9]. Considering the base resistance, the bandgap voltage V_{BG} can be expressed as

$$\begin{aligned} V_{BG} &= V_{BE1} + \frac{R_1}{R_2 + \frac{1}{N} \cdot \frac{R_B}{1+\beta_F} - \frac{R_B}{1+\beta_F}} V_T \ln N \\ &\approx V_{BG}|_{R_B = 0} + \frac{R_1}{R_2} \cdot V_T \ln N \cdot \left(1 - \frac{1}{N} \right) \\ &\quad \cdot \frac{R_B}{(1+\beta_F) R_2} \end{aligned} \tag{7}$$

where R_B is the parasitic base resistance of Q_1. It is clear that, the higher the resistance R_2 is, the smaller the impact of the base resistance R_B on V_{BG}. As a trade-off between the chip area and precision, the chosen values $R_1 = 240\,\mathrm{k}\Omega$, $R_2 = 30\,\mathrm{k}\Omega$, $N = 8$ together with the process data $\beta_F \approx 4.7$ and $R_B \approx 250\ \Omega$ (the worst case for the chosen process technology) indicate that the last term of (7), or the non-PTAT error, is around 0.6 mV. Similar to the error due to β_F spread, this error is also highly

TABLE I
ERROR SOURCES IN A TYPICAL CMOS BANDGAP REFERENCE

Type of error	Typical value	Error contribution	Error property
Opamp offset	±10mV	±8%	Non-PTAT
BJT saturation current spread	±40%	±0.8%	PTAT
BJT current gain spread	±40%	±0.06%	Non-PTAT
Resistor spread	±30%	±0.6%	PTAT
Resistor mismatch	±1%	±0.5%	PTAT
BJT base resistance	250Ω	±0.04%	Non-PTAT
Curvature	3mV ~ 4mV	±0.2%	Non-PTAT

process dependent and is also a limiting factor on the achievable precision of a CMOS bandgap reference.

C. Opamp Offset

After including the effect of the opamp offset, the bandgap voltage V_{BG} can be expressed as

$$V_{BG} = V_{BE1} + \frac{R_1}{R_2} V_T \ln N + \left(\frac{R_1}{R_2} + 1\right) V_{OS} \qquad (8)$$

where V_{OS} is the input referred opamp offset. Since V_{OS} is amplified by the closed loop gain (R_1/R_2+1), a typical opamp offset (several mV) corresponds to an increased error up to a few tens mV at the bandgap output. Since the offset drift of a CMOS opamp is typically non-PTAT, it is difficult to reduce it with a single PTAT trim. Therefore, the offset needs to be removed by offset cancellation techniques [10], which will be discussed in Section III.

D. Curvature of V_{BE}

The discussion related with compensating V_{BE} with a PTAT voltage assumes that V_{BE} has a first order negative temperature coefficient. However, because V_{BE} is in fact slightly nonlinear as function of temperature, the bandgap voltage is not completely temperature independent. With a PTAT biasing current, the base-emitter voltage V_{BE} can be expressed as [11]

$$V_{BE} = V_{g0} - (V_{g0} - V_{BE,Tr})\frac{T}{T_r} - (\eta - 1)V_T \ln \frac{T}{T_r} \qquad (9)$$

where V_{g0} is the extrapolated bandgap voltage at around $-273°\mathrm{C}$, T_r is the chosen reference temperature, and η is a process related constant. The last term in (9) is the origin of the systematic temperature dependency of V_{BG}, which can be expressed as a function of temperature:

$$V_C(T) = \frac{(\eta - 1)V_{T_r}}{T_r}\left[T - T_r - T \ln \frac{T}{T_r}\right]. \qquad (10)$$

The curvature, or variation of $V_C(T)$ over temperature, could be several mV over the temperature range from $-40°\mathrm{C}$ to $125°\mathrm{C}$. The variation needs to be reduced with a curvature correction technique, as will be shown in Section III.

E. Characterization of Error Sources

The error sources and their contributions to the total error in V_{BG} are summarized in Table I. The spread of the BJT saturation current, the spread of the nominal value of resistors and the resistor mismatch, result in PTAT errors that can be removed by a single room temperature trim. The non-PTAT opamp offset, however, contributes the highest error because it is amplified by the closed loop gain in a bandgap reference towards the output. The curvature of V_{BE} is also a nonlinear function of temperature, resulting in a non-PTAT error. After a single trim, the spread of the BJT current gain β_F and the non-zero parasitic BJT base resistances result in residual non-PTAT errors that determine the achievable precision of the bandgap voltage.

The presented bandgap reference is used as a building block of a mixed-signal IC, and a 3σ inaccuracy of $\pm 0.2\%$ is specified for V_{BG}. Table I shows that, in order to achieve the $\pm 0.2\%$ precision, some of the error sources have to be reduced. These error reduction techniques will be discussed in Section III.

III. ERROR REDUCTION TECHNIQUES

The spread of V_{BE} can be corrected by a single room temperature trim, which simultaneously corrects the PTAT error due to resistor mismatch. However, the opamp offset and the curvature of V_{BE} should be reduced by error reduction techniques, so that the room temperature trim is sufficient for achieving high precision. Considering the number of error sources (seven listed in Table I), the $\pm 0.2\%$ precision specification can be well achieved statistically if all error sources are reduced to 1/5 of the specification, or ± 0.5 mV for a 1.25 V bandgap reference. This section discusses how error reduction techniques are used to reduce each error source.

A. Room Temperature Trim

All the PTAT errors can be removed by a PTAT room temperature trim. The number of trimming bits required can be calculated by comparing the resolution V_{Res} of the trimming network with the expected initial spread V_{Spread} as follows:

$$B \approx \log_2 \frac{V_{Spread}}{V_{Res}}. \qquad (11)$$

To achieve $\pm 0.2\%$ inaccuracy from $-40°\mathrm{C}$ to $125°\mathrm{C}$, the initial inaccuracy at the trim temperature is chosen to be $V_{Res} = V_{BG} \times 0.2\% \times 1/5 \approx 0.5$ mV. With an estimated worst case V_{Spread} of around 20 mV, 6-bit resolution should be enough for the trimming network.

As shown in Fig. 3, trimming can be done by changing one of the resistors in the bandgap core. The switch leakage in the trim network should be taken into account, because the leakage current of an off-state MOSFET switch could have negative

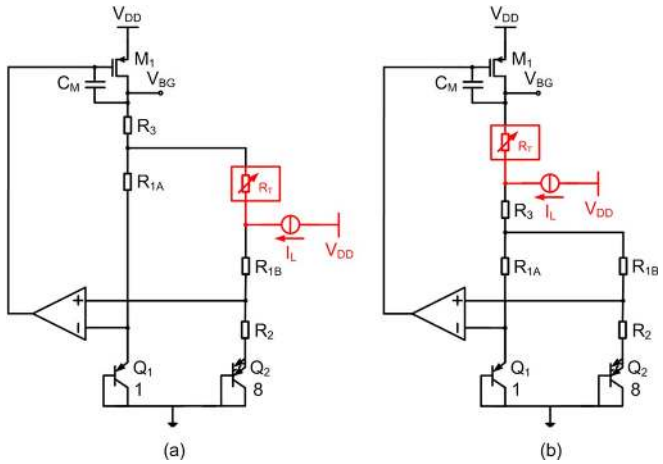

Fig. 3. Comparison of trimming components.

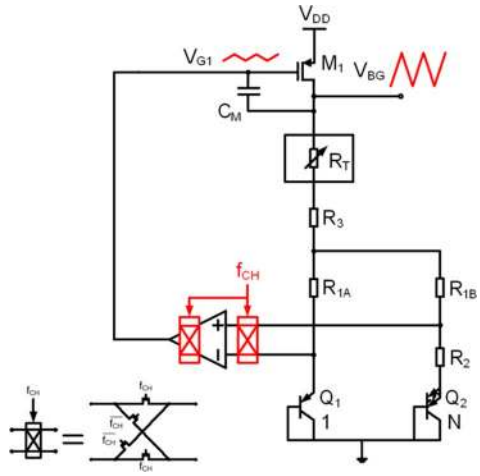

Fig. 4. Bandgap reference with a chopped opamp.

effect on the V_{BG} precision. The leakage current of the trimming switches can be modeled as a current source I_L connected to the bottom of the trim network R_T. As shown in Fig. 3(a), when resistor R_{1B} is trimmed, the leakage current flows through $(R_T + R_3)$, resulting in a voltage drop $I_L(R_T + R_3)$. For some process technologies, such a voltage drop is not negligible since a leakage current $I_L = 5$ nA together with $R_T + R_3 = 100$ kΩ already gives a voltage drop of around 0.5 mV. In contrast, when trimming R_3 (Fig. 3(b)), the corresponding voltage drop is only $I_L R_T$. As a result, R_3 is chosen as the trimming resistor, with the actual trim network R_T stacked on top of it.

B. Opamp Offset Cancellation

The chopping technique is used to reduce the opamp offset, as shown in Fig. 4. Compared to auto-zeroing [4], chopping results in superior noise performance [10], while simultaneously ensures that the opamp's output is continuously available. A folded cascode opamp with a DC gain of 80 dB and an input transconductance of 50 μS is used in this design. As shown in Fig. 5, it is chopped to reduce the offset due to the transistor mismatches. Because the signal path between choppers CH_1 and CH_{2N} is fully differential, the offset due to the mismatches of $M_1 - M_2$ and $M_{10} - M_{11}$ is completely removed by chopping. However, the mismatch errors of $M_4 - M_5$ cannot be completely removed, due to the intrinsic asymmetry of the current mirror configuration. In one phase (PH_1) of chopping, during which M_4 and M_5 are connected to M_6 and M_7 respectively, the drain currents can be written as

$$\sqrt{I_{D6}} = \sqrt{I_{D4}} = \sqrt{\beta}(V_{GS4} - V_{TH4}), \quad (12)$$

$$\sqrt{I_{D7}} = \sqrt{I_{D5}} = \sqrt{\beta}(V_{GS5} - V_{TH5}) \quad (13)$$

where β is the MOSFET tranconductance factor of M_4 and M_5, and V_{TH4}, V_{TH5} are the threshold voltages. Because of $V_{GS4} = V_{GS5}$, I_{D7} is given by

$$I_{D7}|_{PH_1} = I_{D6} + \beta(V_{TH4} - V_{TH5})^2 + 2\sqrt{\beta I_{D6}}(V_{TH4} - V_{TH5}). \quad (14)$$

In the other phase (PH_2), I_{D7} is given by

$$I_{D7}|_{PH_2} = I_{D6} + \beta(V_{TH5} - V_{TH4})^2 + 2\sqrt{\beta I_{D6}}(V_{TH5} - V_{TH4}) \quad (15)$$

simply because M_4 and M_5 are swapped. The residual drain current mismatch can be calculated as

$$\Delta I_{D4,5} = \frac{I_{D7}|_{PH_1} + I_{D7}|_{PH_2}}{2} - I_{D6} = \beta \Delta V_{TH4,5}^2 = \frac{g_{m4,5}^2 \Delta V_{TH4,5}^2}{4 I_{4,5}} \quad (16)$$

where $\Delta V_{TH4,5} = V_{TH4} - V_{TH5}$ represents the threshold voltage mismatch, and $g_{m4,5}$ and $I_{4,5}$ are the transconductance and drain current of M_4 and M_5. The residual opamp offset can then be expressed as

$$V_{OS}|_{\text{Residue}} = \frac{\Delta I_{4,5}}{g_{m1,2}} \approx \frac{\beta \Delta V_{TH4,5}^2}{g_{m1,2}} = \frac{g_{m4,5}^2 \Delta V_{TH4,5}^2}{4 g_{m1,2} I_{4,5}} \quad (17)$$

where $g_{m1,2}$ is the transconductance of M_1 and M_2. To achieve a residual offset around 28 μV (the significance of this value will be discussed in Section III-C), the threshold voltage mismatch $\Delta V_{TH4,5}$ should be smaller than 3 mV under the following practical conditions: $g_{m1,2} = 50$ μS, $g_{m4,5} = 15$ μS, and $I_{4,5} = 2$ μA. For the 0.16 μm CMOS process used in this design, this specification can be achieved with practical transistor sizes by careful layout.

The chopping ripple due to the up-modulation of the opamp offset can be removed by embedding a switched-capacitor notch filter inside the feedback loop [12], [13]. As shown in Fig. 6, the output current of the chopped opamp is integrated synchronously via the sampling capacitor of the notch filter before being transferred to M_1. As a result, the output voltage of the opamp is a triangular wave, which is sampled by the notch filter every chopping cycle. The sample-and-hold operation ensures that the notch filter behaves as a band-stop filter at the chopping frequency f_{CH}, resulting in the ripple reduction. As shown in

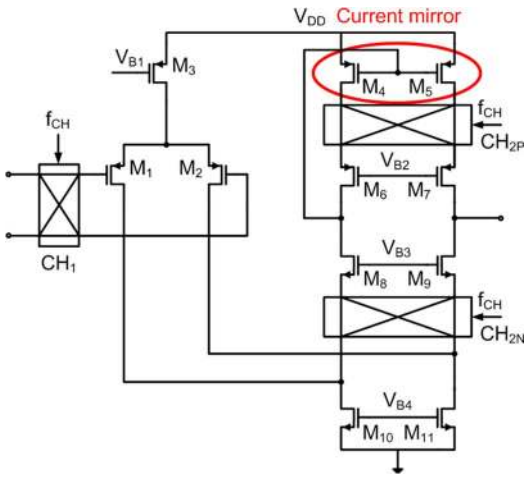

Fig. 5. Chopped single-ended folded cascode opamp.

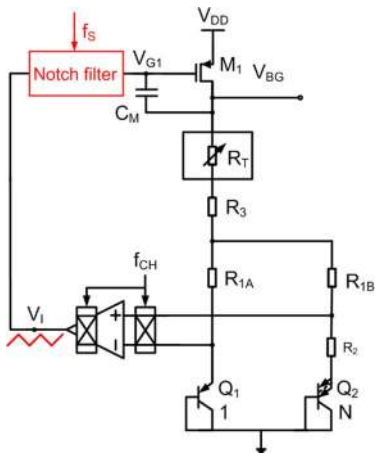

Fig. 6. Ripple reduction with a notch filter.

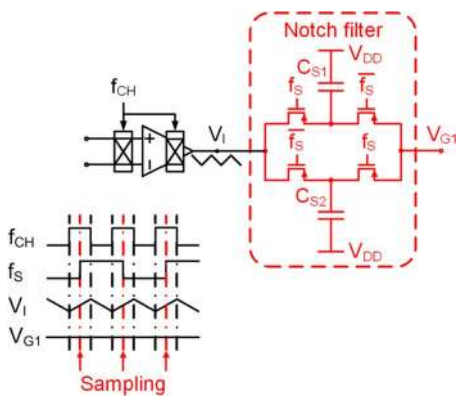

Fig. 7. Implementation of the notch filter.

Fig. 7, the notch filter can be implemented with two sample-and-hold circuits working in Ping-Pong mode. The sampling frequency f_S is chosen to be half of the chopping frequency, so that sampling always takes place at the same slope of the integrated signal V_I. By doing so, the nonlinearities of capacitors C_{S1} and C_{S2} only result in a DC level shift at the output of the notch filter, which can be suppressed by the opamp's large

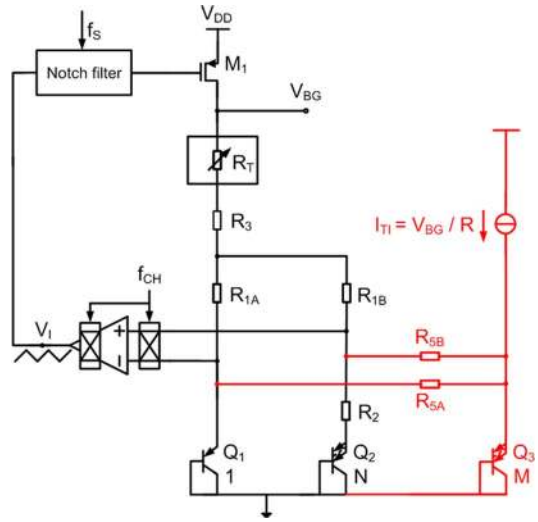

Fig. 8. Curvature correction utilizing a temperature dependent current ratio.

open-loop gain. At the worst case, a 100 mV DC level shift suppressed by an 80 dB opamp DC gain gives only 10 μV input referred offset to the opamp.

C. Curvature Correction

Curvature of V_{BE} can be corrected by utilizing the difference of $V_{BE}s$ between two BJTs with different collector currents [14], [15]. As shown in Fig. 8, this is realized by subtraction of two $V_{BE}s$, of which one (V_{BE} of Q_1) is biased at a PTAT collector current, while the other (V_{BE} of Q_3) is biased at a temperature independent collector current obtained by forcing V_{BG} on a resistor with low temperature coefficient (a poly-silicon resistor in this design). When the resistor ratio is chosen such that [14]

$$\frac{R_1 + 2R_3}{R_5} = \eta - 1 \tag{18}$$

the nonlinear term in (9) is removed, and then the bandgap voltage is given by

$$V_{BG} = V_{g0} - (V_{g0} - V_{BE1,Tr})\frac{T}{T_r} + \frac{R_1 + 2R_3}{R_2} V_T \ln N. \tag{19}$$

With appropriately chosen R_1, R_2, and R_3, the linear term in (19) can be removed, yielding the bandgap voltage $V_{BG} = V_{g0}$.

The PTAT trim of R_3 deteriorates the validity of (18). The residual curvature as a result of R_T trimming, can be roughly expressed as

$$V_C|_{\text{Residue}} \approx \frac{2R_T}{R_5(\eta - 1)} V_C \tag{20}$$

where V_C is the curvature voltage, around 3.5 mV for the chosen 0.16 μm CMOS process from -40°C to 125°C. With $R_5 = 40$ kΩ, $\eta = 4$, and $R_T = \pm 5$ kΩ, $V_C|_{\text{Residue}}$ becomes around ± 0.3 mV, which is less than one fifth of the target inaccuracy. Process variation of the curvature correction circuit itself can also affect the total precision of the bandgap reference. If I_{TI} obtained by forcing V_{BG} on a resistor deviates from the nominal

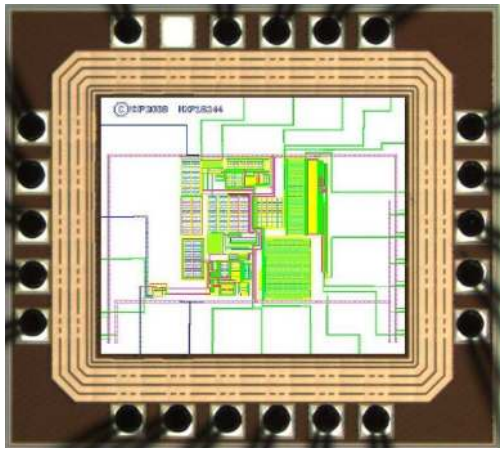

Fig. 9. Die micrograph overlaid by the layout.

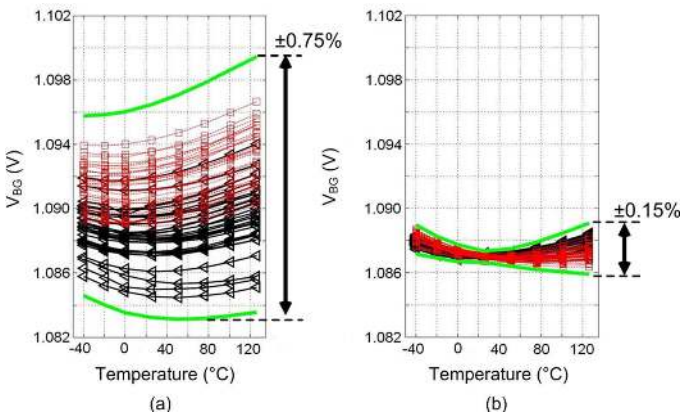

Fig. 10. Inaccuracy of V_{BG} with ceramic package: (a) untrimmed and (b) trimmed. Bond lines indicate the $\pm 3\sigma$ values.

value as a result of the resistance spread, the bandgap voltage can be calculated as

$$V_{BG} = V_{BG}|_{\Delta I_{TI}=0} - \frac{R_1 + 2R_3}{R_5} V_T \frac{\Delta I_{TI}}{I_{TI}} \qquad (21)$$

where ΔI_{TI} is the deviation of I_{TI}. The errors due to I_{TI} deviation is PTAT, which can be removed by the room temperature trim.

Since the curvature correction resistors R_{5A} and R_{5B} are connected to the input of the opamp in the bandgap core, the closed loop gain of the feedback loop in the bandgap core can be calculated as

$$A_{closed\ loop} = \frac{R_1 + 2R_3}{R_2} + \frac{R_1 + 2R_3}{R_5} + \frac{R_3}{R_1} + 1. \qquad (22)$$

Compared to (8) without curvature correction, (22) shows that the offset and noise requirement is more critical, because both the input referred offset and noise are amplified by additional factors. Using practical values of $R_1 = R_3 = 80\ \text{k}\Omega$, $R_2 = 30\ \text{k}\Omega$, $R_5 = 40\ \text{k}\Omega$, it can be calculated that $A_{closed\ loop} \approx 16$. With $V_{BG} = V_{g0} \approx 1.15\ \text{V}$, in order to make the error due to the opamp's offset less than one fifth of the 0.2% target, the maximum acceptable offset is $V_{BG} \times 0.2\% \times 1/5 \times 1/A_{closed\ loop} \approx 28\ \mu\text{V}$. This level of offset is achieved by the chopping technique discussed in Section III-B.

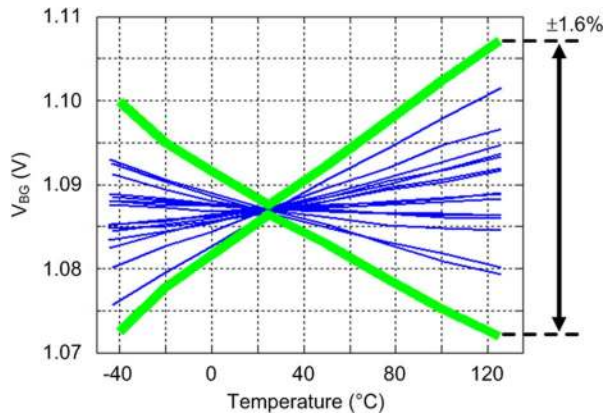

Fig. 11. Inaccuracy of V_{BG} after a room temperature trim, without opamp offset cancellation. Bond lines indicate the $\pm 3\sigma$ values.

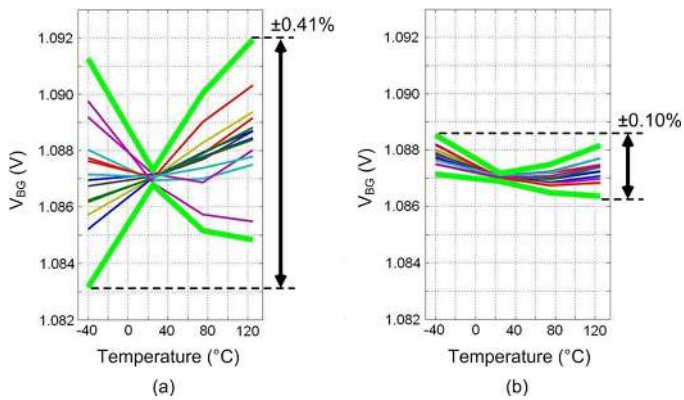

Fig. 12. Inaccuracy of V_{BG} with plastic package: (a) without chip-coating, and (b) with chip-coating. Bond lines indicate the $\pm 3\sigma$ values.

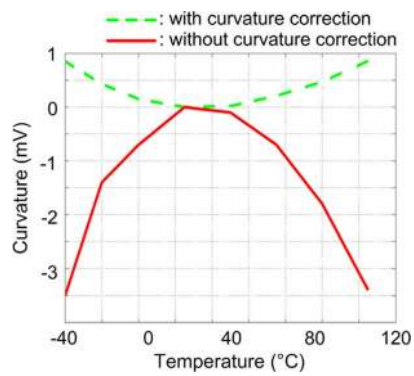

Fig. 13. Temperature curve of V_{BG} with and without curvature correction.

IV. Experimental Results

The bandgap reference was fabricated in a standard 0.16 μm, 1P-5M CMOS process. Fig. 9 shows the chip microphotograph whose active area is 0.12 mm^2. Sixty-one samples from two batches are packaged in ceramic package and measured from -40°C to 125°C. The chopping frequency is chosen to be 200 kHz, which is above the flicker noise corner frequency of the opamp. Fig. 10 shows the measured V_{BG} versus temperature: 30 samples from one batch are plotted (triangles) together with 31 samples from another batch (squares). The untrimmed inaccuracy is around $\pm 0.75\%$ (3σ), which decreases to around

TABLE II
PERFORMANCE COMPARISON

Parameter		This work	[2]	[3]	[5]	[6]
Technology		**0.16μm CMOS**	0.35μm CMOS	0.6μm CMOS	0.18μm CMOS	0.8μm CMOS
Supply Voltage		**1.8V±10%**	1.4V	1.8V–5.5V	1.8V±5%	1.05V–2V
Active Area		**0.12mm²**	1.2mm²	1.2mm²	0.007mm²	0.16mm²
Bandgap Voltage		**1.0875V**	0.858 V	1.15 V	1.226 V	0.71 V
Inaccuracy	Untrimmed	**±0.75% (3σ)**	N.A.	N.A.	±0.86% (3σ)	±1.1%
	Trimmed	**±0.15%[A] (3σ)**	±0.91%[A] (3σ)	±0.11%[B]	N.A.	N.A.
	# of Sample	**61 samples (2 batches)**	11 samples	60 samples (1 batch)	831 samples	4 samples
	Temp.Range	**-40°C to 125°C**	-40°C to 125°C	-20°C to 120°C	1 temp. point	25°C
Temperature Drift (box method)		**5–12ppm/°C[A] (61 samples)**	12.4ppm/°C[B] (One sample)	3–10ppm/°C[B] (60 samples)	10ppm/°C (One sample)	N.A.
Current Consumption		**55μA**	116μA	100μA	3.3mA	8.2 mA
Noise		**6.1μV(rms) (0.1Hz ~ 10Hz)**	9.1μV(rms) (0.1Hz ~ 10Hz)	53μV_{PP} (0.1Hz ~ 10Hz)	N.A.	67μV(rms) (10Hz~100kHz)
PSR		**74dB@DC**	68dB@100Hz	83dB	N.A.	N.A.

[A]One-temperature trim. [B]Two-temperature trim.

$\pm 0.15\%\ (3\sigma)$ after a room temperature trim. After trimming, the spread within each batch is only slightly less, $\pm 0.11\%\ (3\sigma)$ for one batch and $\pm 0.12\%\ (3\sigma)$ for the other, demonstrating the robustness of the room temperature trim on batch-to-batch variations.

To verify the necessity of the opamp offset cancellation, chopping was disabled and 16 samples from one batch were measured. Fig. 11 shows that the inaccuracy of V_{BG} is around $\pm 1.6\%\ (3\sigma)$ after a room temperature trim. This confirms that the opamp offset is a significant error source in CMOS bandgap references, and a room temperature trim is insufficient for achieving high precision.

To observe the impact of packaging, 12 samples were packaged in plastic, while 12 other samples from the same batch were packaged with a stress-relieving chip coating between the die and the plastic molding. As shown in Fig. 12(a), the bandgap reference precision is severely impacted by the package, and a room temperature trim is no longer sufficient. These errors are probably the result of the non-PTAT deviation of V_{BE} due to mechanical stresses. In contrast, when the die is chip-coated, the precision of the bandgap reference is essentially unaffected by the packaging, as shown in Fig. 12(b).

Fig. 13 demonstrates the measured curvature of the bandgap reference. Using the "box" method, the curvature corrected bandgap reference (dashed curve) achieves a temperature drift of 4.7 ppm/°C, while with curvature correction disabled (solid curve), this increases to 16.4 ppm/°C, which shows the curvature has been reduced by a factor of 4. It can be seen that the curvature is slightly over corrected, which is believed to be caused by the difference between the actual and the modeled values of the BJT parameter η (9). By tuning the resistor ratio $(R_1 + 2R_3)/R_5$ in (18), it is expected that the temperature drift

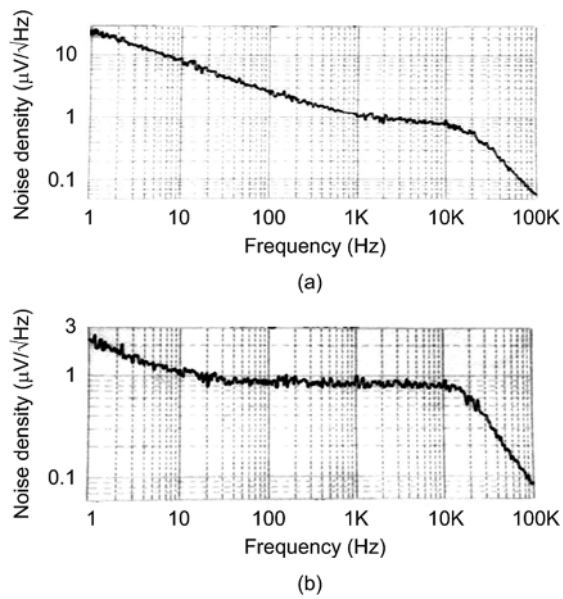

Fig. 14. Noise spectrum of V_{BG} from 1 Hz to 100 kHz: (a) without chopping, and (b) with chopping.

can be made even smaller. After a room temperature trim, the temperature drift of all samples varies between 5 ppm/°C to 12 ppm/°C. This low temperature drift greatly relaxes, and thus reduces the cost of the trimming process, because temperature variations during trimming of even up to a few degrees will result in negligible errors in V_{BG}.

The output noise spectrum is shown in Fig. 14. The noise density at 1 Hz is about 2.5 $\mu V/\sqrt{\text{Hz}}$ with chopping, which increases to about 25 $\mu V/\sqrt{\text{Hz}}$ when chopping is disabled. This

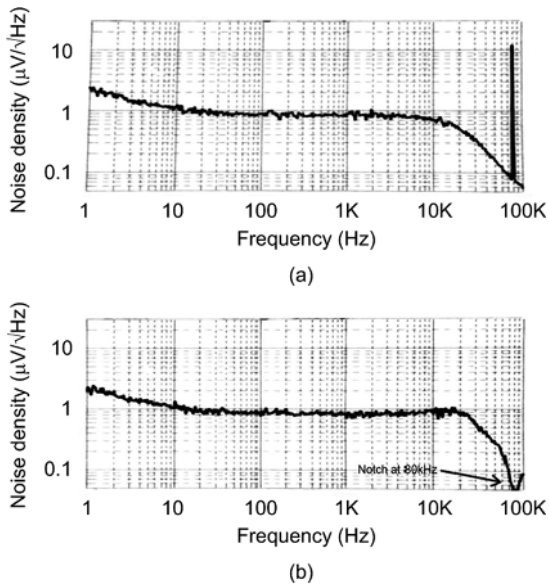

Fig. 15. Noise spectrum of V_{BG} from 1 Hz to 100 kHz: (a) without notch filter, and (b) with notch filter.

shows that chopping effectively suppresses the low frequency noise of the bandgap reference. To verify the ripple reduction effect of the notch filter, the chopping frequency was decreased from 200 kHz to 80 kHz, because the frequency range of the signal analyzer (HP 3562A) we used only extends to 100 kHz. As shown in Fig. 15, the filter effectively removes the ripple by adding a notch in the spectrum of V_{BG} at the chopping frequency. Table II summarizes the performance of the proposed bandgap reference and compares its performance with other previous works [2], [3], [5], [6].

V. Conclusion

A high precision CMOS bandgap reference has been presented. The discussion has focused on three key aspects: room temperature trim to remove the PTAT errors, chopping to reduce the offset of the opamp in the bandgap core, and curvature correction to minimize the temperature nonlinearity of the base-emitter voltage. With a single room temperature trim, a 3σ inaccuracy of $\pm 0.15\%$ from -40°C to 125°C has been achieved. The proposed combination of error reduction techniques can be used in low-cost, area-efficient, precision CMOS bandgap reference designs.

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