2014

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Pages: 1448 - 1458, DOI: 10.1109/TIA.2013.2273751

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***Abstract*—Incorporating a medium-voltage dc (MVDC) integrated power system is a goal for future surface combatants and submarines. In an MVDC shipboard power system, dc/dc converters are commonly employed to supply constant power to electric loads. These constant power loads have a characteristic of negative incremental impedance, which may cause system instability during disturbances if the system is not properly controlled. This paper proposes a sliding-mode duty-ratio controller (SMDC) for dc/dc buck converters with constant power loads. The proposed SMDC is able to stabilize the dc power systems over the entire operating range in the presence of significant variations in the load power and input voltage. The proposed SMDC is validated by both simulation studies in MATLAB/Simulink and experiments for stabilizing a dc/dc buck converter with constant power loads. Simulation studies for an MVDC shipboard power system with constant power loads for different operating conditions with significant variations in the load power and supply voltage are also provided to further demonstrate the effectiveness of the proposed SMDC.**

***Index Terms*—Buck converter, constant power load, dc/dc converter, medium-voltage dc (MVDC) system, sliding-mode controller (SMC), stability.**

I. Introduction

In ADVANCED shipboard power systems, the continuous trend toward "more electric ship" or even "all electric ship" will have a significant portion of the mechanical and hydraulic power been substituted by electric power. These changes will increase the efficiency and reduce cost and environmental impact of shipboard systems. A medium-voltage dc (MVDC) integrated power system has been established as the U.S. Navy's goal in future surface combatants and submarines [1]. The MVDC shipboard power system is a long-term goal for providing affordable electric power dense systems. However, the application still requires standardized methods for system design, stability analysis, control, fault detection, isolation, etc. In particular, the interactions among extensively connected nonlinear power electronic components/modules will increase the dynamic complexity of this type of "power electronics intensive" power system, where the negative incremental impedance-induced instability of the system with constant power loads is one of the main challenges [2], [3].

Most power electronic converters in the MVDC shipboard power system behave as constant power loads when their outputs are tightly regulated with little variations around the reference values. A constant power load has negative incremental impedance because the load current will increase (decrease) with the decrease (increase) in the load voltage [2], [4]. This negative incremental impedance will have a negative impact on the stability of the dc/dc converters, which may consequently threat the power quality and stability of the MVDC system. Therefore, appropriate control methods are needed to ensure the system stability [1].

Classical linear control methods are commonly used in the controller design for dc/dc converters. Small-signal models have been used to analyze the stability and design controllers for dc/dc converters with constant power loads, in which the system's equations are linearized around an equilibrium point and then analyzed by using classical eigenvalue or frequency-domain techniques [5], [6]. However, due to the nonlinearity of the system, the linear control methods can only ensure small-signal stability, but they are not effective when the system is experiencing large perturbations, e.g., step load changes. Recently, large-signal analysis methods, e.g., large-signal phase-plane analysis, Lyapunov analysis, and Brayton–Moser mixed potential method, have been used for stability analysis of dc–dc converters [7], [8], [18]–[22]. These methods can provide analytical estimation of the system's stability region. Sliding-mode and feedback linearization methods [4], [5], [8]–[11] have been used for designing controllers for dc/dc converters. However, these controllers were designed to only handle the systems at one constant power condition [4], [5], [8] or with a resistive load [9]–[11] and cannot guarantee system stability when the load power significantly changes. To ensure stability of an MVDC system with constant power loads, a controller that can guarantee large-signal stability in the presence of both input voltage and load variations is needed.

This paper proposes a novel sliding-mode duty-ratio controller (SMDC) for a dc/dc buck converter with constant power loads. The proposed SMDC outputs a duty ratio, which is used to generate pulsewidth-modulated (PWM) gate signals for the dc/dc converter. This is different from conventional sliding-mode controllers (SMCs) in the literature, whose

Manuscript received June 30, 2011; revised January 25, 2012, June 13, 2012, September 21, 2012, and February 1, 2013; accepted June 18, 2013. Date of publication July 17, 2013; date of current version March 17, 2014. Paper 2011-IACC-198.R4, presented at the 2011 IEEE Industry Applications Society Annual Meeting, Orlando, FL, USA, October 9–13, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Industrial Automation and Control Committee of the IEEE Industry Applications Society. This work was supported in part by the U.S. National Science Foundation under CAREER Award ECCS-0954938 and in part by the University of Nebraska–Lincoln College of Engineering under the Edgerton Innovation Award.

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Digital Object Identifier 10.1109/TIA.2013.2273751

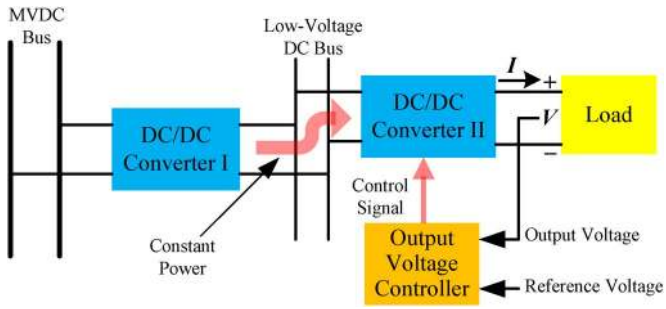

Fig. 1. DC/DC converter II behaves as a constant power load in a shipboard dc-ZED system module.

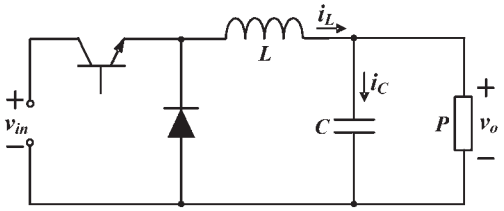

Fig. 2. Buck converter with a constant power load.

outputs were directly utilized as gate signals. The proposed SMDC is capable of stabilizing the dc power systems over the entire operating range in the presence of significant variations in the load power and supply voltage. Simulation studies are carried out in MATLAB/Simulink to validate the proposed controller for stabilizing a dc/dc buck converter, as well as an MVDC shipboard power system with constant power loads. Experimental results on a practical buck converter with constant power loads are provided to further validate the proposed SMDC.

II. Negative Incremental Impedance-Induced Instability in a DC Power System With Constant Power Loads

The electric components, e.g., power electronic converters and motor drives, of advanced MVDC shipboard power systems, especially those in the shipboard dc zonal electrical distribution (ZED) modules, behave as constant power loads when they are tightly regulated. Shown in Fig. 1 is the dc/dc converter II, whose output voltage is regulated to supply a load, e.g., a constant resistive load, in a shipboard dc-ZED module. Consequently, the input power of the dc/dc converter II is constant.

For a constant power load, the product of the load voltage and current (i.e., $P = V \cdot I$) is a constant and the instantaneous value of the load impedance is positive (i.e., $V/I > 0$). However, the incremental impedance is always negative (i.e., $\Delta V/\Delta I < 0$). This negative incremental impedance has a negative impact on the power quality and stability of the system.

A buck converter in Fig. 2 is used as an example to show the instability of a dc/dc converter with a constant power load. The state–space equations of the buck converter when the switch is on (i.e., $0 < t < dT$) and off (i.e., $dT < t < T$) are given by (1-A) and (1-B), respectively,

$$\begin{cases} \frac{di_L}{dt} = \frac{1}{L}\left(v_{\text{in}} - v_o\right) \\ \frac{dv_o}{dt} = \frac{1}{C}\left(i_L - \frac{P}{v_o}\right) \end{cases} \quad \text{when } 0 < t < dT \tag{1-A}$$

$$\begin{cases} \frac{di_L}{dt} = \frac{1}{L}\left(-v_o\right) \\ \frac{dv_o}{dt} = \frac{1}{C}\left(i_L - \frac{P}{v_o}\right) \end{cases} \quad \text{when } dT < t < T \tag{1-B}$$

where d and T are the duty ratio and switching period of the converter, respectively. Using the state–space averaging method [12], [13], the dynamic model of the buck converter can be written as

$$\begin{cases} \frac{di_L}{dt} = \frac{1}{L}(v_{\text{in}} d - v_o) \\ \frac{dv_o}{dt} = \frac{1}{C}\left(i_L - \frac{P}{v_o}\right). \end{cases} \tag{2}$$

Consider small perturbations in the state variables due to small disturbances in the input voltage and duty ratio

$$\begin{cases} v_{\text{in}} = V_{\text{in}} + \tilde{v}_{\text{in}} \\ d = D + \tilde{d} \\ v_o = V_o + \tilde{v}_o \\ i_L = I_L + \tilde{i}_L \end{cases} \tag{3}$$

where V_{in}, D, V_o, and I_L are the average values of v_{in}, d, v_o, and i_L, respectively. Substitute (3) into (2), the dynamic model of the buck converter becomes

$$\begin{cases} \frac{d\tilde{i}_L}{dt} = \frac{1}{L}(V_{\text{in}}\tilde{d} + D\tilde{v}_{\text{in}} - \tilde{v}_o) \\ \frac{d\tilde{v}_o}{dt} = \frac{1}{C}\left(\tilde{i}_L - \frac{P\tilde{v}_o}{V_o^2}\right). \end{cases} \tag{4}$$

Note that the following approximation is made due to the fact that $V_o \gg \tilde{v}_o$:

$$I_L - \frac{P}{v_o} = \frac{P}{V_o} - \frac{P}{V_o + \tilde{v}_o} = \frac{P\tilde{v}_o}{V_o(V_o + \tilde{v}_o)} = \frac{P\tilde{v}_o}{V_o^2}.$$

The transfer functions of the system can be obtained from (4) as follows:

$$\begin{cases} H_1(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{\frac{V_{\text{in}}}{LC}}{s^2 - \left(\frac{P}{CV_o^2}\right)s + \frac{1}{LC}} \\ H_2(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_{\text{in}}(s)} = \frac{\frac{D}{LC}}{s^2 - \left(\frac{P}{CV_o^2}\right)s + \frac{1}{LC}}. \end{cases} \tag{5}$$

Both transfer functions in (5) have poles in the right half plane. Therefore, the system is unstable because of the constant power load. Fig. 3 shows the simulation results of the load voltage and current of the open-loop-controlled buck converter, where the initial duty ratio is 0.25, the source voltage is 40 V, the load voltage is 10 V, and the constant load power is 2 W. A small disturbance in the load current at 1 ms causes the load voltage to increase in order to maintain the constant power, which results in further decrease in the inductor and load currents. This acts as a positive feedback to the circuit. Therefore, the load current eventually decreases to 0.5 A while the load voltage increases to 40 V, which is the same as the source voltage.

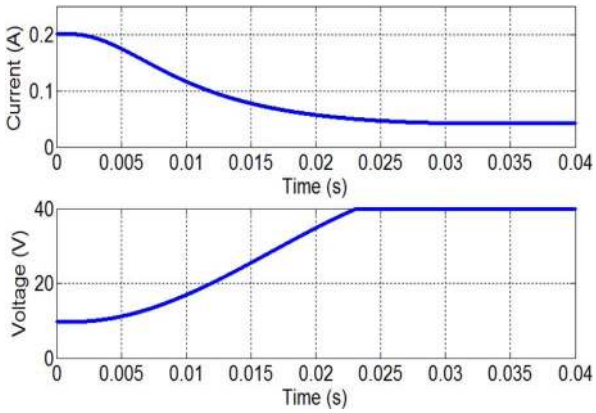

Fig. 3. Simulated load voltage and current of the open-loop-controlled buck converter with a constant power load.

Linear (e.g., PI) controllers can be designed to stabilize the system around a specific operating point based on a linearized small-signal model, such as that described by (5). However, when the operating point (e.g., the input voltage $V_{\rm in}$ or the load power P) significantly changes, the system, which still contains unstable poles, may not be able to be stabilized by using the same linear controller.

As a comparison, under the small perturbations shown in (3), the transfer function of the buck converter with a resistive load instead of a constant power load can be obtained as

$$H_3(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{\frac{V_{\rm in}}{LC}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} \tag{6}$$

where the two poles are in the left half plane. Therefore, the system is stable.

III. Sliding-Mode Control for DC/DC Converter

The SMC is an important robust control approach for nonlinear systems. The most important issue in designing an SMC is to design a switching control law to drive the plant state to a switching surface and maintain it on the surface upon interception [14]. Previous studies have shown that if the sliding mode is enforced, the closed-loop control system will have attractive advantages of robustness to disturbances and low sensitivity to parameter variations [16]. This section presents the design procedure of the conventional SMC for a dc/dc converter.

Consider a unified state–space formulation of a dc/dc converter [16]: $\dot{x} = Ax + uBx$, where scalar x is the state of interest (e.g., the output voltage) of the dc/dc converter; scalar u is the control signal, which is generated by a switching control law; and A and B are parameter matrices of the converter. Suppose that x_d is the reference value for x, then state tracking error can be defined as $\tilde{x} = x - x_d$. The switching control law is commonly designed as $u = u_{\rm sw} = 1/2[1 + \text{sign}(s)]$, where s is a function of the state tracking error defined as $s = c^T\tilde{x}$, and vector c denotes the gradient of s with respect to $\tilde{x}$. More generally, an nth-order s function [14] can be designed as

$$s(x;t) = \left(\frac{d}{dt} + \lambda\right)^{n-1} \tilde{x} \tag{7}$$

where λ is a positive constant. Define a candidate Lyapunov function $V(s) = s^2/2$. Then, to ensure controller stability and convergence of the state trajectory to the sliding surface, the proposed switching control should guarantee that the time derivative of $V(s)$ is always negative when $s \neq 0$, i.e.,

$$\dot{V}(s) = s \cdot \dot{s} < 0. \tag{8}$$

According to the definition of s, the time derivative of s can be calculated as

$$\dot{s} = c^T\dot{x} = c^T(Ax + uBx) = c^TAx + \frac{1}{2}c^TBx + \frac{1}{2}\text{sign}(s)c^TBx. \tag{9}$$

Substituting (9) into (8) yields

$$s\dot{s} = s\left(c^TAx + \frac{1}{2}c^TBx\right) + \frac{1}{2}|s|c^TBx < 0.$$

Then, the necessary condition for the existence of the sliding mode in the vicinity of $s(x;t) = 0$ can be derived as follows:

$$\begin{cases} c^TAx < -c^TBx, & s > 0 \\ c^TAx > 0, & s < 0. \end{cases} \tag{10}$$

In the SMC controlled system, the dynamics of the state of interest in the sliding mode can be written as $\dot{s} = 0$. By solving this equation, an expression can be obtained for u, which is called the equivalent control law $u_{\rm eq}$ [14]. The equivalent control law can be interpreted as a continuous control law that would maintain $\dot{s} = 0$ if the plant dynamics are exactly known. For the dc/dc converter, $u_{\rm eq}$ can be calculated by setting (9) to be 0, which yields $u_{\rm eq} = -c^TAx/c^TBx$. To ensure that (10) is satisfied, $u_{\rm eq}$ needs to satisfy the following inequalities:

$$0 < u_{\rm eq} = -c^TAx/c^TBx < 1. \tag{11}$$

IV. Proposed SMDC for a Buck Converter With Constant Power Loads

In this section, a conventional SMC is first designed based on the method presented in Section III for a buck converter with constant power loads. However, the conventional SMC has an inherent disadvantage of variable switching frequency. This is not suitable for converter applications in which a constant switching frequency is desired. The SMDC is proposed to solve this problem. The control law of the proposed SMDC is a summation of a continuous function, i.e., an equivalent control $u_{\rm eq}$, and a switching function. The continuous function gives a good approximation of the switching control law in the conventional SMC, whereas the switching function is utilized to handle disturbances and parameter uncertainties of the converter model. The output of the SMDC will be used as the duty ratio for a pulsewidth modulator to generate the control signal for the converter. Thus, the operating frequency of the proposed SMDC is fixed. The closed-loop stability and robustness to converter parameter variations are theoretically validated in this section. The proposed SMDC can stabilize the system when large disturbances occur in the input voltage and output power of the converter. This feature is critical to the safe operation of an MVDC shipboard power system, particularly

when the dc bus voltage is unstable and the ZED modules have load variations.

A. Conventional SMC for Buck Converters With Constant Power Loads

Consider the dc/dc buck converter with a constant power load in Section II. According to (7), an s function is designed as follows:

$$s = \left(\frac{d}{dt} + \lambda\right)^2 \left(\int_0^t \tilde{x} dt\right) = \dot{\tilde{x}} + 2\lambda\tilde{x} + \lambda^2 \int_0^t \tilde{x} dt \quad (12)$$

where $\tilde{x}$ is the output voltage tracking error, which is defined as $\tilde{x} = e_v = V_{\rm ref} - v_o$ in this paper, and $V_{\rm ref}$ is the reference value for the output voltage of the buck converter. Then, (12) can be rewritten as

$$s = a_1\dot{e}_v + a_2 e_v + a_3 \int e_v dt \quad (13)$$

where a_1, a_2, and a_3 are positive coefficients. The switching control law of the SMC is designed as

$$u = u_{\rm sw} = \frac{1}{2}\left[1 + \text{sign}(s)\right] = \begin{cases} 1, & \text{when } s > 0 \\ 0, & \text{when } s < 0. \end{cases} \quad (14)$$

To derive a necessary condition to ensure the existence of the sliding mode and that (8) is always valid, the following procedure is conducted. First, the time derivative of s is calculated as $\dot{s} = a_1\ddot{e}_v + a_2\dot{e}_v + a_3 e_v$. According to the dynamic model (2) of the dc/dc buck converter, the first and second time derivatives of the voltage tracking error can be derived as

$$\dot{e}_v = -\dot{v}_o = -\frac{1}{C}\left(i_L - \frac{P}{v_o}\right) \quad (15)$$

$$\ddot{e}_v = \frac{P}{C^2 v_o^2} i_c - \frac{v_{\rm in}}{LC} u + \frac{v_o}{LC}. \quad (16)$$

Substituting (15) and (16) into the expression of $\dot{s}$ yields

$$\dot{s} = \left(\frac{a_1 P}{v_o^2 C^2} - \frac{a_2}{C}\right) i_C - \frac{a_1}{LC}(v_{\rm in} u - v_o) + a_3(V_{\rm ref} - v_o). \quad (17)$$

According to (8), to ensure controller stability and convergence to the sliding mode, $\dot{V} = s\dot{s} < 0$ should be always satisfied by using the proposed switching control law (14). Then, the following two conditions can be derived by substituting (14) into (17) and ensuring $s\dot{s} < 0$.

1) If $s > 0$, $u_{\rm sw}$ will be equal to 1, and $\dot{s}$ needs to be smaller than 0, which yields

$$\dot{s} = \left(\frac{a_1 P}{v_o^2 C^2} - \frac{a_2}{C}\right) i_C - \frac{a_1}{LC}(v_{\rm in} - v_o) + a_3(V_{\rm ref} - v_o) < 0. \quad (18)$$

2) If $s < 0$, $u_{\rm sw}$ will be equal to 0, and $\dot{s}$ needs to be greater than 0, which yields

$$\dot{s} = \left(\frac{a_1 P}{v_o^2 C^2} - \frac{a_2}{C}\right) i_C + \frac{a_1}{LC} v_o + a_3(V_{\rm ref} - v_o) > 0. \quad (19)$$

Based on (18) and (19), the ranges of the coefficients a_1, a_2, and a_3 in (13) can be determined.

In practical applications of the buck converter, the output of the conventional SMC, which is a variable-duration binary signal, can be directly used as the switching signal for the controllable switches in the circuit. However, the switching frequency of the controllable switches will be variable. Thus, the system's operating frequency cannot be determined accurately. This will cause problems to the design of the circuit components and filter. Furthermore, at steady state, the control signal generated by the conventional SMC will be highly sensitive to the parameter uncertainties and disturbances of the converter. To solve these problems, an SMDC using a fixed switching frequency and robust to converter parameter uncertainties is proposed.

B. Control Law Design for the Proposed SMDC

Per discussions in Section III, if the converter dynamics are exactly known, $u_{\rm eq}$ can be used as a continuous control law to maintain $\dot{s} = 0$. According to [17], if the switching frequency of the converter approaches infinity (in practice, a very large value), the averaged dynamics of an SMC-controlled system is equivalent to the averaged dynamics of a PWM-controlled system. This indicates that $u_{\rm eq} = d$, where d is the duty ratio of a pulsewidth modulator. Therefore, it is reasonable to design an SMDC whose output is utilized as the duty ratio directly for pulsewidth modulation of the converter using a fixed switching component. To handle disturbances to the converter, a switching term with a variable magnitude is added to $u_{\rm eq}$ to form the complete control law for the proposed SMDC

$$u = u_{\rm eq} + \frac{|e_v|}{v_{\rm in}}\text{sign}(s) \quad (20)$$

where $u_{\rm eq}$ is calculated by setting (17) to be zero

$$u_{\rm eq} = \frac{L}{v_{\rm in}}\left[\left(\frac{P}{C v_o^2} - \frac{a_2}{a_1}\right) i_C + \frac{1}{L} v_o + \frac{a_3 C}{a_1}(V_{\rm ref} - v_o)\right]. \quad (21)$$

According to (11), $u_{\rm eq}$ should be limited between 0 and 1. Then, the time derivative of the candidate Lyapunov function is calculated as

$$\dot{V}(s) = s \cdot \dot{s} = s \cdot \left(0 - \frac{a_1 v_{\rm in}}{LC} \cdot \frac{|e_v|}{v_{\rm in}}\text{sign}(s)\right) = -\frac{a_1}{LC}|s|. \quad (22)$$

In (22), a_1 is a positive coefficient of the s function. Thus, (22) is always negative when $s \neq 0$. This ensures the controller stability and convergence to the sliding mode.

C. Robustness of the Proposed SMDC to Converter Parameters' Variations

The value of $u_{\rm eq}$ given by (21) can be calculated online by using the system states, e.g., v_o, which are measured online and converter parameters, e.g., C and L, which are usually determined offline. However, the parameters usually vary with the operating condition and cannot be always measured accurately enough. Especially, compared to inductance, capacitance C has larger uncertainties caused by measurement errors under

a high switching frequency. As a result, $u_{\rm eq}$ cannot exactly maintain $\dot{s}$ to be zero. In addition, the disturbance caused by parameter uncertainties should be considered and well handled in the SMDC.

Suppose that the measured capacitance $\hat{C}$ is different from the actual capacitance value C, then the equivalent control $\hat{u}_{\rm eq}$ is expressed as

$$\hat{u}_{\rm eq} = \frac{L}{v_{\rm in}}\left[\left(\frac{P}{\hat{C}v_o^2} - \frac{a_2}{a_1}\right)i_C + \frac{1}{L}v_o + \frac{a_3\hat{C}}{a_1}(V_{\rm ref} - v_o)\right]. \tag{23}$$

The resultant control law of SMDC is

$$u = \hat{u}_{\rm eq} + \frac{|e_v|}{v_{\rm in}}{\rm sign}(s). \tag{24}$$

Substituting (24) into (17) yields

$$\begin{aligned}\dot{s} &= \left(\frac{a_1P}{v_o^2C^2} - \frac{a_2}{C}\right)i_C \\ &\quad - \frac{a_1}{LC}\left[v_{\rm in}\left(\hat{u}_{\rm eq} + \frac{|e_v|}{v_{\rm in}}{\rm sign}(s)\right) - v_o\right] + a_3e_v \\ &= a_3\left(1 - \frac{\hat{C}}{C}\right)e_v - \frac{a_1|e_v|}{LC}{\rm sign}(s).\end{aligned} \tag{25}$$

To ensure system stability and meet the requirements of (8) when $s \neq 0$, the following two conditions should be satisfied.

1) If $s > 0$, $\dot{s}$ needs to be smaller than 0, which yields

$$a_3\left(1 - \frac{\hat{C}}{C}\right)e_v - \frac{a_1|e_v|}{LC} < 0 \Rightarrow \frac{a_1}{a_3} > L(C - \hat{C})\frac{e_v}{|e_v|}. \tag{26}$$

2) If $s < 0$, $\dot{s}$ needs to be greater than 0, which yields

$$a_3\left(1 - \frac{\hat{C}}{C}\right)e_v + \frac{a_1|e_v|}{LC} > 0 \Rightarrow \frac{a_1}{a_3} > L(\hat{C} - C)\frac{e_v}{|e_v|}. \tag{27}$$

To ensure that (26) and (27) are simultaneously satisfied, the ranges of the coefficients a_1 and a_2 should be

$$\frac{a_1}{a_3} > L|\hat{C} - C|. \tag{28}$$

The inequality (28) is a necessary condition to ensure the stability of the controller. In practical applications, (28) is easy to meet by adjusting a_1 and a_2, e.g., selecting $a_1/a_2 > LC$, when considering 100% uncertainty in the capacitance.

In conclusion, due to the introduced switching term, by selecting suitable coefficients of the SMDC according to (28), the resultant SMDC is robust to converter parameters' uncertainties and can ensure the stability of the controller and convergence of the state trajectory to the sliding mode.

D. Implementation of the Proposed SMDC

Per previous discussion, under a high switching frequency, the duty ratio is basically a smooth analytic function of the discrete pulses in a PWM-controlled system. The averaged dynamics of an SMC-controlled system is equivalent to the averaged dynamics of a PWM-controlled system, Therefore, the output of the proposed SMDC can be used as the duty ratio d for PWM control of the converter, namely

$$d = u = \frac{1}{v_{\rm in}}\left[k_1i_C + k_2(V_{\rm ref} - v_o) + v_o\right] + \frac{|e_v|}{v_{\rm in}}{\rm sign}(s) \tag{29}$$

where $k_1 = L(P/Cv_o^2 - a_2/a_1)$ and $k_2 = a_3LC/a_1$. Due to the physical limitation, duty ratio d should be limited within [0, 1]. Therefore, the actual duty ratio for the pulsewidth modulator is designed as

$$d^* = \begin{cases} 1, & d \geq 1 \\ d, & 0 < d < 1 \\ 0, & d \leq 0. \end{cases} \tag{30}$$

The parameter k_1 of (29) is adaptive to the load power and voltage. Since the voltage tracking error is used to design the s function in (12), which is independent from the load power, the proposed SMDC can stabilize the load voltage when the load power changes. The input voltage of the buck converter also appears in (29). Therefore, the duty ratio is also adaptive to the variation of the input voltage.

The proposed SMDC is applied to control the buck converter with constant power loads, as shown in Fig. 4. The output of the SMDC is the desired duty ratio, which is used by a pulsewidth modulator to generate the control signal to drive the controllable switch of the converter. Compared to the conventional SMCs that usually have a variable switching frequency, the switching frequency of the proposed SMDC is determined by the frequency of the carrier signal, which is usually constant. In practical applications, it is difficult to measure the capacitor current i_C, which can be obtained from the discrete-time derivative of the capacitor voltage.

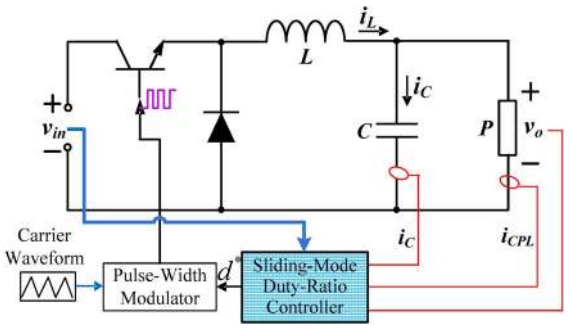

Fig. 4. Schematic of the buck converter with a constant power load controlled by the proposed SMDC.

E. SMDC Parameter Selection and Transient Performance

The three coefficients in (13) will affect the dynamic response and reaching time of the controller. Rewrite (13) as

$$\dot{e}_v + \frac{a_2}{a_1}e_v + \frac{a_3}{a_1}\int e_v dt = 0 \tag{31}$$

which is a typical second-order linear differential equation. To ensure system stability, (28) should be always satisfied.

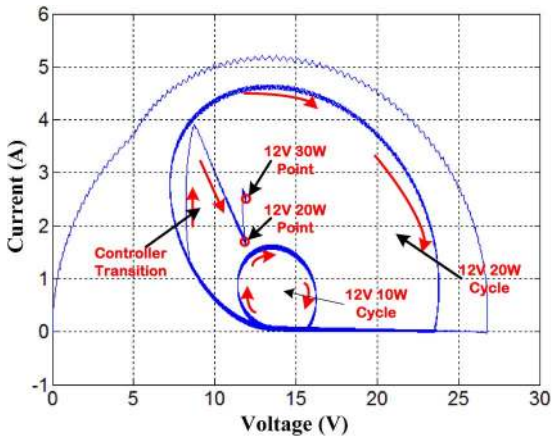

Fig. 5. SMDC with underdamped response.

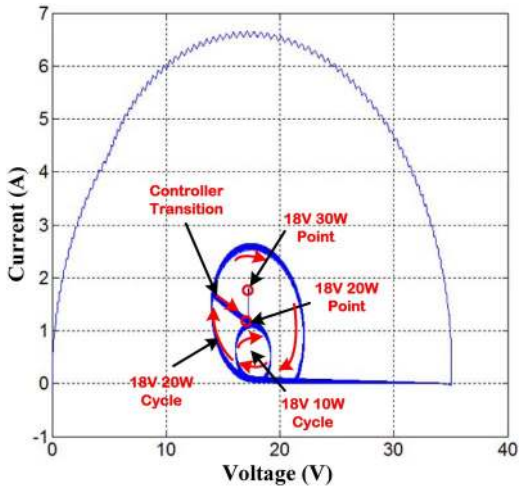

Fig. 6. SMDC with critically damped response.

Then, according to the standard second-order linear system equation, $\ddot{x} + 2\varsigma\omega_n\dot{x} + \omega_n^2 x = 0$, the parameters of (13) can be expressed as $a_2/a_1 = 2\varsigma\omega_n$ and $a_3/a_1 = \omega_n^2$. Define $\omega_n = 2\pi f_{\mathrm{BW}}$, where f_{BW} is the bandwidth and is commonly selected between 1/10 and 1/5 of the switching frequency. There are several choices for the damping ratio ξ according to different types of response: underdamped $(0 \le \xi < 1)$, critically damped $(\xi = 1)$, and overdamped $(\xi > 1)$. Figs. 5 and 6 show the transient performance of the SMDC with the underdamped and critically damped responses, respectively.

At first, a constant duty ratio is used for the buck converter with a constant power load. The limit circles in Fig. 5 clearly show that the system is unstable at any power levels (e.g., 10 W/12 V and 20 W/12 V), where both current and voltage have large oscillations. When the proposed SMDC is added, the phase trajectory approaches to a stable operating point with an underdamped response, which however will experience a relatively long reaching time during the transient stage. As a comparison, Fig. 6 shows the SMDC with a critically damped response, where the phase trajectory leaves the limit circle and settles down to a new stable operating point directly. For both Figs. 5 and 6, the system is always stable under load changes when using the proposed SMDC. However, the transient performance in Fig. 6 is better than that in Fig. 5. This suggests that a critically damped response should be used.

TABLE I
PARAMETERS OF THE DC/DC BUCK CONVERTER

v_{in}	P	C	L	f
200/400/600/800 V	50/250/660 W	0.1 mF	0.18 mH	50 kHz

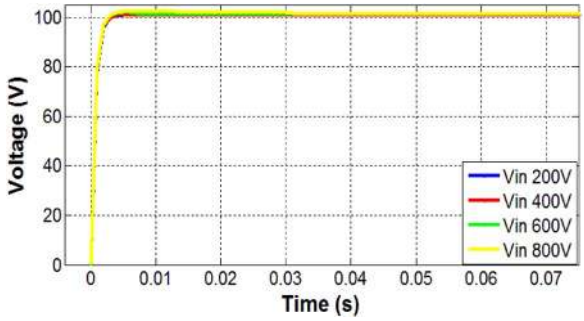

Fig. 7. Output voltage responses of the buck converter controlled by the proposed SMDC.

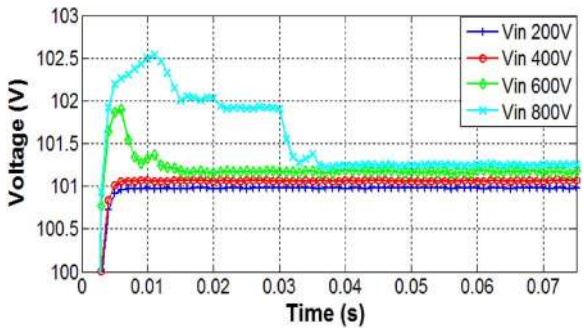

Fig. 8. Output voltage details of the buck converter controlled by the proposed SMDC.

V. SIMULATION RESULTS

Simulations are carried out in MATLAB/Simulink to validate the proposed SMDC for a buck converter with a constant power load. The parameters of the buck converter are shown in Table I. The input voltage of the buck converter is step changed from 0 V to the values in Table I to demonstrate the effectiveness of the SMDC for different input voltage conditions. The output voltage responses are shown in Fig. 7. It shows that the variations of the input voltage have little impact on the output voltage by using the SMDC. After zooming in the output voltage responses around 100 V, Fig. 8 shows that the output voltage has a small overshoot (less than 2 V) when the input voltage is 600 and 800 V, which however does not appear when the input voltage is 200 or 400 V. The small overshoots at high voltage levels can be reduced by increasing the sampling rates of the capacitor and load currents. In this application, the small overshoots in Fig. 8 are acceptable.

To demonstrate the effectiveness of the SMDC for different constant load power conditions, the output power of the converter is step changed from 50 to 250 W at 0.04 s and from 250 to 660 W at 0.08 s, as shown in Fig. 9, whereas the input voltage is kept constant at 400 V. Fig. 10 shows the output voltage

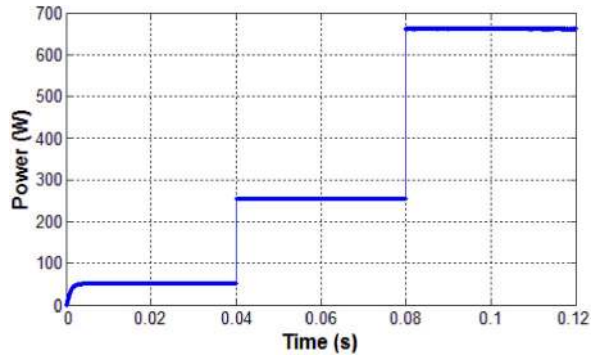

Fig. 9. Step changes in the output power of the buck converter.

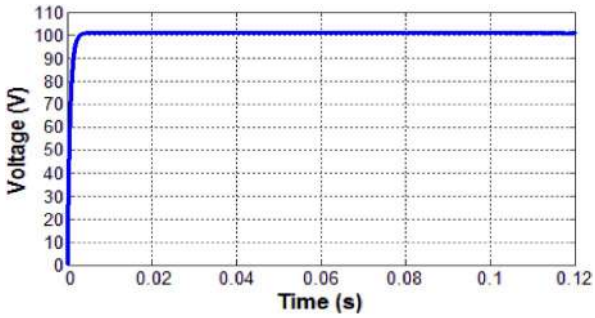

Fig. 10. Output voltage response of the buck converter controlled by the SMDC during step changes in the output power.

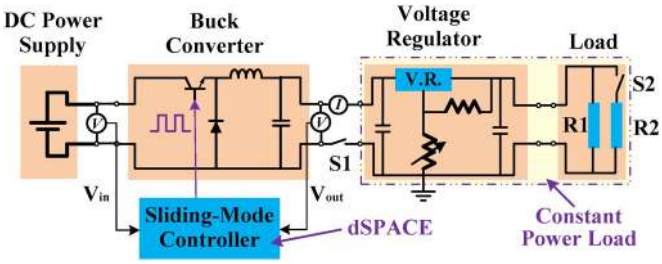

Fig. 11. Block diagram of the test circuits.

response, which is well controlled to be constant at 101 V by the SMDC during the step changes of the output power.

VI. Experimental Results

A. Experimental Setup

Experimental studies are performed to further validate the effectiveness of the proposed SMDC for a buck converter with constant power loads. The block diagram of the test circuits is shown in Fig. 11 and the experimental setup is shown in Fig. 12. The input terminal of the buck converter is connected to a dc source. The converter supplies power to a resistive load through a voltage regulator (VR) circuit. The output voltage of the VR circuit is maintained at 12 V. If the load resistance is not changed, the power flowing into the VR circuit is a constant value. Therefore, the VR and load resistance act as a constant power load for the buck converter.

A conventional PID controller is also designed for 15 V/5 W load condition (the equivalent resistance of the constant power load is $15^2/5 = 45\ \Omega$) to show the superiority of the SMDC.

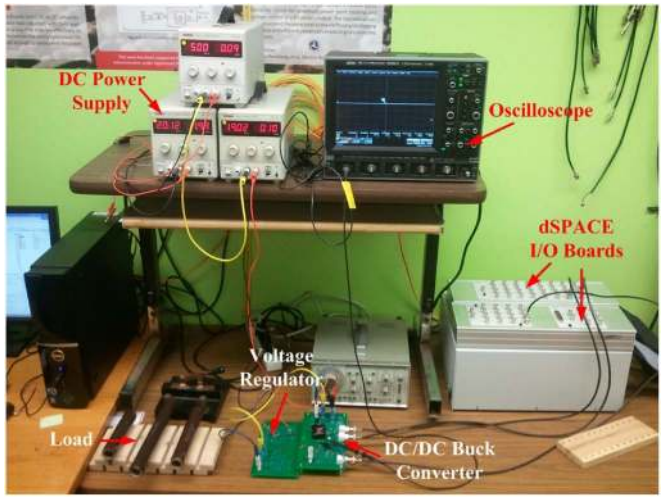

Fig. 12. Experiment setup.

The PID controller has two control modes, namely, a power control mode and a voltage control mode. In the power control mode, the PID controller is designed to control the power output of the buck converter to match the desired power of the constant power load, whereas in the voltage control mode, the PID controller maintains the output voltage of the buck converter at the reference value and stabilizes the system under load changes by appropriately controlling the duty ratio of the power switch in the converter.

To implement the linear PID controller, an equivalent resistance calculated from the desired power and voltage levels of the load is used to linearize the model (2) of the buck converter with a constant power load. By using classical frequency response techniques, a Bode plot is generated for the small-signal model of the converter; the PID controller is then designed by adjusting the Bode plot to obtain the desired loop gain and phase margin for the close-loop system. This design procedure ensures small-signal stability of the system around the designed operating point but cannot stabilize the system when the load significantly changes. In the power control mode, the output current and voltage of the buck converter are measured to calculate the power, which is used as the input for the PID controller and compared with a reference power value to generate an error signal. While in the voltage control mode, only the output voltage of the converter is used as a feedback signal. The output of the PID controller is the desired duty ratio, which is then used for PWM control of the converter. Both the PID controller and the proposed SMDC are implemented in a dSPACE system.

B. Experimental Results

The following experiments are designed to compare the performance of the PID controller and the proposed SMDC during load changes. Initially, both switches S1 and S2 are open such that the buck converter is operated at the no-load condition. Then, S1 is closed so that the buck converter supplies constant power to the load resistance R1. After this, S2 is closed so that another resistance R2 is added to the load and the constant power supplied to the load from the buck converter increases.

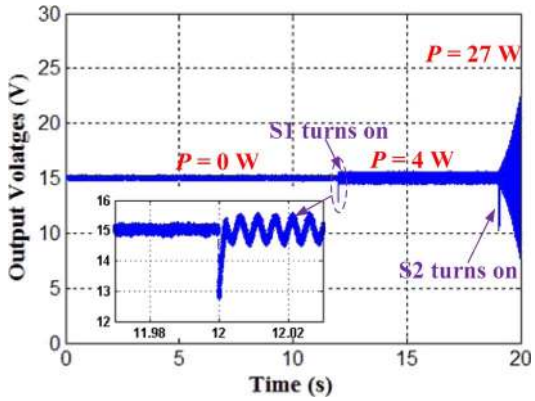

Fig. 13. Output voltage response of the buck converter controlled by a PID controller in the voltage control mode during load changes.

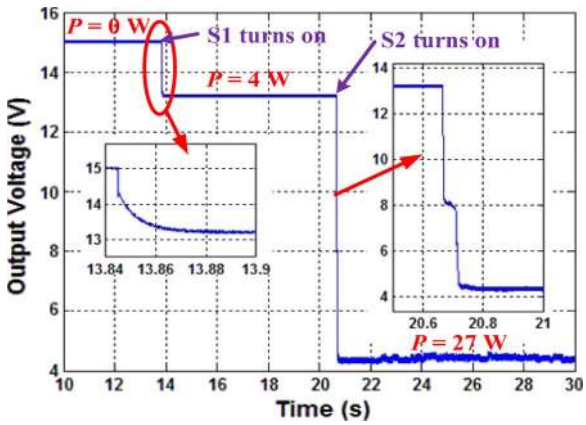

Fig. 14. Output voltage response of the buck converter controlled by a PID controller in the power control mode during load changes.

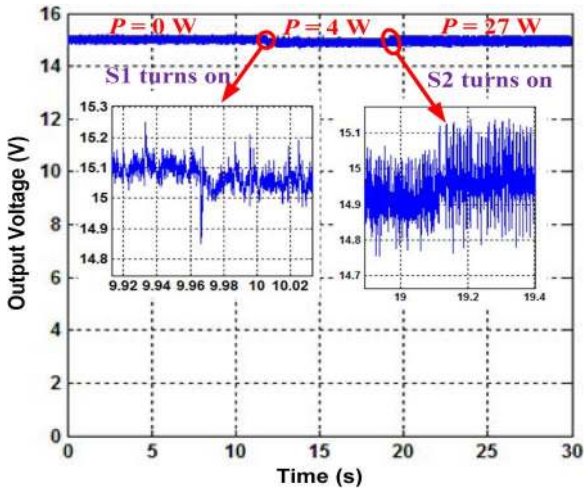

Fig. 15. Output voltage response of the buck converter controlled by the proposed SMDC during load changes.

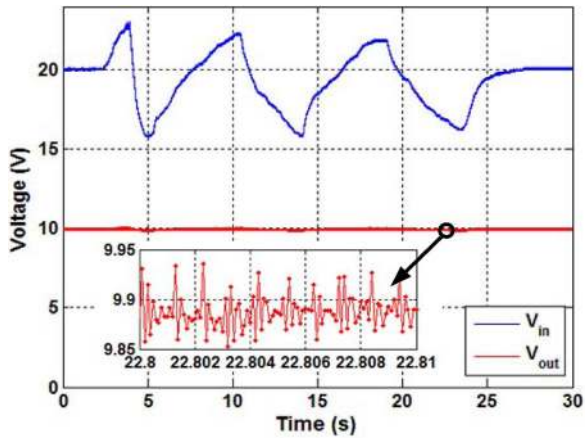

Fig. 16. Output voltage profile of the buck converter controlled by the proposed SMDC when the input voltage changes.

The values of R1 and R2 are 39 and 6.3 Ω, respectively. To initialize the experiments from open circuit for the PID controller, when S1 and S2 are open and power is 0 W, the PID controller first works in the voltage control mode to regulate the output voltage of the buck converter at 15 V. When the output current of the converter becomes larger than a margin of 2 mA (assume open circuit when the output current is smaller than this margin), the PID controller can be switched to the power control mode. The reference voltage for the SMDC in (19) is always 15 V.

Fig. 13 shows the output voltage responses of the buck converter with the PID controller operated in the voltage control mode. In the no-load condition, the output voltage of the converter is maintained at 15 V with the ripple less than 2%. When S1 is closed, a 4-W constant power load is added to the circuit. A 2-V output voltage dip is observed when the load has the step change. The controller regulates the output voltage back to 15 V. However, an oscillation with the peak–peak amplitude of 0.8 V around the operating point is observed in the output voltage waveform. When S2 turns on, the output voltage has a larger oscillation, and the magnitude of oscillation quickly diverges; the system loses stability under this large step load change.

Fig. 14 shows the output voltage responses of the buck converter with the PID controller operated in the power control mode. At the no-load condition (i.e., $P = 0$), the PID controller works well to maintain the output voltage of the buck converter at 15 V. When S1 is closed, the buck converter supplies a constant power value of 4 W to load R1; however, the output voltage of the converter drops to 13.25 V and cannot be maintained at 15 V by the PID controller. The system works at a wrong operating point, although no instability is observed. In this condition, the theoretical output voltage of the buck converter is $\sqrt{(45\ \Omega)(4\ \mathrm{W})} = 13.42$ V, which is close to the experimental result. Moreover, when S2 is closed, the buck converter supplies a constant power value of 27 W to loads R1 and R2. However, the output voltage of the converter drops to 4.5 V and cannot be regulated back to 15 V by the PID controller. During the experiment, the output current of the buck converter is limited to 6 A to protect the circuit from overcurrent. Without setting this current limit, the output voltage of the converter will drop to zero with a large current, which will burn the circuit. This result indicates that the PID controller cannot stabilize the voltage of the buck converter under a large load change.

Fig. 15 shows the output voltage responses of the buck converter with the SMDC for the same load change tests. When the load power is step changed from 0 to 4 W and from 4 to 27 W, the SMDC controls the output voltage of the buck converter correctly at 15 V; no voltage transient is observed in the voltage

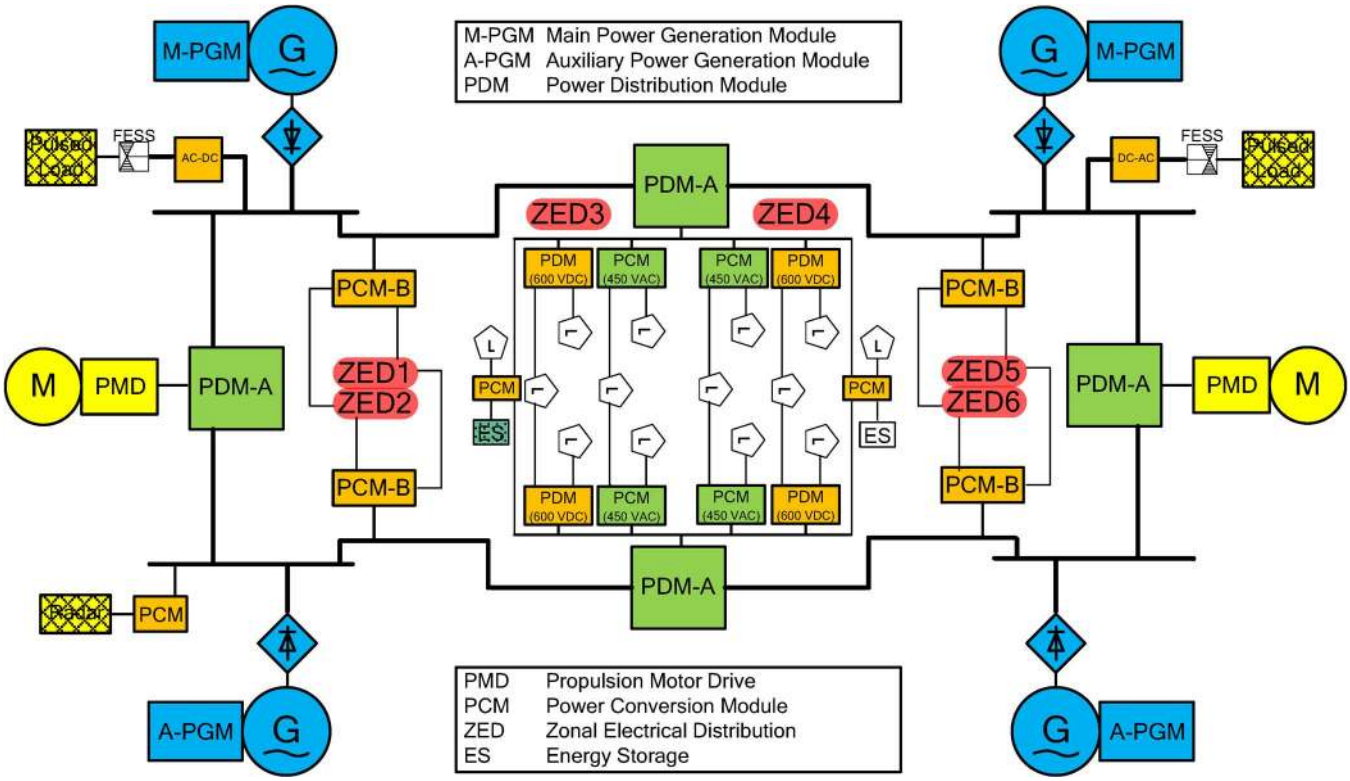

Fig. 17. Typical shipboard MVDC system with dc-ZED modules behaving as constant power loads.

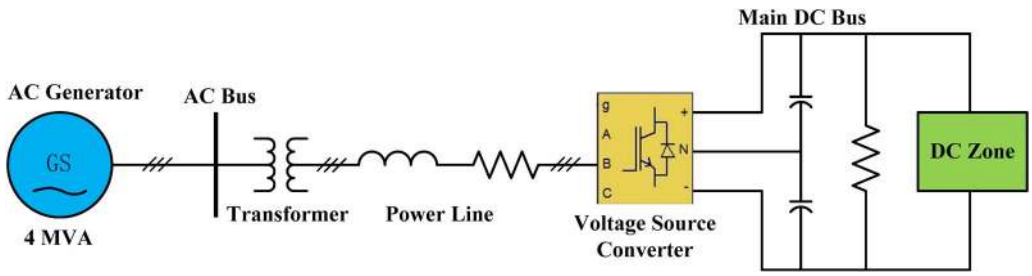

Fig. 18. One-generator MVDC system having a constant power load.

waveform during the step changes in the load. This result agrees with the simulation results in the previous section and shows that the proposed SMDC is robust to load variations, which however cannot be achieved by traditional linear controllers.

In another experiment, the effect of input voltage variations on the performance of the SMDC is evaluated. During the experiment, the source voltage is changed continuously around 20 V, as shown in Fig. 16, where S1 is closed and S2 is open. The output voltage of the buck converter is shown in Fig. 16 as well, which is maintained at 10 V by the SMDC, and the voltage ripple is smaller than 1%. This result verifies that the proposed SMDC is robust to input voltage variations when supplying a constant power load.

VII. MVDC Shipboard Power System With Constant Power Loads

Fig. 17 shows a typical MVDC shipboard power system based on the national MVDC architecture in [1] and [2]. Two main power generation modules (M-PGMs) of 36 MW each are mainly used to supply power to the two propulsion motor drives. The two auxiliary power generation modules (A-PGM) are used to satisfy other electrical demand of the system. The four generators are connected to the main dc bus through voltage source converters (VSCs), which are operated coordinately to maintain the voltage of the main dc bus and share the load demand among the four generators. The operation of this MVDC system is similar to that of the multiterminal HVDC systems described in [15].

The power distribution grid of the system adopts the ZED topology. These dc zones are connected to the main dc bus through power conversion modules (PCMs) and power distribution modules (PDMs). The dc voltage quality and stability are critical to the sensitive loads in the shipboard power system, especially when load shedding happens. The PCMs convert the main dc bus voltage to appropriate dc or ac voltages required by the loads in each zone. These dc and ac zones can be viewed as constant power loads from the input terminals of the corresponding PCMs and PDMs. The proposed SMDC is used to control the dc/dc converters of these PCMs.

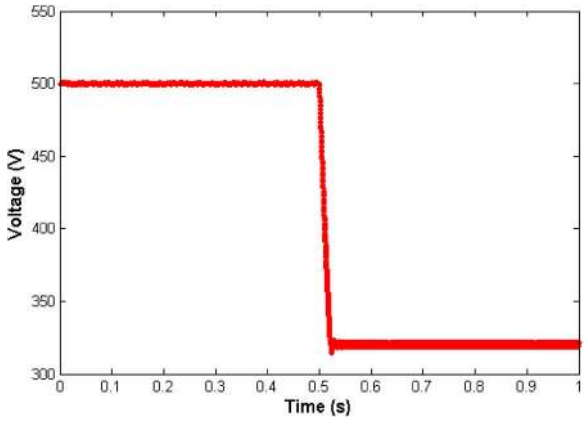

Fig. 19. Voltage profile at the main dc bus.

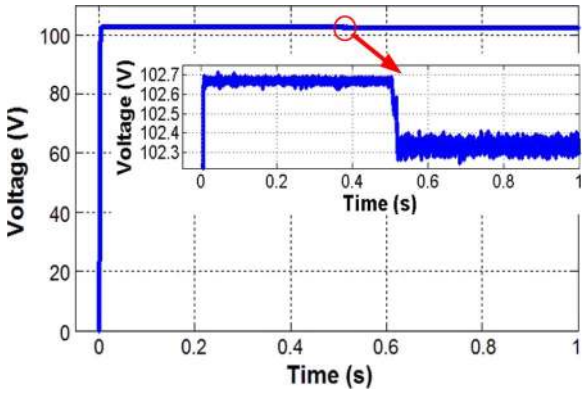

Fig. 20. Load voltage response.

A. Testing System Description

Fig. 18 illustrates a one-generator MVDC system having a dc zone behaving as a constant power load, which is a part of the system in Fig. 17. The dc zone is modeled by two buck converters connected in series with a constant power load, as shown in Fig. 1. The source-side buck converter is connected directly to the 500-V main dc bus (i.e., the dc terminal of the VSC), working as a VR to maintain the input voltage of the load-side buck converter at the desired level. The load-side buck converter is controlled by the proposed SMDC to supply constant power to the load. The generator is fed to the main dc bus through a three-level ac/dc PWM IGBT converter, which has the power rating of 500 kW. The ac/dc PWM converter is controlled by PI regulators to maintain a constant voltage for the main dc bus and a unity power factor for the generator.

B. Simulation Results

Simulations are carried out in MATLAB/Simulink to validate the proposed SMDC for controlling the load-side buck converter with the constant power load. In the simulation, the main dc bus voltage drops from 500 to 320 V at 0.5 s, as shown in Fig. 19. Fig. 20 shows that the load voltage only slightly changes from 102.6 to 102.3 V. Fig. 21 shows the power consumed by the load, which is a constant of 208 kW. The main dc bus voltage drop has almost no impact on the output power of the load-side buck converter. These results clearly show that

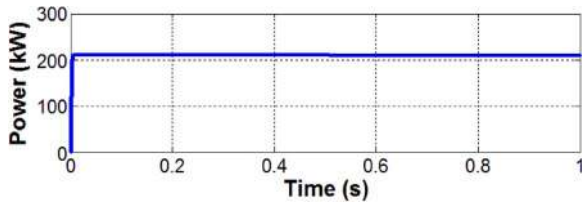

Fig. 21. Load power response.

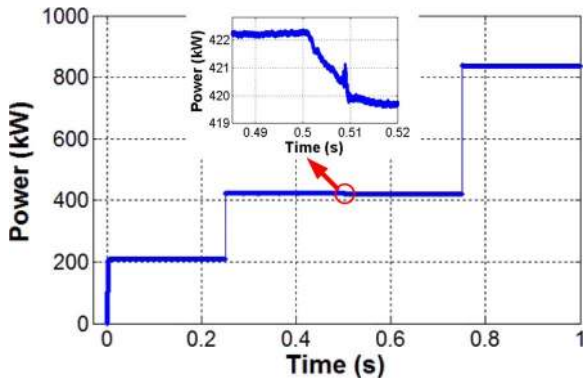

Fig. 22. Step changes in the load power while the main dc bus voltage drops at 0.5 s.

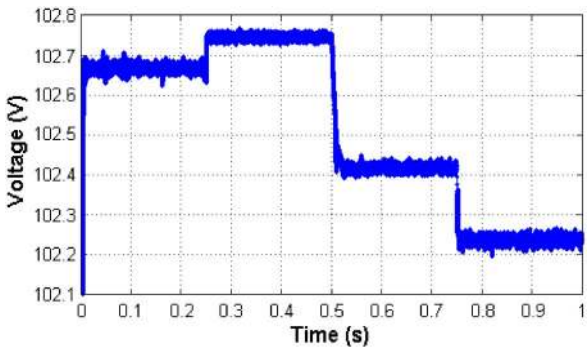

Fig. 23. Load voltage response during step changes in the load power.

the proposed SMDC successfully control the load-side buck converter to adapt to the large disturbance in the main dc bus.

In the second test, the load power is step changed from approximately 210 to 420 kW at 0.25 s and from 420–840 kW at 0.75 s, as shown in Fig. 22. In addition, the main dc bus voltage drops from 500 to 320 V at 0.5 s, which causes the load power to drop slightly from 422 to 420 kW. Fig. 23 shows that load power variations have little impact on the output voltage. The steady-state load voltage variation is less than 0.3 V. These results clearly show that the proposed SMDC successfully control the load-side buck converter to adapt to the large disturbance in the load power.

VIII. Conclusion

This paper has analyzed a negative incremental impedance-induced instability of a dc/dc buck converter with constant power loads. Such power electronic systems cannot be stabilized by using conventional linear controllers. To solve this problem, this paper has proposed an SMDC to stabilize dc/dc buck converters with constant power loads. Simulation studies

have been carried out in MATLAB/Simulink to validate the SMDC for stabilizing a dc/dc buck converter, as well as an MVDC shipboard power system with constant power loads. Experimental results on a practical buck converter with constant power loads have been provided to further validate the proposed SMDC. Results have shown that the SMDC is capable of stabilizing the dc power systems under significant load power and supply voltage variations. However, this performance cannot be achieved by using traditional PI or PID controllers.

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