A Smart IGBT Gate Driver IC with Temperature Compensated Collector Current Sensing

by

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Abstract

Precision current measurement is a critical function that must be incorporated into modern high voltage and high current power systems. Conventional IGBT current sensing methods usually employ discrete sensors such as lossy shunt resistors and involve accessing the high voltage collector load of the IGBT. This would normally present difficulties for integration. In this thesis, an IGBT collector current sensing technique which only utilizes the low voltage signal at the gate terminal is presented. This technique is based on the unique Miller plateau relationship between the gate current and collector current (I_G and I_C) for a particular gate resistance (R_G), and allows for a cycle by cycle measurement of I_C during both turn-on and turn-off transients. This technique is theoretically verified, experimentally demonstrated and integrated into an IGBT gate driver IC. The presented gate driver IC has a highly configurable gate driver, an on-chip CPU for local data processing and an integrated current sensor. This IC is prototyped using TSMC 0.18µm BCD Gen-2 process. A polynomial curve fitting is implemented by the on-chip CPU to predict I_C based on the digitized I_G value. Measurements using a double pulse test setup at room temperature show that an accuracy of ±1 A could be

ensured with a 2nd order polynomial curve fitting, within the current range between 1 to 30 A for turn-on and 1 to 50 A for turn-off. After the temperature effect is analyzed and factored in, a 3rd order polynomial curve fitting is implemented, an estimated accuracy of ±0.5 A could be achieved within the current range of 1 to 30 A for turn-on and 1 to 50 A for turn-off from 25 to 75 ^{o}C.

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List of Glossary

IGBT:	Insulated Gate Bipolar Transistor
IPM:	Intelligent Power Module
FWD:	Freewheeling Diode
SMD:	Surface Mounted Device
EMI:	Electro Magnetic Interference
ADC:	Analog to Digital Converter
DAC:	Digital to Analog Converter
DSM:	Delta Sigma Modulator
CMFB:	Common Mode Feedback
SNDR:	Signal to Noise and Distortion Ratio
S/H:	Sample and Hold
SC:	Switched Capacitor
PCB:	Printed Circuit Board
LDO:	Low Dropout Regulators
CIC:	Cascaded Integrator-Comb
IoT:	Internet of Things
AI:	Artificial Intelligence

Chapter 1

Introduction

Power semiconductor switches are essential components in all modern power electronic systems which determine the performance, efficiency, size, and the cost of the electronic systems. Recently, wide bandgap power devices have attracted significant attentions due to their superior device characteristics. However, these devices are still in early generations of development and they are intended to replace Si devices in very high voltage, high frequency and high power applications. Therefore, Si based power MOSFETs and Insulated Gate Bipolar Transistors (IGBTs) remain dominant in the landscape from low to medium power conversion applications. As the silicon device technology evolves to a highly mature state, their performance is already approaching the physical limits. In order to further exploit silicon power devices, much effort has been put into the design of smart gate driver ICs to optimize the overall system performance. In the past decades, various gate drive circuits have been proposed and discussed, with more and more functions incorporated into the gate driver to make them 'smart'.

Meanwhile, precision current measurement is a critical function that must be incorporated into modern high voltage and high current power systems. Accurate measurement of current flow in power switches such as power MOSFETs and IGBTS is necessary for output regulation and for safety purposes. However, conventional current sensing methods for power switches using resistive sensors consume more power, increase discrete components count and involve accessing the high voltage load side; posing difficulties for integration into gate driver ICs.

This thesis focuses on developing a new collector current sensing method for IGBTs and integrating this technique into a smart gate driver IC. In Chapter 1, a brief introduction to IGBTs, smart gate ICs and conventional IGBT collector current sensing methods is provided. This is followed by an overview of the research work. Chapter 2 introduces the proposed collector current sensing method for IGBTs. A discrete implementation which demonstrates the ideal is also presented. Chapter 3 describes the gate driver IC design details with the integrated current sensor. Chapter 4 discusses the experimental setup and measurements results. Conclusions and suggestions for future work are given in Chapter 5.

In this introductory chapter, the fundamentals on IGBT device structures and applications are reviewed in Section 1.1. The design trend in smart gate driver ICs for IGBTs is analyzed in Section 1.2. The conventional collector current sensing methods for IGBTs and their disadvantages are presented in Section 1.3. An overview of the research work conducted in this thesis are summarised in Section 1.4.

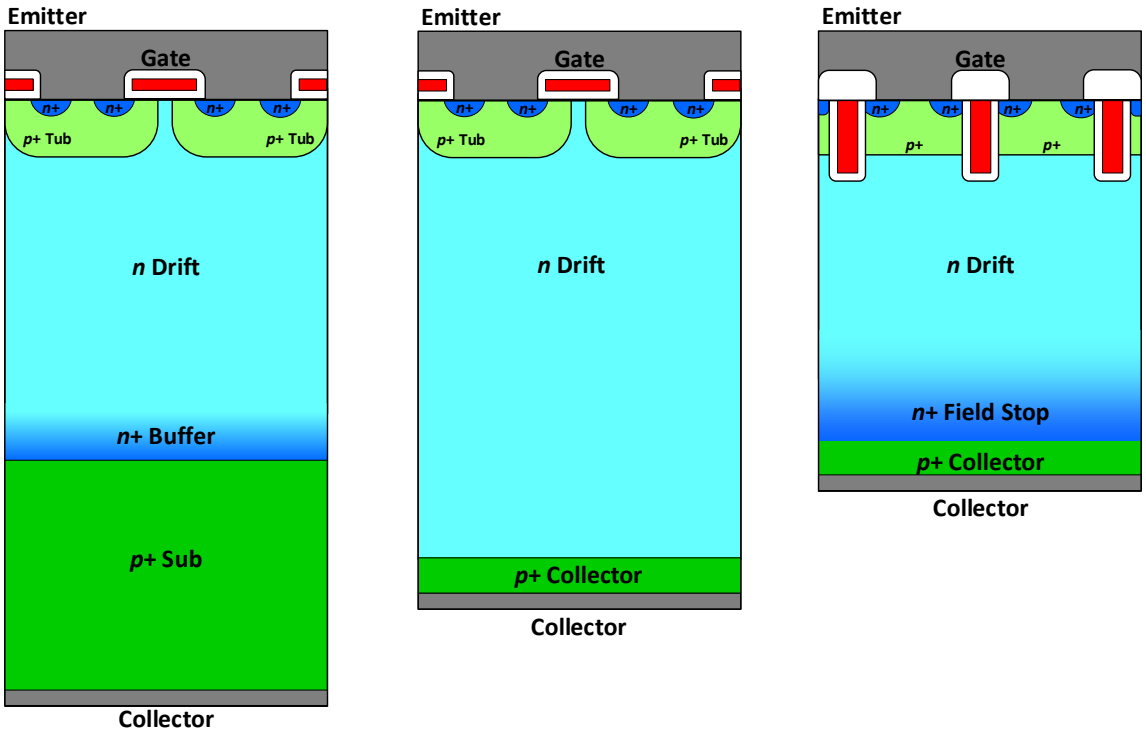
1.1. IGBT Devices and Applications

IGBT is widely used in a variety of power switching applications due to its superior electrical characteristics. It is basically a merged MOSFET-bipolar power transistor, synergizing the high-input impedance MOS-gate control with high bipolar current conduction. The size and complexity of the controlling circuitry is reduced compared to the power bipolar transistors, hence the overall system size and cost are reduced as well [1, 2].

1.1.1. IGBT Device Structures

Ever since the IGBT concept was discovered and developed in the early 1980s, breakthrough technical innovations for IGBT structural optimization have been achieved over the past decades. Basic IGBT structures are derived from replacing the *n*+ drain with a *p*+ layer at the bottom of a vertical power MOSFET. This *p*+ layer is called the injection layer which injects holes into the *n*-drift base region; adding one more

conducting carrier to increase the device current drive capability. Early generations of IGBTs feature planar gate and Punch-Through (PT) type bulk structure, as illustrated in Figure 1.1(a). The PT-IGBT is fabricated by growing the *n*-epitaxial drift layer on a highly-doped *p*+ substrates. This design provides strong hole injection from the collector into the drift region to achieve high conductivity and hence low on-state voltage drop. At the same time, the carrier life time control becomes necessary as the injected minority carriers in the drift region should be removed quickly when device needs to be turned off. However, device performance would be limited in this case since it is hard to optimize carrier profile, on-state voltage, and turn-off speed. In addition, PT structure has poor short circuit capability and is unsuitable for parallel operations due to its negative temperature coefficient [3].



(a) (b) (c)

Figure 1.1: (a) Conventional Planar Gate and Punch-Through IGBT; (b) Planar Gate and Non-Punch-Through IGBT; (c) Trench Gate and Non-Punch-Through IGBT.

The Non-Punch-Through (NPT) IGBT is developed to solve the aforementioned issues, as shown in Figure 1.1(b). The NPT bulk is fabricated using the float zone wafers instead of epitaxial wafers; which results in less crystal defects. The impurity concentration in the

p+ collector is well controlled in order to suppress the carrier injection volume. As a result, no lifetime control is required; and positive temperature coefficient is achieved, facilitating parallel operations for large current capacity applications [2, 3].

The NPT IGBT also has the advantage of higher withstand capability because of the thick *n*-drift region. However, there is a trade-off since the thicker *n*-drift region would reduce the carrier transport efficiency and increase the on-state resistance. The Field Stop (FS) IGBT was introduced to further improve the device characteristics. As shown in Figure 1.1(c), there is an extra high concentration field stop *n*+ layer inserted at the bottom of the *n*-drift region. It serves the purpose of stopping the depletion layer, allowing a thinner wafer to be used for the same high breakdown voltage. With the FS technology, it is possible to reduce the *n*-drift layer thickness of the NPT structure by approximately one third. This translates to less excess carriers and faster switching speed, hence lower switching loss for IGBT at turn-off [3].

Other than the bulk structure evolution, a new gate structure called 'trench gate' has also been developed for IGBTs. As illustrated in Figure 1.1(c), the gate region is formed by etching a trench into the upper surface and locating the gate inside the trench with a liner oxide for isolation from the bulk [4]. When the gate is biased with the proper voltage, a channel is formed along the vertical wall of the trench perpendicular to the surface of the chip. This is different from the conventional planar structure where the channel forms under the gate parallel to the surface of the device. The vertical channel requires less chip area, allows for substantially higher cell density and reduces the on-state voltage drop of the IGBTs [5]. Therefore, FS trench gate structure is widely adopted for modern IGBT designs. Recently more efforts have been carried out to further optimize the trench gate region design, in order to achieve better short circuit ruggedness [6], lower switching loss [7] and better *di/dt* control during IGBT switching transients [8].

1.1.2. IGBT Power Modules

Power Modules were developed to assemble multiple IGBT dies in a single package to provide complex functionality. The modules usually integrate free-wheeling diodes

(FWD) and IGBTs to provide single or multi-phase output stages for motor drive or power conversion applications [9]. Basic IGBT power modules usually do not contain control or protection circuitry inside the modules. They are normally driven by external gate drivers or controller boards [10]. The cross-sectional view of a basic IGBT power module is shown in Figure 1.2. The module has a copper baseplate which provides mechanical support for the module. It also absorbs heat during power transients and then transmits the heat to the heat sink. On top of the baseplate, a Direct Bonded Copper (DCB) substrate is attached and the silicon chips (IGBTs and FWDs) are mounted on the DCB substrate using solder, epoxy or other alloying methods. The DCB substrate provides electrical isolation of the silicon chips from the baseplate and heatsink. Therefore, it needs to withstand high temperatures and with low thermal resistance. In addition, the DCB layer should have similar thermal expansion coefficients to that of silicon to ensure good thermal cycling performance. In this case, the most suitable materials for the DCB layer are ceramics such as alumina (Al_2O_3), aluminum nitride (AlN), and silicon nitride (Si_3N_4) [11, 12].

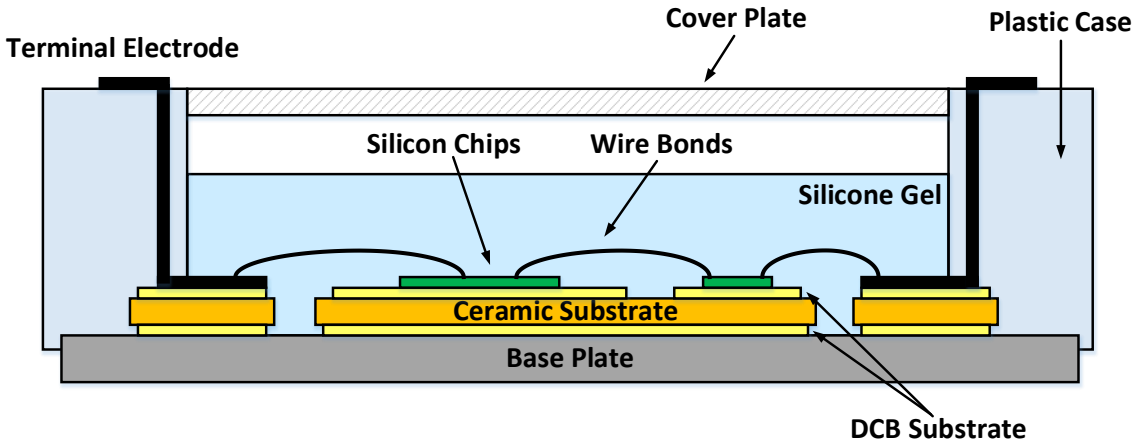


Figure 1.2: Cross-sectional view of a basic IGBT power module.

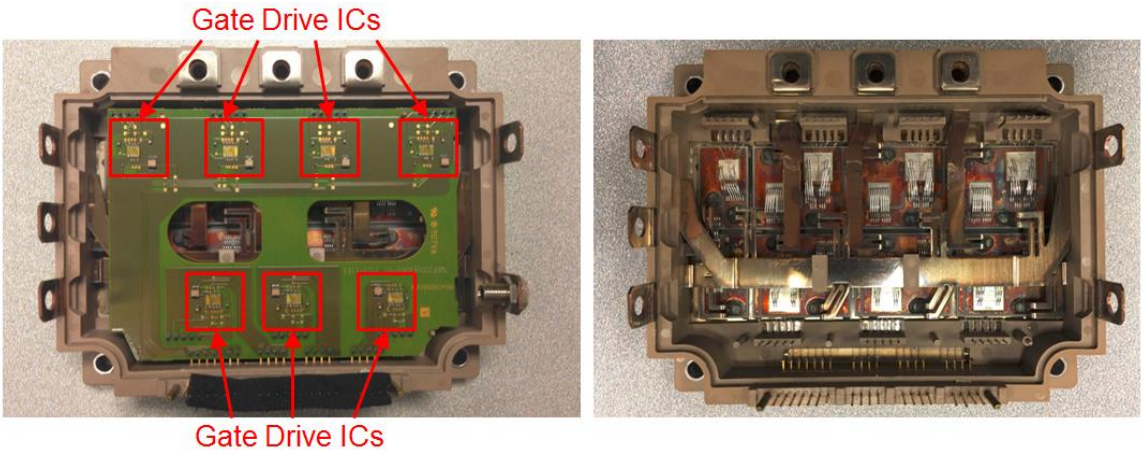
After mounting the substrate and silicon chips onto the baseplate, wire bonding is performed to interconnect the chips and connect them to the electrodes of the module. Aluminum wires are usually used with ultrasonic bonding technology [11]. During the IGBT thermal cycling, the bonded interface between the Al wire and the metalized Si chip top experiences repeatedly stress, leading to potential bonding wire damages such as

bonding lifting and cracking. These types of damages were reported as the dominant failure modes for modern power modules [13].

For the purpose of providing insulation between the Al wires to prevent electric discharge and also protect the silicon chips from moisture corrosion and contamination, a layer of encapsulation such as silicone gels is used to fill the empty spaces between all the interconnects, devices and insulation layers inside the module [14]. Finally, a plastic case/cover provides protection against any mechanical and environmental abuse [11].

1.1.3. Intelligent Power Modules

In order to provide self-protection and load monitoring capability to the IGBTs, the concept of Intelligent Power Module (IPM) was introduced in the late 1980s [15, 16]. IPMs incorporate a dedicated circuit board with control and protection functions to improve their performance and reliability [17, 18].



(a) (b)

Figure 1.3: A Fuji Electric 7MBP200VEA060-50 IPM module. (a) The driver and control circuit board, (b) the IGBTs and FWDs on the bottom.

Figure 1.3 shows an off-the-shelf Fuji Electric IPM Module 7MBP200VEA060-50. The top circuit board serves as an interface between the microcontroller and the IGBTs. It contains the gate driving ICs and the protection circuits to prevent under-voltage, over-current, over-temperature, and short-circuit fault conditions. The bottom of the module are the IGBT and FWD chips with interconnects.

The IGBT chips installed in IPMs have different design requirements compared to those discrete IGBT devices. The most significant one is the short circuit withstand time. The discrete IGBTs are typically used in power inverters and are expected to survive a certain time period (usually around 10μs) in short circuit operation before the protection circuits are triggered. Special design techniques are needed to ensure adequate saturation current during short circuit condition. However these techniques such as regulating the MOS-channel current would usually compromise the on-state voltage drop in the normal operating condition of the IGBT [10]. While for the IGBTs in IPMs; these techniques are no longer necessary because of the fast short circuit protection scheme (usually 2~3μs).

Another important feature of the IGBTs designed for IPMs is the integration of on-chip current and temperature sensor, as illustrated in Figure 1.4. The Sense-FET structure directs a small portion of the total collector current for over current protection. The details of this current sensing method will be discussed in a later section. A simple *pn* diode is placed in the center of the chip to monitor the junction temperature of the IGBT chips [10].

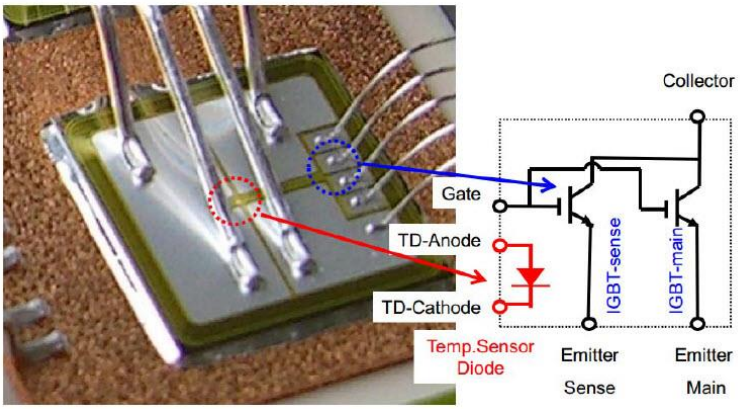


Figure 1.4: Photo and simplified schematic of an IGBT chip for IPMs with on chip current and temperature sensors [10].

The development of IPMs greatly reduces the time-to-market for the products and offers customers with advantages of reduced design efforts, lower manufacturing costs, and also improved system performance and reliability [15]. IPMs are now widely used in many electronic applications.

1.1.4. IGBT Applications

IGBTs have found widespread applications in medium to high power systems. Figure 1.5 illustrates the application spectrum for modern IGBTs. Their characteristics are suitable for applications with operating conditions of 200V and above, e.g. lamp ballasts, consumer appliances, and motor drives, etc. Compared to traditional Si-based IGBTs, SiC IGBTs offer promising characteristics with higher blocking voltages, higher switching frequencies and better thermal reliability. However, due to the lower wafer yield and higher cost, Si IGBTs are still the dominant power devices except for special applications such as smart grid which requires extremely high blocking voltages [1]. The IGBTs discussed in this thesis are limited to Si-based IGBTs.

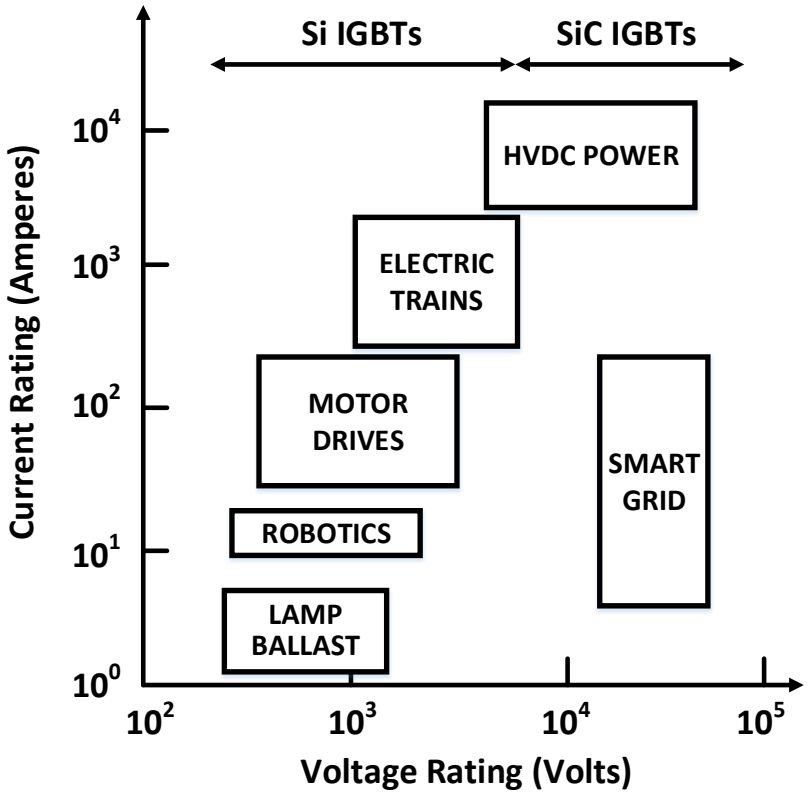


Figure 1.5: Application spectrum for IGBTs [1].

IGBTs play an important role in the modern transportation sector. They are the most cost-effective choice for the switches in power electronic systems. More significantly, the IGBT-based inverters are used in electric and hybrid electric vehicles such as electric

buses, trains, electric trams and trolleys, and subways. The development of IGBT has a great impact on the industrial sector as well. IGBTs are the dominant power switches used in industrial motor drives. For all these applications, IGBTs offer many technical advantages when compared to other power switches including lower component count and power rating for the driver circuit, lower switching loss and steady state on-state loss, better short circuit withstand capability, better performance under parallel configurations and feasibility of higher blocking voltages [19, 20].

IGBTs are also widely used in many modern lighting systems. They enabled the introduction of the Compact Fluorescent Lamp (CFL) because of their high power handling capability and monolithic gate driver which makes the control system more compact. Other applications of IGBTs for lighting include LED drivers, dimmable luminaries and flash tubes used in digital still cameras [21].

In addition to above mentioned applications, IGBTs are extensively used for the control of power delivery in major home appliances used by consumers. These major appliances include air conditioning, heat pump unit, kitchen cooking range, washing machines, microwave, and refrigerator [22]. IGBTs also found numerous applications in the medical sector now as they have taken a critical role in the power delivery for major medical diagnostic tools such as CT scanners, MRI imagers, ultrasound machines, and medical lasers [23].

1.2. Trends in Smart Gate Driver ICs for IGBTs

1.2.1. Gate Drivers for IGBTs

Gate drivers for power semiconductor switches are crucial components in power systems. Investigations on the gate drive circuits for silicon power switches started as early as the devices were introduced [24]. The basic gate drive circuit for IGBT is simple because of its MOS-gate structure. The device can be controlled using relatively low voltage (typically 10-15V), and only transient currents are required to charge and discharge the

MOS-gate which can be delivered using integrated circuits [24]. Common gate driver topology can be categorized into three groups: voltage source gate driver, current source gate driver and resonant source gate driver [25]. Simplified circuits describing these topologies during the charging and discharging intervals are shown in Figure 1.6.

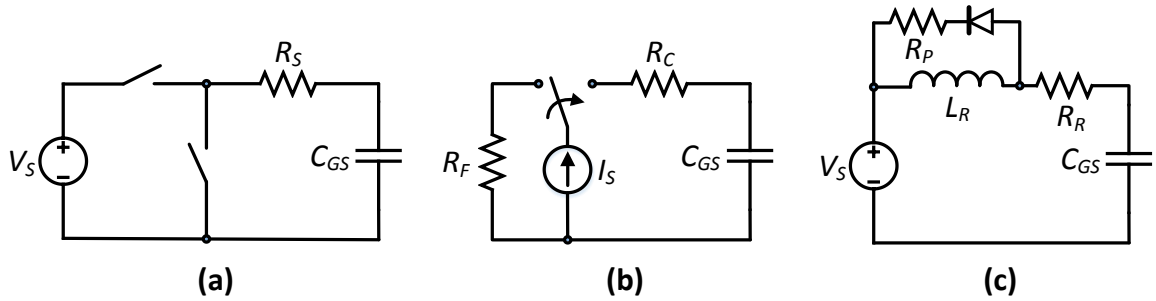


Figure 1.6: Simplified circuit for (a) voltage source, (b) current source and (c) resonant gate driver topologies during charging and discharging intervals [25].

Voltage source topology is the most popular gate driver topology due to its simplicity. This type of driver operates by charging and discharging the input gate capacitance of the IGBT (C_{GS}) with a voltage source through a series resistance R_G. R_G is a critical factor for switching speed control. It is normally chosen based on the value of C_{GS} to make sure that the charging interval is less than 5% of the entire switching period of the IGBT. Larger R_G would inevitably limit the switching speed. However, it would not increase the power consumption of the gate driver. The energy dissipated in R_G during charging process is always equal to the energy stored in C_{GS}, which is given by [25]:

$$E_v = \frac{1}{2} C_{GS} V_S^2 \tag{1.1}$$

Considering the same holds true for the discharging process, the power consumed in R_G for a switching frequency of f_s for the IGBT can be calculated as [26]:

$$P_v = f_S C_{GS} V_S^2 \tag{1.2}$$

Equation (1.2) implies that at higher switching frequency, the gate driver power consumption will become significant enough to affect the efficiency of the system. Therefore, current source gate driver topology as shown in Figure 1.6 (b) is introduced.

These gate drivers operate by charging the gate capacitance with a constant current source, and the charging time is inversely proportional to the charge current I_S. It can be demonstrated that the current source driven gate driver consumes less power than the voltage source gate driver with proper choice of the passive components [25]. However, this type of topology is less commonly used as it requires a high efficiency current source which is more difficult to design. In practical terms, a small inductor is usually implemented as part of the current source. This approach ventures into the resonant driver domain [26].

Figure 1.6(c) presents a simple resonance driven gate driver which is the most popular topology used in high frequency switching applications. In this type of driver, the resonant current charges and discharges the gate capacitance through the resonant inductor. There are two operation modes: full resonance and clamped resonance. Under full resonance condition, the inductor transfers all the energy to the gate capacitance. The turn-on time and the final gate voltage value are determined by the Q-factor. While under clamped resonance condition, the gate voltage will be clamped at a given voltage, the remaining energy in the inductor is then diverted [25]. All the commonly used resonance gate driver circuits are discussed with their advantages and limitations in [27].

In this research work, the IGBT devices under investigation are switching around 20 kHz only. Resonance type gate drivers require inductors which is not desirable for space and cost saving in integrated circuit design. Therefore, the voltage source topology is adopted for this thesis.

1.2.2. Smart Gate Drivers

In the past decades, various gate drive circuits have been proposed and discussed, with more and more functions incorporated into the gate driver to make them ‘smart’. These driving techniques and smart functions can be broadly divided into three categories, as shown in Figure 1.7.

The techniques in the first category are mainly used to optimize the switching behavior of the power devices. For example, active gate driving has been discussed extensively in

literature [28-33], focusing on the turn-on /turn-off voltage and current waveform shaping for the power devices. The ultimate goal is to ensure acceptable compromise between switching speed, switching power loss and electromagnetic interferences (EMI). These are the most important design aspects for smart switching designs. Adaptive driving is an example of such system where closed-loop analog control is used to adjust the *dv*/*dt* and *di*/*dt* characteristics [28-30]. This control technique usually features simple circuit design, high dynamic speed and low power consumption. However, the analog control strategy and analog circuit necessitate major re-design effort for different devices, operating conditions and processing technologies. Another popular trend is to employ intelligent digital control to achieve adaptive slope shaping [31-33]. These types of gate drivers have the key advantage of high flexibility in driving strategies and high configurability for various design parameters such as gate resistance, gate current and drive stages. Some works also combine analog feedback and digital control to achieve intelligent switching [34, 35].

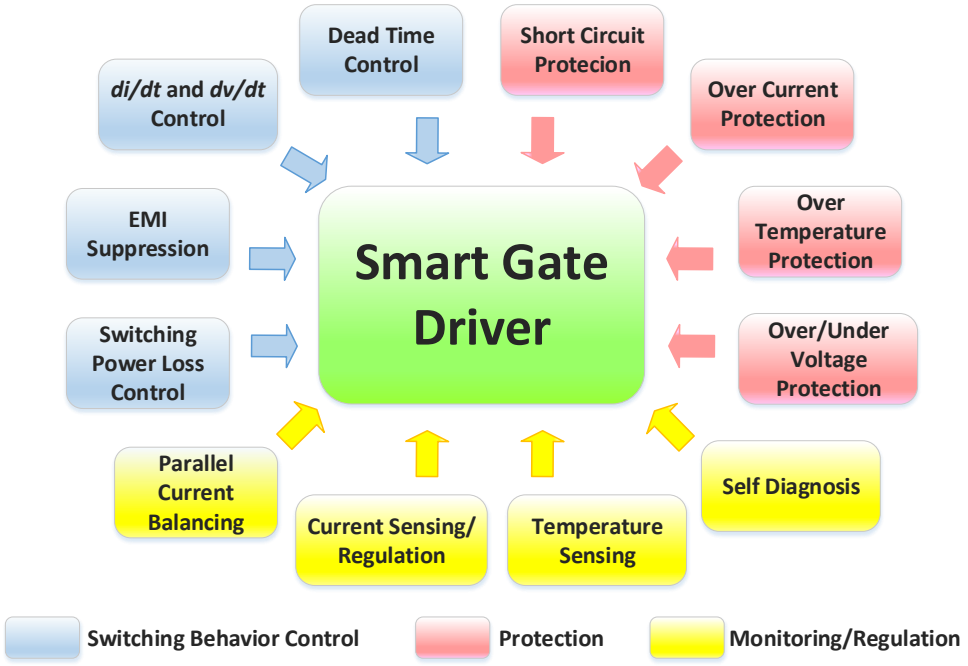


Figure 1.7: Developed features of modern smart gate drivers for power MOSFETs and IGBTs.

In the second category, there are various protection circuits for the power switches, including short circuit protection, over current protection, over temperature protection,

and over/under voltage protection. All of these are compulsory features for device reliability and safe operation. These functions have been well developed in the past decades [36]. Recent effort is to focus on how to make the protection schemes more robust and with faster reaction time [37].

The techniques in the third category are more for monitoring and regulation, such as temperature sensing [38], current sensing [39], current regulation and current balancing in parallel connected topology [40], and self-diagnosis for fault detection [41]. These are popular new features in smart gate drivers to improve functionality, flexibility and reliability.

1.2.3. Integrated Smart Gate Drivers

Modern smart gate drivers integrate all the components into a single package, resulting in a significantly smaller system size and enhanced reliability. The smart gate-driver ICs also simplify the PCB board layout and reduce design uncertainty. Some of the smart functions mentioned in Section 1.2.2 were initially implemented using discrete components and then gradually integrated into the gate driver IC. A generalized block diagram for recent smart gate driver ICs is shown in Figure 1.8.

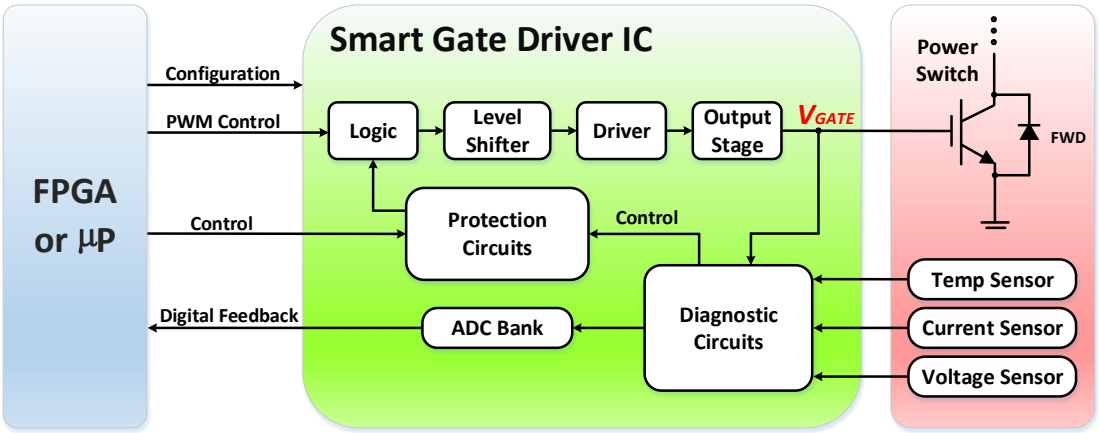


Figure 1.8: Functional block diagram of a generalized smart gate driver IC.

Modern smart gate driver ICs usually rely on an external FPGA or a microprocessor to provide digital control, such as setting all the configurable parameters for the chip and PWM (Pulse Width Modulation) control for the driver. Recently, numerous gate drivers

ICs with digital controlled adaptive driving features were developed. One example is the segmented and programmable gate drivers [42-44]. Segmented drivers are composed of several paralleled output stages to achieve variable output resistance. In order to achieve fast switching speed, a lower gate resistance is needed for large *di*/*dt* and *dv*/*dt* but this results in higher EMI. A larger gate resistance could reduce EMI but increase the switching loss, leading to lower efficiency. The digitally controlled segmented gate driver could dynamically change the gate driver output resistance to suppress the EMI while maintaining similar switching speed and switching loss. Furthermore, multiple changes in the gate resistance during a single turn-on or turn-off transient are possible by appropriately changing the number of active segments in real time. An algorithm was developed in [45] to optimize the segmentation process according to the load current, the operating voltage, the temperature, and other variations in power devices.

Smart gate driver ICs could also process the feedback signals from sensors on the power switches or the load. These signals can be used to trigger certain protection circuits directly. In most designs, the processed signals are digitized by an ADC and fed back to an FPGA or microprocessor. After further processing, the FPGA or microprocessor will trigger the protection circuits or dynamically adjust the driving control signals to realize local regulation. A gate driver IC with integrated short circuit protection function based on a filtered feedback signal is introduced in [46]. A smart driver IC for inductive loads with self-monitoring capability by using the signals from a resistive sensor on the load side is presented [47]. Finally, the concept of integrating the *di*/*dt* and *dv*/*dt* analog feedback into the gate driver IC is described in [35]. This fully integrated closed-loop gate driver could provide digital slope shaping based on the analog feedback signals.

Recently, techniques that utilize the gate signal (gate voltage or gate current) to detect short circuit condition [48-50], to predict device junction temperature [51], to regulate the imbalance of currents in paralleled IGBTs [52] have been proposed. These types of techniques only use the low voltage signal on the gate driver, ensuring the feasibility of low cost integration. As illustrated in Figure 1.8, the diagnostic circuit could process the gate signal directly instead of monitoring the feedback signals from the high voltage load side which poses significant voltage isolation difficulties in monolithic integration.

1.2.4. BCD Process Technology

Whether a certain feature should be integrated is not only dependent on the circuit design, but also on the integration cost. With rapid advancements in semiconductor fabrication technology, the cost of gate-driver ICs is becoming comparable to discrete circuits, making the IC solution even more attractive and feasible for most applications.

Most modern power ICs are fabricated using BCD (Bipolar CMOS DMOS) technology. It typically offers low-voltage transistors (for digital and analog signal processing), high voltage power transistors (for output stage), and also diodes, capacitors and resistors in the same process; with feature size ranges from 0.35 µm to 0.13 µm [53]. A typical cross section shows the BCD technology with a combination of bipolar, CMOS and DMOS devices on the same IC are illustrated in Figure 1.9. Robust isolations between low voltage and high voltage circuitries are required by using deep-trench isolation (DTI) and highly doped deep buried layers. The deep buried layers could shield any disturbances coming from the substrate and prevent any parasitic transistors from turning on, while the DTI technique could ensure great lateral isolation. Compared to previous LOCal Oxidation of Silicon (LOCOS) and Shallow Trench Isolation (STI) techniques, DTI technology offers much better physical isolation with increased area density.

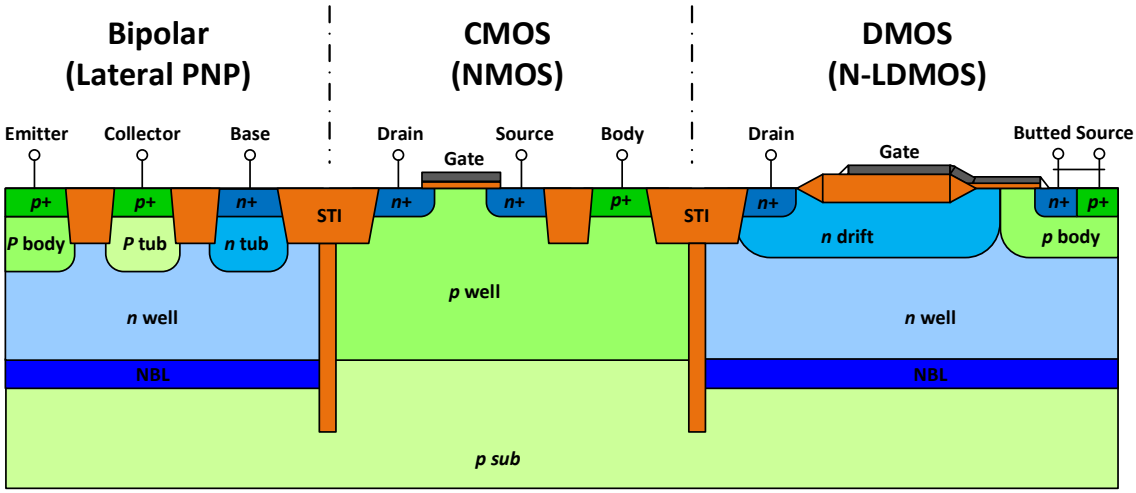


Figure 1.9: Illustration of the BCD IC technology which includes bipolar, CMOS and DMOS devices on the same IC.

Another solution with better isolation capability is to use SOI (Silicon-on-Insulator) BCD [54]. A gate driver IC in SOI technology is presented in [55] which integrates all primary and secondary side driver functions for a three-phase MOSFET power inverter system on a single chip. This is possible because the insulated substrate enables full dielectric isolation for devices operating in different voltage domains. In addition, improved EMC and robustness could be realized by using SOI technology. However, due to the higher cost of the SOI substrate, it is usually only employed in high profit margin applications such as bio-medical and automotive sectors, etc.

1.3. Conventional IC Sensing Methods for IGBTs

Current sensing has always been critical for protection and regulation in modern high voltage and high current power systems. Different current sensing techniques have been reviewed in [56-58]. These current sensors include series/shunt resistors or magnetic/inductive sensors such as Rogowski coils, current transformers and Hall Effect sensors. Efforts have been made to integrate the above-mentioned sensors to various industrial power systems to monitor the output currents [59-61]. A few popular current sensing methods used for IGBTs and IGBT modules will be discussed next.

1.3.1. Current Sensing using Shunt[1] Resistors

For current sensing in IGBT modules, the shunt resistor sensors remain the most popular due to their low cost and small size. As shown in Figure 1.10 (a), a low-value ohmic shunt resistor is inserted between the emitter of the IGBT and ground. The voltage drop across the resistor will be used by another circuit for monitoring and detection [58, 59, 62].

In order to achive fast response time to potential high-impluse and heavy-surge currents, coaxial shunts are usually used [63]. Neverthelss, calibrations are still needed when

[1] Shunt resistor is usually placed in series with the load, and a voltage is generated across the shunt resistor which is proportional to the load current.

integrating them to different switching systems even for coxial shunts with excellent frequency response [64]. For highly compact electronic systems, the bulky coaxial shunt resistors are no longer suitable and Surface-Mounted-Device (SMD) resistors with small physical dimensions are generally used instead. However, the small size of SMD resistors causes the parasitic industance become a major concern as the frequency reponse could be seriously deteriorated. Compensation techniques using filters are sometimes needed to improve the bandwith for SMD shunt resistors [56].

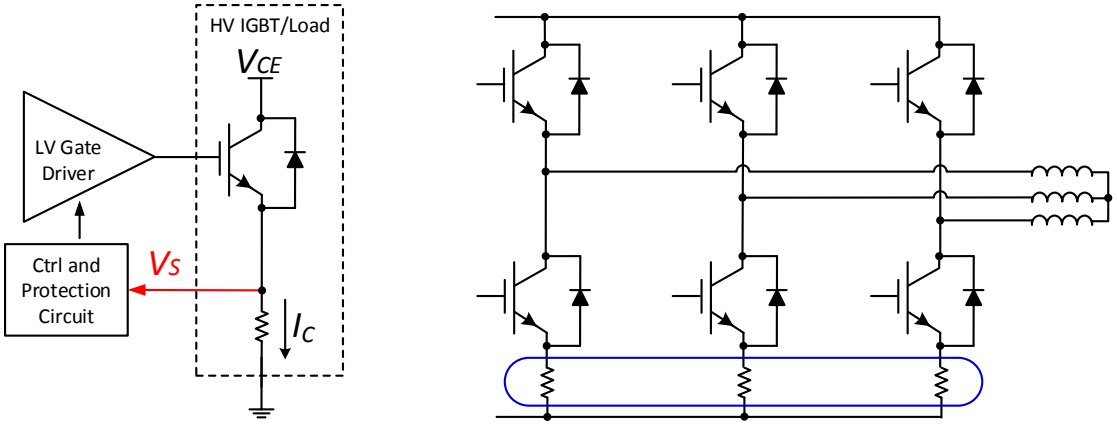


Figure 1.10: (a) Traditional IGBT collector current sensing methods using a shunt resistor (b) shunt resistor current sensing implemented in a 3-phase power inverter.

For either the coaxial shunts or SMD resistors, the resistance values are usually quite small and in the milli-ohm range. The extracted V_S often needs to be amplified to an acceptable level before further processing. The amplifer stage may further limit the bandwith. Morevoer, the induced voltage due to the self-inductance of the shunts and the parasitic inductance of the contact leads may become comparable to the resistive voltage drop [65], causing noises on the measurements.

Another major disadvantage of shunt current sensing is its low efficiency. Considering the fact that IGBTs are usually implemented in high power systems, the power loss across the shunts can be very high when high currents are being switched. Sometimes a heat-sink may even be required; the system cost and size are then increased drastically. In addition, measuring V_S can be difficult as the load side voltage could have a swing of several hundreds of volts.

Figure 1.10 (b) shows the application of shunt current sensing in a 3-phase power inverter. The shunt resistors are placed below the low side switch of each branch for current monitoring. The sampling technique is critical as the phase current passes through the low side switch for only a portion of the fundamental cycle. Special algorithms should be developed and implemented to utilize the available current information effectively, so that the full output phase current waveforms could be reconstructed accurately [66].

In summary, the shunt resistor current sensing has poor accuracy, consumes too much power and provides no measurement isolation from load side. The only reason that they are still widely adopted in low end industrial drives is because of their low cost [59].

1.3.2. Sense-FET Current Sensing

Another common collector current sensing method for IGBTs is to embed a sense structure inside the IGBT chip. This is similar to the sense-FET used in power MOSFETs [67, 68], as illustrated previously in Figure 1.4. The small sense current, I_{Sense} is directly proportional to the main collector current, I_C, and can be measured though a sense resistor. Figure 1.11 illustrates a typical application of using Sense-FET for over current protection.

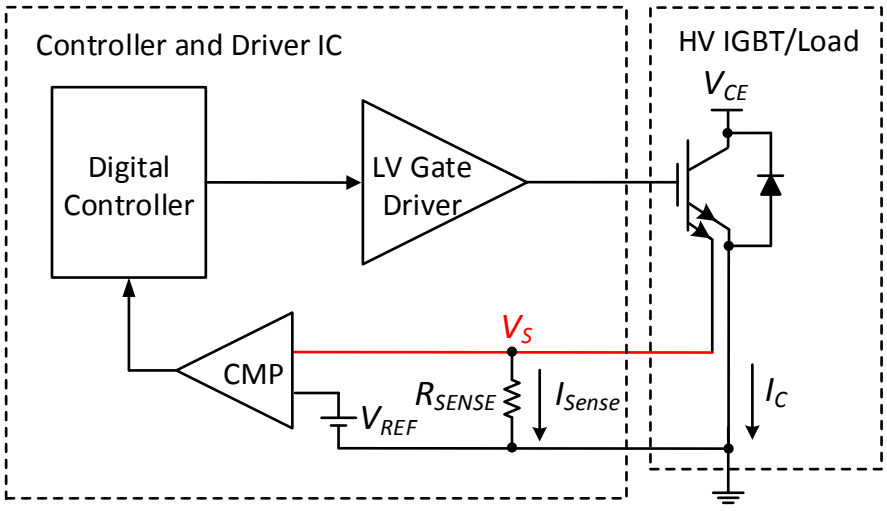


Figure 1.11: Schematic of using a Sense-FET for over current protection.

Due to the unique characteristics of the IGBT, there are three options for the embedded current sensor: 'active current sense', 'MOS current sense' and 'bipolar current sense'. The linearity of these sensors has been studied in [69], and it is found that the active current sensor has the best linearity, while the MOS current sensor has least temperature dependence. Many steps have been taken to improve the accuracy and robustness of these integrated sensors through layout optimization [67, 70-72]. However in practical applications, it is almost impossible to achieve a constant current sensing ratio across all the entire operating condition of the IGBT. For example, the current sense ratio is sensitive to the collector emitter voltage V_{CE}. Even special sensing topology is implemented, the current sensing ratio can exhibit a variation of 5~10% across the normal operating range of V_{CE} [67, 71].

It is also well known that the current sensing ratio has a great dependence on the actual collector current I_C. As illustrated in Figure 1.12, the IGBT usually consists of tens of thousands of small cells connected in parallel, and the sense emitter uses part of these cells [73]. Ideally the current sensing ratio should be equal to the emitter area ratio. In reality, there are parasitic resistors at the emitter ends due to the interconnectors and leads. The values for the sense emitter parasitic resistor RL_{SE} and that for the main emitter RL_E are comparable in this case. Since the current flowing through the main emitter I_C is much greater than the current flowing through the sense emitter I_{Sense}; the voltage drop across the sense device V_{CE_SE} is much less than V_{CE_E} which is the voltage drop across the main IGBT device. When a shunt resistor is inserted to the sense emitter, the voltage drop difference across the parasitic resistors may cancel out to certain extent. Therefore the real current sensing ratio is never just the emitter area ratio. It depends on the parasitic resistance values and the external shunt resistor value; causing considerable and nonlinear variations when the main emitter current level changes [73]. Therefore, in practical applications, it is compulsory to measure the current sensing ratio under actual use conditions to determine the correct overcurrent limit.

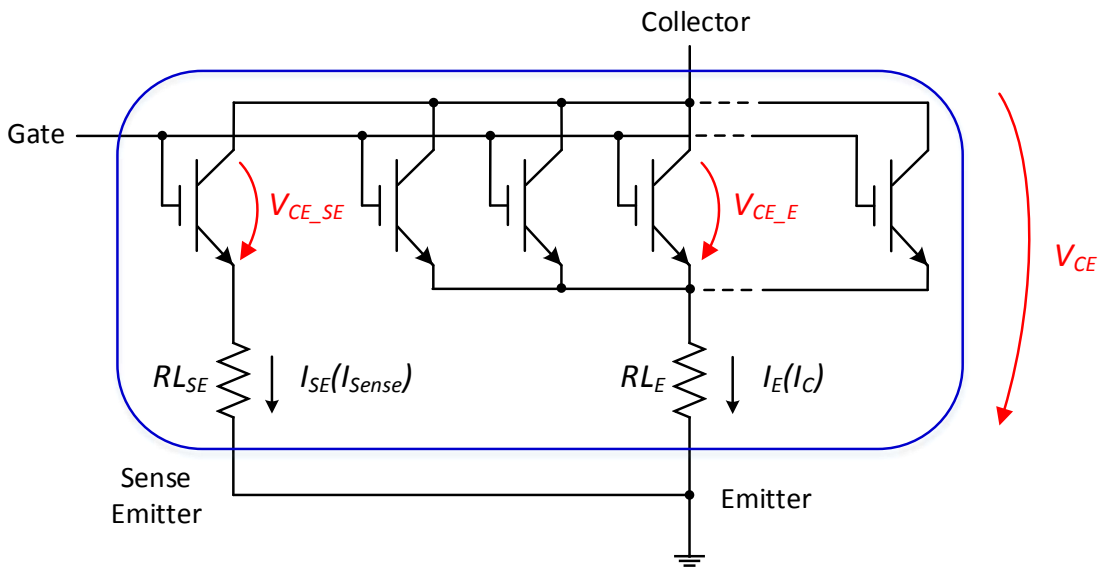


Figure 1.12: Schematic explaining the effect of residue resistance exerting on the current sensing ratio variation [73].

Another major drawback of the Sense-FET current sensing is the current overshoot problem when turning on the IGBT device. During the turn-on transient of the IGBT, there is normally a large overshoot in I_C due to the diode drawing reverse recovery current from the dc supply [74]. Excessive ringing on I_C can also be observed during turn-on when the gate drive resistance is small and the turn-on process is exceedingly fast, causing undesirable EMI (Electro Magnetic Interference) [43]. Consequently, the sense current I_{Sense} would also exhibit large over shoot and ringing. This could falsely trigger the over current protection circuity. Therefore, a blanking circuit is normally required for the protection circuit to have a blocking period during the turn-on transient to avoid any false triggering. However, the blanking circuit is not desirable and possibly harmful if a real short circuit condition happens during the blocking time.

Other than the above mentioned disadvantages, the Sense-FET current sensing ratio also has large dependence on the IGBT junction temperature [67, 72, 73]. This is attributed to the physical structure and location of the Sense-FET on the IGBT chip. Normally the Sense-FETs are placed at the side the chip while the temperature sensor is placed in the middle of the chip. Thus the average temperature of the Sense-FET is usually different from that the main emitter cells.

In addition, the sense resistor must be sufficiently small to keep the potential at the sense electrode to be less than 50mV. As a result, the sensing circuit has poor noise immunity [36]. Therefore, this current sensing method is widely adopted in IPMs for short circuit protection only as it lacks the accuracy required for current regulation.

1.3.3. Other Current Sensing Methods

Another IGBT current sensing technique is inspired by the MOSFET current sensing method using the $R_{DS}(on)$. It assumes the MOSFET acts like a resistor when it is turned on, and the drain current can be deduced by measuring the voltage drop across the MOSFET [75]. International Rectifier extended this application to IGBT current measurement through measuring the $V_{CE}(on)$ of the IGBT [76]. The accuracy of this technique depends on the tolerance of the on-resistance of the IGBT. Blanking circuit or filters are needed to prevent the noisy spikes from false triggering the protection circuits. Temperature effects are yet to be compensated. Moreover, this approach involves a HVFET which connects directly to the switching node for V_{CE} sensing; therefore, an expensive discrete component is necessary.

All the above mentioned current sensing techniques are based on resistive sensing and involving touching the high voltage power switch or load side which may cause safety concerns. For this reason, current sensors which are based on in-direct sensing and provide inherent electrical isolation are normally more attractive for applications where isolation is required [56]. For example, the Hall Effect sensor, Rogowski coils and Current Transformers are widely used in power electronic systems for current sensing.

Hall Effect sensor is a popular magnetic field sensor. It predicts the current level by sensing a voltage caused by the magnetic field. Therefore, it is non-intrusive and power efficient. It can be used for both DC and AC current sensing up to hundreds of kHz [57]. In addition, it has small and simple structure and can be fabricated using CMOS technology. However, Hall Effect sensor is usually more expensive than a Rogowski sensor or a current transformer. Other than the cost, the sensor often exhibits an unstable offset voltage which may vary over time. Meanwhile, it is also sensitive to temperature

and external magnetic field which make them less attractive for integrated applications [56].

Rogowski Coil is an application based on Faraday's law of induction. It is an air-cored coil placed around the conductor in a toroidal fashion [57]. The induced voltage across the coil can be measured to estimate the derivative of the primary current. Simple integration could then be carried out to predict the exact the current level. Rogowski Coil sensor has small size, low cost, high bandwidth and excellent linearity. Reference [60] presents a new power module concept which integrates a tiny PCB Rogowski Coil for IGBT switching current measurement in a compact converter. However, external circuitry including an integrator and ADC is needed to process the output voltage.

Current Transformers are widely used for AC current sensing. Similar to the Rogowski Coils, Current Transformers also exploit Faraday's law of induction to measure current. This technique thus provides galvanic isolation and consumes little power. Unlike the Rogowski Coil technique using an air core, Current Transformer has a magnetic core and needs to be terminated with a sense resistor. The core material design needs to be carefully considered as the hysteresis of the core material may degrade the measurement accuracy. Besides, the core should not be saturated under any condition especially in low frequency applications. This may lead to increased size and cost. Therefore, the Current Transformer technique is not suitable for DC current measurement [56-58].

It can be seen that all the non-intrusive current sensing methods either based on Faraday's Law or Magnetic field sensing are inevitably making use of external components which pose difficulties for system integration. These sensors are also sensitive to various parasitic effects and temperature, making them difficult to achieve high accuracy in practical applications.

A new current sensing method which involves no external component and can be fully integrated into an IGBT gate driver IC will be introduced in Chapter 2. This technique is based on the Miller effect of the IGBT devices, and it allows a cycle by cycle measurement of the IGBT switching current with high accuracy. A brief Comparison of

the proposed current sensing technique versus the existing current sensing methods is listed in Table 1.1 and Table 1.2.

Table 1.1: Comparison of existing current sensing methods and the proposed current sensing technique

Current Sensing Methods	Accuracy	Estimated Bandwidth	Cost	Power Loss	Isolated
Shunt resistor	Medium	DC-10MHz	Low	High	No
Sense-FET	Medium	<1MHz	Medium	Low	No
$V_{CE\,(on)}$	low	<1MHz	Medium	Low	No
Hall effect sensor	Medium	DC-1MHz	High	Low	Yes
Rogowski coil	High	0.1-100MHz	Low	Low	Yes
Current transformer	Medium	0.1-100MHz	High	Low	Yes
Miller Effect (I_G)	High	<1MHz	Medium	Low	Yes

Table 1.2: Application hints for existing current sensing methods and the proposed current sensing technique

Current Sensing Methods	Integrability	Typical Application
Shunt resistor	No	Industrial applications where low-cost is the primary concern
Sense-FET	No	Over current protection in IPMs
$V_{CE\,(on)}$	No	Over current and short circuit protection
Hall effect sensor	No	Industrial motor drive current sensing
Rogowski coil	No	High frequency, high current, and non-intrusive current sensing
Current transformer	No	AC current sensing
Miller Effect (I_G)	Yes	Integrated current sensor in gate driver IC to realize on-chip current regulation.

1.4. Thesis Overview

The recent trend for IGBT gate driver IC is to integrate more and more sophisticated functions to optimize and protect the IGBTs. These include turn-on and turn-off R_G selection, closed loop *di/dt* and *dv/dt* control for optimizing the trade-off between switching loss and Electro-Magnetic Interference (EMI) [44]. In order to achieve higher

functionality and flexibility for a wide variety of applications, programmable digital circuits are incorporated into the gate driver circuits to achieve adaptive switching control [33, 77]. To add more flexibility, a simple stack based micro-controller named SPRUCE (Stack PRocessor Unit for Controlling Energy) was proposed in [78]. This embedded processor in the gate driver IC can provide reconfigurable control algorithm for many types of closed loop control functions for the IPMs. In this thesis work, an IGBT gate driver with an integrated collector current sensor and on-chip SPRUCE CPU for digital control and local data processing is presented. The temperature compensated current sensing technique monitors only the gate current during the Miller Plateau region to predict the collector current.

This research work was motivated by the compelling need to find a new technique to indirectly measure the collector current (I_C) from the gate side using only the gate current (I_G) or gate voltage (V_{GE}). The objective is to incorporate this technique into a gate driver IC chip. At the same time, an on-chip CPU is also desirable for all the digital processing and achieving high configurability. Therefore in this case, all circuits remain on the low voltage side in the gate driver. There is no need to touch the high voltage collector terminal or the load side. Moreover, no extra discrete components are needed and the IPM functionality is increased.

An analysis is introduced to demonstrate the theoretical basis for using the IGBT gate current (I_G) to predict the collector current (I_C) during the Miller plateau region of the IGBT turn-on and turn-off switching transients. The details are presented in Chapter 2. Basic IGBT switching characteristics are discussed and the physical relationship between the I_G and I_C are deduced. This is followed by experimental verification of the proposed technique by switching a discrete IGBT on and off under different load current and load voltage conditions. The corresponding I_G and I_C are recorded and discussed.

Chapter 2 also presents the discrete implementation of the proposed current sensing technique. The prototype circuit board can automatically sense the Miller plateau region during IGBT switching transient and digitize I_G during the plateau regions to predict I_C.

After the proposed technique is demonstrated with discrete implementation, an integrated version with on-chip gate driver, SPRUCE unit and a current sensing system is designed and fabricated using TSMC's 0.18μm BCD GEN2 process. Chapter 3 provides the details of each circuit block in the gate driver IC chip with simulation results.

Chapter 4 describes the test setup for the gate driver IC chip, followed by the presentation of the experimental results. Since the proposed current sensing technique is sensitive to temperature. The temperature effect is also presented and analyzed. A compensation technique is also proposed and verified.

Finally in Chapter 5, the conclusion and future work to further extend this topic are presented.

Chapter 2

Proposed IGBT Collector Current Sensing Technique and Discrete Implementation

As reviewed in Chapter 1, the conventional collector current sensing methods for IGBTs which utilize resistive sensors such as shunts and Sense-FETs reduce the system efficiency and normally suffer from poor accuracy. The inductive and magnetic current sensing approaches are usually expensive and bulky, causing difficulties for integration. These problems could be eliminated if a measurement technique is available to monitor the low voltage and low current waveforms directly at the gate driving circuits.

This chapter introduces the proposed current sensing method which is based on the Miller Effect during the IGBT switching transients. The theoretical background of the proposed current sensing method is described and verified experimentally. This Chapter is organized as follows: Section 2.1 reviews the basic switching transients of the IGBT, models the behavior during the Miller plateau region and deduces the relationship between I_G and I_C. Section 2.2 presents the simulation and experimental results on the relationship between I_G and I_C during the Miller Plateau. The discrete implementation of an automatic current sensing system is introduced in Section 2.3. A brief chapter summary is provided in Section 2.4.

2.1. Proposed Current Sensing Method

It is well known that for IGBTs, the gate-emitter voltage (V_{GE}) exhibits a Miller plateau at both turn-on and turn-off [79]. During this plateau, V_{GE} is effectively clamped due to the charging (discharging) of the gate-collector capacitor (C_{GC}) during turn-on (turn-off). The voltage at which the V_{GE} plateau occurs is determined by the I_C waveform [80]. The proposed technique utilizes this phenomenon and its effect on the IGBT gate current (I_G) to indirectly measure I_C. In this case, I_G is measured by monitoring the voltage across the gate drive resistance (R_G).

2.1.1. Basic IGBT Switching Transients

Since the proposed current sensing method depends on the IGBT's gate charge transfer characteristics during the switching transient, it is necessary to examine the IGBT's basic switching behavioral. IGBTs are commonly used to drive inductive loads such as the winding of motors, where the load inductance is sufficient to maintain nearly constant current flow throughout the switching cycle. This could be simulated by using the "Clamped Inductive Load", as illustrated in Figure 2.1 [74].

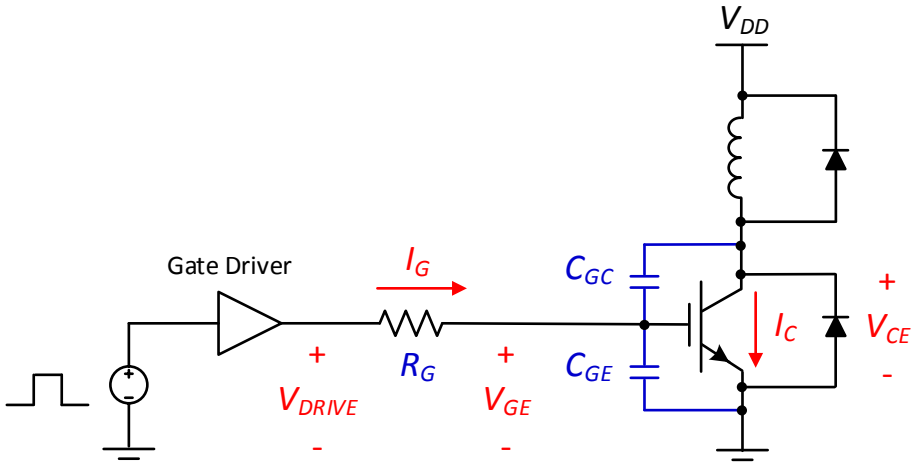


Figure 2.1: Test bench schematic for IGBT switching transient analysis with inductive load.

The IGBT device is connected in series with an inductive load and the DC power supply, with a high side free-wheeling diode connected across the load to re-circulate the current flow when the IGBT device is off [81]. In practice, a switching voltage source is usually applied to the gate of the IGBT device through a gate driver and a discrete gate resistor. The gate driver works as a power amplifier which amplifies low voltage digital input from a microcontroller and produces high current drive output to drive the power switch gate. Noting that power switches such as IGBTs usually exhibit large gate-emitter capacitance (C_{GE}), thus gate drivers are required to ensure proper driving strength and ensure reasonable switching speed. Typical gate driver design options have been discussed in Section 1.2.1. The gate resistor R_G provides an extra degree of freedom for switching speed tuning. However, it should be carefully selected for switching behavior optimization. This will be explained later in this section.

The switching behaviour of an IGBT is also strongly related to the stray and depletion-layer capacitances of the device, especially the Miller capacitor C_{GC}. The idealized turn-on and turn-off switching waveforms of a typical IGBT are shown in Figure 2.2 and Figure 2.3. These can be obtained by using the test bench schematic in Figure 2.1 with the inductor substituted by a current source. This current source is acting as the inductor which carries a constant current I_0 in this case.

Turn-on

IGBT is operating like a MOSFET driving a PNP transistor. By virtue of the IGBT's MOS gate structure, the turn-on process of an IGBT is quite similar to that of an MOSFET. As plotted in Figure 2.2, the turn-on process can be divided into four distinct time intervals. At time t_1, a positive voltage is applied to the gate resistor (R_G). During time interval 1, current begins to flow into the gate and charge up C_{GE}. At time t_2, V_{GE} reaches the threshold voltage. During time interval 2, V_{GE} increases exponentially with a time constant equals to $[R_G \times (C_{GE} + C_{GC})]$. I_C begins to increase as V_{GE} continues to rise. At the same time, the current in the high side freewheeling diode decreases. However, the diode is still forward biased. Therefore, a non-zero V_{CE} still exists across the IGBT during time interval 2. During time interval 3, the Miller capacitance is being charged. The gate

voltage remains almost constant as the gate current begins to charge C_{GC}. This phenomenon occurs as V_{CE} continues to decrease. This drop in V_{CE} voltage causes an increase in the effective C_{GC} capacitance. The magnitude of this increase in capacitance can be as much as two to three times when V_{CE} becomes very low [82]. At time t_4, the gate-source voltage plateau ends and the gate source voltage increase exponentially during time interval 4. V_{GE} reaches its final value at t_5 at which point the IGBT achieves full conduction [74, 80].

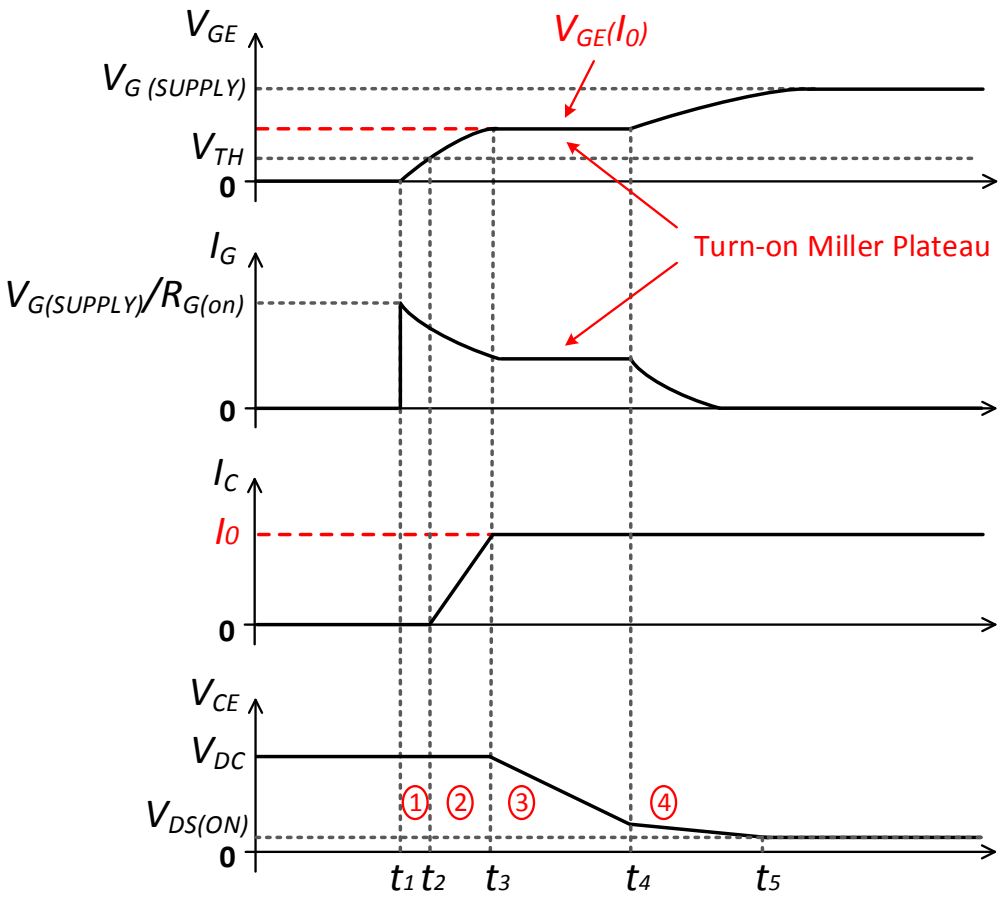


Figure 2.2: Typical turn-on waveforms for IGBTs.

Turn-off

Unlike the turn-on process which is a majority carrier phenomenon, the turn-off process is more dependent on the PNP transistor characteristics. The turn-off sequence (as shown in Figure 2.3) is essentially the reverse of the turn-on process and can also be defined

using four time intervals. During time interval 5, V_{GE} falls to a level determined by the I_C DC transfer characteristic. The Miller plateau is reached during time interval 6 as the gate current discharges C_{GC}. At t_8, when V_{CE} has increased to V_{DD}, I_C starts to drop rapidly. However, this rapid reduction in I_C is followed by a long current tail due to the minority carrier recombination phenomenon in the long drift region. The charges recombine at a rate mainly determined by the carrier lifetime, less influenced by the charge being removed from the gate [74].

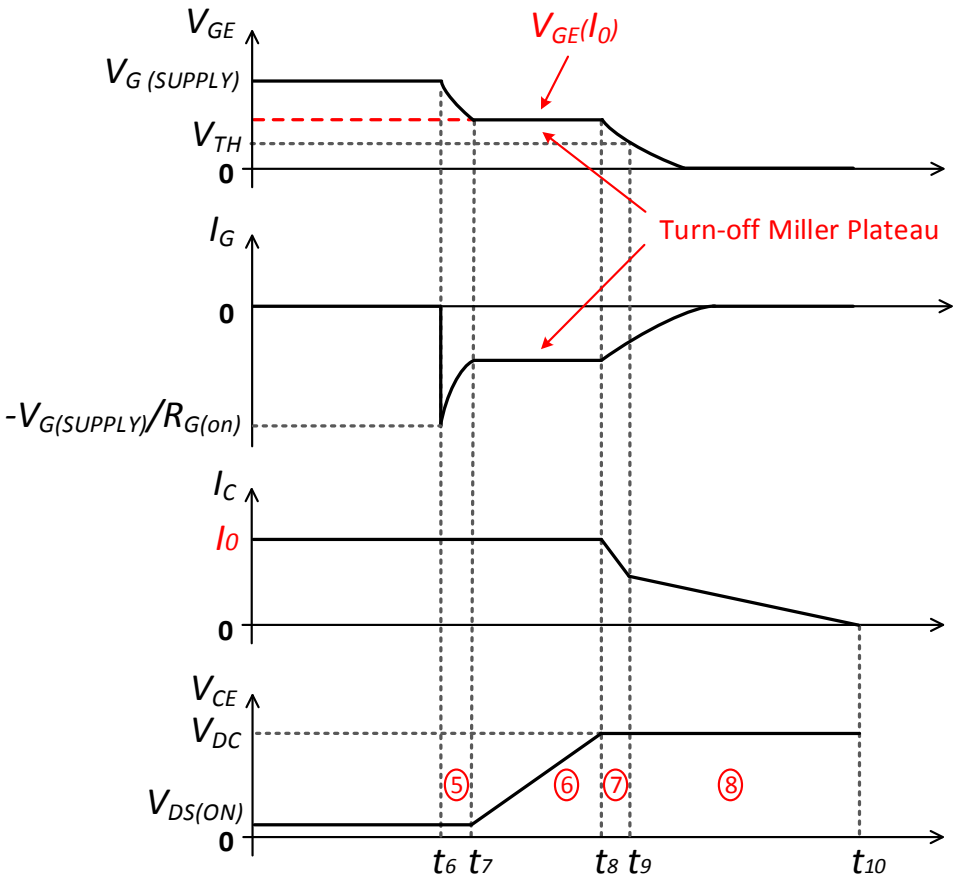


Figure 2.3: Typical turn-off waveforms for IGBTs.

With proper selection of R_G, the Miller plateau can be easily identified and measured for both turn-on and turn-off of the IGBT. If R_G is too small, the gate charging/discharging current will be too large and the plateau will be difficult to identify from transient waveforms. In addition, the fast charging rate at turn-on may cause I_C overshoot which may cause significant conducted EMI and reduce the lifetime of the IGBT [43]. However,

if R_G is too large, the rate of gate charging/discharging will be too slow, potentially increasing switching loss in the IGBT.

As the Miller plateau phenomenon is caused by the influence of I_C on C_{GC}, the value of V_{GE} for the Miller plateau should exhibit a distinct relationship with I_C. Therefore, I_C can be obtained by measuring the plateau value of V_{GE} or by measuring I_G, which should also become constant at the Miller plateau. Practically, it may not be possible to measure V_{GE} directly as the emitter of the IGBT may not be connected directly to ground. Especially for those IGBT modules, there is a large parasitic inductor between the IGBT emitter and ground which is mainly contributed by the large inductance of the lead pads. Therefore, in this work, the proposed measurement technique involves an indirect measurement of I_C by measuring I_G.

2.1.2. IGBT Modeling

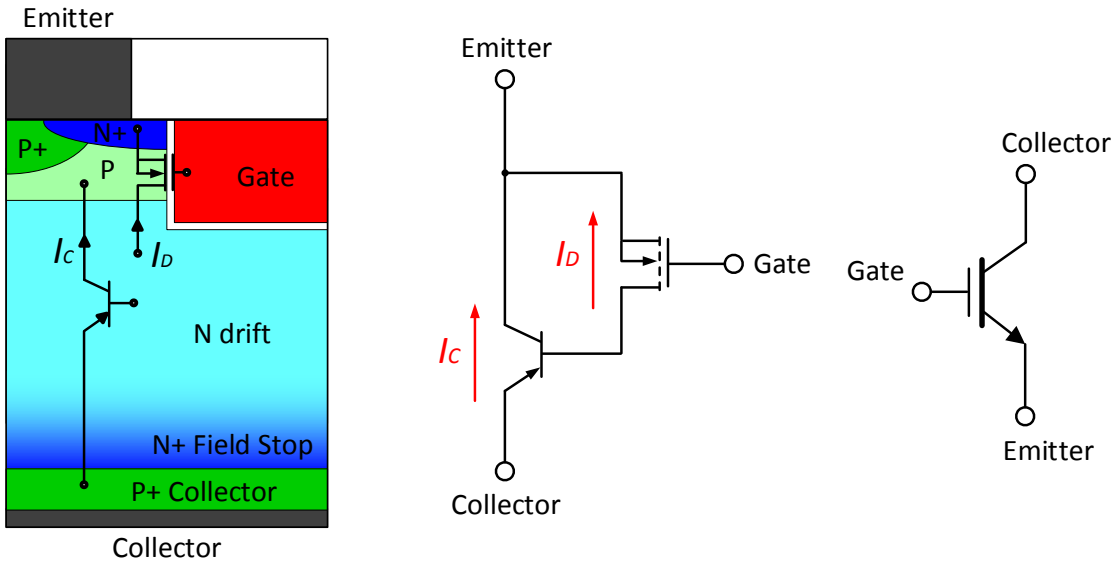
To understand the theoretical relationship between I_G and I_C, the following analysis is carried out based on the basic IGBT modeling. Figure 2.4 (a) shows the cross section of a typical trench gate field-stop IGBT, which is the most popular IGBT structure with short turn-off time and low on-state voltage drop [4].

Figure 2.4 (b) shows the simplified model of the IGBT which is a MOSFET driving a wide based PNP transistor. The physical locations of the MOSFET and the PNP transistor in the trench gate field-stop IGBT is shown in Figure 2.4 (a). In this IGBT, the electron current (I_n) flowing through the MOSFTE serves as the base drive current for the PNP transistor. Therefore, the hole current (I_p) flowing through the PNP transistor is [83]:

$$I_p = \beta_{PNP} I_n = \left(\frac{\alpha_{PNP}}{1-\alpha_{PNP}} \right) I_n \tag{2.1}$$

where β_{PNP} denotes the common emitter gain of the PNP transistor; and α_{PNP} is the common base gain. The emitter current of the IGBT, I_E can be obtained by adding up the electron and hole currents as:

$$I_E = I_n + I_p = \frac{I_n}{1-\alpha_{PNP}} \tag{2.2}$$



(a) (b) (c)

Figure 2.4: (a) Cross section of a typical trench gate field-stop IGBT, (b) a simplified IGBT model, (c) typical IGBT symbol.

Due to the high input impedance of the MOS gate structure, the gate current, I_G is zero in steady state. Even during switching, the charging and discharging gate currents are much smaller than the emitter current. Therefore, I_E is approximately equal to the collector current, I_C. The electron current, I_n is in fact the drain current of the MOSFET. Therefore, I_C and I_D can be related as shown below:

$$I_C = \frac{I_D}{1-\alpha_{PNP}} \tag{2.3}$$

Suppose a voltage source, switching between V_{DRIVE} and ground, is applied to the IGBT, as illustrated in Figure 2.1. During the turn-on process, the gate current I_G of the IGBT (also the MOSFET) and drain current of the MOSFET (I_D) can be expressed as:

$$I_G = \frac{V_{DRIVE} - V_{GE}}{R_{G(ON)}} \tag{2.4}$$

$$I_D = \frac{g_m\left(V_{GE} - V_{TH}\right)}{2} \tag{2.5}$$

Combine equations (2.4) and (2.5):

$$I_G = \frac{V_{DRIVE} - V_{TH} - \frac{2I_D}{g_m}}{R_{G(ON)}} \tag{2.6}$$

Substituting (2.3) into (2.6), the relationship between I_C and I_G is given by:

$$I_C = -\frac{R_{G(ON)} g_m}{2(1-\alpha_{PNP})} I_G + \frac{g_m (V_{DRIVE} - V_{TH})}{2(1-\alpha_{PNP})} \tag{2.7}$$

where g_m is the transconductance of the MOSFET. It is related to the transconductance of the IGBT G_m by [84]:

$$G_m = \frac{g_m}{1-\alpha_{PNP}} \tag{2.8}$$

During the turn-on transient, I_C can be determined by:

$$I_C = -\frac{R_{G(ON)} G_m}{2} I_G + \frac{G_m (V_{DRIVE} - V_{TH})}{2} \tag{2.9}$$

A similar derivation for I_C can also be applied to the turn-off process:

$$I_C = -\frac{R_{G(OFF)} G_m}{2} I_G + \frac{G_m V_{TH}}{2} \tag{2.10}$$

where $R_{G(ON)}$ and $R_{G(OFF)}$ are the turn-on and turn-off gate resistance. V_{TH} is the threshold voltage of the IGBT. R_G, V_{DRIVE} and V_{TH} are usually constants. G_m of the IGBT can be found from the I_C versus V_{GE} transfer curves in the device data sheet. Therefore, there is indeed a relationship between the gate current, I_G and collector current, I_C. This is a unique relationship for a particular IGBT structure and is only affected by temperature and process variations. The temperature compensation method will be introduced in Chapter 4. However, this relationship is only valid in the Miller plateau region where the device is in saturation mode. In practical applications where on-the-fly computing should

be minimized, it is easy to model this relationship by a simple lookup table or curve fitting.

2.2. Demonstration of I_G and I_C relationship

Based on the theoretical derivations, physical experiments have been carried out to demonstrate the relationship between I_G and I_C during the Miller plateau under different conditions.

Figure 2.5 shows a schematic of the experimental test-bench. *Infineon IGB30N60H3* IGBTs are used to construct a power inverter. The high-side IGBT is disabled (V_{GE} = 0) throughout the experiment and only the freewheeling diode (FWD) can be turned on. I_G is obtained by measuring the difference between V_{DRIVE} and V_{GE}, and then divided by R_G. The inductor current (I_L) is determined using a TEKTRONIX TCP312 current probe. Measurement of I_L allows for an easy determination of I_C just after turn-on or just before turn-off.

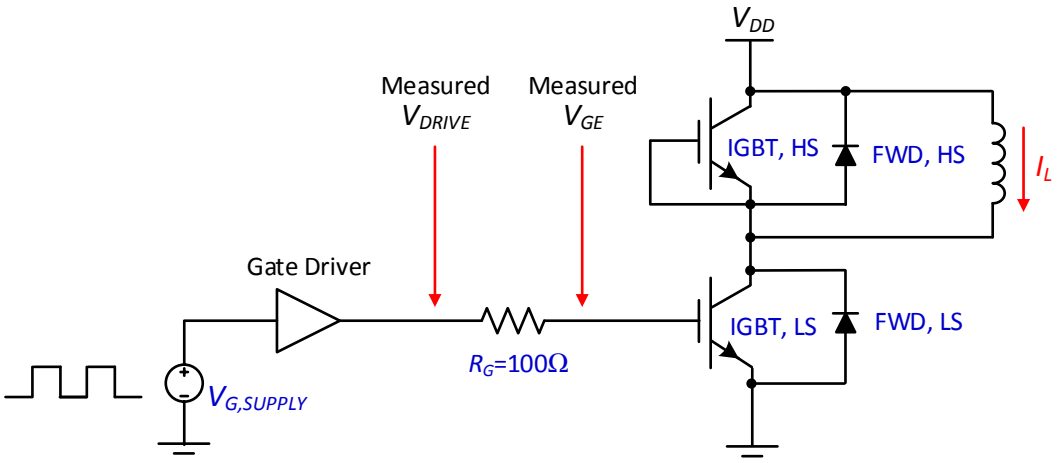


Figure 2.5: Experimental test bench schematic (IGBT model: IGB30N60H3).

An *Altera Cylcone II FPGA* is used to generate the input signals for the gate driver. A double pulse experiment was employed whereby the gate driver turns on and off the low-side IGBT twice in quick succession. The length of the first turn-on period is adjusted in order to control I_C. The I_G and I_C measurements are performed during the rising and

falling edge of the second turn-on period. Both the turn-on and turn-off I_G values were measured as I_C was varied. Figure 2.6 shows several signals of interest for the aforementioned double pulse technique.

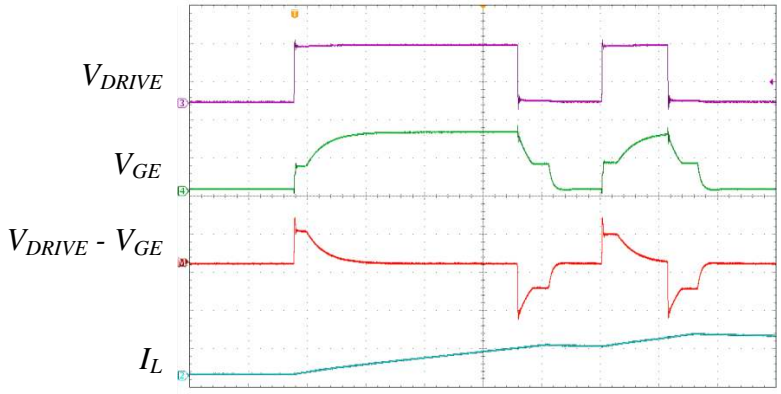
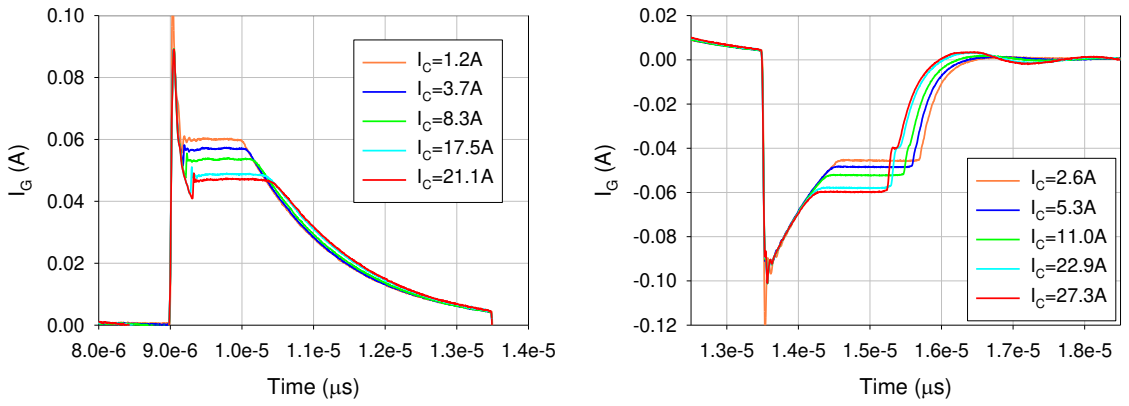


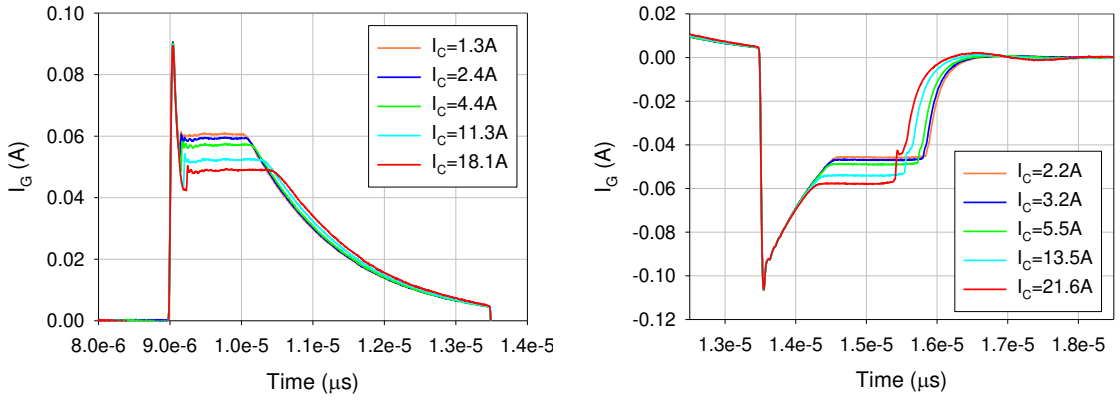
Figure 2.6: Sample waveforms for V_{DRIVE}, V_{GE}, V_{DRIVE}-V_{GE} and I_L.

The turn-on and turn-off behavior of I_G was recorded for several V_{DD} voltages ranging from 25V to 250V. Several I_G waveforms for different I_C values during turn-on and turn-off for V_{DD} = 25V, 100V and 250V are as illustrated in Figure 2.7 to Figure 2.9. I_C was varied from 1A to 30A. From these waveforms, it is evident that the Miller plateau behavior is consistent across low and high V_{DD} conditions. Furthermore, the plateau region is always explicitly visible.



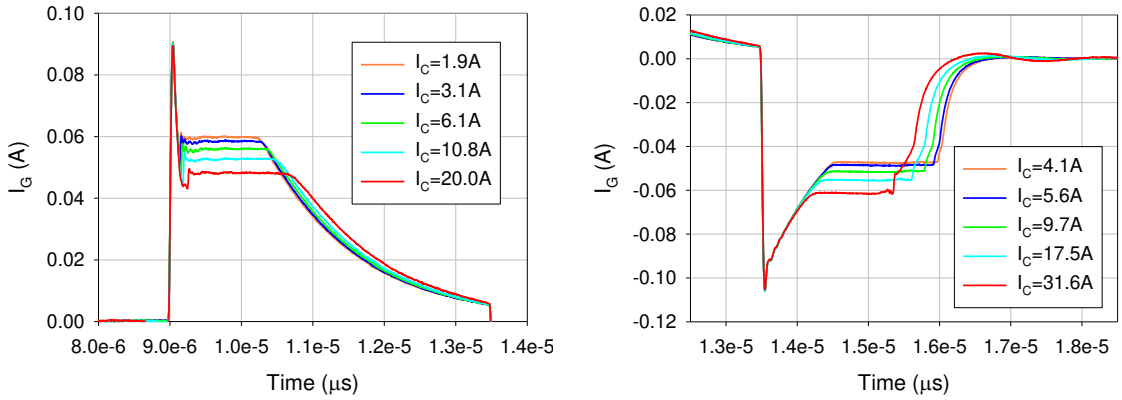
(a) (b)

Figure 2.7: Measured I_G waveforms for different I_C when V_{DD} = 25V at (a) turn-on and (b) turn-off.



(a) (b)

Figure 2.8: Measured I_G waveforms for different I_C when V_{DD} = 100V at (a) turn-on and (b) turn-off.



(a) (b)

Figure 2.9: Measured I_G waveforms for different I_C when V_{DD} = 250V at (a) turn-on and (b) turn-off.

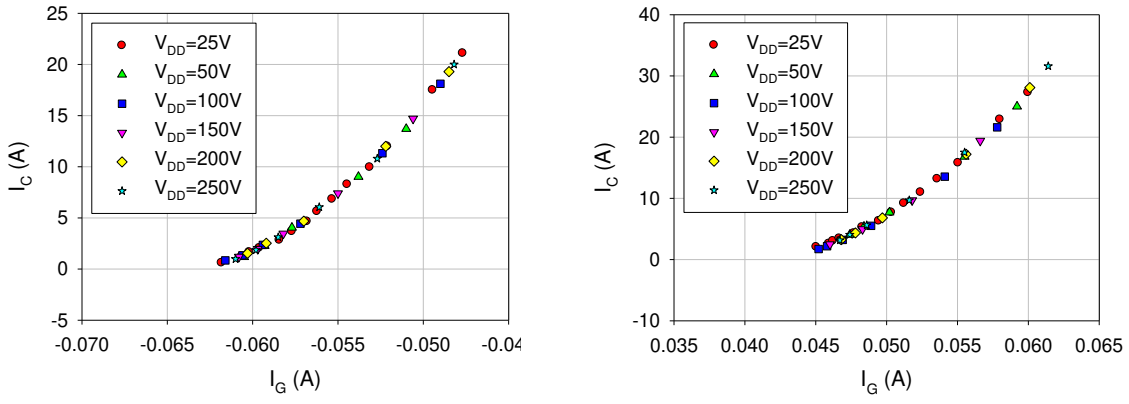
The impact of changing I_C has on I_G for each V_{DD} condition is obvious from Figure 2.7 to Figure 2.9. For the turn-on transient, higher I_C leads to lower I_G plateau value. Considering the constant V_{DRIVE} as in Figure 2.5, lower I_G in the plateau region means higher V_{GE}. This is expected from the gate transfer characteristics of the IGBT, where I_C increases with gate bias voltage V_{GE}. For the turn-off transient, since V_{DRIVE} is essentially zero, higher I_C will translate to higher V_{GE} and thus higher I_G.

For the same V_{DD} voltage level, the I_G plateau length varies less than 5% when I_C changes from 1A to 30A in this case. Intuitively, the gate-drain capacitance C_{GD} is dominated by V_{DD} instead of I_C. Nevertheless, the variation of I_C would slightly change the on-state

voltage drop across the IGBT, therefore, the C_{GD} as well as the required gate charge to fully turn-on the device will also vary to certain extent [85]. However, the plateau length change due to I_C is much smaller compared to the impact of the V_{DD} change.

It can be seen that the plateau length of I_G increases prominently for comparable I_C values when V_{DD} increases from 25V to 250V. This is mainly due to the high initial DC voltage drop across the collector and emitter ends of the IGBT; which requires a much longer charging time to provide increased gate-drain charge Q_{GD}. Meanwhile the plateau level of I_G sustains the same for a give I_C no matter how V_{DD} changes.

In Figure 2.10, the Miller plateau values for I_G during turn-on and turn-off were extracted and plotted against I_C for difference V_{DD} voltages. It clearly shows that the measurement results remain consistent regardless of different V_{DD} levels. These measurements are in good agreement with the simulation results discussed above. Furthermore, these results demonstrate a clear relationship between I_C and I_G regardless of the V_{DD} voltages. The plateau values of I_G was extracted by averaging all the values during the plateau interval, and the worst case maximum discrepancy between the actual value and the average value is 1.5% for turn-on plateau and 1.8% for turn-off plateaus. The main source of discrepancy comes from the fact that I_C always changes slightly during the short plateau region (I_C is not constant during the double pulse test), causing the I_G plateau to tilt slightly as well.



(a) (b)

Figure 2.10: Measured I_C vs. I_G for (a) turn-on plateau values (b) turn-off plateau values.

Therefore, the experimental results show that the idea of measuring the IGBT collector current I_C indirectly using its gate current I_G is feasible. It is observed that the proposed technique could be used for voltage up to 250V and currents up to 30A with 2% inaccuracy.

It was also found that the proposed technique is subjected to temperature change. The examination of the temperature influence on the technique and the temperature effect compensation will be discussed in Chapter 4.

2.3. Discrete Implementation of an Automatic I_C Current Sensing Circuit

Now we have the I_G and I_C relationship demonstrated; it can still be problematic to extract I_G during the plateau region in practical applications. Proper signal processing techniques need to be implemented such that I_G can be extracted automatically and accurately in order to predict I_C.

Before integrating this technique into a gate driver IC, a discrete version of the automatic I_C current sensing was designed and tested. Figure 2.11 shows the block diagram and testing configuration of the current sensing circuit. A gate driver is used to control the low side the IGBT and a Field Programmable Gate Array (FPGA) is implemented to provide all the digital control and processing. The I_C sensing circuit can be divided into two blocks, the Low Voltage portion (3.3V) and the High Voltage portion (15V). The Low Voltage circuit senses the time period for the turn-on and turn-off plateau, and feedback the signal to the FPGA for digital processing. The FPGA generates a pulse that matches the Miller plateau region. This pulse will trigger a fully differential high voltage integrator that integrates the voltage difference across the gate resistor R_G during the plateau region. According to

$$V_{OUT\_DIFF} = \frac{V_{IN\_DIFF}}{RC} t = \frac{I_G \times R_G}{RC} t \tag{2.11}$$

RC is the time constants and is known through the components selection, t is the integration time which equals the pulse width. In this application, a fixed time integration is used and will be explained in detail later. The fully differential input voltage V_{IN_DIFF} can be expressed as I_G times R_G. This resistance should also be fixed in real application. The fully differential output voltage V_{OUT_DIFF} is digitized by an ADC at the end of the integration time. Equation (2.11) shows the relationship between I_G and I_C, based on which we could expect there exists a similar relationship between V_{OUT_DIFF} and I_C. Therefore, a lookup table is constructed between the digitized V_{OUT_DIFF} and the collector current I_C. For each cycle's turn-on and turn-off transients, I_C could be deduced by examining the digitized output of V_{OUT_DIFF}.

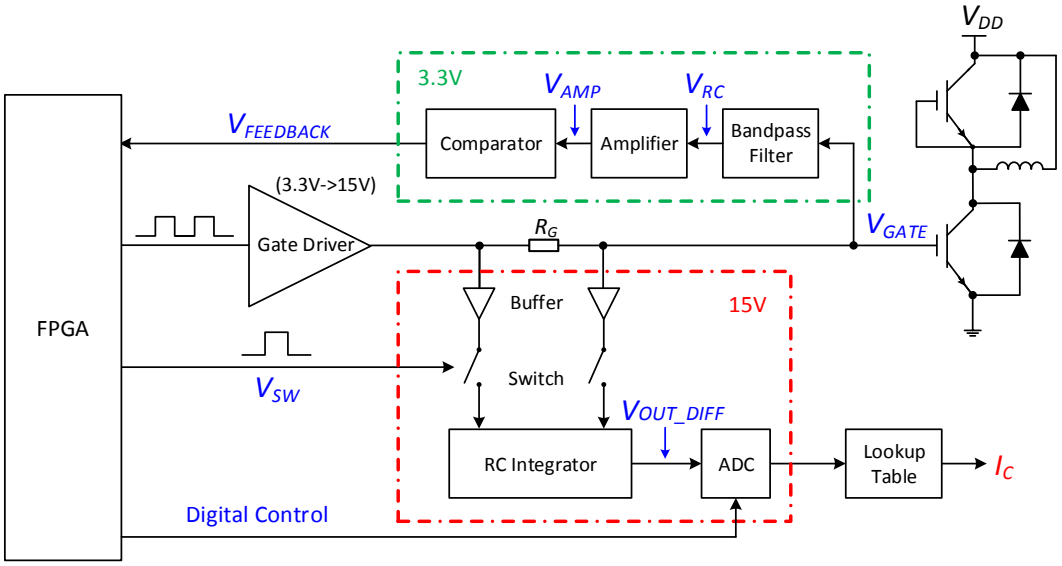


Figure 2.11: Block diagram for the discrete implementation of the current sensing circuit.

The reason for using an integrator instead of sensing the gate voltage directly is due to the fact that the plateau region is usually very short and noisy. In addition, as mentioned in Section 2.2, I_G may tilt slightly during the plateau region. Therefore, the integration provides an averaging function that filters out the change in I_G and also strongly suppresses noise. Another reason for the integration is the fact that the change in gate current is relatively small when compared to the changes in the collector current (as it can be seen from Figure 2.10). Therefore, the integrator can amplify the changes in gate current to provide higher sensitivity and higher accuracy.

2.3.1. Experimental Test Bench Setup

The experimental test setup used to verify the current sensing circuit is shown in Figure 2.12 (a). Three levels of customized PCBs are cascaded onto the base level of a Fuji 7MBP200VEA060-50 IPM module. The power module contains a three phase output stage using six IGBTs and six freewheeling diodes, as previously shown in Figure 1.3 (b). The first level PCB only contains connection headers which allows for easy addition and removal of the control and current sensing circuits. The second level PCB allows access to an FPGA board that plugs directly onto the board. It includes the segmented gate drivers constructed using discrete components. It also provides access to important nodes via the third level PCB that contains all the analog components. The third level board is the actual I_C current sensing system, which is connected to the second level PCB via headers to provide access to the FPGA digital control and gate signal generation circuits.

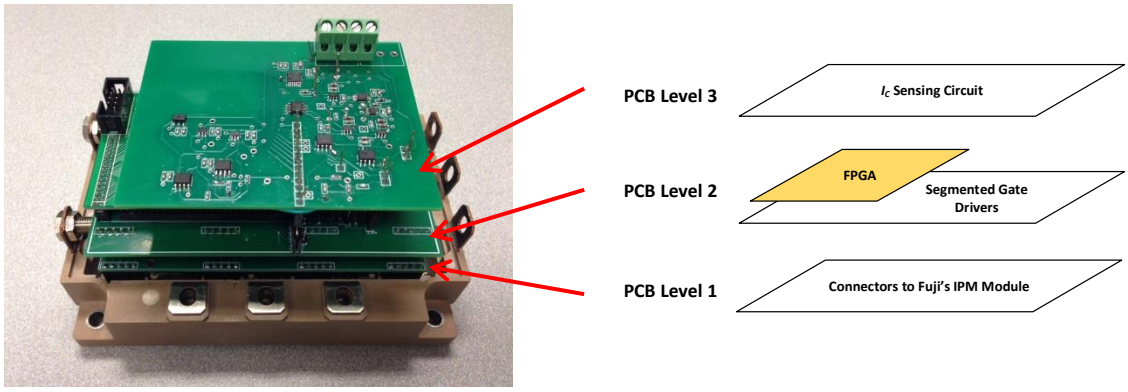


Figure 2.12 (a): Experimental Testbed for Current Sensing System.

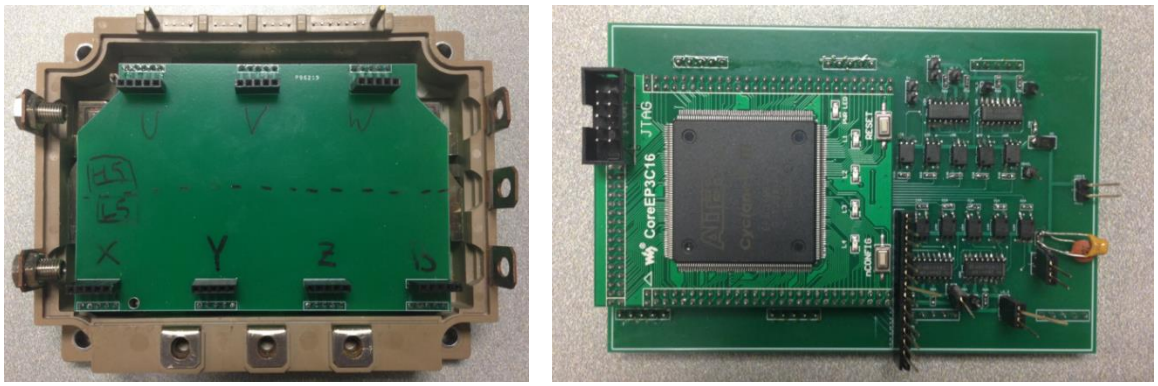


Figure 2.12 (b): First level PCB with connectors to the module base (left) and 2nd level PCB with an FPGA and segmented gate drivers (right).

The same double gate pulse technique is used to first set the collector current of the IGBT. The IGBT turn on and off transients are then measured as illustrated in Figure 2.13. Measurements are performed at the rising and falling edge of the second gate pulse. The width of the first gate pulse is adjusted in order to set the level for I_C. The voltage at the switching node, V_{SW} is the pulse used to trigger the fully differential integrator. It is basically a representation of the turn-off Miller plateau of the IGBT. The ADC samples the output of the integrator near the end of the Miller plateau. The output of the ADC can be read directly through the SPI interface of the oscilloscope.

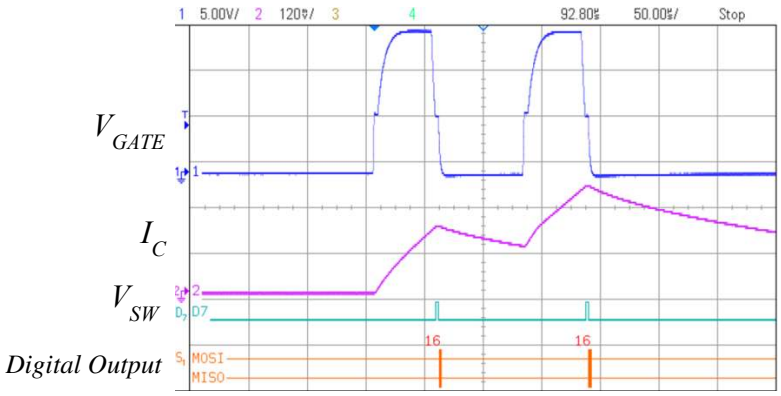


Figure 2.13*:* Typical waveforms for V_{GATE}, I_C, $V_{SW\,(turn\text{-}off)}$ and digital outputs.

2.3.2. Turn-on and Turn-off Plateau Sensing

The Miller plateau sensing block is designed based on a passive band pass filter. Figure 2.14 illustrates the schematic for the turn-on Miller plateau sensing block. A high pass filter is used to sense the gate node of the IGBT, where the time derivative of the plateau region equals zero. This is followed by a low pass filter which filters out the high frequency noise. The resulting V_{RC} is then amplified and compared with a constant reference voltage. The digitized $V_{FEEDBACK}$ is sent to an FPGA for digital processing. The FPGA uses a state machine and a fixed time integration block to generate V_{SW} which corresponds to the plateau regions. To sense the turn-off plateau, a similar circuit is used except that V_{RC} needs to be inverted, as shown in Figure 2.15.

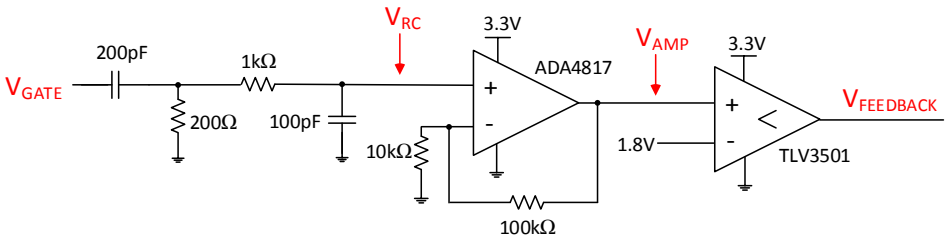


Figure 2.14: Schematic for the turn-on Miller plateau sensing circuit.

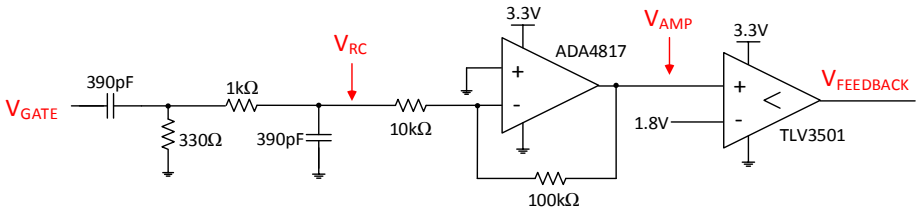
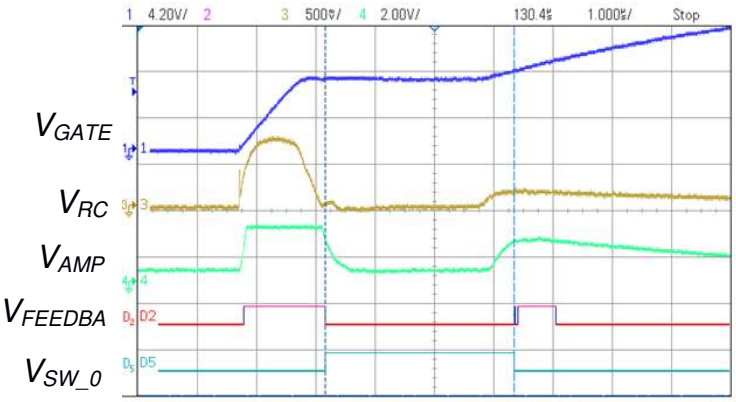
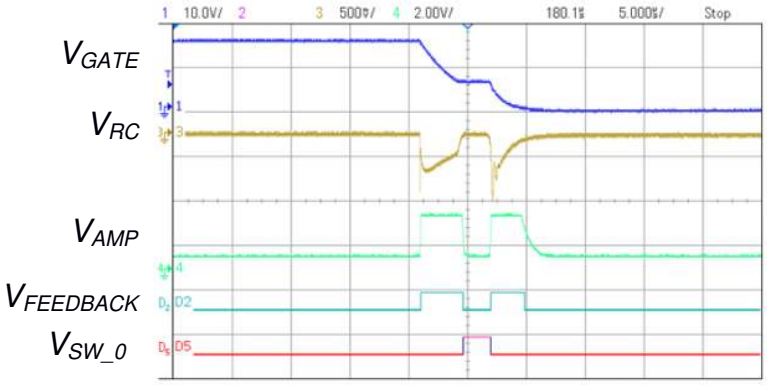


Figure 2.15: Schematic for the turn-off Miller plateau sensing circuit.

The high pass filter followed by a low pass filter results in a bandpass filter with frequency response peaks around 700 kHz for turn-off and 2.4 MHz for turn-on. The output of the filter needs to be within the input range of the amplifier stage afterwards. The amplifier and the comparator should have wide enough bandwidth for the signal. A high speed comparator is used to avoid excessive delay between the plateau start and the triggering for the integrator. Figure 2.16 shows the typical waveforms for the turn-on and turn-off Miller plateau sensing. The V_{SW_0} signal is state machine output which will be further processed by the fixed time integration block to generate V_{SW}. V_{SW} corresponds to either the turn-on or turn-off Miller plateau of the IGBT, and is the triggering signal of the integrator.



(a)



(b)

Figure 2.16: (a) Sample waveforms for sensing the turn-on Miller plateau. (b) Sample waveforms for sensing the turn-off Miller plateau.

2.3.3. Integrator Design and ADC Interface

The fully differential integrator is used to integrate the voltage across the gate resistor R_G during the IGBT turn-on and turn-off plateau period. The schematic for the integrator is illustrated in Figure 2.17.

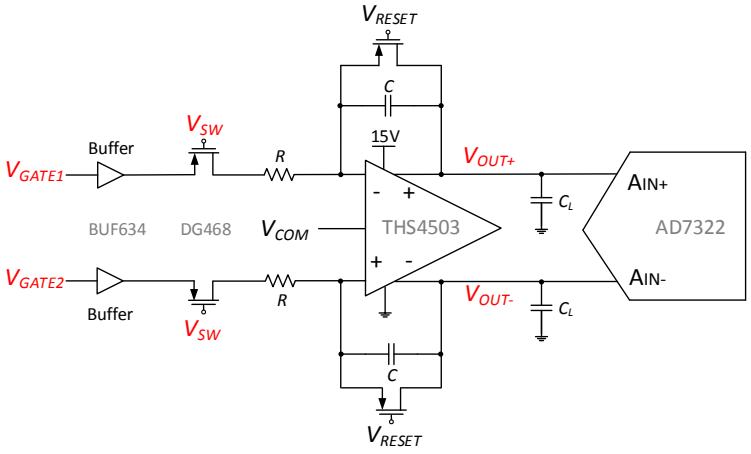
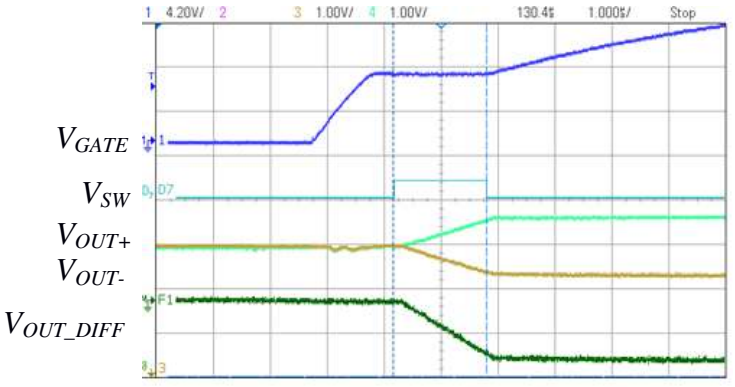


Figure 2.17: Schematic for the fully differential integrator.

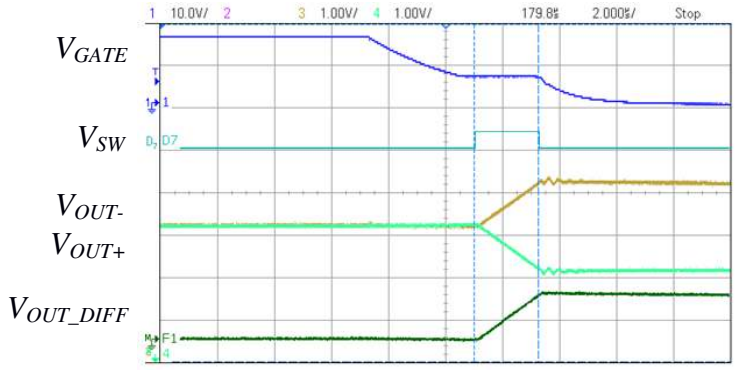
The two inputs of the integrator are supposed to connect to the two ends of the gate resistors. However, two high voltage buffers (BUF634 from Texas Instrument) are inserted here to make sure that the integrator would not interfere with the gate drive circuit. After the HV buffers, two analog switches (DG468 from VISHAY) are used to connect and disconnect the integrator. The analog switches can sustain up to 15V while

be controlled using low voltage digital logic. Moreover, they feature reasonable switching action time (around 100ns) to minimize the delay between plateau sensing and integrator triggering.

The common mode voltage needs to be carefully selected to accommodate both the common mode input range of the integrator Op Amp as well as the ADC. The integrator R and C values are determined based on the integration time t in order to obtain reasonable resolution from the output voltage. The value for C should be no less than 200 pF to avoid excess charge injection from the reset switches. Therefore, R is selected to be 10 kΩ and C is 390 pF. The integration time t is between 2µs to 3µs and is determined by the fixed time integration block. The trigger signal and output waveforms for the fully differential integrators during turn-on and turn-off are shown in Figure 2.18.



(a)



(b)

Figure 2.18: (a) Output waveforms of the differential integrator during turn-on; (b) Output waveforms of the differential integrator during turn-off.

The Analog to Digital Converter (ADC) is a 12-bit SAR ADC (AD7322 from Analog Devices). It is configured to accept fully differential inputs in the range of ±10V (resolution is 2.441mV) for turn-off and ±5V (resolution is 1.22mV) for turn-on. This is based on the fact that the effective plateau length for turn-on is shorter than turn-off for the same R_G value. Therefore, the ±10V input range setting could not provide enough resolution for the turn-on plateau sensing.

Figure 2.19 illustrates all the interfacing signals of the fully differential integrators with the ADC for turn-off. It shows that error may result if V_{SW_0} is used directly as the integrator triggering signal. The ADC samples V_{OUT+} and V_{OUT-} signals when the chip selection signal V_{CS} goes low and needs 16 clock cycles to complete the conversion. V_{CS} is set to be enabled at the first rising edge of a clock cycle after the falling edge of V_{SW_0}. However, V_{SW_0} is the state machine output and is not synchronized with the clock signal which generates V_{CS}. Therefore, the sampling point of the ADC could vary, and may cause error.

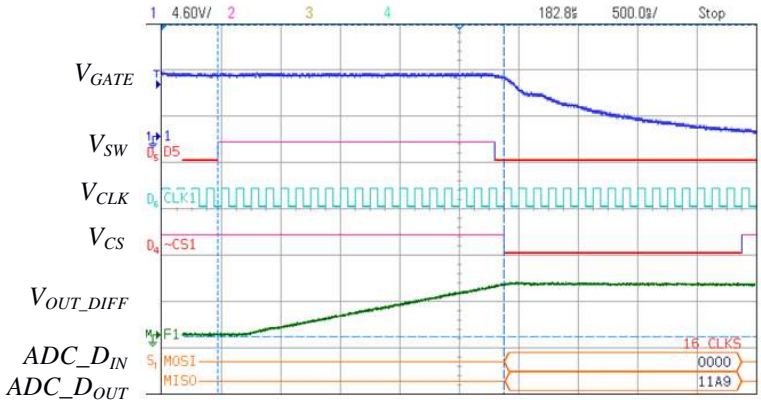


Figure 2.19: Switching waveforms of V_{GATE}, V_{SW}, V_{OUT+}, V_{OUT-} and V_{OUT_DIFF} during turn-off.

2.3.4. Fixed Time Integration

In order to eliminate the error source mentioned in the previous section, a fixed time integration method was proposed and tested. Based on extensive testing results, it is found that this fixed time integration could achieve much higher accuracy. The signal V_{SW} is generated from V_{SW_0} through a chain of D Flip-Flops as shown in Figure 2.20. This

fixed time integration method ensures that a multiple cycle of the master clock (8 MHz) are used. The integration time is determined based on the graph in Figure 2.21; where I_G is plotted as a function of time for different I_C levels and with V_{CE}. In practical applications, V_{CE} is normally fixed at very high voltages. When V_{CE} is higher, the plateau length will be slightly longer, as demonstrated in Section 2.2. In this case, the plateau length varies from 2.7 to 2.75 µs when I_C changes from 2 to 30 A with V_{CE} at 20 V. The variation is less than 2%. Therefore, the fixed time integration is practical and the time should be chosen to be as long as possible but shorter than the minimum plateau length. In this case, the integration time is chosen to be 1.6 µs for turn-on and 2.4 µs for turn-off.

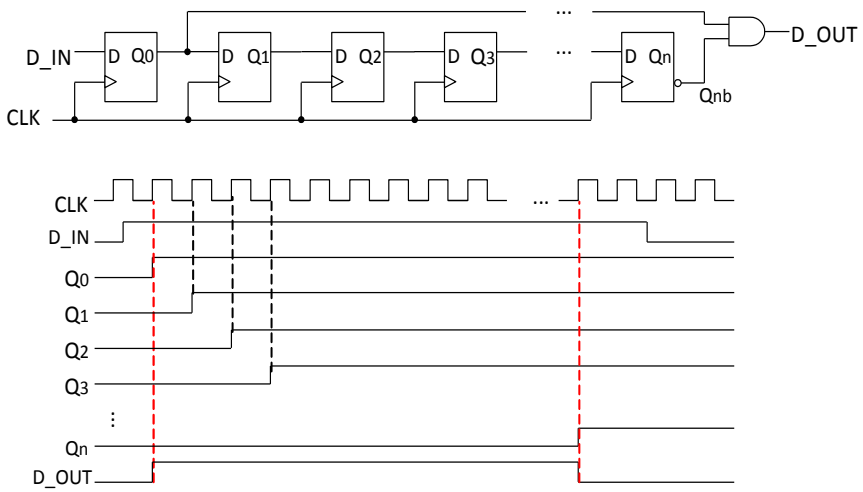


Figure 2.20: D Flip-Flop chain for fixed time integration.

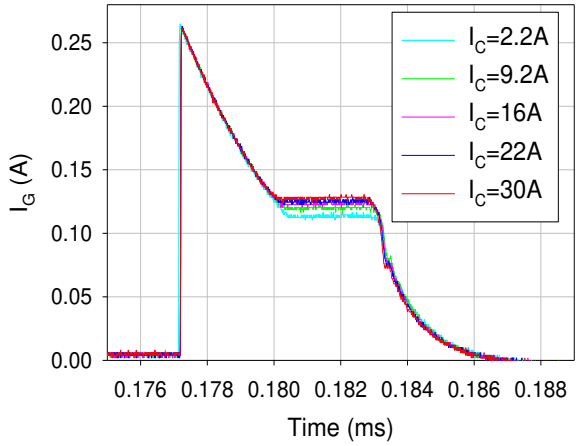
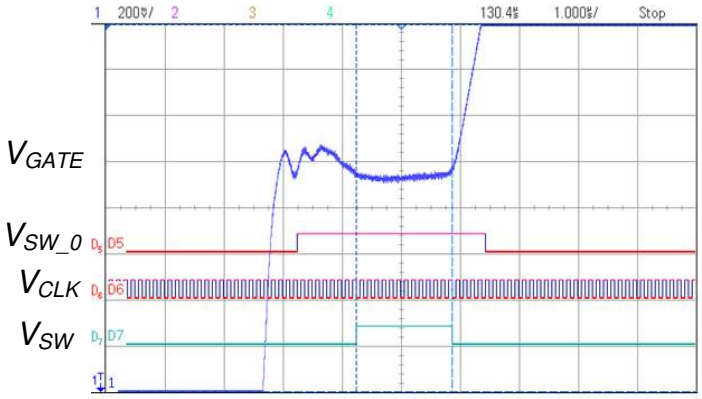
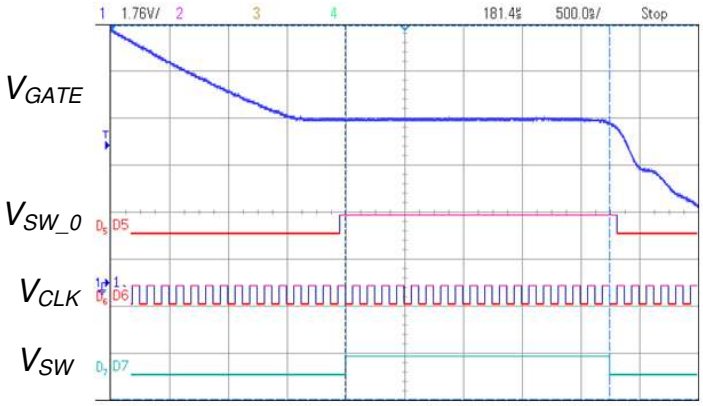


Figure 2.21: I_G as a function of time at different I_C levels for turn-off when V_{CE} = 20 V.

Figure 2.22 (a) and (b) illustrate the switching waveforms for the fixed time integration for turn-on and turn-off. The gate signal at turn-on is purposely zoomed in to show the initial ringing at the plateau region which is due to the Electromagnetic Interference of the switching. Therefore, the starting point of the V_{SW} signal for turn-on is purposely delayed for several clock cycles.



(a)

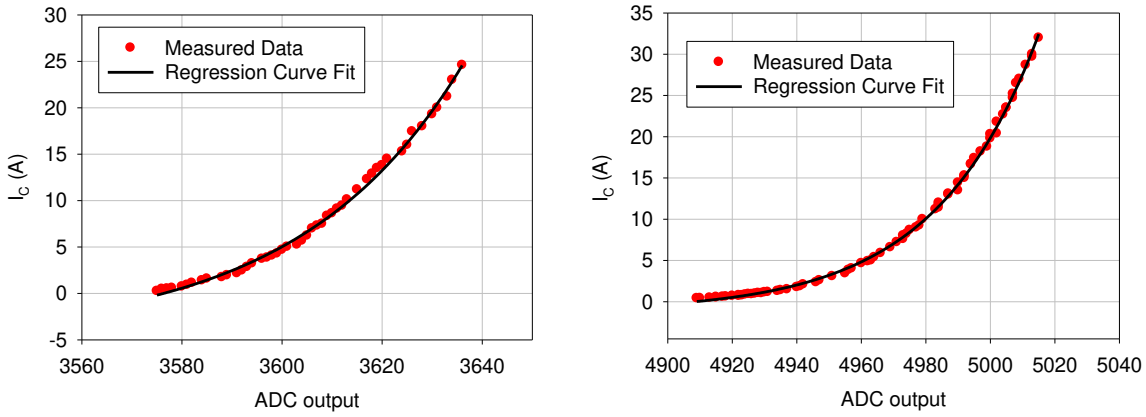


(b)

Figure 2.22: (a) Typical waveforms illustrating the fixed time integration for turn-on and (b) turn-off.

The extracted I_C versus ADC digital output for both turn-on and turn-off are as shown in Figure 2.23, matching the previously obtained I_C vs. I_G relationship very well. A regression analysis is performed on the actual I_C and the ADC outputs in order to evaluate the accuracy of the technique. The maximum deviation is less than 0.8 A for both turn-on and turn-off over the entire testing range, as shown in Figure 2.24. Therefore,

it is demonstrated that the IGBT collector current can be measured digitally from the low voltage gate drive circuit.



(a) (b)

Figure 2.23: (a) I_C vs. digital ADC output for turn-on. (b) I_C vs. digital ADC output for turn-off.

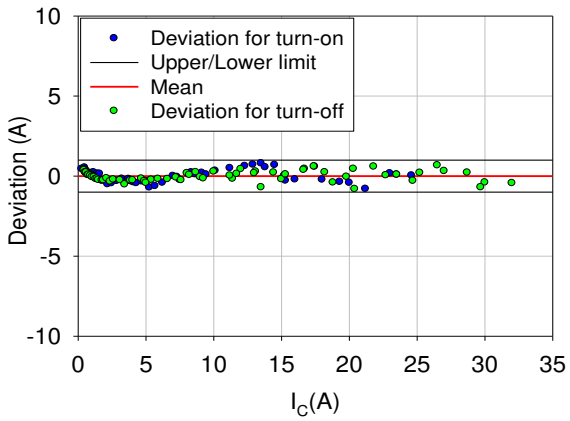


Figure 2.24: Deviation of the measured I_C to the regression fitted curve vs. I_C.

2.4. Chapter Summary

In this chapter, a unique method is introduced to measure the IGBT collector current (I_C) indirectly from the gate node. The proposed technique leverages the Miller effect to allow the monitoring points to be entirely in the low voltage gate drive circuit. The basic IGBT switching behavior is modelled and analyzed in order to explain the physical relationship

between I_G and I_C. It is theoretically verified that there is a relationship between the Miller plateau gate current, I_G and collector current, I_C. This relationship is unique for a particular IGBT structure and is only affected by temperature and process variations. As this measurement can only take place at turn-on and turn-off, this technique allows for a cycle-by-cycle measurement of I_C.

An experiment is carried out to demonstrate the feasibility of this technique. It is observed that the proposed technique could be used for voltage up to 250V and currents up to 30A with 2% inaccuracy. In addition, increasing the load side V_{DD} (or V_{CE} of the IGBT) will only increase the V_{GE} or I_G plateau length without changing the plateau level. Therefore, the proposed technique is quite robust considering the possible fluctuations of V_{DD} or V_{CE} in real applications.

An automatic gate current sensing system implemented with discrete components was constructed and tested. A Miller plateau sensing circuit has been designed such that I_G can be measured in the plateau region during the turn-on and turn-of phase of the IGBT. The value of the I_G is integrated and digitized using an ADC. A regression analysis is performed on the actual I_C and the ADC outputs. It shows the maximum deviation is less than 0.8 A for both turn-on and turn-off over the entire testing range. The testing results show that the maximum deviation is ±0.8A within the range of 1~25A for turn-on and 1~30A for turn-off.

Since this technique utilizes only the measurement of low voltage signals. It is suitable for integration into a gate driver IC. This not only reduces the system cost but also provides a platform for applications which could utilize this technique such as current regulation. The next chapter presents the design of an IGBT gate driver with an integrated collector current sensor and on-chip SPRUCE CPU for digital control and local data processing.

Chapter 3

Integrated IGBT Collector Current Sensing with Gate Driver and CPU

This chapter introduces the details of the IGBT gate driver IC design with I_C current sensing. It was demonstrated in the previous chapter that the proposed I_C sensing technique using discrete components. However, discrete components greatly increase the system complexity, cost and size. Therefore, it is not a very practical approach. Considering the fact that the proposed current sensing method only uses the low voltage gate signals, integrating the current sensing function into an IC chip is completely feasible. However, the integrated current sensing design is challenging as it involves complicated mixed signal processing. Moreover, this chip should not rely on an external FPGA to provide digital configuring and processing. An on-chip intelligent stack-based CPU could function as a programmable digital controller. The interface between the CPU and the current sensing needs to be carefully designed for performance optimization.

This chapter is organized as follows: Section 3.1 provides a system design overview of the gate driver IC chip. Section 3.2 briefly introduces the SPRUCE CPU design. Section 3.3 presents the gate driver topology and characteristics. Section 3.3-3.8 discusses all the sub-module designs in the I_C current sensor, which include the input stage, the plateau sensing circuit, the switched-capacitor integrator, the sample and hold circuit, and the Delta-Sigma ($\Delta\Sigma$) ADC. The system integration is addressed in Section 3.9. Section 3.10 summarizes this chapter.

3.1. Design Overview

The block diagram of the proposed gate driver chip is shown in Figure 3.1. It includes a segmented IGBT gate driver, a SPRUCE (Stack Processing Unit for the Controlling of Energy) unit and the collector current sensing circuit. There are three voltage domains in the gate driver IC: 1.8 V for the CPU core and gate driver logic control; 3.3 V for the CPU I/O and the current sensing circuit block; and up to 20 V for the gate driver output stage. All the current sensing function is realized within the low voltage gate driver chip block. No sensing circuit needs to access the IGBT's high voltage load side which could easily be a few hundreds of volts.

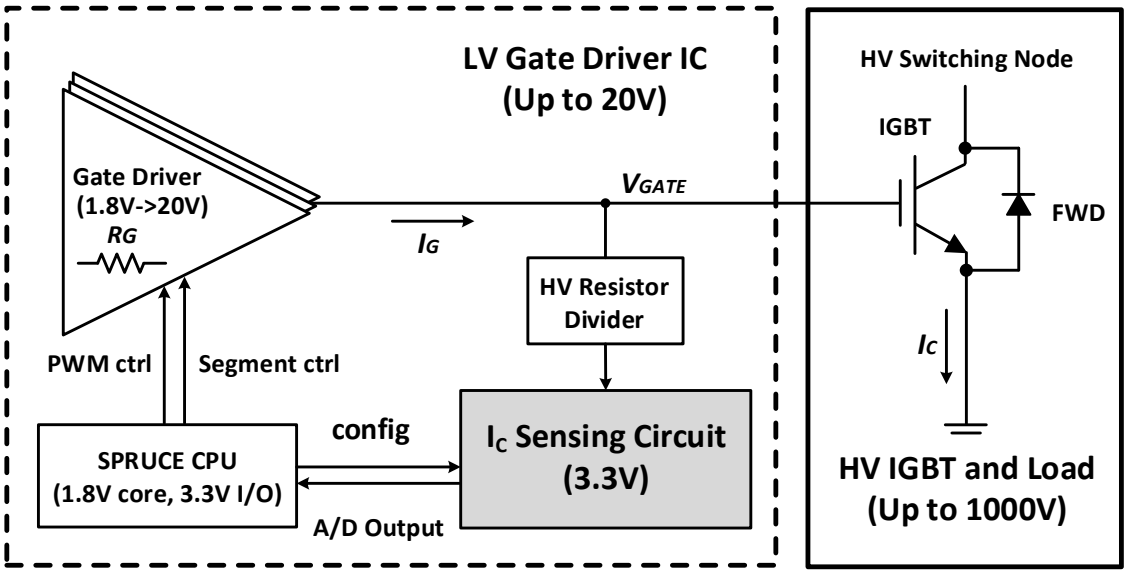


Figure 3.1: Block diagram of the proposed gate driver IC with current sensing.

The block diagram of the I_C sensing circuit is shown in Figure 3.2. First a high voltage resistor divider network scales the V_{GE} to below 3.3 V in order to be compatible with the signal processing circuit. A plateau sensing circuit block is then used to produce timing pulses that indicate the turn-on and turn-off of the plateau. These pulses serve as the triggering signals for the switched-capacitor (SC) integrator, which accumulates the voltage difference across R_G (represented by the voltage across the input and output of the gate driver with selectable output segments) inside the plateau. The sample and hold

(S/H) circuit maintains the integrator output until the next cycle. This provides sufficient time for the delta sigma (DSM) ADC to perform 100× over sampling. The output from the 1-bit DSM is fed back to the on-chip SPRUCE unit. It performs digital averaging/filtering before producing the actual ADC output.

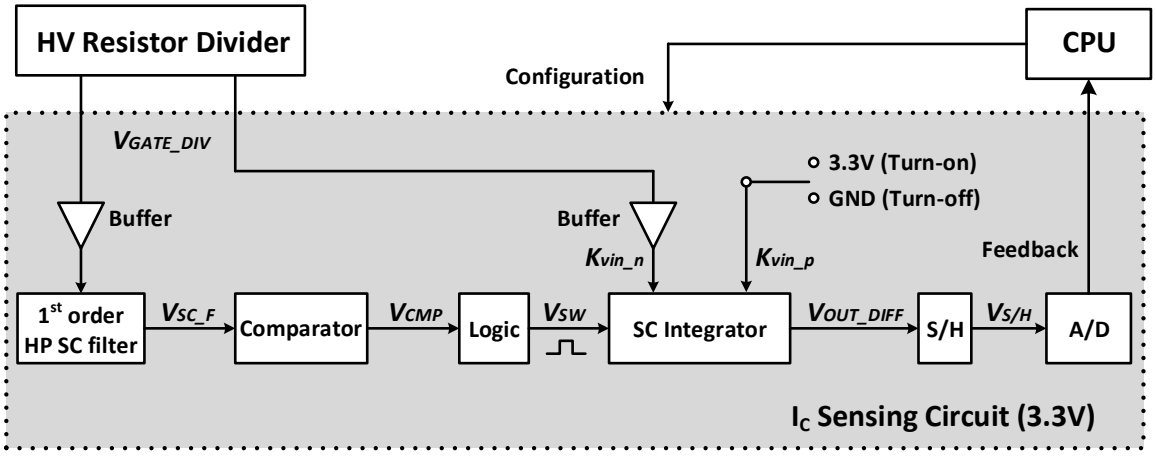


Figure 3.2: Block diagram of the I_C sensing circuit.

3.2. Embedded SPRUCE Processing Unit

Compared to conventional smart gate driver ICs, this chip does not require an external FPGA or microprocessor. The on-chip CPU could provide all the digital configuration and digital signal processing. The CPU is a simple stack based machine with a codename called SPRUCE. This process was designed by Andrew Shorten (PhD student in our group) and has been reported extensively in [78]. SPRUCE is a simple micro-controller that provides reconfigurable control functions. It also features small die area, low power consumption and ease of programming. This CPU is capable of achieving many types of closed loop control for IGBT based IPMs. In this particular design, the SPRUCE unit provides all the dynamic controls for the gate driver, all the configuration bits control and digital filtering for the DSM (Delta Sigma Modulator) output.

The block level diagram for the SPRUCE unit and its peripheral digital modules are illustrated in Figure 3.3. Included in this module are a CPU module, a SPI controller and a main memory composed of 1024 × 20 bits of memory. Several memory mapped

modules are controlled by the SPRUCE unit. They are the DPWMs (Digital Pulse Width Modulator), the gate driver and current sensing circuitry configuration bits, 20 GPI (General Purpose Input) registers and 20 GPO (General Purpose Output) registers for I/O interfaces, and a 100 bits shift register to temporarily store the DSM outputs for digital processing. All these modules are pre-mapped into dedicated memory locations and can be easily configured and accessible by the CPU.

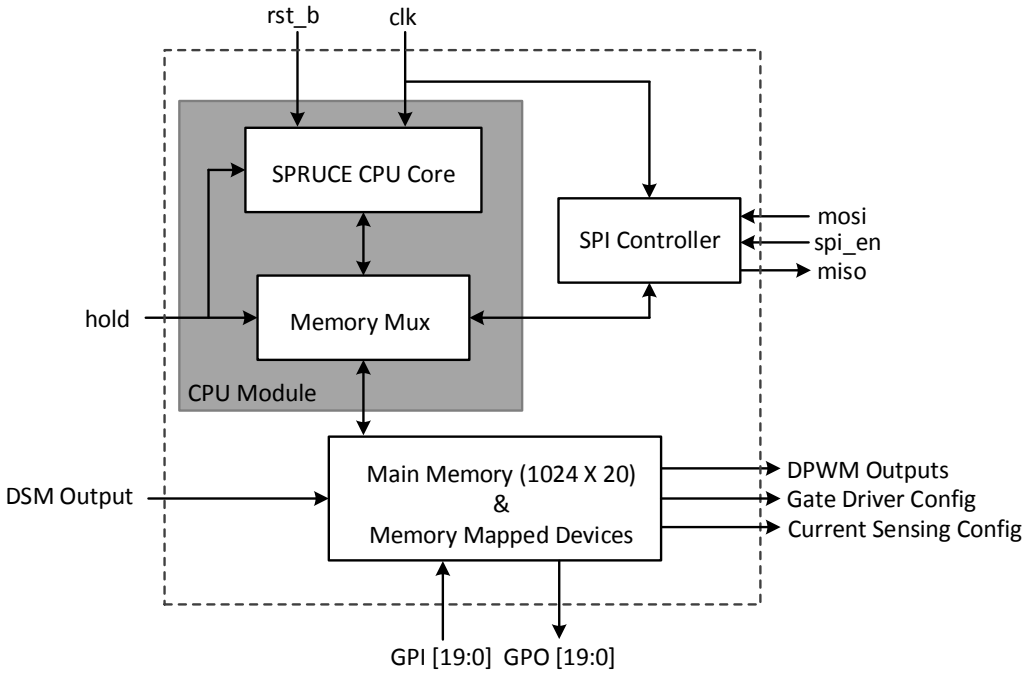


Figure 3.3: The block level diagram for the SPRUCE unit and its peripheral digital modules on the gate driver IC.

The SPRUCE unit is a simple stack machine in that the operations are performed by manipulating a stack of data. Figure 3.4 illustrates the block diagram of the SPRUCE core architecture. This CPU is different from traditional CPUs which use registers to store data being operated on. Moreover, SPRUCE differs from traditional stack machines that the stack used by SPRUCE is internal. The main advantage of this approach is a significant reduction of memory accesses performed by the CPU. For a given operation, once the operands have been loaded, no data memory access is needed until data is stored back into memory. Hence, the CPU processing speed is improved [78]. The stack in this prototype IC is constructed using D flip-flop registers, 20-bit wide each with a depth of

10. The 20-bit word length is selected based on power converter requirements for digital control, where typically 10-bit DPWM and ADC are required. Simulations also demonstrated that the depth of 10 is more than sufficient for different power converter applications. The SPRUCE unit is implemented using 4-bit instructions. Every five instructions can be packed into a 20-bit word. Table 3.1 documents each of the 16 instructions that SPRUCE uses [78].

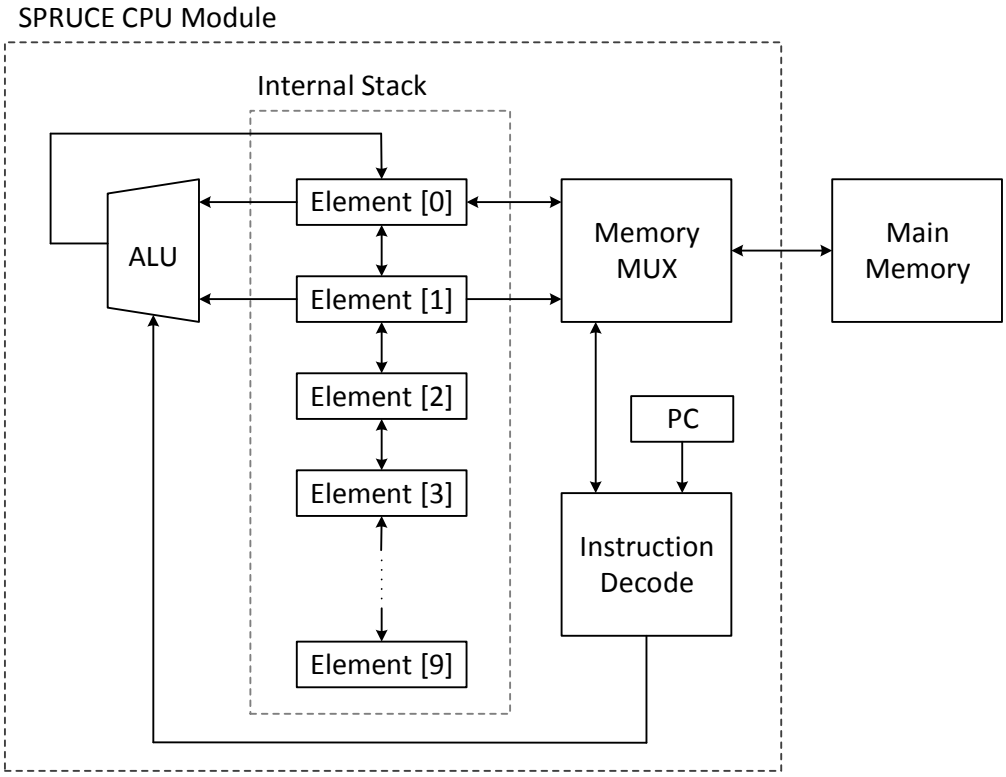


Figure 3.4: Block Diagram of the SPRUCE architecture [78].

Other than the internal stack, there are also an arithmetic logic unit (ALU), a Program Counter (PC), an instruction register and a memory MUX inside the CPU module. The ALU takes the top two elements of the stack and preform operations including ADD, SUB, NAND and SHR. The operands are then popped and the results pushed back to the top of the stack. The Program Counter holds the address of the instruction to be executed and is incremented after fetching another instruction. The instruction is stored in the instruction register and is unpacked by 4 bits at a time. A dedicated state machine controlled by the memory MUX is implemented for the instruction decode process.

Table 3.1: SPRUCE Instruction Set [78]

Name	Binary Encoding	Description
SWP	4'b0010	Swap the top two elements of the stack
DUP	4'b0011	Push a duplicate of the top element onto the stack
POP	4'b0100	Pop the top element of the stack
MUL	4'b1000	Multiply top two elements of stack, pop operands, push result
ADD	4'b1001	Add top two elements of stack, pop operands, push result
SUB	4'b1010	Subtract top two elements of stack, pop operands, push result
NAN	4'b1011	Logical NAND top two elements of stack, pop operands, push result
SHR	4'b1100	Bit-Shift second element of stack number of spaces specified in first element of stack
JME	4'b1101	Jump to addressed stored in top of stack if second and third element are equal
JMG	4'b1110	Jump to addressed stored in top of stack if second element is greater than third element
JMP	4'b1111	Unconditionally jump to addressed stored in top of stack
STR	4'b0101	Store data in second element of stack to address stored in top element of stack
LOD	4'b0110	Load data at address stored in top element of stack
PSH	4'b0111	Push the data stored in the next word of memory after the current program counter
END	4'b0000	No Operation
PPC	4'b0001	Push the program counter onto the stack, can be used to build sub-routines

The purpose of the SPI controller in Figure 3.3 is to provide an external method by which the memory space may be programmed and read. Also, the behavior of SPRUCE can be monitored for testing purposes. The SPI protocol used is as described in Figure 3.5. The conventional 4-wire serial buses are implemented here: SPI_EN, CLK, MOSI and MISO. The SPI word length is 7 bytes long: 3 bytes for an address, 3 bytes for data and 1 byte for the command to be performed by the interface. There are only two SPI commands available: read or write.

Under normal operation for the SPRUCE unit, the "hold" line is kept low and SPRUCE operates as the memory master using the protocol described in Figure 3.5. During this operation, program data is loaded from memory into the instruction register starting from address 0 and progressing linearly through memory unless jump instructions are encountered. However, when the "hold" line is brought high, control of the memory interface is passed from SPRUCE to the SPI interface.

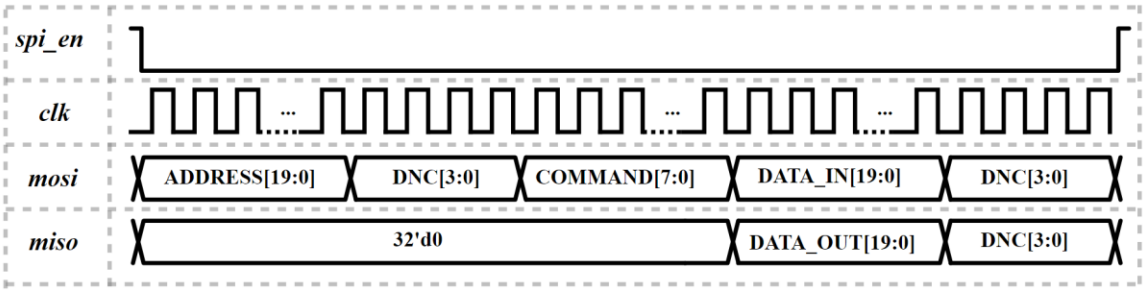


Figure 3.5: SPRUCE SPI Communication Protocol.

The SPRUCE unit can operate across a wide range of power supplies and clock frequencies. Under the power supply of 1.8V, SPRUCE could achieve stable operation with clock frequency up to 120 MHz. In this particular application, SPRUCE is running at 100 MHz. SPRUCE has been taped out and tested previously, as reported in [78]. The main change in this version is the memory size and memory map. The memory map for this chip is listed in Appendix A. The technique of using the CPU to do digital filtering for the DSM is discussed in Section 3.10.

3.3. Gate Driver Design

The gate driver uses a voltage driven topology, containing a chain of inverters with selectable output driver segments. Figure 3.6 illustrates the general schematic for one segment of the gate driver circuit. The push-pull complementary output stage is controlled by two non-overlapped signals. This is to minimize any potential overshoot current in the output stage. The inverter chain is carefully sized in order to achieve desired driving speed for the IGBTs, which typically exhibit an input capacitance of 1nF to 10nF. The digital control circuit of the gate driver circuit utilizes 1.8V low voltage devices. The actual gate drivers are operating at 3.3V to drive the gate of IGBTs. Level shifters are required to convert the 1.8 digital signals to 3.3V signals.

Figure 3.7 depicts a simplified diagram for the segmented gate driver. There are 8 output segments for pull up and pull down strength variation; ranges from 0.35 Ω to 41.9 Ω. This output stage has been implemented and characterized previously [42]. The designed

gate resistance value and the actual measured values are listed in Table 3.2. In this case, no external discrete gate resistor is needed for the IGBT.

The driver is highly configurable using the intelligent SPRUCE control, which includes output segments selection, PWM control and dynamic switching. The gate driver's performance can be easily optimized.

In this particular application, the PWM control is used to implement the "Double Pulse Technique" for the functionality test of predicting I_C. While the output segment selection function is used in order to find the appropriate gate resistance value. The desired gate resistance value should produce in a reasonable gate plateau length during the IGBT switching transients.

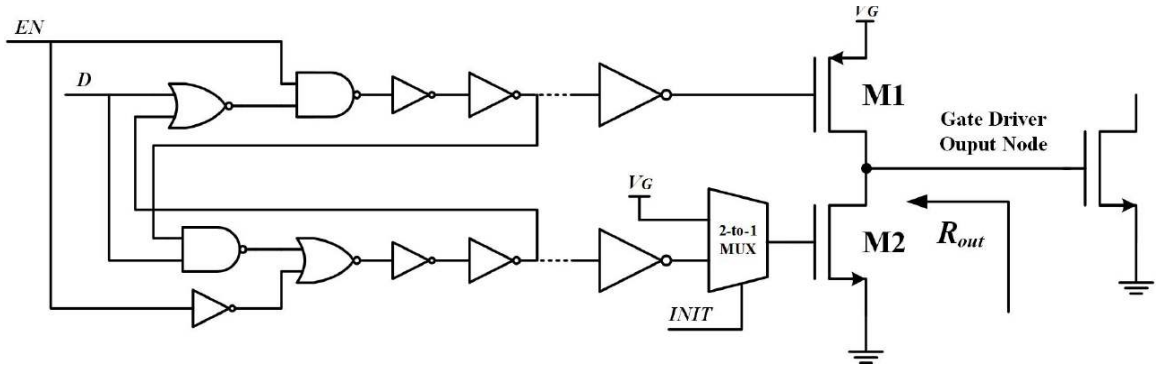


Figure 3.6: General schematic of each gate driver segment [86].

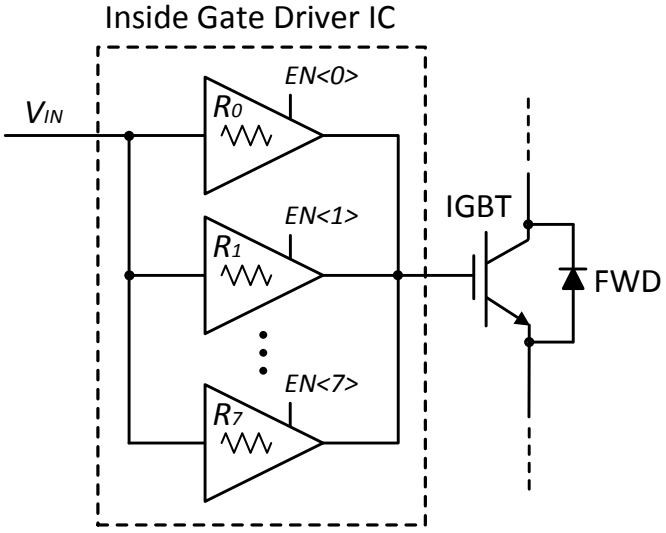


Figure 3.7: Simplified diagram for the segmented gate driver [44].

Table 3.2: Gate driver output resistance for each segment.

No. of Active Segments	Designed R_{OUT} (Ω)	Measured R_{OUT} (Ω)
0	41.9	41.6
1	21	21.6
2	10.5	11.1
3	5.26	5.77
4	2.81	3.17
5	1.41	1.71
6	0.7	0.88
7	0.35	0.46

3.4. I_C Sensing Input Stage

The I_C sensing input stage consists of a high voltage resistive divider and an analog input buffer. The resistor divider is used to bring down the voltage level at the IGBT gate from 10V~15V to below 3.3V for compatible signal processing in the I_C sensing circuit. As illustrated in Figure 3.2, the resistor dividers are needed before the switched-capacitor filter and integrator. However, an analog buffer is inserted between the HV resistor and the switched-capacitor circuits to make sure the the current sensing circuitry would not interfere with the gate driver circuit itself.

3.4.1. High Voltage Resistor Divider

The schematic of the high voltage resistor divider is depicted in Figure 3.8. The high voltage resistor divider is made configurable with high voltage (20V) NMOS transistor switches. Drivers are needed to control the HV NMOS transistors as they have relatively large input capacitor. Inverter chains are implemented to make sure reasonable turn-on and turn-off speed. Note that the switches are set before the startup of the I_C sensing circuit, therefore the driving speed for the NMOS switch is irrelevant.

The V_{OUT}/V_{IN} ratio can be configured with different combination of RC<3:0>. With the default setting, only RC<2> is on; and the ratio is 15 kΩ/51 kΩ = 0.294. The initial turn-on voltage for the high voltage side is pinned at 10V as a safety precaution. Therefore, the maximum voltage for V_{OUT} is only 2.91V. RC<3:0> can be configured using the memory mapped device in the CPU module directly.

The resistors selected for the IC implementation are high voltage N-well resistors. The resistance values are selected so that the resistor network would not draw too much current, while the current level is enough for subsequent signal processing. The top 36 kΩ resistor is in fact twelve 3 kΩ resistors connected in series. Therefore the whole resistor divider has eighteen 3 kΩ resistos in total. The layout is carefully designed to ensure matching for the resitor network, as N-well resistors usually exibit large variations in resistance values. The layout for the HV resistor divider network is shown in Figure 3.9.

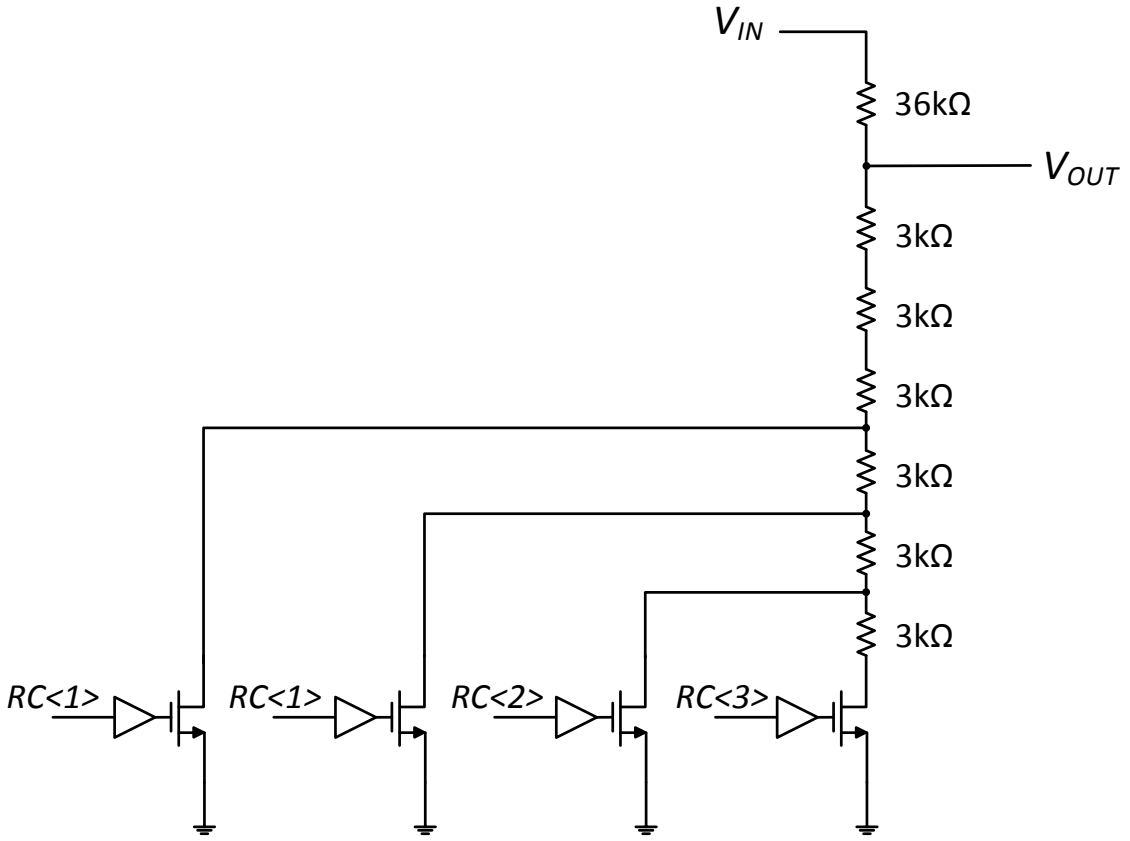


Figure 3.8: High voltage resistor divider network.

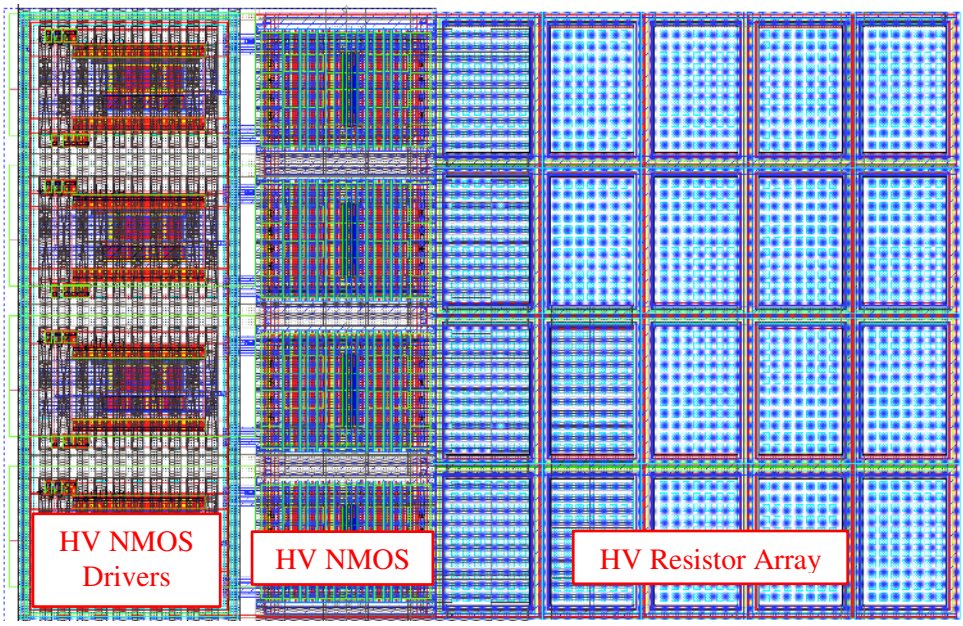


Figure 3.9: HV resistor divider layout. The total area used is 440µm × 270µm.

3.4.2. Input Analog Buffer

The design focus for the analog input buffer is to ensure fast output response speed and good linearity especially around the plateau voltage level. A simple two-stage op-amp is designed and used as a unity gain non-inverting configuration to realize the input buffer. The two-stage op-amp schematic is shown in Figure 3.10 with all transistor sizes and passive components values labeled.

The input signal to the input buffer is the output of the HV resistor divider, basically a scaled version of the switching IGBT gate signal. The intrinsic IGBT switching frequency is low, only around 20 kHz in this case. However, it is mandatory to preserve the waveform around the turn-on and turn-off plateau region where the signal is going through fast transient. The amplifier design should maintain signal fidelity at the frequency of interest and therefore the targeted unity gain bandwidth for the op-amp is above 25 MHz. The target open loop DC gain for the op-amp is above 70 dB to ensure that the close loop gain error is less than 0.03 %.

Considering the subsequent stage after the input buffer is either the SC filter or SC integrator, and different loading capacitors will be introduced to the input buffer. As will

be discussed later, the input capacitor of the SC filter is estimated to be around 800 fF, while that of the SC integrator is around 200 fF. The input buffer itself is loaded with a capacitor of 4.5 pF. Figure 3.11 shows the open loop frequency response of the input buffer when it is connected to the SC filter; the obtained DC gain is 77 dB and unity gain frequency is 31 MHz. Figure 3.12 shows the open loop frequency response when connected to the SC integrator; the DC gain is 77.7 dB and unity gain frequency is 32.3 MHz.

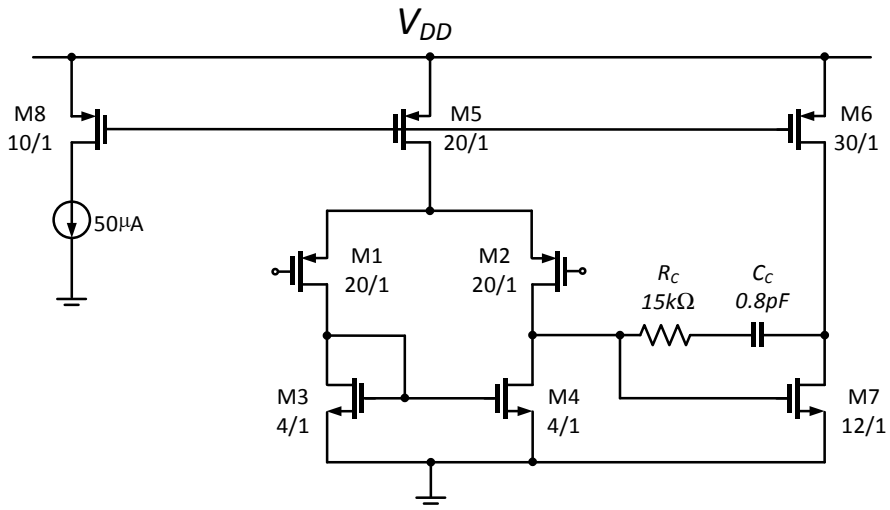


Figure 3.10: Schematic of the two-stage op-amp used as the input buffer. The transistor size unit is in µm.

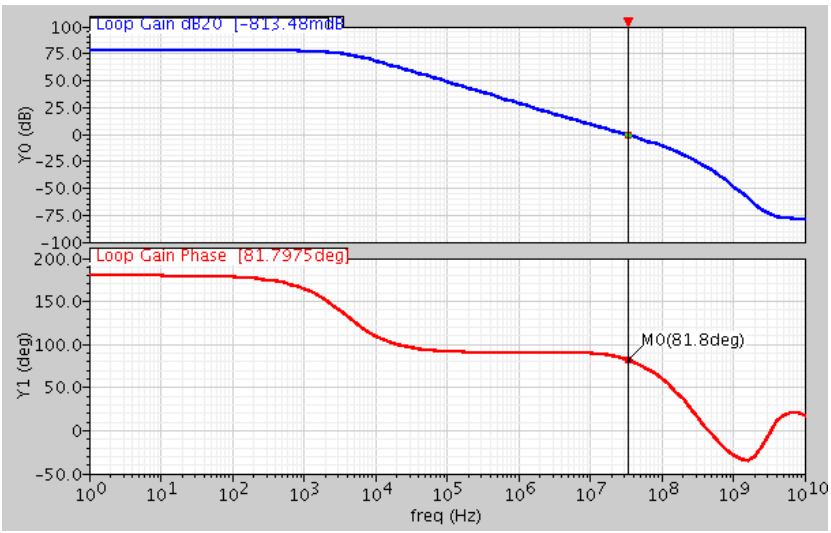


Figure 3.11: Input buffer open loop frequency response when connected to SC filter.

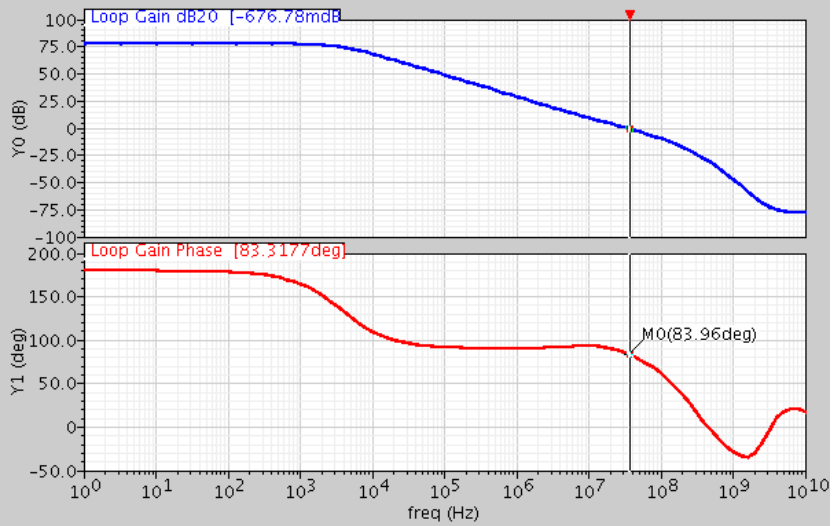


Figure 3.12: Input buffer open loop frequency response when connected to SC integrator.

The transient simulation result for the input buffer is shown in Figure 3.13. The resistor divider output is the input for the buffer. The input is purposely set to a have large swing range to demonstrate the output swing limit of the input buffer. However, the system performance would not be affected even if the input is slightly over this range, since we only need the signal to be accurate around the plateau region. The voltage level should be only around 1~2V. In practice, the input is controlled to be within the acceptable swing range of the input buffer. This can be realized through the configurable resistive divider.

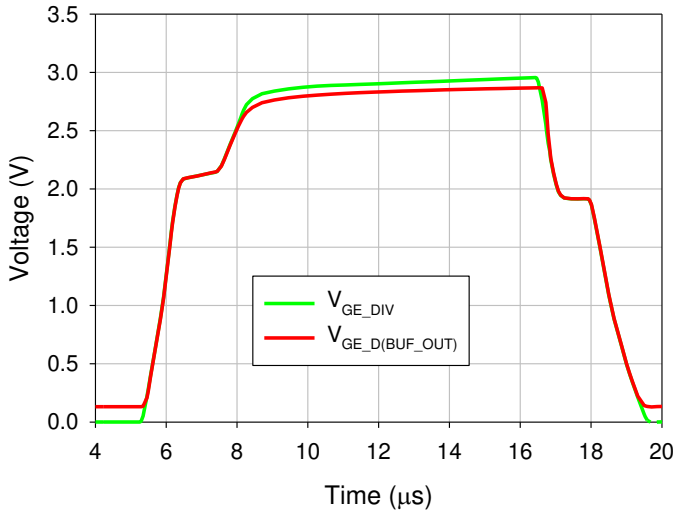


Figure 3.13: Transient simulation results for the input buffer block.

The layout for the input buffer block is shown in Figure 3.14. All the capacitors used in this chip are the MIM capacitor between M4 and M5.

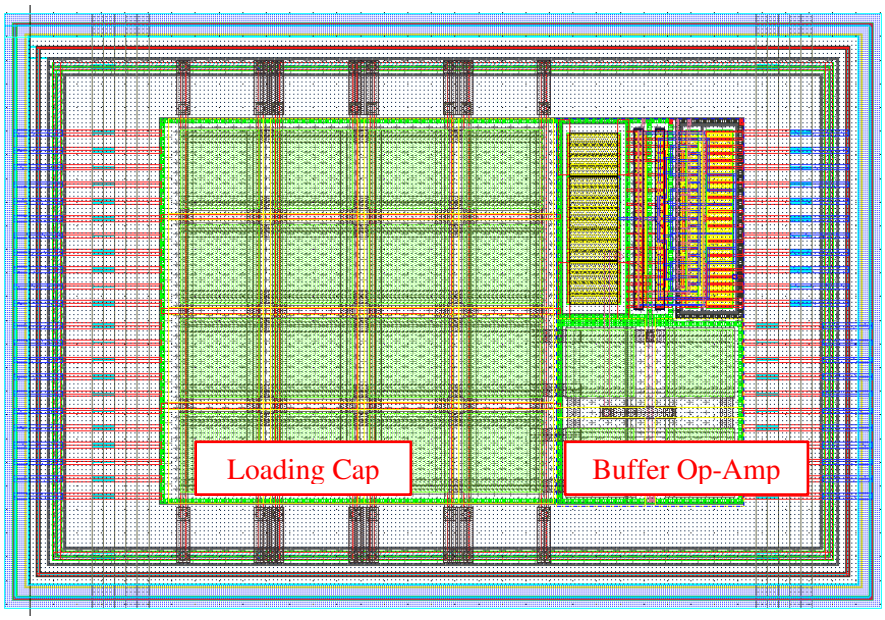


Figure 3.14: Layout for the input buffer block. The total area used is 125µm × 185µm.

3.5. Plateau Sensing Circuit Block

The plateau sensing circuit consists of a switched-capacitor (SC) filter, a comparator and a logic block. The SC filter is used to catch the plateau region during turn-on and turn-off switching transients. The filter output will be digitized by a comparator. A logic block is employed to implement the fixed time integration technique as introduced in Section 2.3.4.

The design and target specifications of the plateau sensing circuit block are based on the previous discrete implementation. In order to accommodate the integrated design, the continuous time filter is changed to switched-capacitor filter. This is because it is difficult to have high precision resistors and capacitors in the IC environment. The switched-capacitor circuits could achieve higher accuracy as long as the matching between capacitors is properly managed in the layout design. In addition, the sensitivity of temperature change on the filter characteristics is greatly reduced compared to continuous RC filter, where both the resistor and capacitor are sensitive to temperature change.

3.5.1. Switched-Capacitor Filter Design

Referring to the discrete design, the desired filter is a bandpass filter. However, the classic switched-capacitor bandpass filter design is usually two-stage and the design procedure can be complicated. Therefore, it was decided that the bandpass filter should be realized as a first order high pass filter, with the loading capacitor made relatively large and the sampling switch made relatively small. The first order high pass filter is constructed based on the typical first order switched-capacitor filter circuit as shown in Figure 3.15. This is a single ended implementation. The final design is fully differential with the same transfer function but better performance in terms of common-mode noise rejection.

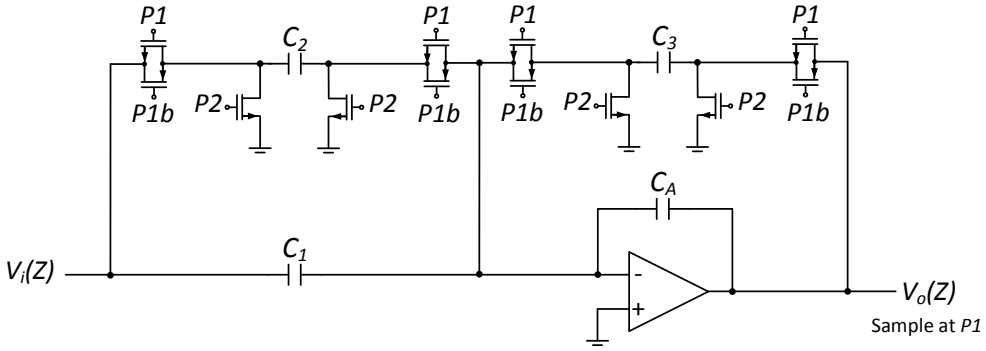


Figure 3.15: A typical first order switched-capacitor filter [87].

The general transfer function for the filter shown in Figure 3.15 is [87]:

$$H(\mathrm{z}) = \frac{V_o(\mathrm{z})}{V_i(\mathrm{z})} = -\frac{(\mathrm{C_1}+\mathrm{C_2})\,\mathrm{z}-\mathrm{C_1}}{(\mathrm{C_A}+\mathrm{C_3})\,\mathrm{z}-\mathrm{C_A}} \tag{3.1}$$

Equation (3.1) contains one zero and one pole. The zero is found by equating the numerator to zero, which results in:

$$Z_Z = \frac{C_1}{C_1 + C_2} \tag{3.2}$$

The denominator is found by equating the denominator to be zero, which results in a pole location, given by:

$$Z_P = \frac{C_A}{C_A + C_3} \tag{3.3}$$

Recall from Section 2.3.2 that the bandpass filter in the discrete design has a frequency response that peaks at around 700 kHz for turn-off and 2.4 MHz for turn-on plateau sensing. For this high pass filter, we need a pole at around 1.5 MHz. In addition, the desired gain at DC should be zero. This means placing a zero at 1 in the z-domain. The sampling frequency is chosen to be 15 MHz. Considering the frequency warping between the s-domain and z-domain, where

$$s = \frac{z-1}{z+1} = \frac{e^{j\omega}-1}{e^{j\omega}+1} = j\tan(\frac{\omega}{2}) \tag{3.4}$$

and a pole of 1.5 MHz with a clock frequency of 15 MHz, this translates to an ω of 0.2π rad/sample. Therefore:

$$\Omega = \tan(\frac{\omega}{2}) = \tan(\frac{0.2\pi}{2}) = 0.3294 \tag{3.5}$$

This means that in the continuous time domain, we have the pole at:

$$P_P = -0.3249 \tag{3.6}$$

Mapping this pole back to the z-domain:

$$Z_P = \frac{1+P_P}{1-P_P} = 0.5095 \tag{3.7}$$

Therefore, the transfer function of this filter is given by:

$$H(\mathrm{z}) = \frac{k(\mathrm{z}-1)}{z-0.5095} \tag{3.8}$$

Only moderate gain is needed for this filter, and k is thus determined by setting the gain equal to about 20 when the frequency in the continuous time domain is 3 MHz (this translates to the z-domain value of 0.7265). In this case, k is chosen to be 8.

Equating the coefficients of Equation (3.8) to (3.1), this results in:

$$\begin{aligned} C_1 &= -8C_A \\ C_2 &= 0 \\ C_3 &= C_A \end{aligned} \tag{3.9}$$

Note that C_1 is negative. While in fully differential implementation, the effective negative capacitance can be realized by interchanging the input wires [87]. The value for capacitor C_A is determined to be 100 fF. The final filter schematic and capacitor sizing are shown in Figure 3.16.

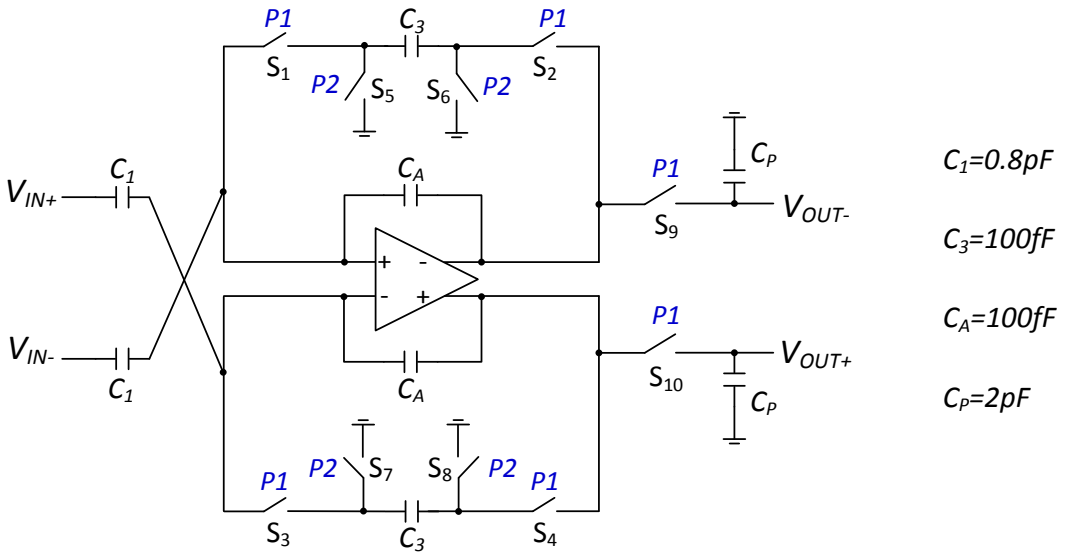


Figure 3.16: Switched-capacitor filter schematic.

The switches are mostly realized using transmission gates to allow signals passing through with a wider swing, except those with one end connected to the ground are realized using NMOS only. The switches are sized such that the settling time of the RC components are much less than half of the switching period, 33.33 ns in this case (15 MHz sampling frequency). Table 3.3 lists the sizes and properties for all the switches shown in Figure 3.16. For each transmission gate, The NMOS and PMOS are designed to have the same size for better charge injection cancellation.

Table 3.3: Transistor sizes and properties for the switches in the SC filter.

Switch		S1, S2, S3, S4	S5, S6, S7, S8	S9, S10
Type		Transmission Gate	NMOS	Transmission Gate
Size (µm) and R_{ON}	NMOS	W/L = 5/0.6 (500 Ω)	W/L = 5/0.6 (500 Ω)	W/L = 5/0.6 (1.26 kΩ)
	PMOS	W/L = 5/0.6 (1.2 kΩ)		W/L = 5/0.6 (3 kΩ)

The sampling capacitor (C_P) and sampling switch (S9 and S10) form a low pass filter with a corner frequency at around 40 MHz. The overall frequency response of the SC filter is simulated using Spectre PSS analysis and the result is shown in Figure 3.17. The frequency response peaks at around 3MHZ with a moderate gain of 18 dB.

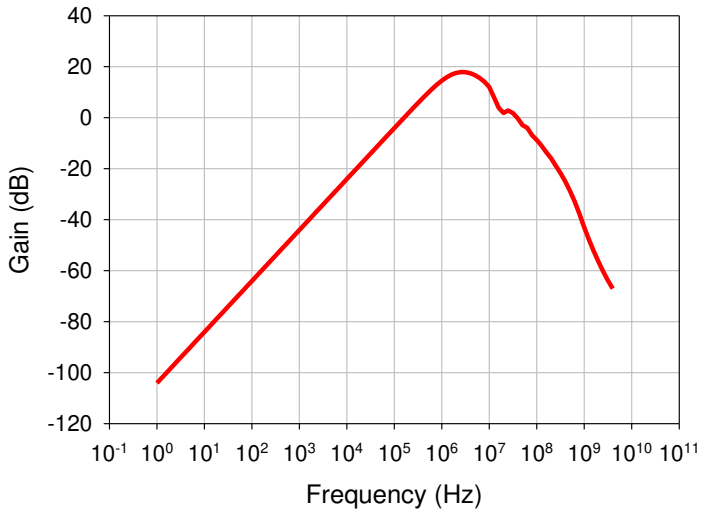


Figure 3.17: Switch capacitor filter frequency response using Spectre PSS analysis (with real transistors for the op-amp).

For the transient analysis of the SC filter, the scaled IGBT gate signal is applied to the filter at K_{vin_p} while K_{vin_n} is grounded, the output waveform is a series of weak analog double pulses where the time in between correspond to the Miller plateau region during turn-on and turn-off, as illustrated in Figure 3.18. The filter output is fully differential with a common mode voltage of 1.65V, where the positive output ($V_{SC\_F\ (turn\_on)}$) is for turn-on plateau sensing and the negative output ($V_{SC\_F(turn\_off)}$) is used for turn-off plateau sensing.

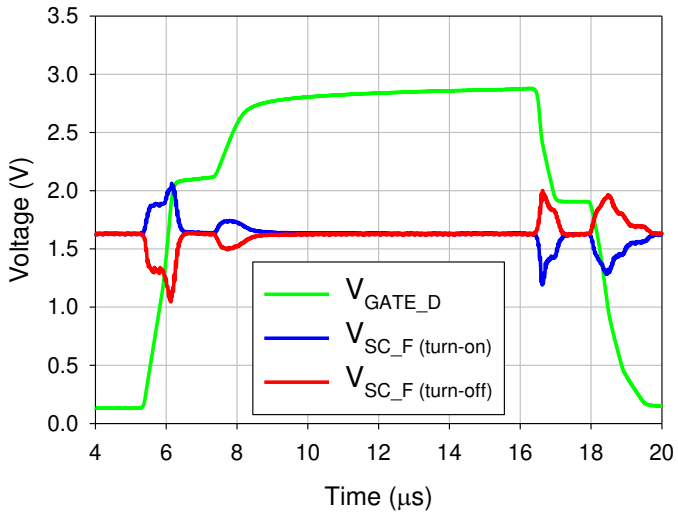


Figure 3.18: Simulated response for the Miller plateau detection at the output of the high pass (HP) SC filter (with real transistors for the op-amp).

Both Figure 3.17 and Figure 3.18 are simulation results with real transistor models. The op-amp design for the SC filter block is discussed in the next section.

3.5.2. Folded-Cascode Op-amp Design

The op-amp design for the SC filter requires large DC gain to achieve high DC accuracy. In order to save the design effort, the same op-amp is used in the SC integrator and also the ΔΣ ADC. The SC integrator is also switching at 15 MHz and the ΔΣ ADC has a system sampling clock at 10 MHz. Therefore, this op-amp should have relatively larger input and output swings to accommodate signals at different conditions. Based on all above considerations, the gain-boosted folded-cascode topology is employed for the op-amp. The design targets for this op-amp are a DC gain larger than 70 dB, a unity gain frequency great than 100 MHz, and an output swing larger than ±1.2 V. The power consumption should be less than 15 mW with a V_{DD} of 3.3 V.

The schematic for the main branch of the folded-cascode op-amp is shown in Figure 3.19. The op-amp is designed such that 49% of the current will go through the output branch, and the remaining 51% of the current will go through the input differential pair branch. During a slew rate event, the output branch would still have current flowing to help the

transistors to get out of the triode faster. Table 3.4 lists the transistor sizes for the main branch of the folded-cascode op-amp. All the transistors are implemented using the 5V devices in TSMC's 0.18 µm BCD Gen2 technology, where the minimum gate length for the NMOS is 0.5 µm and for PMOS is 0.6 µm. In order to achieve higher speed, all the transistors (both NMOS and PMOS) are set to have channel length of 0.6 µm for simplicity.

The PMOS input pair is chosen over NMOS-input pair as PMOS input pair has better phase margin, lower flicker noise and can accommodate lower input voltage level. Both the common mode input voltage and the common mode output voltage for the op-amp is set to be 1.65 V. Since this op-amp has a differential output, the dynamic common-mode feedback (CMFB) circuit is needed to maintain the output common mode voltage in all situations. The detailed CMFB circuit will be introduced later.

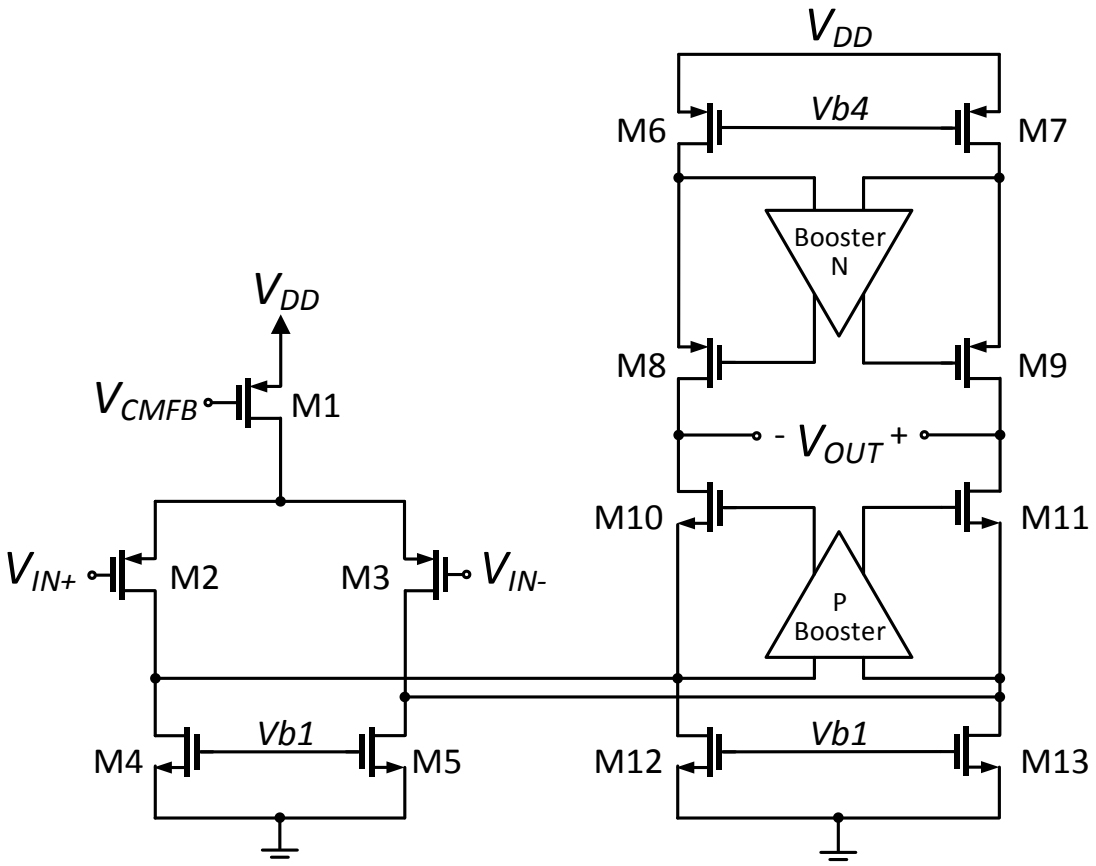


Figure 3.19: Schematic for the gain-boosted folded-cascode op-amp.

Table 3.4: Transistor sizes for the folded-cascode op-amp.

Transistor	W/L	Fingers
M1	12µm/0.6µm	20
M2, M3	12µm/0.6µm	20
M4, M5	5µm/0.6µm	10
M6, M7	12µm/0.6µm	10
M8, M9	12µm/0.6µm	10
M10, M11	5µm/0.6µm	10
M12, M13	5µm/0.6µm	10

The schematic for the op-amp biasing circuit is shown in Figure 3.20. Wide swing cascade current mirrors are used to generate the bias voltages for the cascode devices.

Table 3.5 lists all the sizes for the transistors in the biasing circuit. In order to minimize the current consumption, all the transistors are having a single finger. The biasing circuit is designed such that all the transistors in the main op-amp and gain boosting amplifiers are biased in saturation region with desirable input and output swing range. The obtained biased voltage levels are listed in Table 3.6.

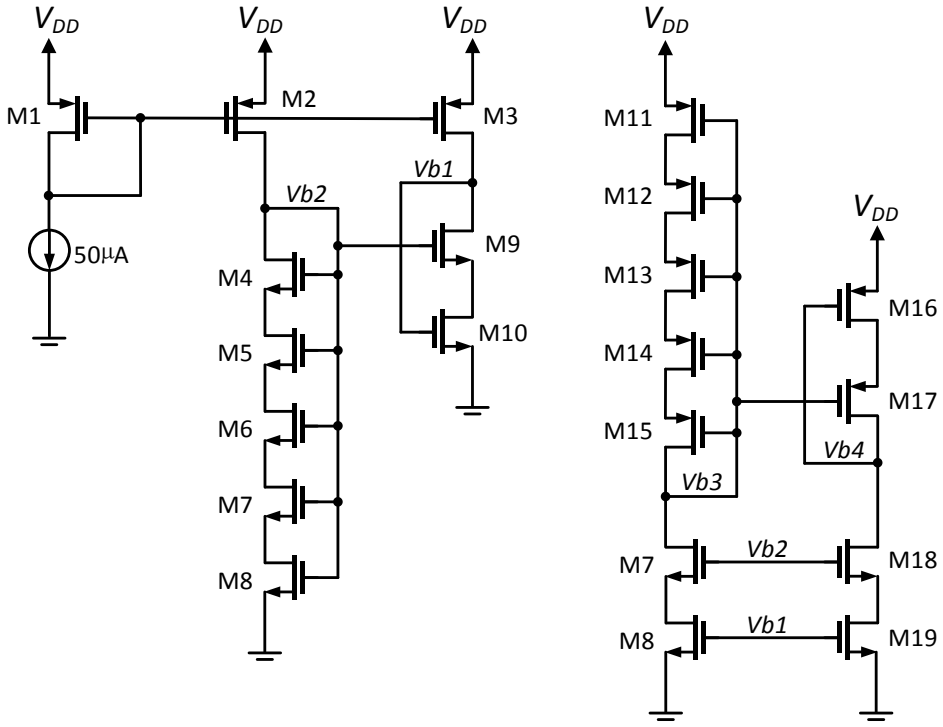


Figure 3.20: Schematic for the op-amp bias circuit.

Table 3.5: Transistor Sizes for the Op-amp Bias Circuit

Transistor	W/L	Fingers
M1, M2, M3	15 µm/0.6 µm	1
M4, M5, M6, M7, M8	6 µm/0.6 µm	1
M9, M10	6 µm/0.6 µm	1
M11, M12, M12, M14, M15	15 µm/0.6 µm	1
M16, M17	12 µm/0.6 µm	1
M18, M19, M20, M21	6 µm/0.6 µm	1

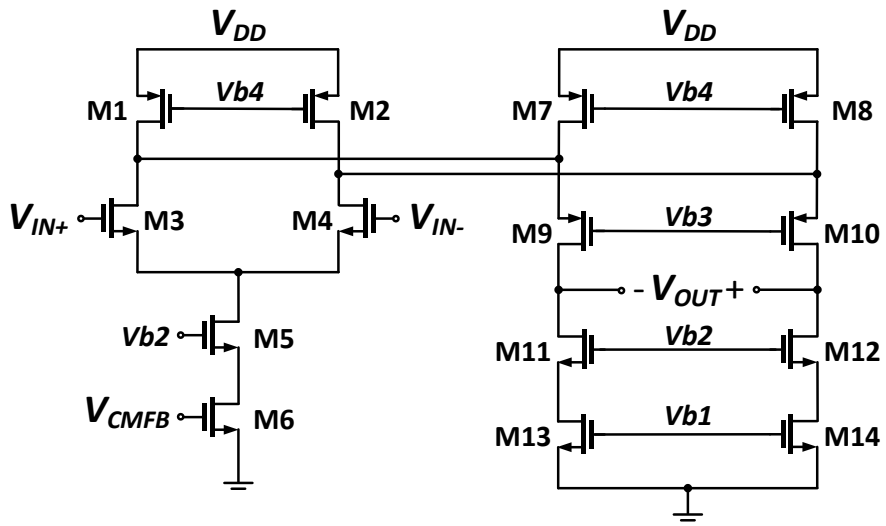
Table 3.6: Bias voltage levels for the op-amp.

Bias Voltages	Voltage
Vb1	1.12 V
Vb2	1.74 V
Vb3	1.50 V
Vb4	2.19 V

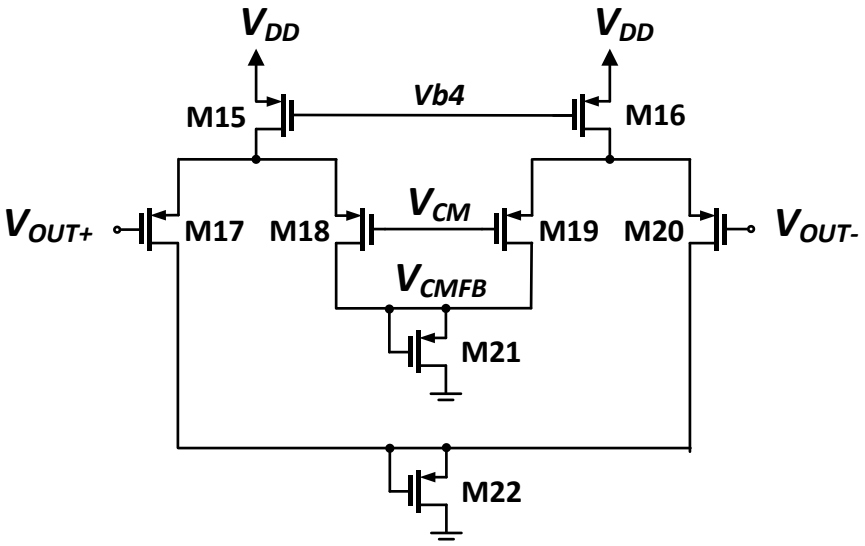
There are two gain-boosting stages shown in Figure 3.19. Without the gain-boosting, the op-amp's low frequency gain is only around 40dB. This would introduce significant third harmonic distortions into the switched-capacitor circuits.

The NMOS input gain booster (n-booster) is used to handle the higher voltage inputs. The schematic is shown in Figure 3.21 and the transistor sizes are shown in Table 3.7. The PMOS input gain booster (p-booster) is employed to handle the lower voltage inputs. The schematic for the p-booster is shown in Figure 3.22 and the transistor sizes are listed in Table 3.8. The gain-boosting technique basically amplifies the output resistance of transistors M8, M9, M10 and M11 in Figure 3.19. Therefore, the final DC gain the op-amp can be increased substantially.

Stability analysis needs to be carried out to demonstrate the loop stability of the gain boost circuits. The AC analysis results for the n-booster and p-booster are presented in Figure 3.23 and Figure 3.24, respectively. In order to stabilize the loop, a compensation capacitor (C_C) of 100 fF is added in the n-booster and a C_C of 50 fF is added in the p-booster. It should be noted that the unity gain frequency of the gain boost circuit should be much larger than the unity gain bandwidth of the main op-amp without the gain boosters.



(a)

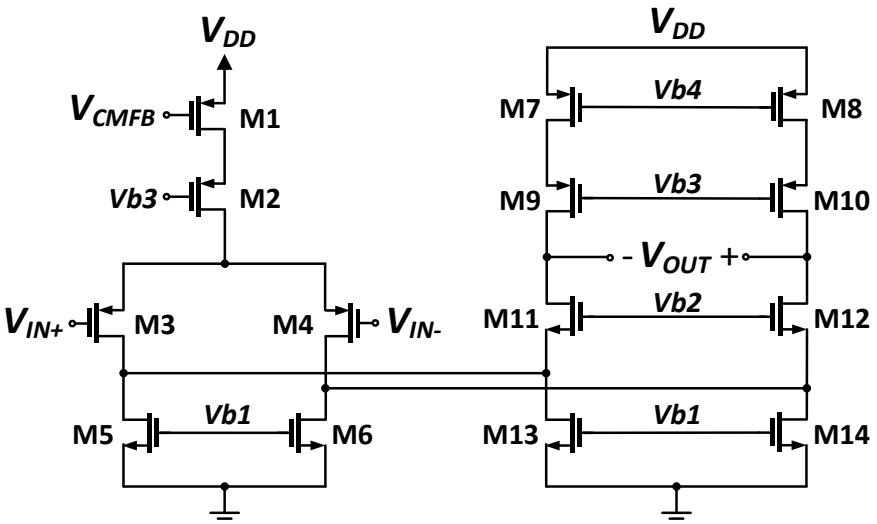


(b)

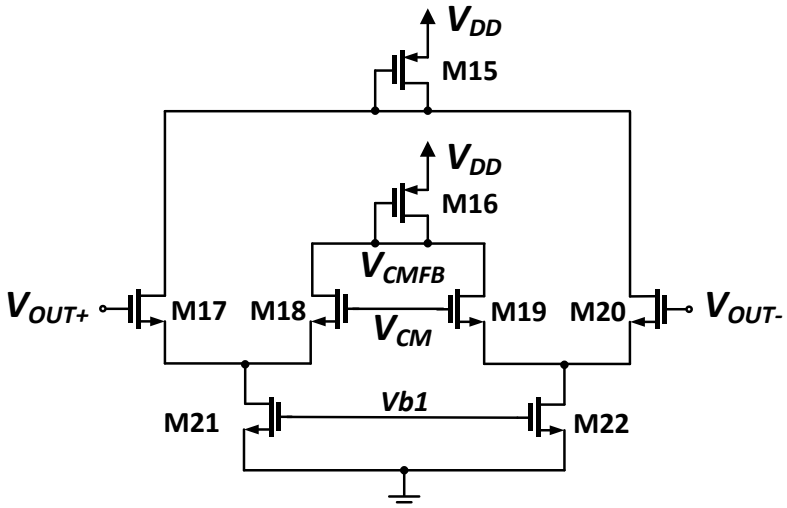
Figure 3.21: Schematic of the n-booster circuit (a) main circuit branch (b) CMFB circuit.

Table 3.7: Transistor Sizes and Properties for the Switches in the n-Booster

Transistor	W/L	Fingers
M1, M2	15 µm/0.6 µm	2
M3, M4, M5, M6	12 µm/0.6 µm	2
M7, M8, M9, M10	15 µm/0.6 µm	2
M11, M12, M13, M14	6 µm/0.6 µm	2
M15, M16	16 µm/0.6 µm	1
M17, M18, M19, M20	8 µm/0.6 µm	1
M21, M22	6 µm/0.6 µm	1



(a)



(b)

Figure 3.22: Schematic of the p-booster circuit (a) main circuit branch (b) CMFB circuit.

Table 3.8: Transistor Sizes and Properties for the Switches in the p-Booster

Transistor	W/L	Fingers
M1, M2, M3, M4	15 µm/0.6 µm	4
M5, M6	6 µm/0.6 µm	2
M7, M8, M9, M10	15 µm/0.6 µm	2
M11, M12, M13, M14	6 µm/0.6 µm	2
M15, M16	15 µm/0.6 µm	2
M17, M18, M19, M20	6 µm/0.6 µm	1
M21, M22	5 µm/0.6 µm	2

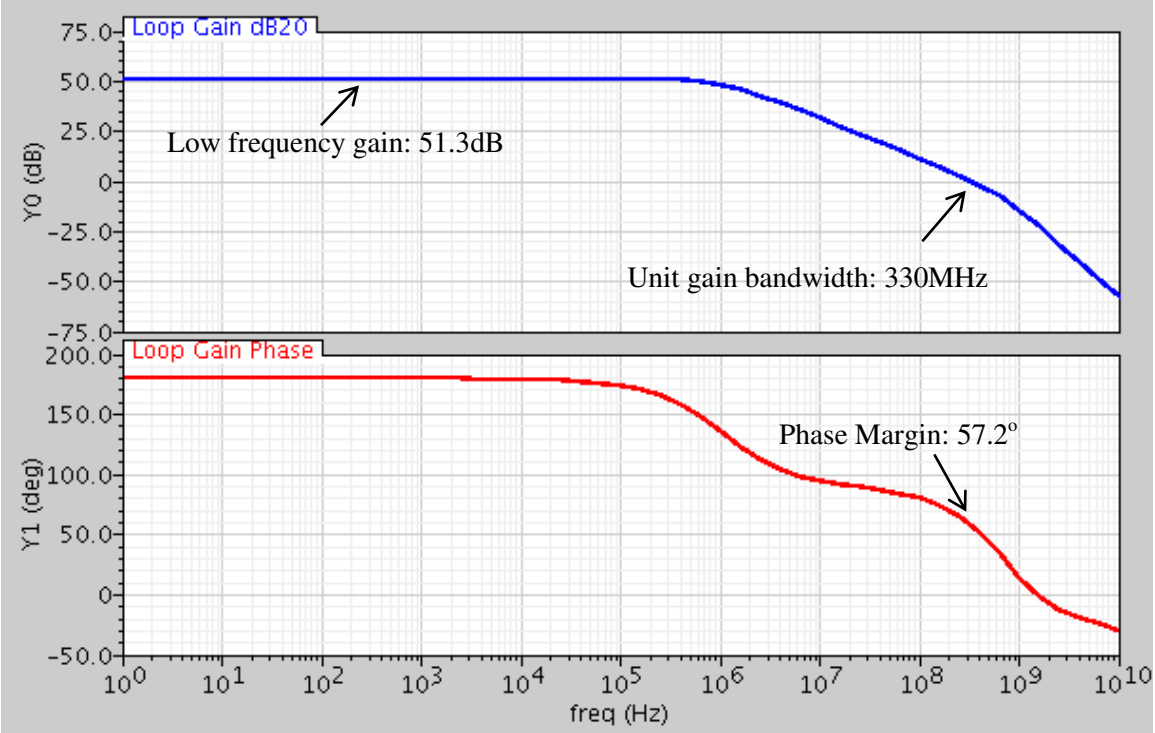


Figure 3.23: Stability analysis result for the n-booster.

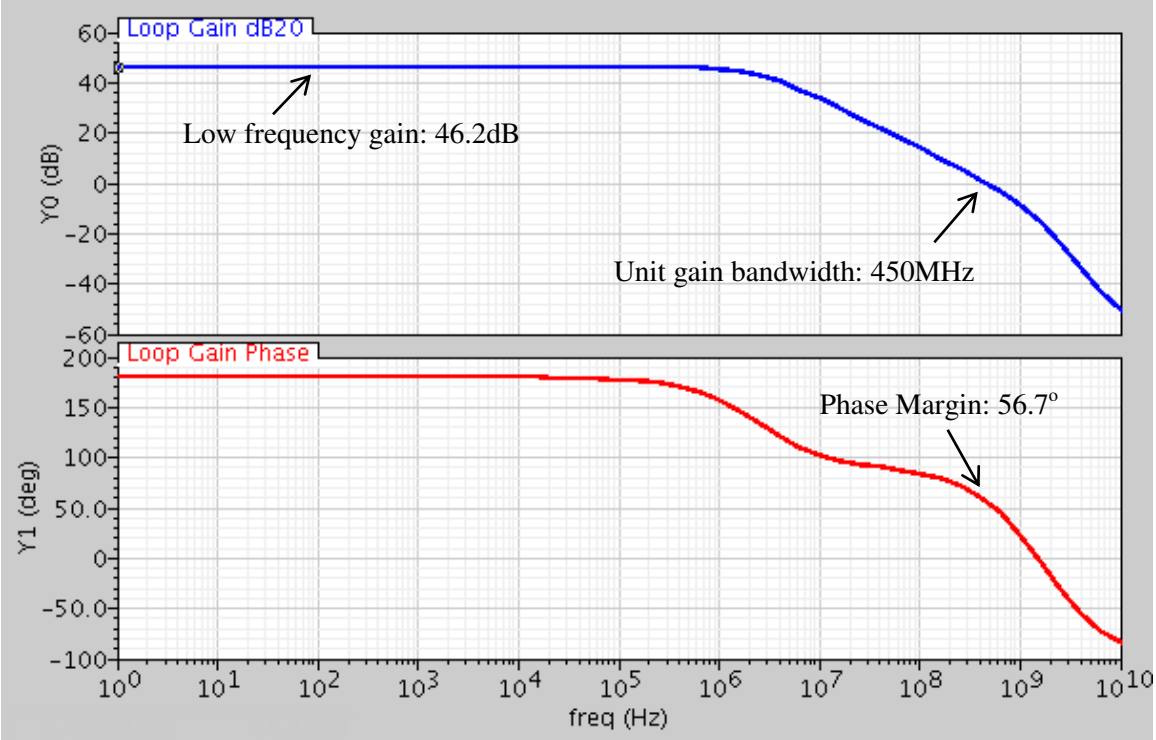


Figure 3.24: Stability analysis result for the p-booster.

CMFB circuits are needed for both the main op-amp and the gain boosters as they all have fully differential outputs. For the gain boosters, the CMFB stages are continuous time circuits. This is because the output swings of the boosters do not vary that much. Therefore, continuous CMFB should be sufficient. The CMFB loop stabilities for the both gain boosters are also verified through simulations.

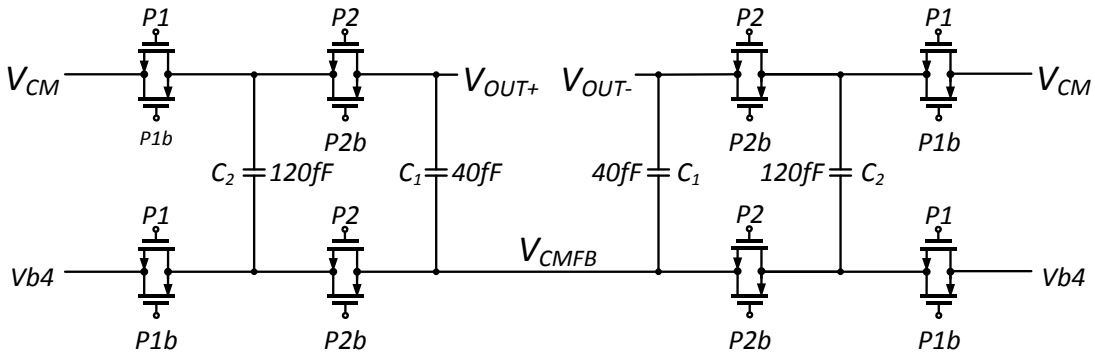


Figure 3.25: Schematic of the switched-capacitor CMFB circuit.

For the main op-amp, the CMFB circuit should allow much larger output swing. Therefore, a dynamic switched-capacitor CMFB topology is implemented, as illustrated in Figure 3.25. When clock P1 is on, the voltage differences between the reference voltages V_{CM} and V_{b4} is stored in capacitor C_2. When clock P2 is on, the reference voltages controls the output dc levels through C_1. The value for C_1 should be reasonably sized as it would overload the output nodes, degrading the op-amp performance. However, smaller C_1 may cause the common mode voltage to deviate from the desired level due to charge injection. Minimum sized transmission gates (for both NMOS and PMOS are W/L = 1 µm/0.6 µm) are used in the CMFB circuits to alleviate the charge injection effect.

The SC CMFB circuit needs to be driven by non-overlapping two-phase clocks. Inside each op-amp, there is a clock generator which serves the SC CMFB only. When the op-amp is put inside the SC filter, SC integrator or the DSM, the clock of the CMFB circuit must be synchronized with the switched-capacitor system clock. This is to minimize any distortion during the sampling point resulted from the CMFB circuit settling. In addition, the CMFB clock does not need to operate as fast as the system clock in order to save power. For example, in the SC filter block, the system clock is 15 MHz. The CMFB

clock is set to be 4 times slower with a clock divider, which is 3.75 MHz. Figure 3.26 illustrates the transient response of the CMFB circuit when a 100 mV common mode step disturbance is applied to the input of the op-amp. It can be seen that the settling time of the CMFB circuit (from V_{DD} to the common mode) is around 1 µs with a CMFB clock frequency of 3.75 MHz. In addition, both the op-amp outputs are plotted to show that the common mode disturbance would not result in any differential signal drift.

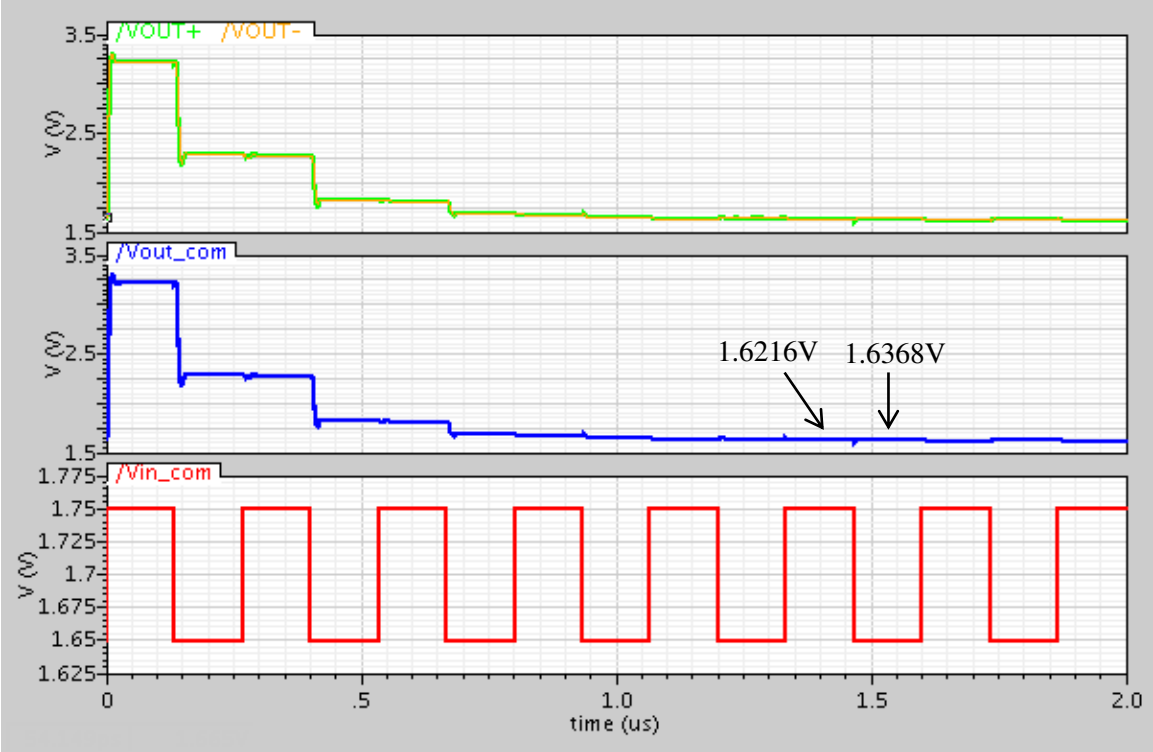


Figure 3.26: Transient response of the CMFB circuit with a 100mV common mode input step disturbance.

For the loop configuration and loading condition in the SC filter, the AC amplitude and phase response of the final op-amp is shown in Figure 3.27. The CMFB circuit is replaced by an ideal CMFB circuit with equivalent resistive and capacitive loading for the AC simulation. The low frequency DC gain is 79.3 dB, and unity gain bandwidth is 161 MHz with a phase margin of 84°. The loading conditions used here is when the op-amp is put in the SC filter at P1 state. At P2 the open-loop gain bandwidth will be 120 MHz and phase margin is 88°. No extra compensation capacitors are needed for the SC filter case. The bandwidth and phase margin are over designed to allow enough margins for the mismatches in the layout and fabrication processes. When the op-amp is used in

the SC integrator and DSM, the loading conditions are slightly different and the AC simulation results will be discussed later on.

Other than the AC simulations, all the remaining characteristics of the op-amp are simulated with the real CMFB circuit. The simulation results are summarized in Table 3.9. The maximum output swing that could be achieved is ±1.4V, wider than the required ±1.2V range.

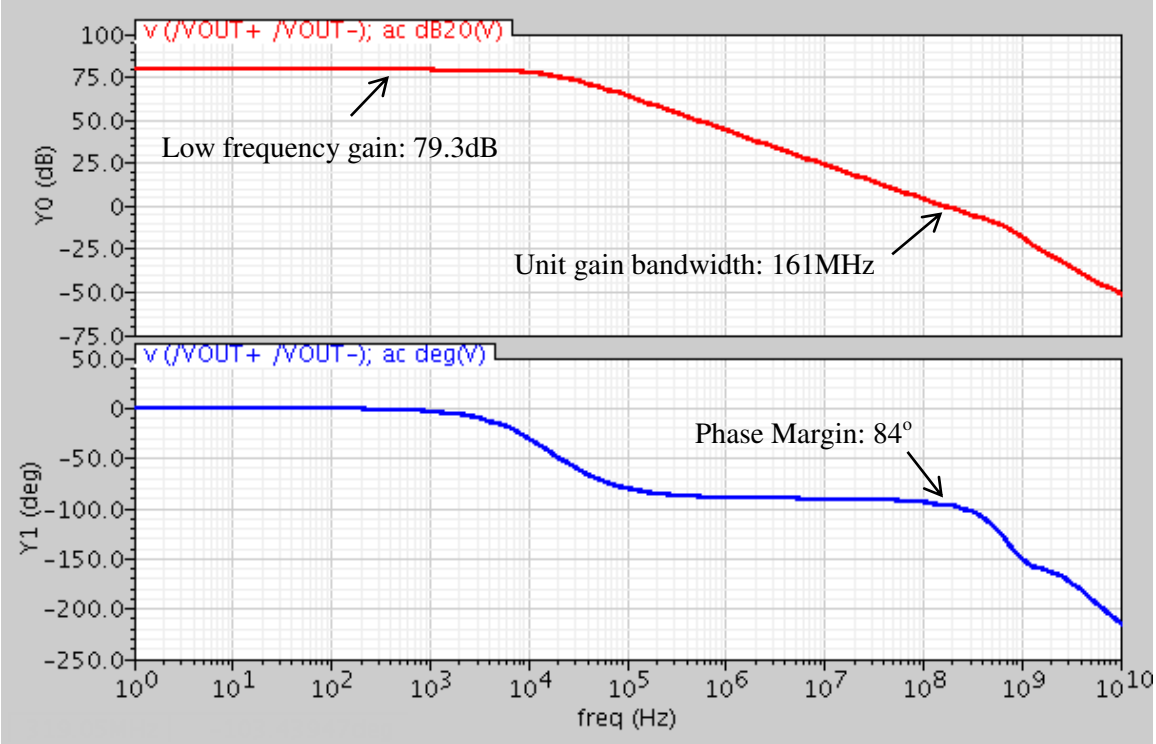


Figure 3.27: Amplitude and phase response of the folded cascode op-amp.

Table 3.9: Summary of the Simulation Results for the Folded Cascode Op-amp

Parameters	Simulation Results
Supply Voltage	3.3 V
Power Consumption	13.2 mW
Low-Frequency Gain	79.3 dB
Unity gain Frequency	161 MHz
Phase Margin	84°
Output Swing	±1.4 V
Slew Rate	680 V/µs
Settling Time (0.05%)	3.7 ns

The layout of the designed op-amp is shown in Figure 3.28. In order to minimize the offsets, all the transistors are carefully laid out using interdigitated patterns with dummy transistors laid at the edges. The CMFB circuit layout is symmetric for both the transistors and the capacitors. Figure 3.29 shows the actual SC filter layout for this op-amp.

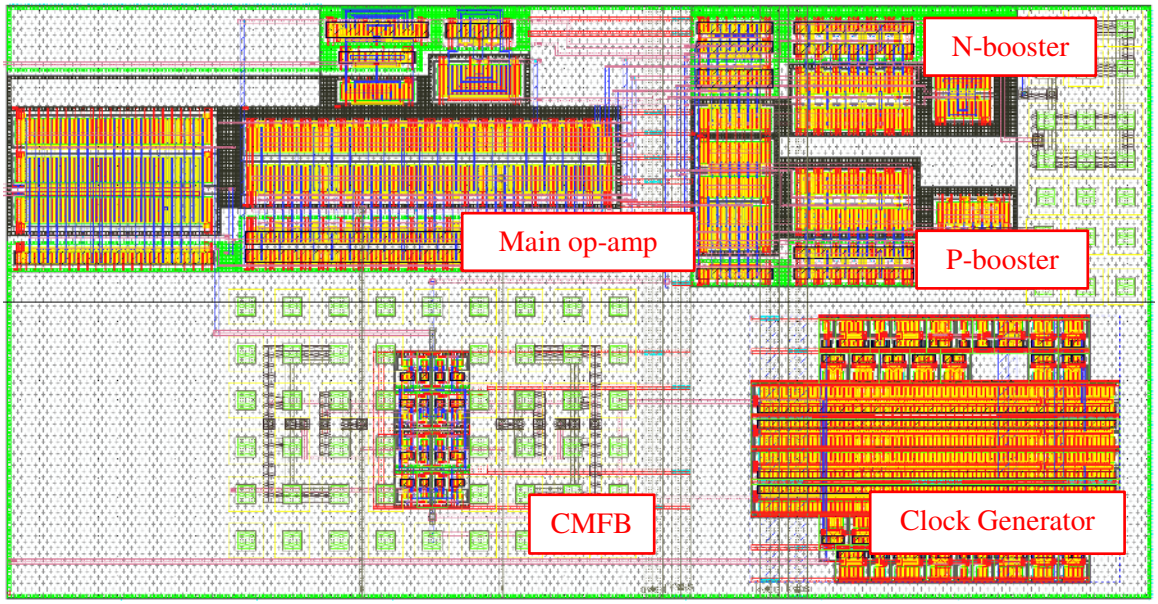


Figure 3.28: Layout of the designed folded cascade op-amp. The total area used is 293µm × 152µm.

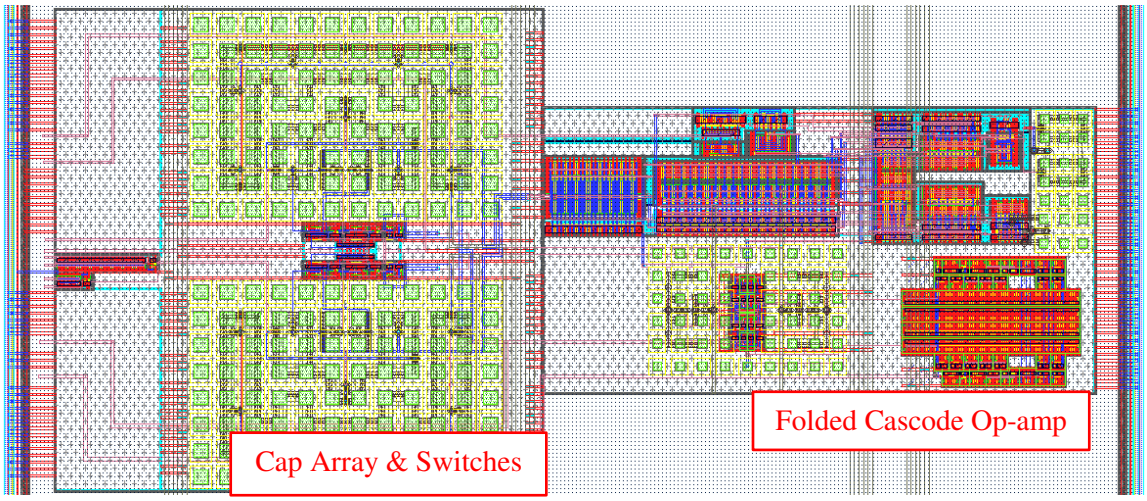


Figure 3.29: Layout of the designed SC filter. The total area used is 606 µm × 260 µm.

Comparator Design

The comparator used in the plateau sensing circuit is to digitize the SC filter output. The clocked comparator is chosen over the continuous time comparator as it is faster and can be synchronized with the SC filter output. The design of this comparator is based on the comparator presented in [88]. The complete schematic of this comparator is shown in Figure 3.30. It consists of a preamplifier, a strong-arm latched decider and a conventional SR latch stage to hold the output. All the transistor sizes for the comparator are listed in Table 3.10.

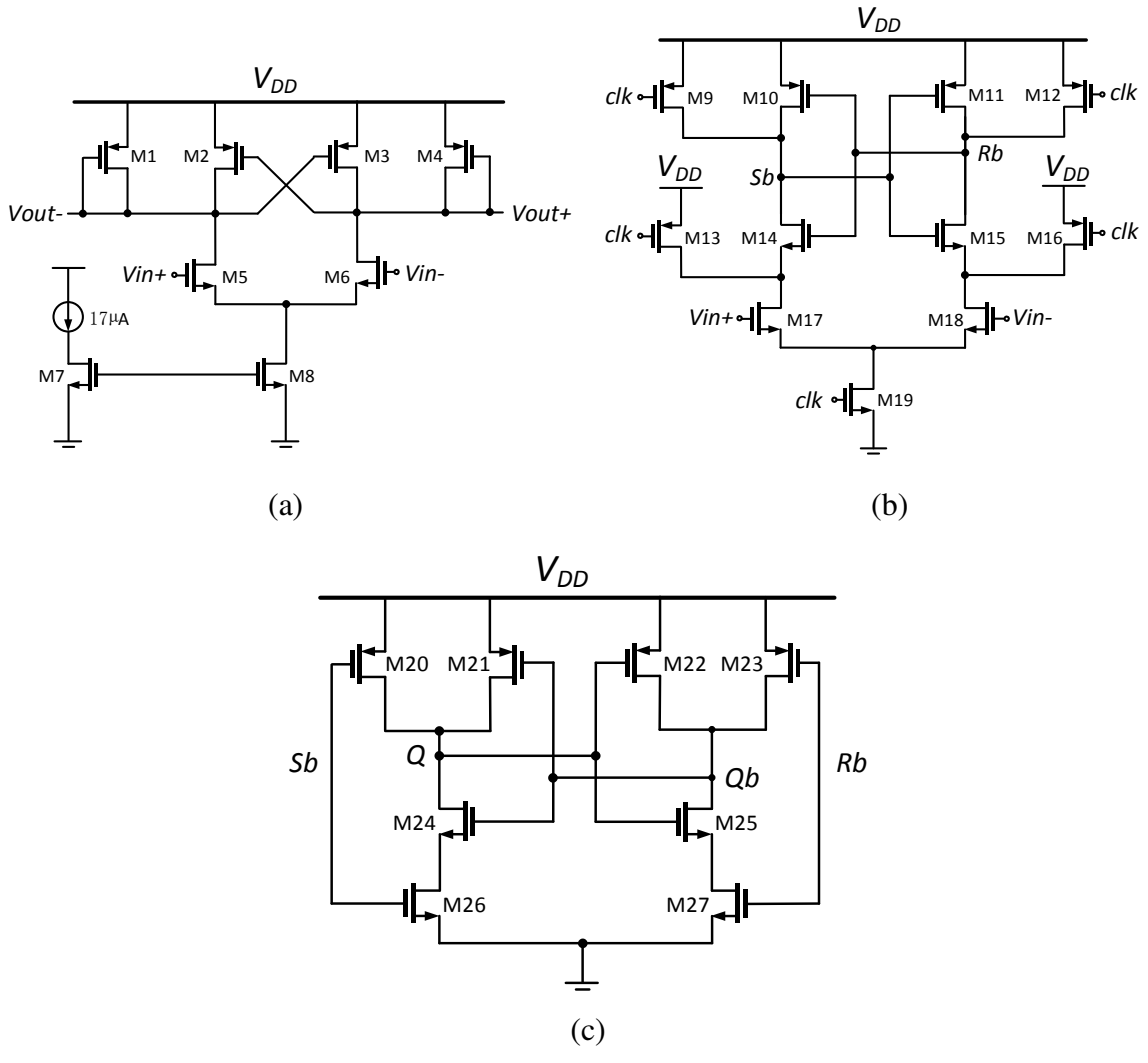


Figure 3.30: Schematic of (a) the preamplifier used in the comparator, (b) the strong-arm latched decider, (c) the conventional SR latch.

Table 3.10: Transistor Sizes for the Comparator

Transistor	W/L	Fingers	Transistor	W/L	Fingers
M1, M4	2 µm/1 µm	2	M9, M10, M11, M12	2 µm/0.6 µm	2
M2, M3	2 µm/1 µm	1	M13, M16	2 µm/0.6 µm	2
M5, M6	2 µm/1 µm	4	M14, M15, M17, M18	2 µm/0.6 µm	1
M7	2 µm/1 µm	2	M19	2 µm/0.6 µm	2
M8	2 µm/1 µm	4	M20~M27	1 µm/0.6 µm	1

The preamplifier using Bult's topology [89] provides higher resolution for the comparator while preventing any charge kickback effect. The preamplifier is designed to have a moderate gain (6.3 V/V) and reasonable unity gain bandwidth (around 100MHz). The latched decider is clocked at 15 MHz and sampled at Ph2 of the system clock; meanwhile the SC filter output is sampled at Ph1 and would remain constant at Ph2. The transistors M10, M11, M14 and M15 in the decider form a positive feedback latch as back-to-back inverters. A minuscule difference in the current flowing through the positive feedback paths can cause the output node to either go high or low. The result of this decider is then fed to the SR stage which would maintain the output when the comparator clock is off. The simulation results of this comparator are summarized in Table 3.11. The hysteresis of the comparator is simulated with one input set to 1.6V, the other slowly sweeping up and then down. The offsets during the output transitions for both rising and falling are around 38.2 µV. Thus the total hysteresis is 76.4 µV. The sensitivity level is found with one input set at 1.6V, and the other input is set close to 1.6V and with very small increments. The output fails to resolve when the other input is higher than 1.5997V. Therefore, the sensitivity of this comparator is found to be 0.3 mV.

Table 3.11: Summary of the Simulated Performance for the Comparator

Parameters	Simulation Results
Supply Voltage	3.3 V
Clock Frequency	15 MHz
Power Consumption	1.93×10^{-16} J/conversion
Hysteresis	76.4 µV
Sensitivity	0.3 mV

Figure 3.31 shows the transient response of this comparator after the SC filter stage. The resultant waveform $V_{CMP\ (turn\_on)}$ is a single pulse while $V_{CMP\ (turn\_off)}$ is a double pulse. This is due to the fact that the charging process after the turn-on plateau is slow, causing the second analog pulse of the filter output having small amplitude. The reference voltage for the comparator is purposely set a bit higher (1.8 V compared to the common mode voltage of 1.65 V). This is to make the comparator immune to the potential ringing noise from EMI during the turn-on plateau. The comparator output only gives the starting range for the plateau sensing. The exact integration durations for both turn-on and turn-off transients are determined from experimental data and realized using the subsequent fixed pulse width modulation block.

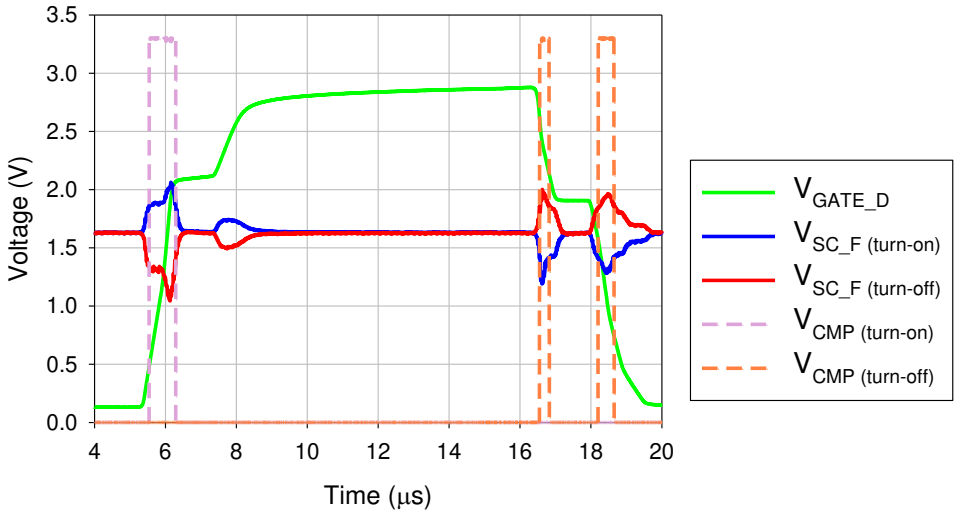


Figure 3.31: Simulated transient response for the Miller plateau detection at the output of the comparator.

3.5.3. Logic Circuit for Fixed Time Integration

The logic block for fixed time integration is designed based on the discrete version implemented using FPGA. Some modifications have been made to improve configurability and to be more appropriate for the integrated design.

Figure 3.32 illustrates the simple logic circuit which is used for the turn-on and turn-off plateau start detection. It should be noted that only the first pulse for the comparator

output is important. This logic circuit will generate a pulse with its rising edge corresponds to the falling edge of the first pulse which is roughly the desired starting point of the Miller plateau.

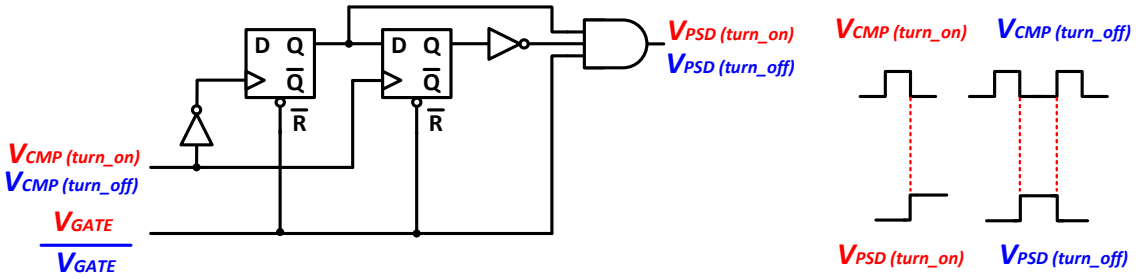


Figure 3.32: Simple logic circuit for turn-on and turn-off plateau start detection.

The exact start and end point of the plateau sensing output is then determined by the fixed pulse width modulation block. The circuit implementation and sample waveforms are illustrated in Figure 3.33. This block is composed of a chain of D Flip-Flops and two MUXs for the selection of the exact rising and falling time. The MUX is implemented to provide programmability for different IGBT modules, and can be configured by the SPRUCE unit. This block ensures that the output is always an integer multiple of the master clock and the obtained pulse is always well within the Miller plateau region.

The fixed time integration method could greatly improve the accuracy of this technique. Since the integration time is now immune to any EMI noise which would potentially impact the comparator output and cause the integration time to vary. The exact integration time is chosen to be as long as possible but shorter than the minimum Miller plateau length. This fixed integration time is determined by the lower bound V_{CE} value as explained in Section 2.3.4. The input clock for this block is 3.75 MHz and is obtained from the 15 MHz system clock through a clock divider. The system clock synchronization will be further discussed in Section 3.9.1.

Figure 3.34 shows the simulated transient response of this logic block. It can be seen that the output signals $V_{SW(turn\text{-}on)}$ and $V_{SW(turn\text{-}off)}$ correspond to the turn-on and turn-off plateaus, respectively and are well within the plateau regions. These two signals will serve as the triggering signals for the SC integrator.

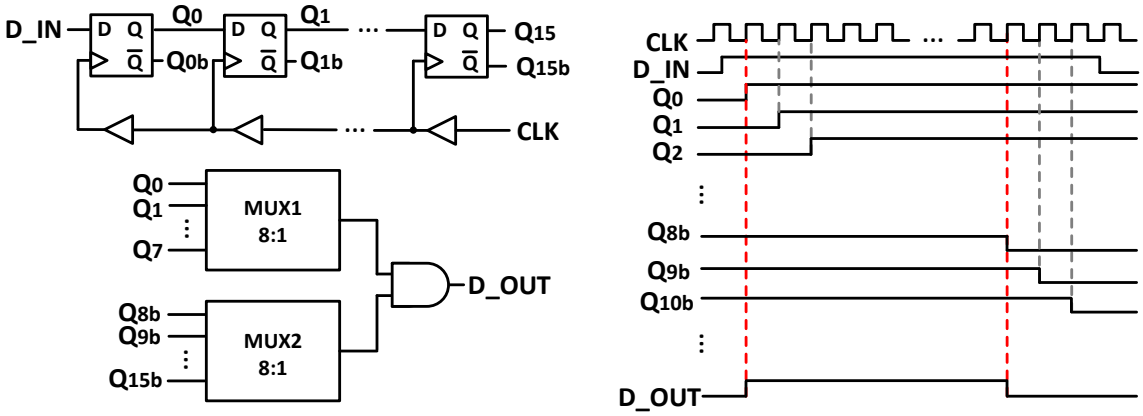


Figure 3.33: Circuit implementation for the fixed pulse width modulation.

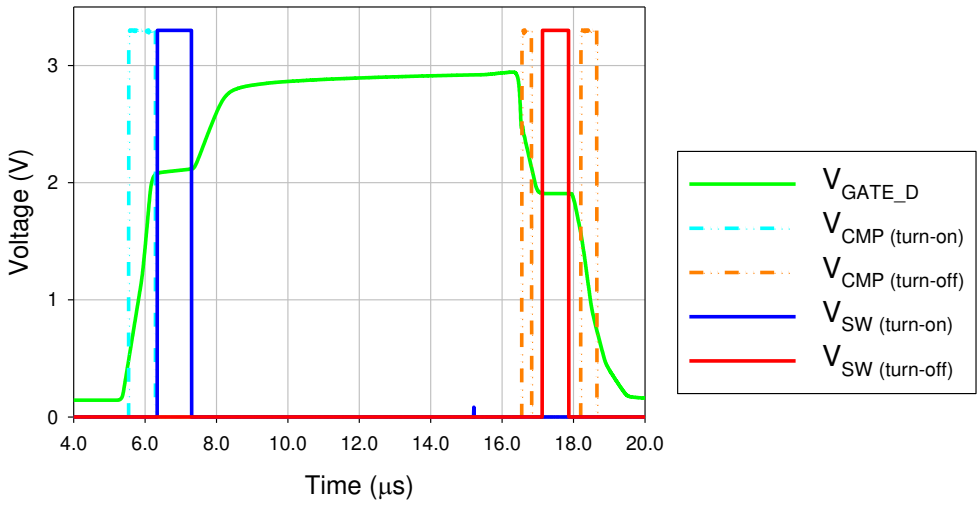


Figure 3.34: Simulated transient response for the Miller plateau detection at the output of the fixed time integration block.

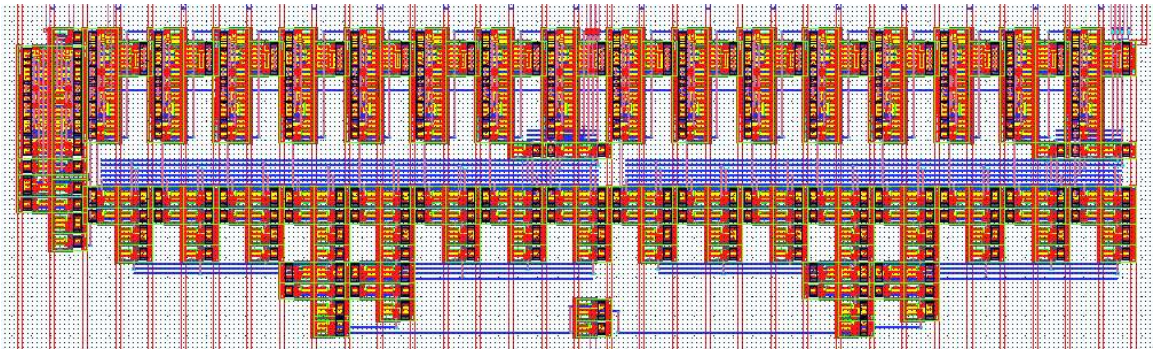


Figure 3.35: Layout of the fixed time integration block. The total area used is 285 µm × 80 µm.

3.6. Switched-Capacitor Integrator Design

The SC integrator employs a parasitic-insensitive and delayed topology, as shown in Figure 3.36. The capacitance for C_2 is 6 times larger than that for C_1. This means that the output decreases by 6 times for each cycle. The same switching frequency of 15 MHz is used. The exact integration time (t) can be determined based on experimental data and adjusted through the previous fixed time integration block. Therefore the transfer function of the integrator for one cycle can be expressed as:

$$V_{out\_diff} = (V_{in\_diff} - V_{\mathrm{ref}\_diff}) \times \frac{t}{(1/15\mathrm{e}^6)} \times \frac{1}{6} \tag{3.10}$$

This subtraction and amplify stage could increase the sensitivity of the gate current to the collector current relationship, and reduce the accuracy requirement for the ADC. The reference voltages are supplied using off-chip adjustable LDOs. The output of the integrator is carefully controlled to be within the desired input range for the ADC (±1.2 V). The integrator resets every cycle and the outputs would go to the common mode voltage, to get ready for the next cycle.

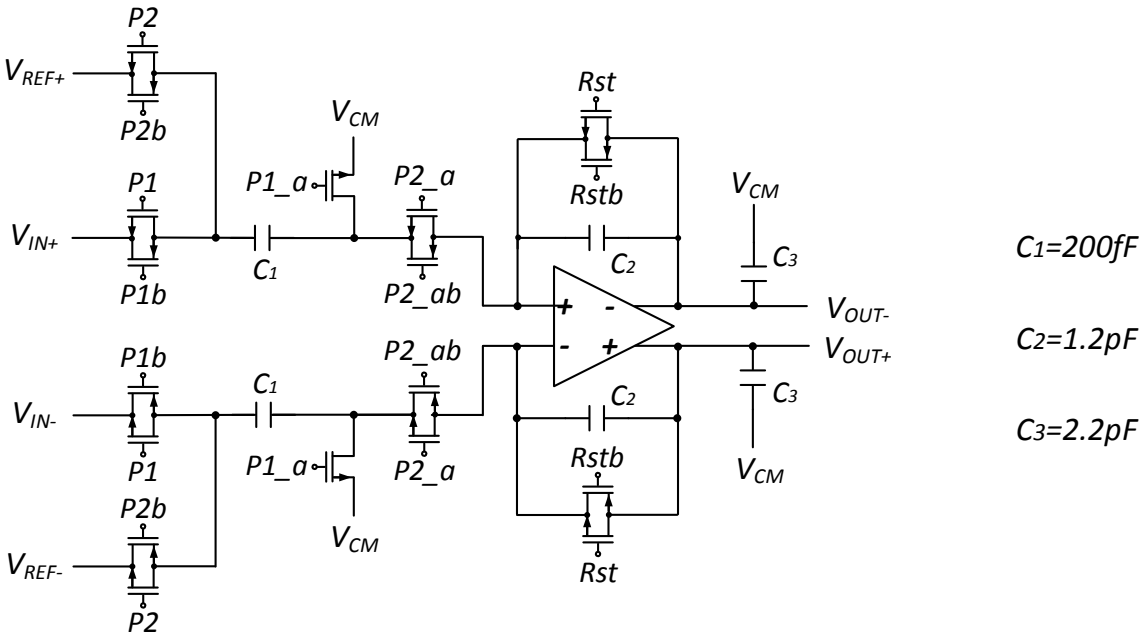


Figure 3.36: Schematic of the SC integrator.

All the switches in the SC integrator are realized using transmission gates except the two switches connected to the common-mode are implemented using NMOS. The transmission gates are sized with both NMOS and PMOS having W/L=5 µm/0.6 µm, the same holds for the NMOS switch as well. This sizing makes sure reasonable settling time for the capacitors while minimizing the charge injection effects.

The op-amp presented in Section 3.5.2 is re-used in this SC integrator. The open loop AC simulation results of the op-amp with the loading condition in the SC integrator at P1 state are presented in Figure 3.37. At P2 state the AC simulation results remain similar with slightly larger unit gain bandwidth at 160 MHz.

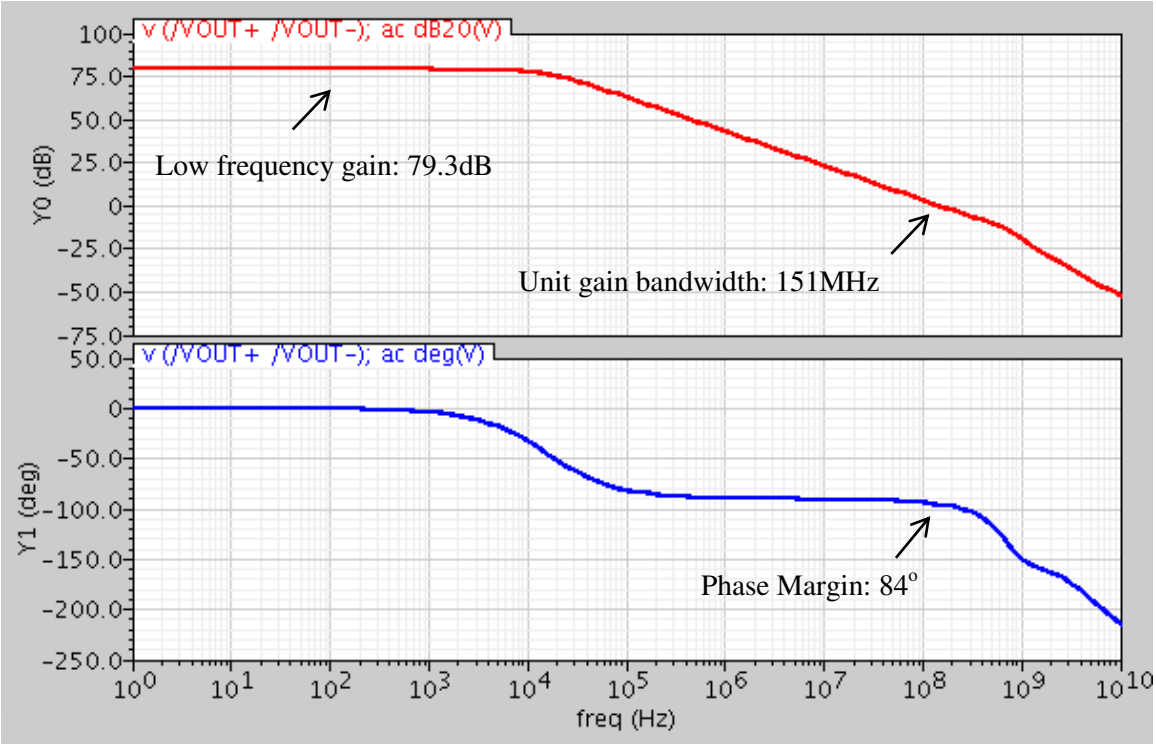


Figure 3.37: AC simulation results for the op-amp in the SC integrator.

During the turn-on Miller plateau, the integrator accumulates the voltage difference between 3.3 V and the scaled gate voltage (common mode voltage is around 2 V). During the turn-off Miller plateau, it accumulates the voltage difference between the scaled gate voltage and ground (common mode voltage is around 1 V). The simulated FFT plots for the SC integrator for turn-on and turn-off are shown in Figure 3.38 and Figure 3.39, respectively. The input signal is around 1 MHz with 2 V peak to peak, where the output

is in the desired range of ±1.2 V. The worst case SNDR (Signal to Noise plus Distortion Ratio) is 64.3 dB.

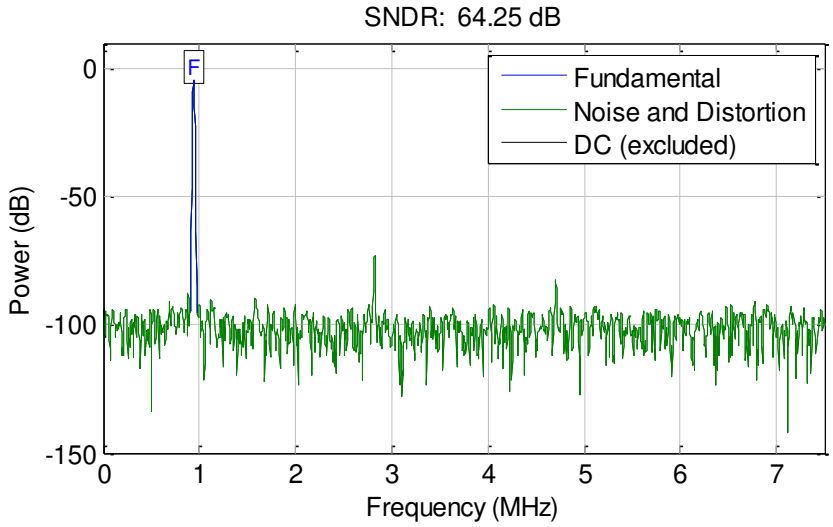


Figure 3.38: Simulated FFT plot for the SC integrator showing the SNDR performance for turn-on.

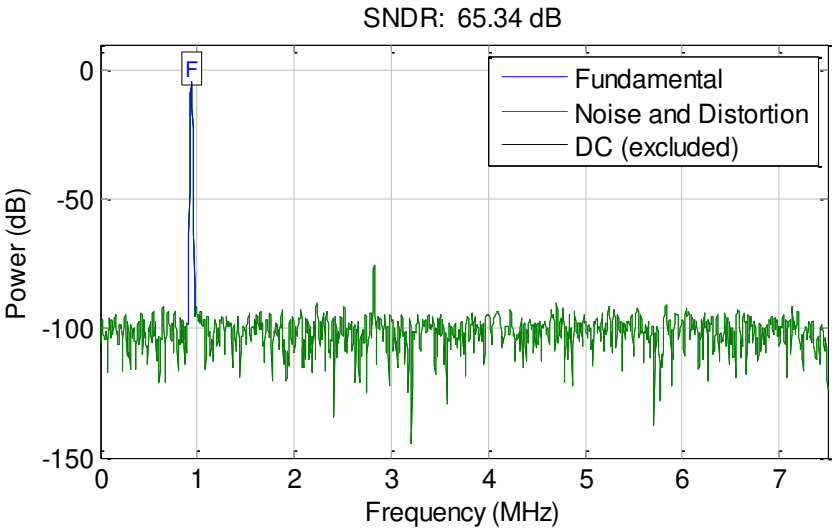


Figure 3.39: Simulated FFT plot for the SC integrator showing the SNDR performance for turn-off.

Figure 3.40 illustrates the transient response of the SC integrator in the current sensing circuit. The V_{OUT_DIFF} level after the plateau region is an analog representation of the collector current I_C. It will be sampled and fed to the ADC to get a digital interpretation of I_C.

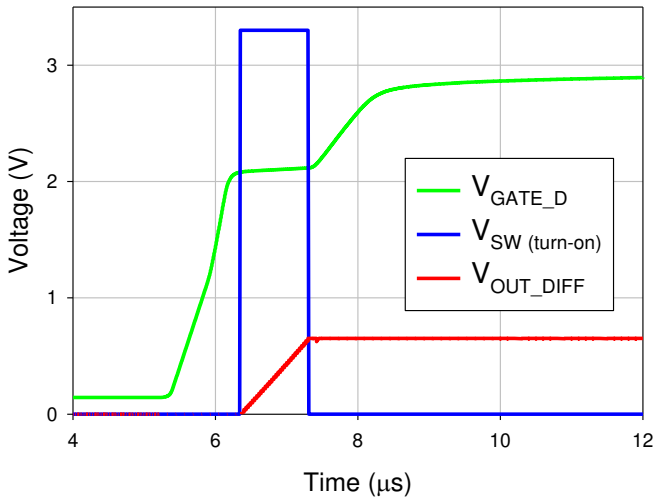


Figure 3.40: Simulated V_{OUT_DIFF} waveform. This voltage is an analog representation of the collector current.

Theoretically, V_{SW} should be the triggering signal for the discrete SC integrator. However, this is not a continuous time integrator and non-overlapping clock phases are needed as depicted in Figure 3.36. V_{SW} is generated from the fixed integration time logic block with a clock frequency of 3.75 MHz. Therefore, it should be an integer multiples of the system clock which is 15 MHz. However, due to delays caused by all the previous blocks, V_{SW} may not be synchronized with the system clock any more. Therefore, extra synchronization block is needed for the SC integrator.

As illustrated in the simulation results shown in Figure 3.41, V_{SW} is no longer synchronized with the system clock V_{CLK1}. However, it is now possible make the triggering signal to synchronize with V_{CLK1b} which is the complement of V_{CLK1}. Post layout simulation is also carried out to demonstrate that the layout does not add noticeable delay. In this case, V_{SW} is made in conjunction with V_{CLK1b} to form the V_{SI_CLK} signal. Then V_{SI_CLK} goes through another non-overlapping clock generator inside the integrator block to generate the corresponding clock phases to operate the SC integrator. The system clock synchronization technique will be further discussed in Section 3.9.1.

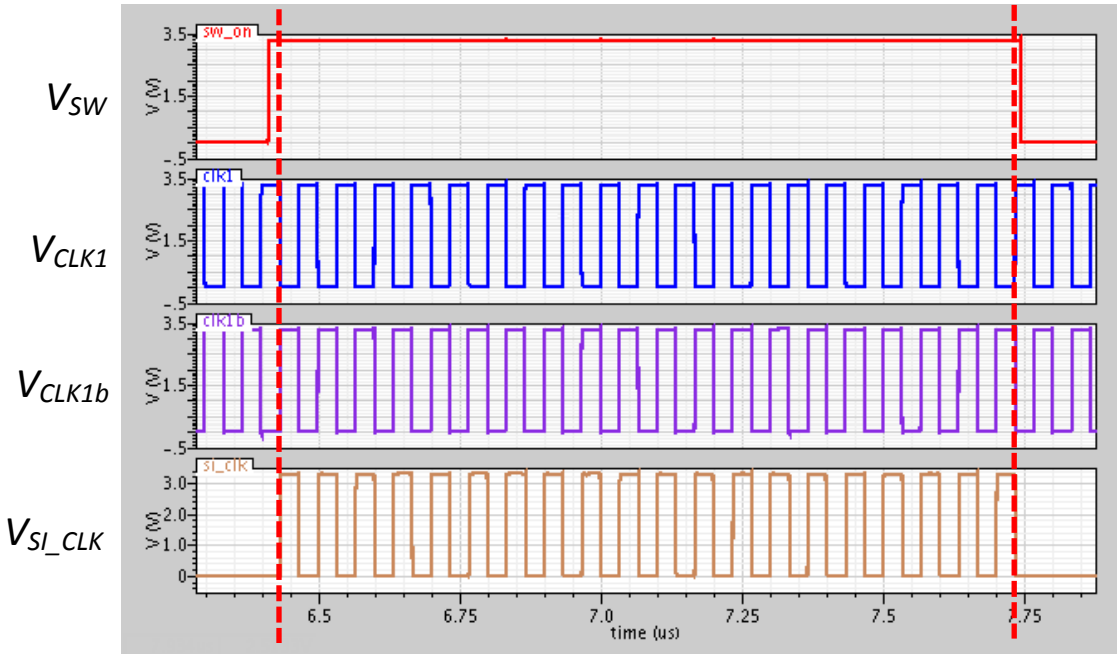


Figure 3.41: Synchronization for the SC integrator triggering clocks.

The layout of the SC integrator is shown in Figure 3.42. The capacitors are carefully laid out using common centroid technique to cancel out the charge injections as much as possible.

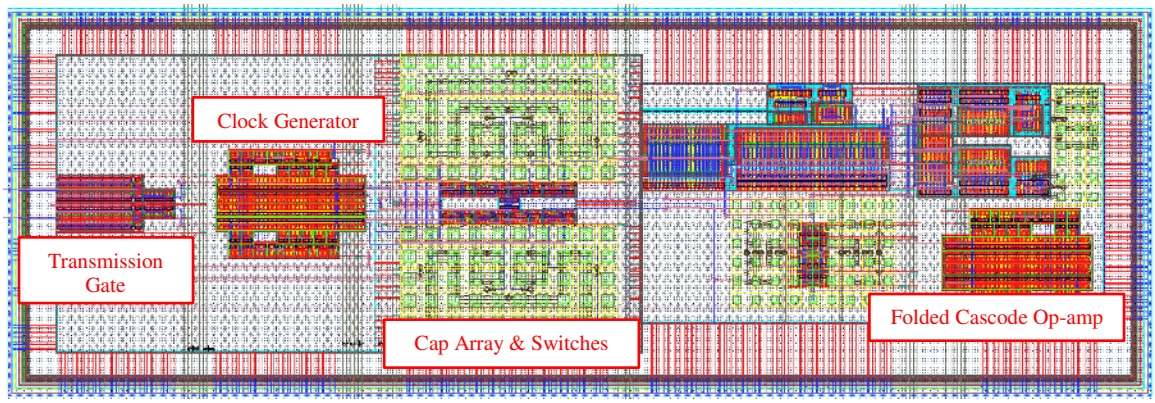
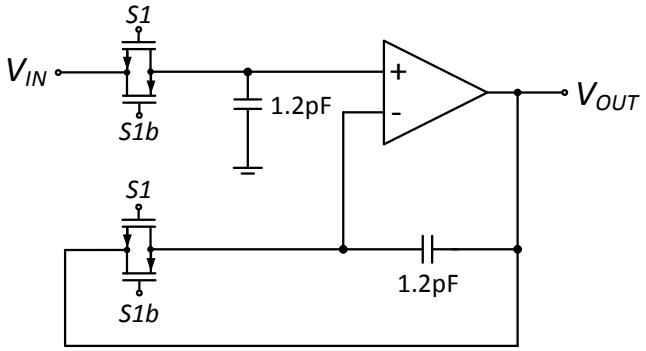


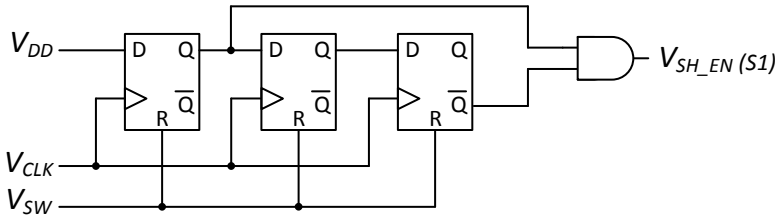
Figure 3.42: Layout of the designed SC integrator block. The total area used is 725 µm × 247 µm.

3.7. Sample-and-Hold Design

The sample-and-hold block implements the non-inverting topology with clock-feedthrough cancellation technique [90]. The schematic is illustrated in Figure 3.43 (a). This is a single ended topology, therefore two sample and hold blocks are needed for the fully differential integrator outputs. Figure 3.43 (b) shows the digital circuit used to generate the triggering signal for the sample-and-hold block. V_{CLK} is synchronized with the system clock (15 MHz) but four times slower, thus is 3.75 MHz. V_{SW} is the triggering signal for the integrator. V_{SH_EN} (S1) is the output of the logic circuit which is used to activate the switches in the sample-and-hold circuits.



(a)



(b)

Figure 3.43: (a) Sample-and-hold schematic (b) Logic for the sample-and-hold triggering signal.

As depicted in Figure 3.44, V_{SH_EN} is triggered shortly after V_{SW} to ensure that the correct integrated output is sampled and held until the next cycle. The output serves as the input to the subsequent DSM (Delta Sigma Modulator) stage. The pulse width of V_{SH_EN} is twice the period of V_{CLK}, which is 533 ns. This provides time for the sample-and-hold block to settle.

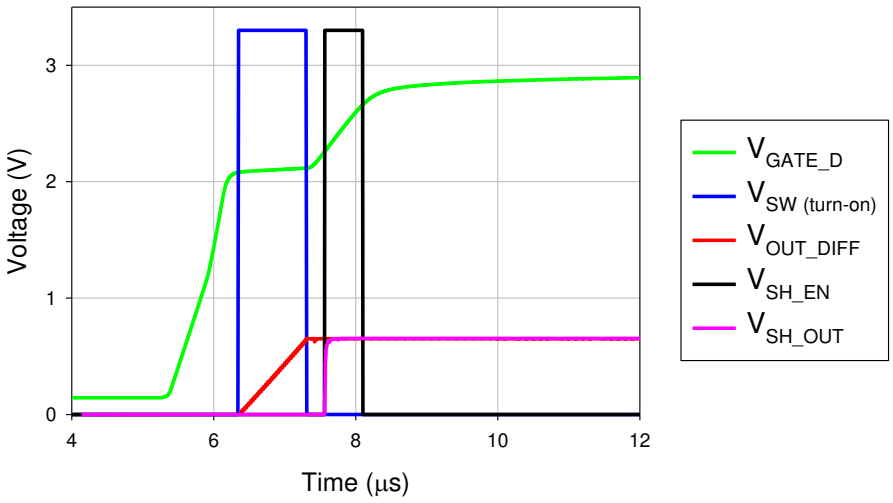


Figure 3.44: Transient simulation shows the sample-and-hold enable signal (V_{SH_EN}) and output waveform (V_{SH_OUT}) in the I_C current sensing circuit.

The functionality of the sample-and-hold circuit is demonstrated by feeding it with a slow sinusoidal wave with peak to peak amplitude of 2.4 V, as illustrated in Figure 3.45. The maximum offset is observed when V_{OUT_DIFF} is around 1.2 V, where the offset is around 2 mV. The switching frequency can go as fast as 20 MHz; while the offset level remains almost the same.

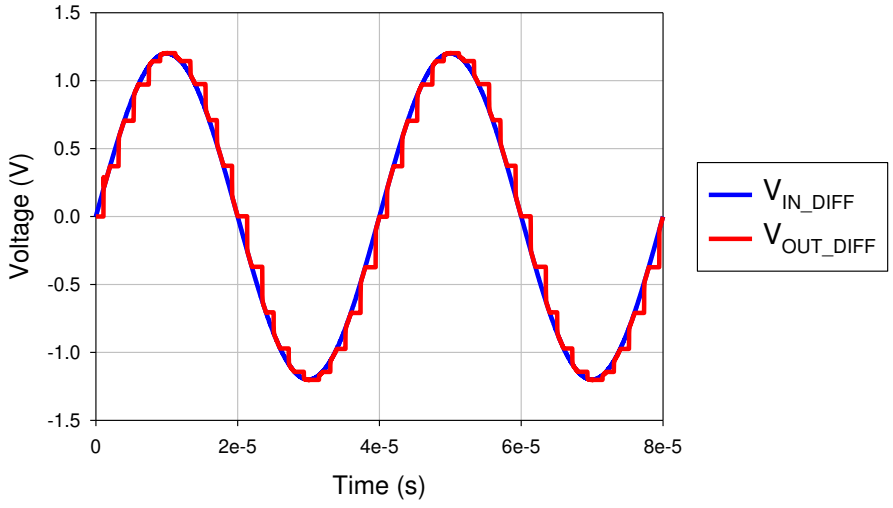


Figure 3.45: Transient simulation shows the functionality of the sample-and-hold circuit.

The layout of the sample-and-hold circuit block is shown in Figure 3.46. Since two single ended sample-and-hold circuits are used for a fully differential signal. The layout is designed to be symmetric along the middle horizontal line. Post layout simulation for this block shows a worst case offset less than 2.2 mV.

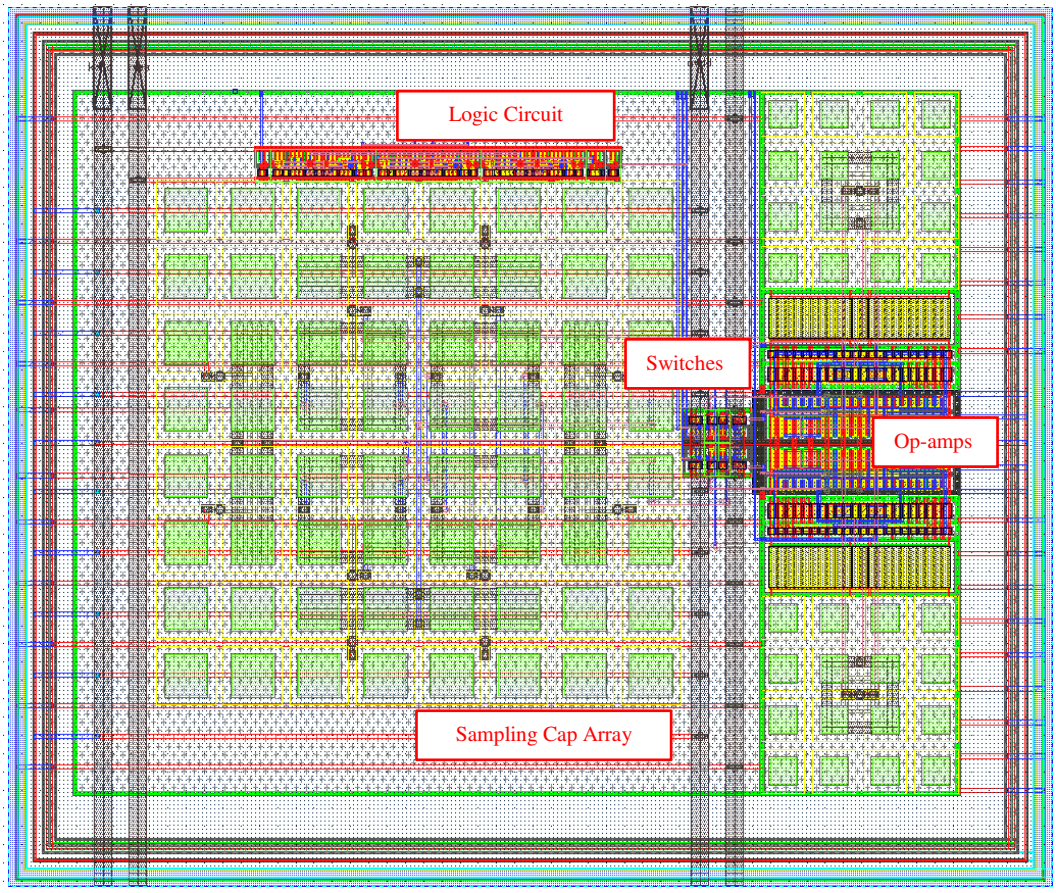


Figure 3.46: Layout of the designed sample-and-hold block. The total area used is 285 µm × 240 µm.

3.8. Delta-Sigma ADC Design

The reason for choosing a delta-sigma ADC to digitize the output is because the input signal is relatively slow (20 kHz for a typical IGBT module), allowing a high over sampling ratio (OSR). In addition, the DSM has simple architecture and good tolerance to analog component inaccuracy, but requires additional digital processing which could be handled by the on-chip SPRUCE unit.

3.8.1. Architecture Modeling using MATLAB

In the previous discrete implementation, the ADC (AD7322) has 12-bit resolution with input range selection of ±10V. The I_C testing range was up to 30A only but it already used the full 12-bit resolution in order to achieve an accuracy of ±1A. The main reason is that the signal processing level in the I_C sensing circuitry was kept at above 10V, meanwhile there was no subtract/amplify stage in the integrator, causing the integrator output to have high voltage level and small variation across the I_C testing range.

In the integrated design, the target I_C testing range is further extended to 50A with the same accuracy requirement of ±1A. Due to the lower signal processing level (3.3V) with configurable integration time and adjustable integrator reference voltage, the estimated resolution requirement of the ADC is around 10 mV to 20 mV. With a supply voltage of V_{DD} = 3.3 V, this translates to an Effective Number of Bits (ENOB) for the ADC to be between 8 bits (3.3/256 ≈ 12.89 mV) to 9 bits (3.3/256 ≈ 6.45 mV). In order to leave some margin for the design and make the gate drive IC more adaptive for other IGBT devices, the target ENOB for the ADC is 10 bits (3.3/1024 ≈ 3.22 mV). It should be noted that for Delta Sigma ADCs, the final ENOB is more dependent on the digital filter design. In this case, SPRUCE can be used to implement a highly re-configurable digital filter. However, a higher ENOB could also be achieved if the digital processing speed is relaxed. These details will be discussed in Section 3.8.4 and Section 4.4.

For design simplicity, linearity and easier interfacing with the CPU, a 1-bit quantization implemented with one comparator is chosen. In order to obtain a 10-bit ENOB (SNR = 6.02 ENOB + 1.76, equivalent to 62 dB) with a 1-bit quantizer, a MOD 2 topology and an OSR of 100 are chosen for a theoretical 86 dB peak SQNR [91], taking into account of thermal noise, layout mismatch and process variations. The Delta Sigma Tool box by Schreier *et al*. is used to synthesize, simulate and construct the topology of the DSM [92]. Figure 3.47 depicts the expected SQNR versus the input signal level. It can be observed that the SQNR peaks in the vicinity of -1.6 dBFS; and then drops abruptly as the input amplitude approaches full scale. In order to maximize the SQNR and also leave margin for all the non-idealities which may cause the modulator to go unstable, the input signal level is chosen to be around -2.5 dBFS. Therefore, with a desired input range of ±1.2 V, the full input range of the DSM is ±1.6 V.

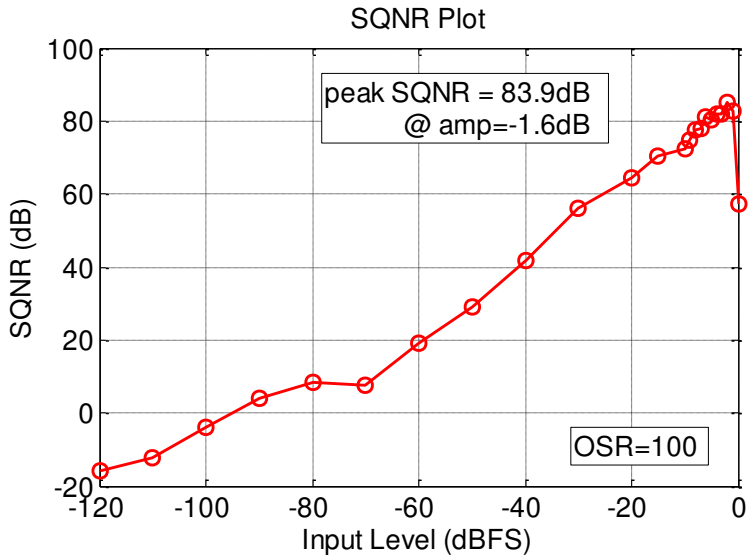


Figure 3.47: Simulated SQNR of MOD2 with OSR=100.

A behavioral model of the MOD2 DSM is constructed and simulated using MATLAB Simulink. Dynamic scaling is performed to the coefficients so that the output signals of each stage would be in the desired range. Figure 3.48 shows the second order modulator structure with the coefficients after dynamic scaling.

The minimum sampling is 2 times the OSR and the input frequency. The input frequency in this case is the same as the IGBT switching frequency at 20 kHz. The minimum sampling frequency is 4 MHz. In order to allow better margins for digital processing, a 10 MHz clock is chosen. Simulink simulations were carried out to demonstrate that with the ideal model the SQNR could reach 82.7 dB with a -2.5 dBFS and 12.5 kHz input, as shown in Figure 3.49.

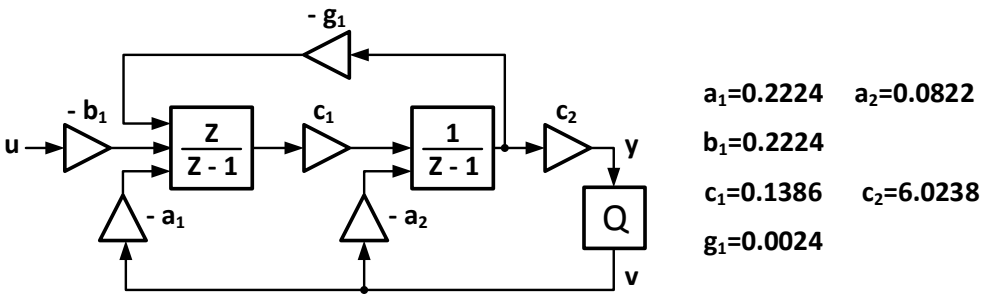


Figure 3.48: Designed MOD2 ΔΣ ADC modulator.

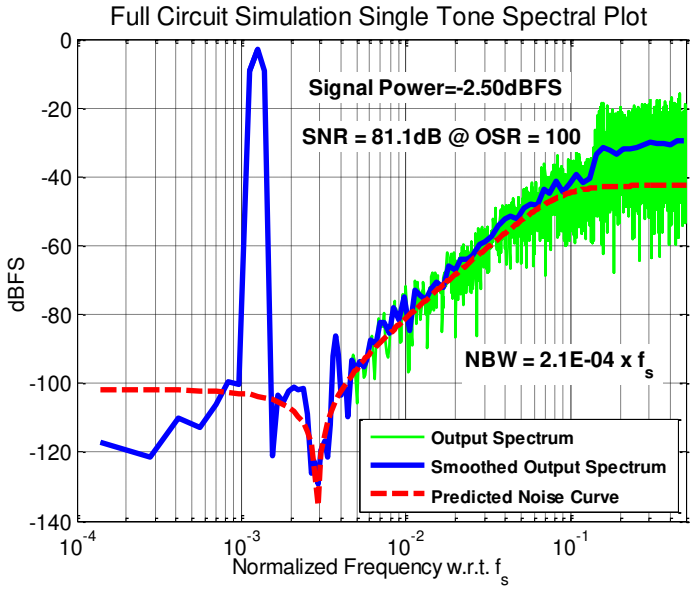


Figure 3.49: The output power spectral density with ideal MATLAB modeling.

3.8.2. Circuit Implementation

The real MOD2 DSM circuit consists of a 2-stage SC integrator, one comparator for the 1-bit quantization, a clock generator which generates the 2-phase non-overlapping clock

signals and an SC feedback DAC which converts the digital output of the modulator back into analog form and compared to its analog input.

2-Stage Integrator Design

The 2-stage SC integrator is implemented with the capacitors sized according to the coefficients (g_1 is neglected as it is too small to realize with real capacitors), as shown in Figure 3.50.

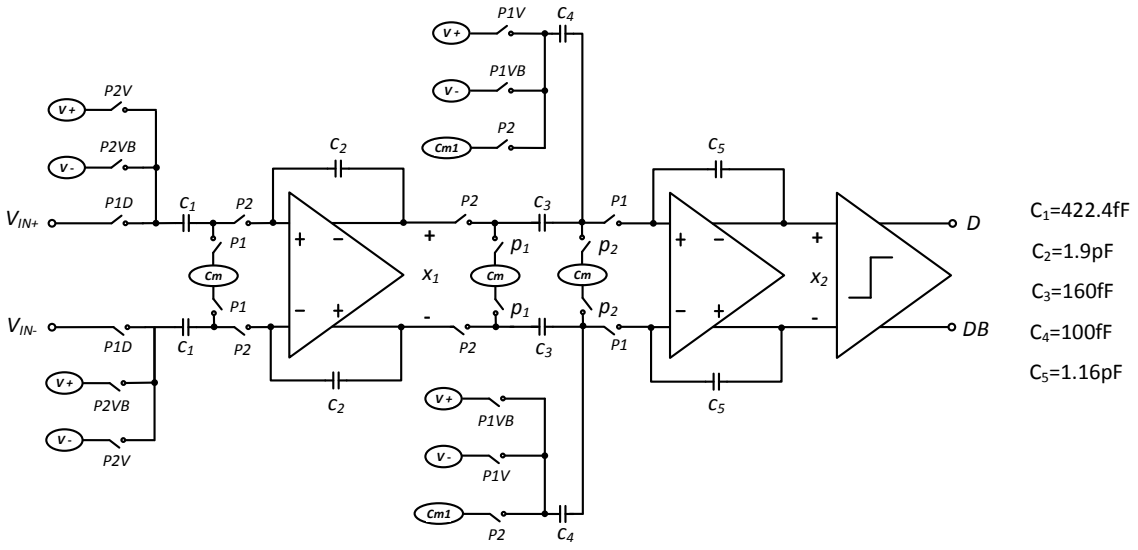


Figure 3.50: Circuit diagram of the MOD2 DSM.

The input capacitor size is determined mainly by the input referred noise power for the first stage. The in-band noise of the second integrator is greatly attenuated by the first stage gain. In order to have an estimated SNR of above 90 dB with −3 dBFS input signal for the first stage, the input signal power is calculated as:

$$\overline{V_s^2} = \frac{1}{2} \times \frac{A^2}{2} = 0.64\text{V}^2 \tag{3.11}$$

The in-band noise power is:

$$\overline{V_{n,in-band}^2} = 0.64 \times 10^{-9}\text{V}^2 \tag{3.12}$$

The input referred noise for the first stage becomes:

$$\overline{V_n^2} = \overline{V_{n,in-band}^2} \times OSR = 6.4 \times 10^{-8} \mathrm{V}^2 \tag{3.13}$$

For a single input capacitor C_1, at Phase 1, the input referred noise is KT/C_1. Assume Phase 2 will introduce another equal noise of KT/C_1, and then the total input referred noise for C_1 is 2 KT/C_1. Considering that this is a fully differential stage, the total input referred noise for the first stage is estimated as 4 KT/C_1.

Therefore, the minimum size of C_1 should be:

$$C_{1(min)} = \frac{4KT}{\overline{V_n^2}} = 259 \text{ fF} \tag{3.14}$$

The final value for C_1 is selected to be 422 fF to simplify layout and to provide a modest amount of margin for the design. It is realized through 8 units of 52.8 fF capacitors (7 µm × 7 µm square) connected in parallel. The rest of the capacitor sizes are listed in Figure 3.50. Both the input and output common mode input voltages for the 2-stage SC integrator are set to be 1.65 V. Since the full input range is ±1.6 V, the positive reference voltage is set to be 2.5 V and the negative reference voltage is set to be 0.8 V.

In order to minimize the delay and offset in signal introduced by the real switches: switches that are connected to the 1.65 V common mode nodes and the 0.8 V reference nodes are NMOS transistors. Those connected to the 2.5V reference are PMOS transistors. The rest of the switches are transmission gates. The switches sizing procedure is similar to those for the SC filter and SC integrator. The delay is minimized while the voltage should settle to its final value within half of the switching period. The final sizing for all NMOS and PMOS transistors are W/L = 8 µm/0.6 µm, including the NMOS and PMOS in the transmission gates.

The op-amps used for the 2-stage SC integrator are the same as the ones presented in Section 3.5.2. For the first stage, the op-amp is compensated with 2pF loading capacitors, and the worst case happens at state P2 which has an open-loop bandwidth of 154 MHz

and phase margin of 83°. For the second stage, the op-amp is also compensated with 2pF loading capacitors and the worst case condition is at P1 state which has a unit gain bandwidth of 161 MHz and phase margin of 82° in the second stage.

Clock Generator Design

The two-phase non-overlapping clock generator is designed to incorporate clocks with proper dead time; as well as having delaying clocks to counter the charge injection error. The schematic of the clock generator is shown in Figure 3.51. The logic gates are carefully sized in order to achieve desired delay time, dead time and also appropriate diving strength for the transistor switches. The transient simulation results of the block are presented in Figure 3.52. The dead time between P1 and P2 is 2.3ns. The delay time between P1 and P1D, or P2 and P2D are around 600ps.

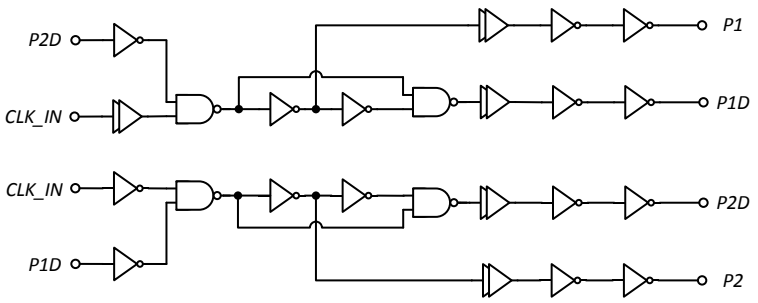


Figure 3.51: Schematic of the non-overlapping clock generator.

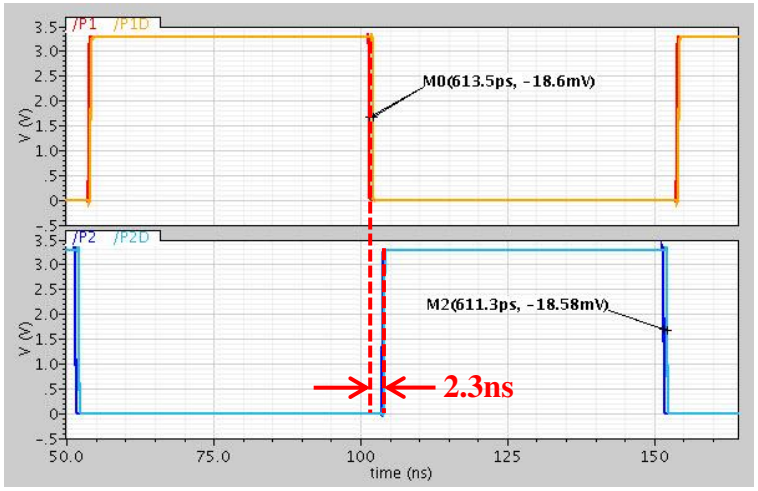
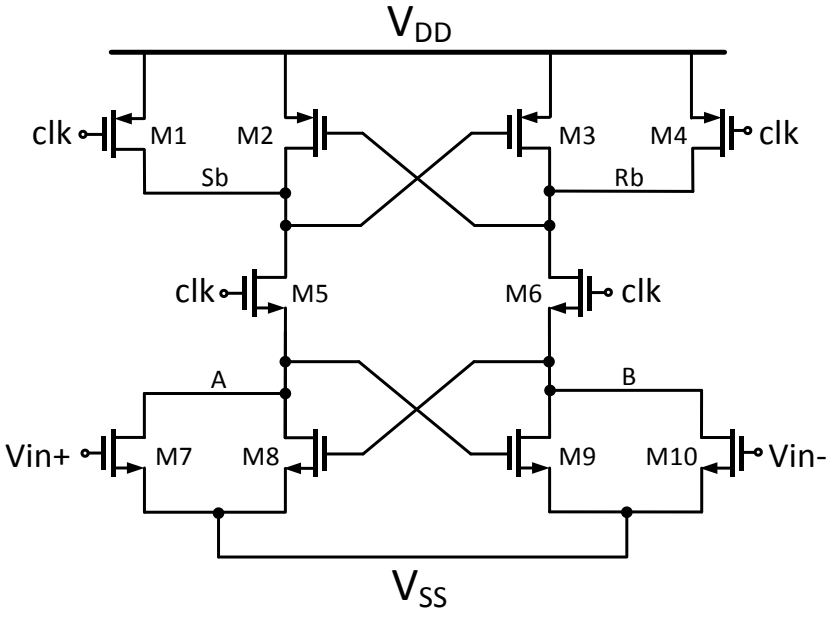


Figure 3.52: Transient simulation results of the clock generator in the ΔΣ ADC.

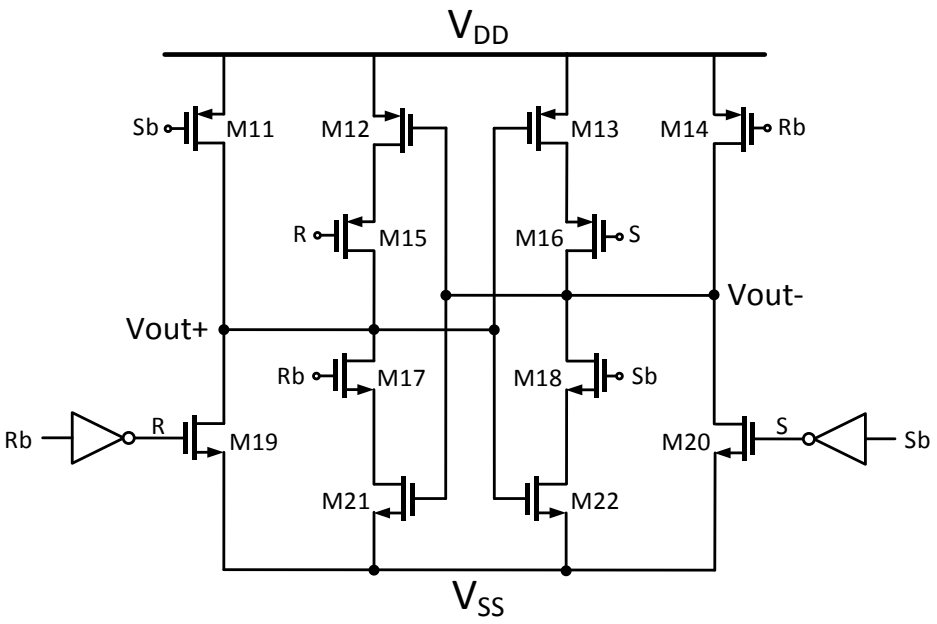
Comparator Design

The DSM does not have high requirement for the resolution of the comparator as it serves the purpose for quantization only. However, it still needs low hysteresis. Therefore, a reset function is necessary. Figure 3.53 shows the schematic of the dynamic latched decider and the SR latch stage. There is a preamplifier before the decider which uses the same design as presented in Section 3.5.3. The dynamic decider features high speed, low offset and low power consumption [93].

The clock signal (reset signal) of this comparator is the P2 clock in the ADC system. When the clock goes low, transistor M1 and M4 are turned on. Both outputs Sb and Rb go high. Meanwhile M5 and M6 are turned off, and nodes A and B discharge to ground through transistors M8 and M9. When the clock goes high, charging current flows from the PMOS transistors to NMOS transistors. The difference between the input voltage pairs is quickly amplified through the latches. This results in a voltage swing nearly equal to V_{DD} at Sb and Rb. The signals Sb and Rb are fed to another latch stage as shown in Figure 3.53 (b). The transistor sizes for the decider and the SR latch are summarized in Table 3.12.



(a)



(b)

Figure 3.53: Schematic of the (a) fully differential dynamic latched decider (b) SR latch.

Table 3.12: Transistor Sizes for the Comparator in the DSM

Transistor	W/L	Fingers
M1, M2, M3, M4	4 µm/0.6 µm	1
M5, M6	1 µm/0.6 µm	1
M7, M8, M9, M10	1 µm/0.6 µm	1
M11, M12, M13, M14	1 µm/0.6 µm	1
M15, M16	1 µm/0.6 µm	1
M17, M18, M19, M20	2 µm/0.6 µm	1
M21, M22	2 µm/0.6 µm	1

The SR latch shown in Figure 3.53 (b) is an improved SR latch stage as presented in [94]. Compared to conventional SR latch, it is symmetric, and with reduced delay and improved driving capability.

The transient simulation results for this comparator are shown in Figure 3.54. The input signal is a pair of slow sine wave with 0.4 V peak to peak, which is the actual input signal range of the comparator in the DSM. With a latch clock frequency of 10 MHz, the maximum observed comparator decision time is 1.8 ns.

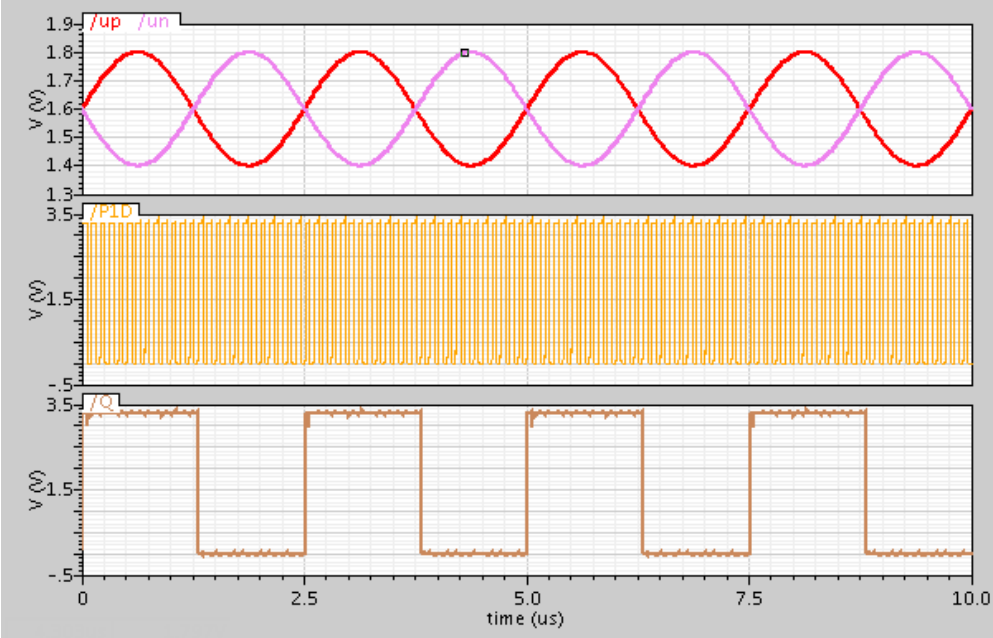


Figure 3.54: Functionality simulation for the comparator in DSM. From top to bottom: two input signals, latch clock, comparator final output.

DAC Design

The DAC is designed to deliver the desired feedback charge to the SC integrators. The schematic is depicted in Figure 3.55. The input and output signals correspond to the signals are labeled in Figure 3.50. The logic gates are carefully sized to achieve proper delay and driving strength for the switches.

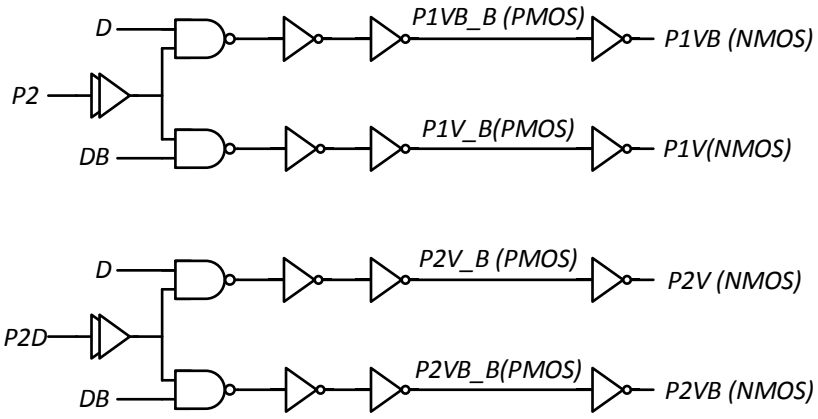


Figure 3.55: Schematic for the DAC.

3.8.3. DSM Top Level Verification

The transient simulation results of the MOD2 DSM are shown in Figure 3.56. The simulation was conducted with a low input frequency of 12.5 kHz and an amplitude of 1.2V. The input frequency is purposely set lower than the actual operating frequency so that we can observe the third harmonic distortion of the system. The fist SC integrator stage output is within the range of ±1.2 V, and the second stage output is within ±0.3 V. Both are well within the output swing range of the op-amp.

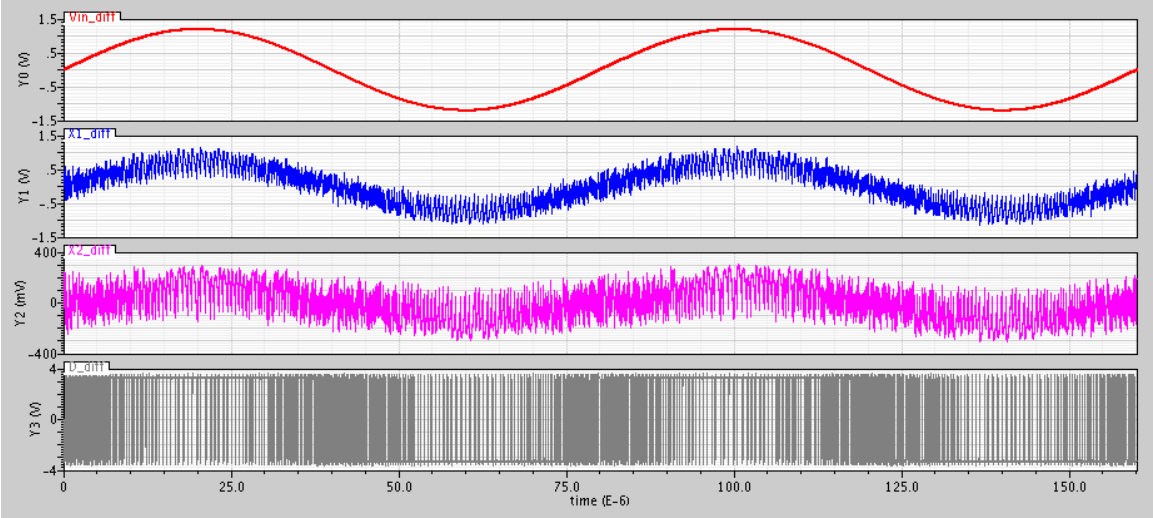


Figure 3.56: Transient simulation results of the DSM block. From top to bottom: 12.5 kHz input sine wave, first SC integrator stage outputs (X1), second DC integrator stage outputs (X2), DSM final 1-bit output.

The DSM final output is sampled at P1 and extracted for the SNDR plot. The final SNDR result is simulated to be 77.9dB based on 4800 sampled data points as illustrated in Figure 3.57.

The layout for the DSM block is depicted in Figure 3.58. The analog circuit (including the op-amps, 2-stage switched-capacitor integrators, comparators and bias current circuit, etc.) and the digital circuit (including the clock generator and DAC) are separated using different isolation rings and powered with different power supplies to avoid noise coupling.

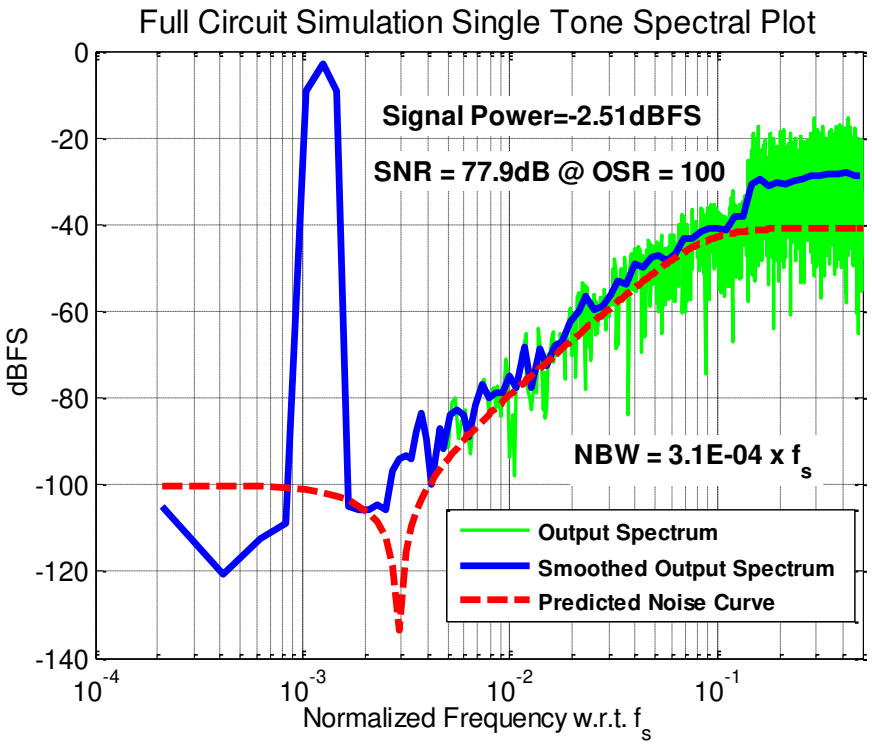


Figure 3.57: Final SNDR simulation results with -2.5dBFS and 12.5 kHz input.

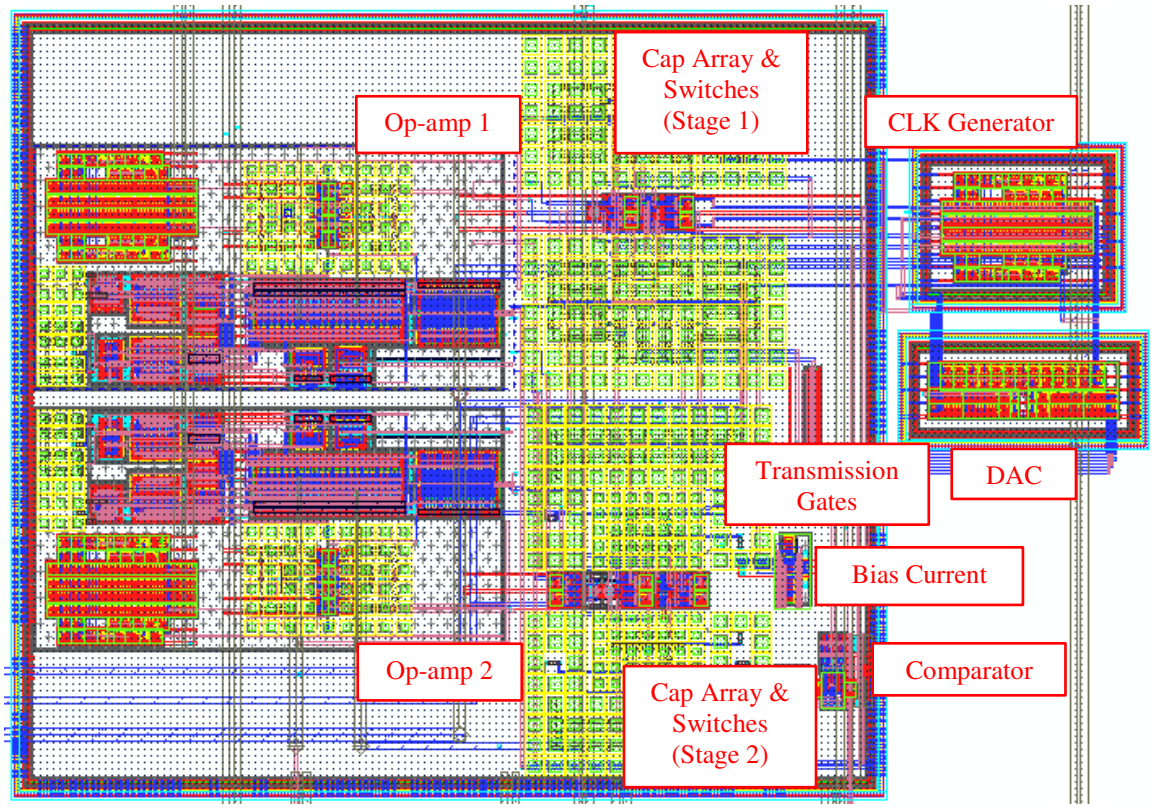


Figure 3.58: Layout for the DSM block. The total area used is 722 µm × 490 µm.

3.8.4. SPRUCE Implemented Decimation Filter

The digital filtering for the designed DSM block is implemented by the SPRUCE unit. The interface between the DSM and SPRUCE is illustrated in Figure 3.59. The 1-bit output of the DSM block is clocked into a 100-bit shift register which is memory mapped to 5 words (length is 20 each) in the main memory. The corresponding memory location can be found in the memory map in Appendix A. The DSM could be started and stopped via the GPO controlled oscillator. It is triggered after the plateau region when the integrator finishes integrating and the sample hold block settles. The DSM is allowed to run free for a short time to allow initial settling of the switched capacitors. Then the last 100 bits of data are stored in the shift registers.

These 100 bits of data go through a SPRUCE implemented digital filter for noise suppression. It is required to have -62 dB of stopband rejection and also have enough attenuation for out-of-band quantization noise. The digital filter consists of a 3rd order CIC (Cascaded Integrator-Comb) filter and an FIR filter.

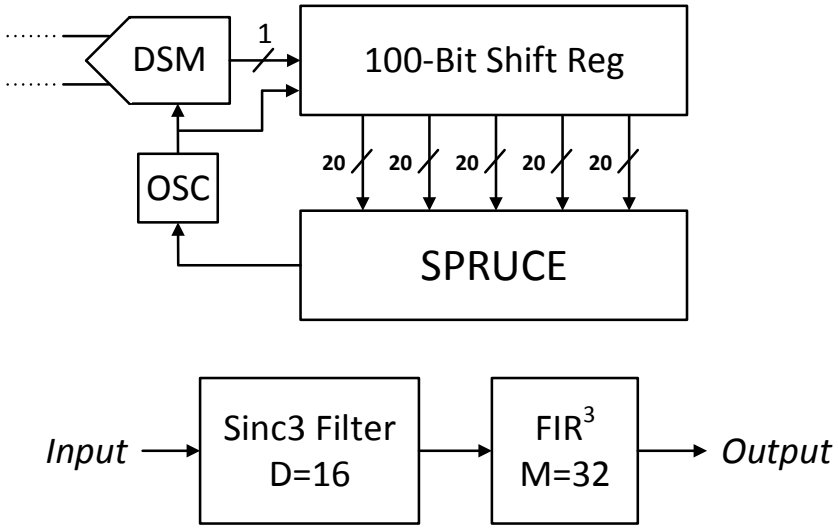


Figure 3.59: The interface between the DSM and SPRUCE (upper) the architecture of the digital filter implemented by SPRUCE (lower).

The architecture of this CIC filter is depicted in Figure 3.60. It includes three integrator stages and three comb stages. The z-domain transfer function for the CIC function is given by:

$$H(z) = \frac{(1 - Z^{-16})^3}{(1 - Z^{-1})^3} \tag{3.15}$$

The frequency response of this CIC filter is shown in Figure 3.61.

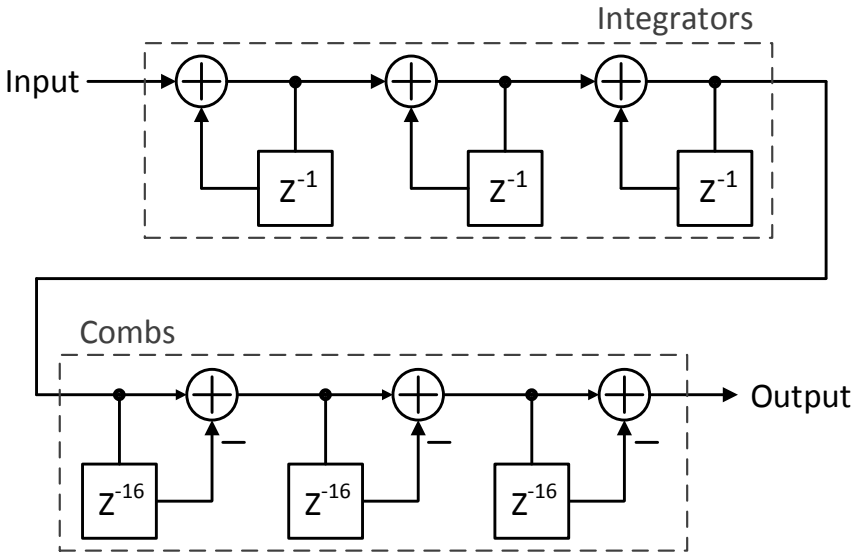


Figure 3.60: The 3rd order CIC (Cascaded Integrator-Comb) filter.

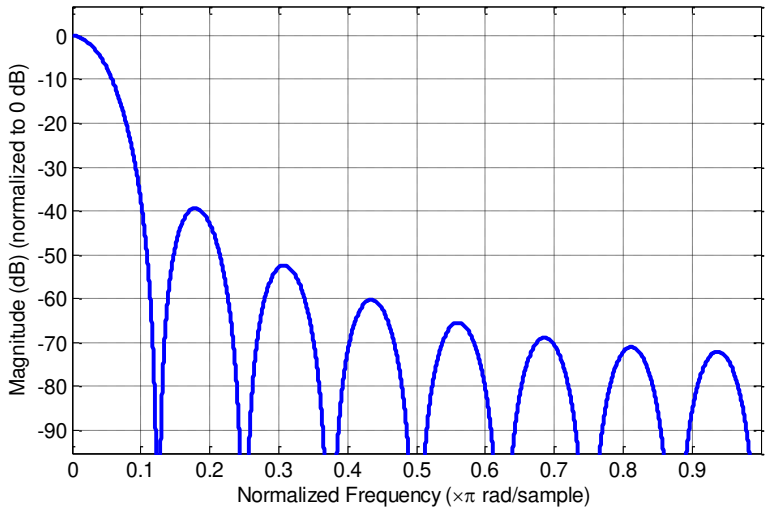


Figure 3.61: Frequency response of the 3rd order CIC filter with D=16.

The FIR filter after the CIC filter is implemented with a 3-stage moving average filter to further suppress the noise. Each moving average filter is with an order of 32 and the overall transfer function is:

$$H(z) = \frac{1}{32^3} \frac{(1 - Z^{-32})^3}{(1 - Z^{-1})^3} \tag{3.16}$$

The frequency response for this FIR filter is shown in Figure 3.62.

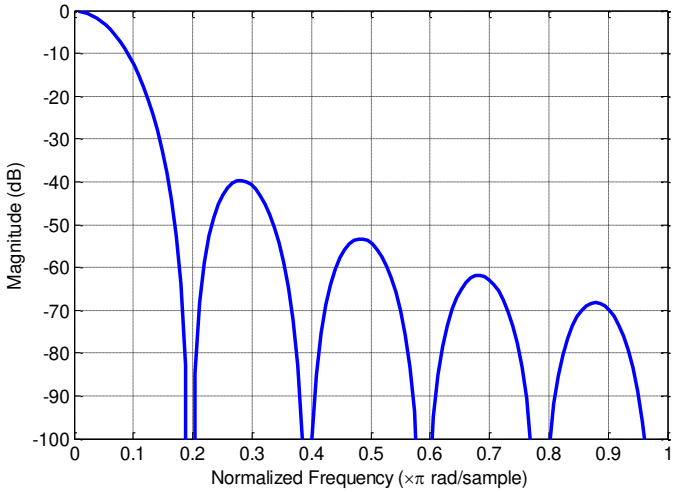


Figure 3.62: Frequency response of the 3-stage moving average filter.

With the data stored in the shift registers in the SPRUCE unit, both the CIC filter and FIR filter perform the arithmetic logic using the ALU. Every shift register is 20-bit wide and the SPRUCE unit is operating at 100MHz. After the 100-bit of data are fed through the filters, the outputs reach its final peak value at the 118th output. Therefore, the outputs are counted, and the 118th output is sampled and stored. In order to avoid integer overflow, the outputs at each stage of the filter are scaled by the gain of the filter. (The gain for the CIC filter is 4096, and the gain for each moving average filter is 32). The final result is stored in a specific memory address for further use.

The final FFT plot for the ADC after the decimation filter is illustrated in Figure 3.63. The input given is a slow sine wave with frequency of 7.3 kHz ($3\times10^7 / 4096$ Hz) and amplitude of ±1.2 V. The sampling data are divided into 100 points per group and fed into the designed decimation filter. With 4096 ADC output codes, the obtained SNDR is 61.3 dB. This translates to an ENOB of 9.9 bits. This is slightly below the design target (10 bits) but the resolution is more than enough for this application.

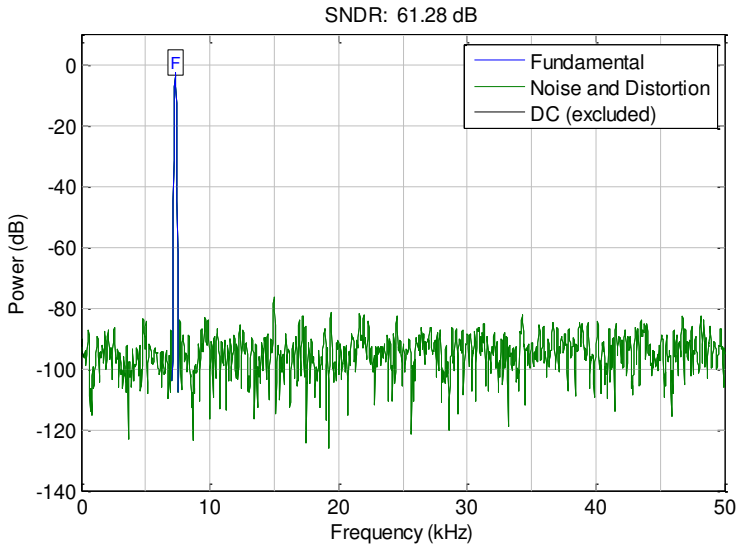


Figure 3.63: Final simulated SNDR plot after the decimation filter based on 4096 ADC output results.

The linearity of the ADC is determined with a histogram test as illustrated in Figure 3.64. The histogram of the 16384 output codes are recorded for a large number of samples for a slow input sinewave (1/0.16384 = 6.1 Hz) in one cycle. The results are compared with the number of samples from the theoretical sine-wave probability density function. The simulated static linearity performance for the ΔΣ ADC is shown in Figure 3.65. The specifications and simulation results for the ΔΣ ADC are summarized in Table 3.13.

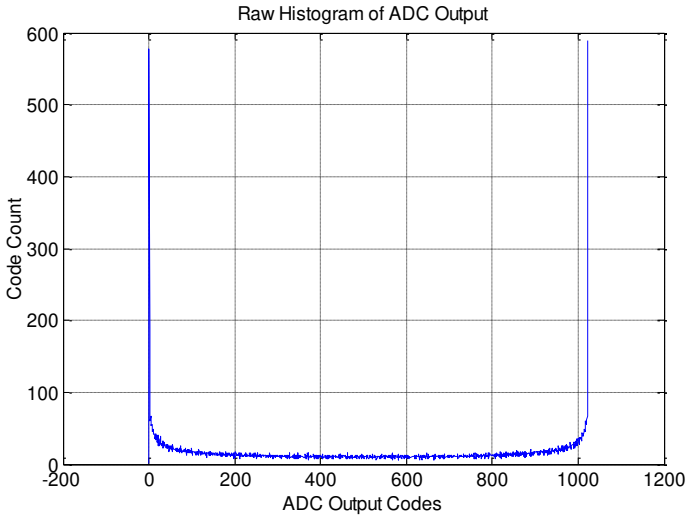


Figure 3.64: Histogram for the ADC linearity test.

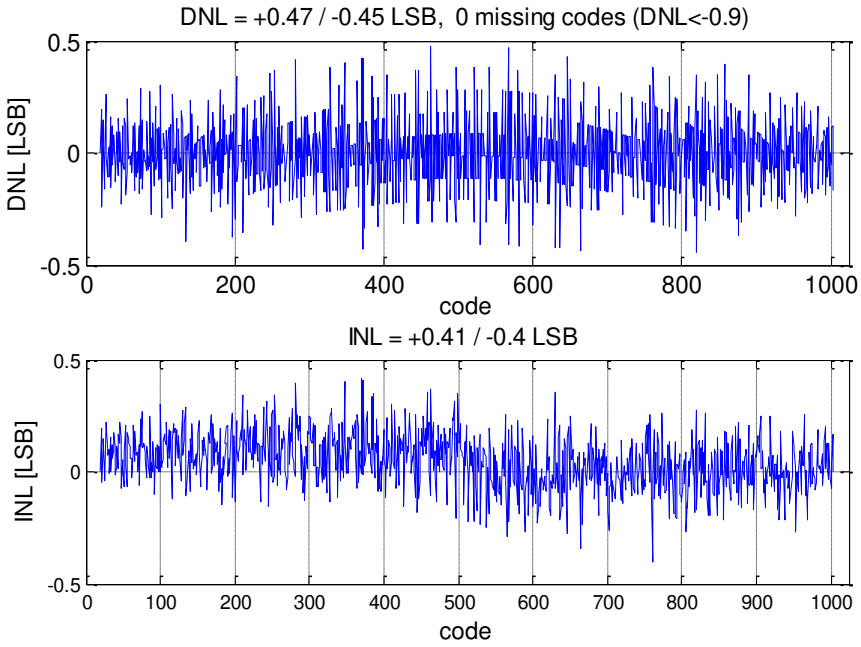


Figure 3.65: Simulated static linearity of the ΔΣ ADC.

Table 3.13: Summary of the specifications for the ΔΣ ADC.

Parameter	**Value**
V_{DD}	3.3 V
Quantization	1 bit
Technology	0.18um HV
Architecture	2nd Order
OSR	100
Input Signal Frequency	20 kHz
Clock Frequency	10 MHz
Input / Output Common Mode Voltage	1.65 V
Full Input Range	±1.6 V
Peak Input Amplitude	-2.5 dBFS (±1.2 V)
DAC Reference Voltages	0.8 V, 2.5 V
Simulated SNDR for the DSM	77.9 db
Simulated SNDR for the ADC	61.28 dB
Simulated DNL	±0.5 LSB
Simulated INL	±0.5 LSB
Power Consumption	71.4 mW

3.9. System Integration

3.9.1. Clock Synchronization

The I_C sensing circuitry involves several switched-capacitor circuit blocks and also clocked logic blocks. Therefore the system clock synchronization is of great importance. The system clock tree for the I_C sensing circuit is presented in Figure 3.66. There is only one input clock which is 15 MHz. It would go through a clock generator and generate two pairs of non-overlapping clock outputs. Ph1_a and Ph2_a are slightly advanced clock outputs compared to Ph1 and Ph2 in terms of timing. The architecture of the clock generator is similar to the one used for the ΔΣ ADC. The simulation results for the system clock generator are shown in Figure 3.67. The clock output Ph1 then goes through a clock divider to generate a synchronized output CLK2 of 3.75 MHz, which is 4 times slower.

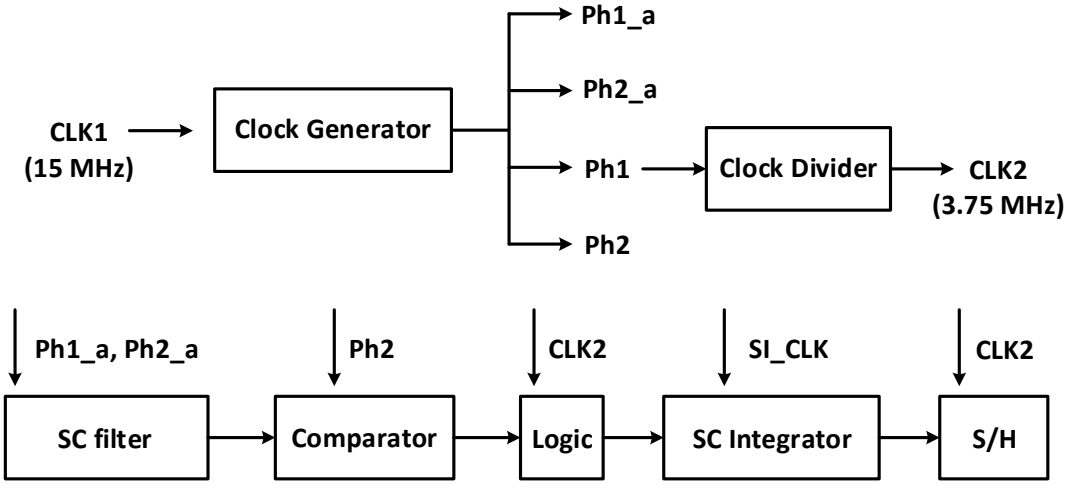


Figure 3.66: System clock tree for the I_C sensing circuit part.

The SC filter uses Ph1_a and Ph2_a as the two non-overlapping input clocks directly (they correspond to the P1 and P2 switching signals in the SC filter schematic in Figure 3.16). The subsequent comparator block samples the SC filter output at Ph2 when the SC filter output is stable. The slower CLK2 is used for the logic block for the fixed time integration and also the sample-and-hold block. In addition, the SC common mode

feedback circuits in the op-amps in the SC filter and SC integrator are using the 3.75 MHz CLK2 as well, since they do not need to operate as fast as the main circuits. The synchronization for the input clock of the SC integrator is processed separately as described in Section 3.6.

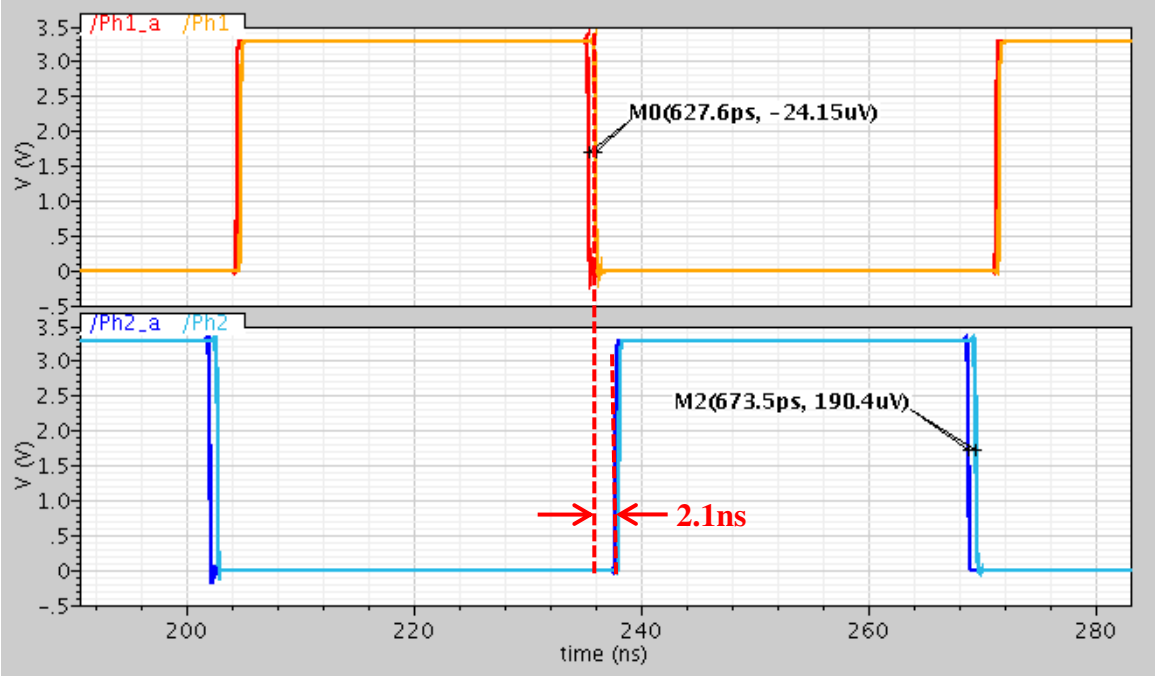


Figure 3.67: Transient simulation results of the system clock generator.

The ΔΣ ADC has a sampling clock frequency of 10 MHz. It samples the sample-and-hold block outputs which are held constant for almost the whole cycle. Therefore, the ADC clock does not need to be synchronized with any other clocks in the system.

The CPU is operating at 100 MHz. It only provides initial configuration for the I_C sensing circuitry and takes in the DSM outputs for digital filtering. Therefore, the CPU clock is standalone and is not necessary to synchronize with the ADC clock or the I_C sensing circuit clock as well.

3.9.2. System Configurability

Since the proposed current sensing method relies on the Miller plateau characteristics which may vary for different kinds of IGBTs, the chip is designed with high

configurability via the SPRUCE unit. In addition, the configurability could potentially improve the chip performance and overcome any process variations and mismatches to certain extent. The configuration bits with their default values for the I_C sensing circuit are listed in Table 3.14.

Table 3.14: Summary of the configuration bits for the I_C sensing circuitry.

pin_name	function	default
CB<3:0>	bias control	0011
EN_PA<1:0>	comparators enable	10
ON_EN	integrator input selection bit	0
OFF_EN	integrator input selection bit	1
S<5:0>	fixed time integration block configuration	0
SW_EN<3:0>	external signals option for functionality test	0101
MUX<3:0>	integrator configuration	0110
RC<3:0>	resistive divider control	0100
EN_BUF	output buffers enable	1
ADC_S<1:0>	adc input selection	10

There are 29 configuration bits in total. Some are used to prevent unexpected process variations such as RC<3:0> illustrated in Section 3.4.1. They are used in the HV resistive divider network. Similar design is used for the bias current generator as depicted in Figure 3.68. With default setting, CB<0> and CB <1> are on. This results in an output current of 17 µA for all the output branches.

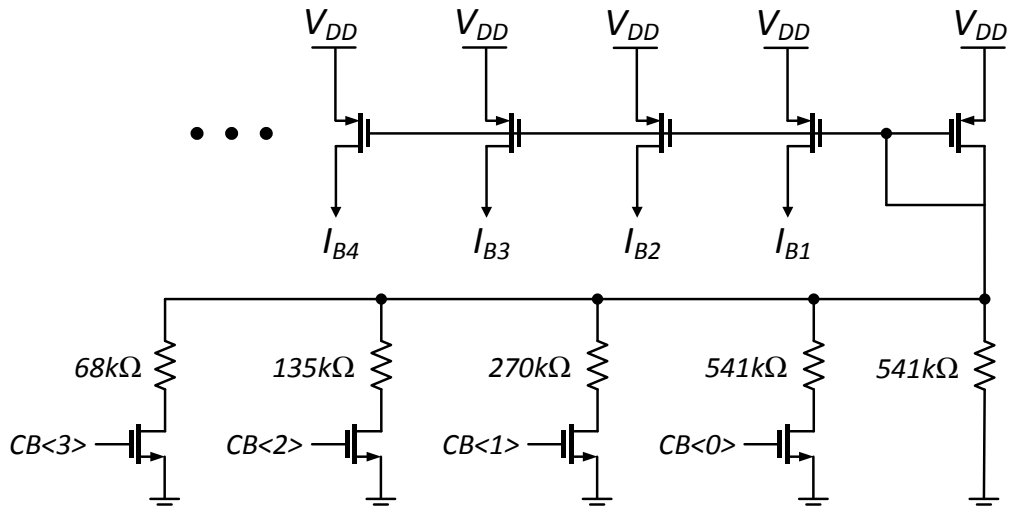


Figure 3.68: The configurable bias current generator for the I_C sensing circuit [88].

This chip needs to be configured differently for turn-on and turn-off testing, parameters including ON_EN, OFF_EN, and MUX<3:0> are set for this purpose. The S<5:0> bits used in the fixed time integration block are to improve the flexibility of this chip to adapt to different IGBT modules as explained in Section 3.5.4. Parameters SW_EN<3:0> and ADC_S<1:0> are used to make sure some of the key blocks including the SC filter, the SC integrator and the ADC can be tested separately for certain functionality evaluation. The remaining configuration bits EN_PA<1:0> and EN_BUF are used to shut down certain blocks when not in use to save power.

The configuration bits can be configured by SPRUCE directly by pushing the "on" or "off" (i.e. 1 or 0) instructions into the corresponding memory locations. The memory locations for these bits can be found in the memory map in Appendix A under X-Config section. Level shifters are needed between SPRUCE and the I_C sensing circuit, as SPRUCE is operating at 1.8V and the I_C sensing circuit is 3.3V.

Another way to set the configuration bits is to use a chain of shift registers as illustrated in Figure 3.69. There are four external pins, including clock, data, update and reset. Theoretically they can be used for unlimited number of configuration bits, but more bits would take longer time to program. With each clock cycle, each bit of data is shifted one block further into the chain of shift registers. After the last bit of data has been shifted in, the update signal will change all the configuration bits all together. The reset signal can reset all the shift registers to their default settings and the configuration bits will all go to their default values.

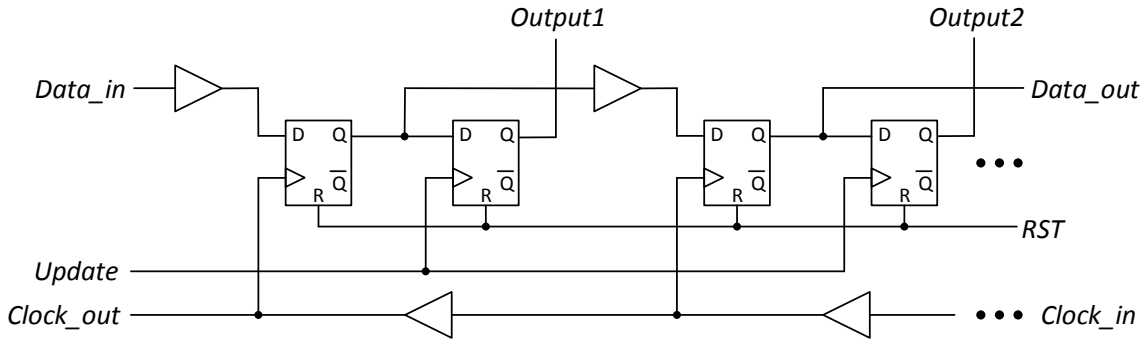


Figure 3.69: Shift registers used for the configuration bits.

3.9.3. Final Chip Layout

The final chip area is 5 mm × 5 mm. Based on the bond wire connection plan, the top level layout blocks were placed as shown in the micrograph of the chip in Figure 3.70. The SPRUCE unit is placed in the center of the chip to facilitate easy control access to the upper gate drivers (with selectable segmented output stage and PWM control) and the lower I_C sensing circuit (with configurations, ADC, and decimation filter, etc.). The output buffers (including digital output buffers and analog output buffers) surrounded the I_C sensing circuit are connected to the output pins for output probing purpose.

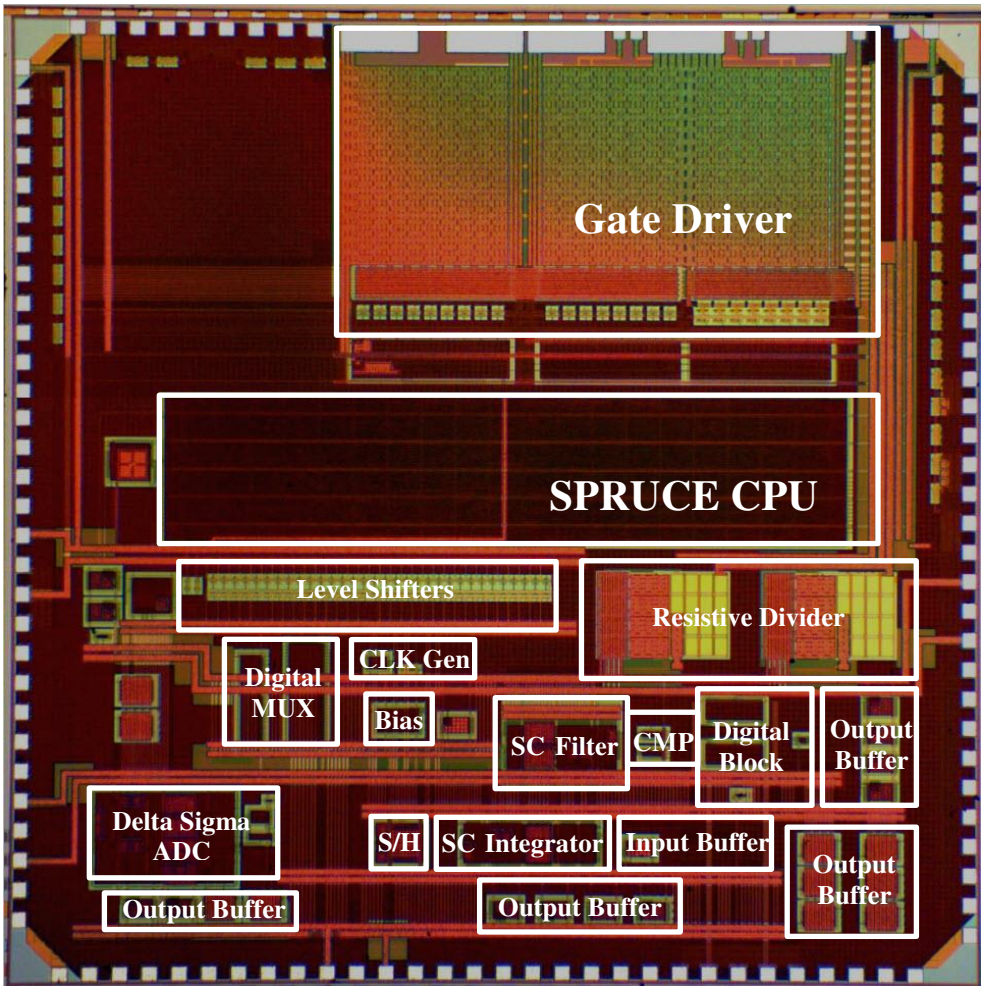


Figure 3.70: Micrograph of the gate driver IC, fabricated using TSMC's 0.18 µm BCD Gen-2 process (chip area 5 mm × 5 mm).

The package chosen for this gate driver IC is QFN100 due to the number of pins required to perform all the functionality tests. The bonding diagram of packaged IC is shown in Figure 3.71.

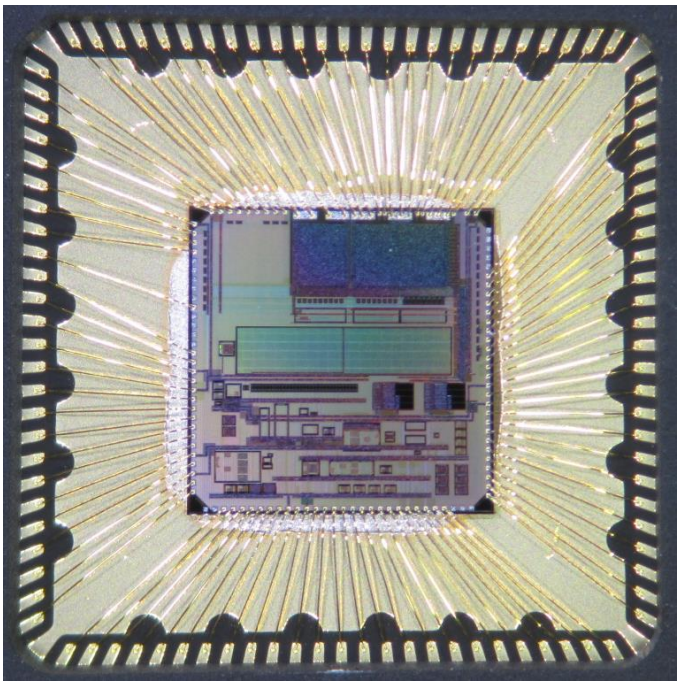


Figure 3.71: Bonding diagram of the gate driver IC chip in QFN 100.

3.10. Chapter Summary

This chapter presents the IC design information for the gate driver chip with integrated I_C current sensor. It is demonstrated with simulation results that each sub-block can meet the required design targets. Therefore, it is expected that the designed gate driver chip can perform I_C current sensing during turn-on and turn-off switching transients with an accuracy of ±1A at room temperature. Chapter 4 will discuss the testing setup and testing results for this gate driver chip. Due to the temperature sensitivity of the proposed current sensing method, extensive tests are also carried out at different ambient temperature conditions. Compensation techniques for the temperature effect will also be discussed.

Chapter 4

Results and Discussion

This chapter presents the testing results of the designed gate driver IC chip. The PCB board design and test setup is described in Section 4.1. Section 4.2 presents and discusses the functionality test results at room temperature. Section 4.3 includes the setup for the temperature effect testing, analysis of test results under different temperature conditions and the proposed technique for temperature effect compensation. Finally, Section 4.4 summarizes the results and issues encountered.

4.1. Test Setup

The fabricated gate driver IC is housed in a QFN100 package and mounted on a custom PCB plugged directly on top of a modified Fuji Electric 7MBP200VEA060-50 IGBT module, with the original driver board removed. The experiment test setup is shown in Figure 4.1. The setup is similar to the discrete implementation. Below the top level PCB is the PCB "Level 1" with only connectors as shown previously in Figure 2.12 (b) in Section 2.3.1. The bottom of the setup is the power module base with six IGBTs and six freewheeling diodes (FWDs) as shown in Figure 1.3 (b) in Section 1.1.3.

The test PCB board on the power module is designed to drive one of the low-side IGBTs in the IPM as illustrated in Figure 4.2. The PCB includes LDOs for the power supplies and reference voltages, oscillators for the clock inputs, a connector to a Raspberry Pi for initial CPU programming, and a 4 digit LED display connected to the SPRUCE GPO

(General Purpose Output) to provide the ADC output (from 0 to 1024), or to provide the instant readout for the turn-on and turn-off I_C level. The LED display has a built in driver and a serial interface, simplifying the connection to the CPU. The pull-up and pull-down resistors next to the connector for the Raspberry Pi are used to hold the output states of the output pins. Thus once the initial programming of the SPRUCE is done, the connection to the Raspberry Pi can be shut off, and the system can still run on its own without any external micro-controller. Detailed list and descriptions of the components for this PCB are provided in Table 4.1.

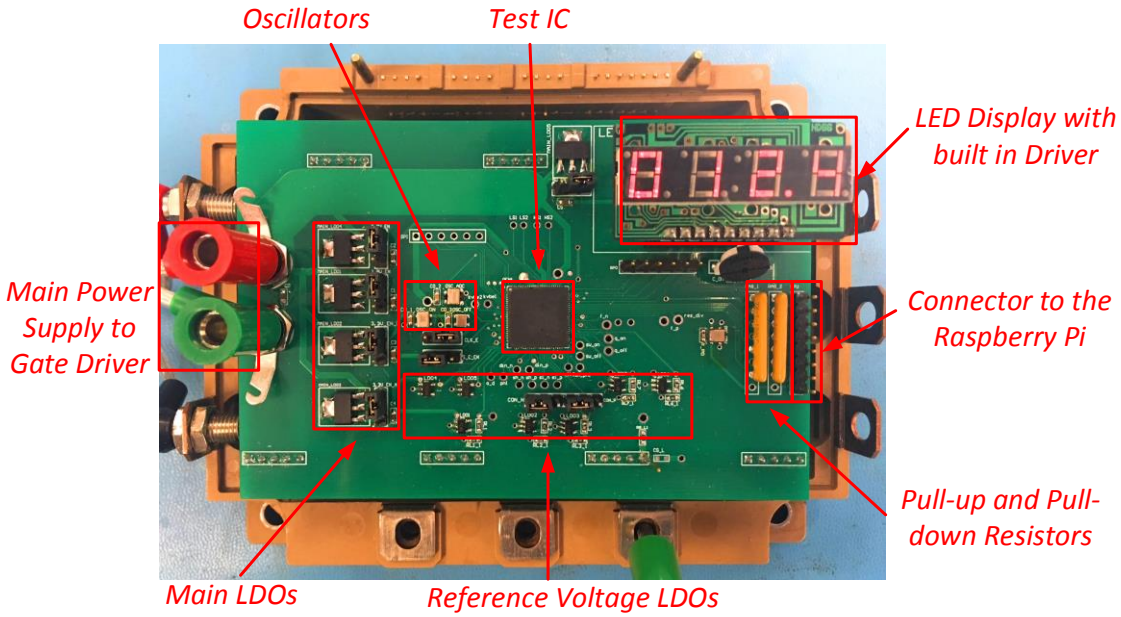


Figure 4.1: Experimental test setup for the gate driver IC with real time collector current display.

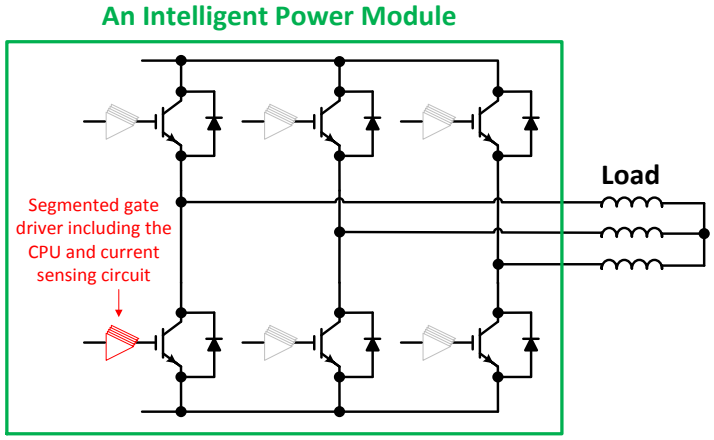


Figure 4.2: The proposed gate driver IC is intended to be incorporated into IPMs.

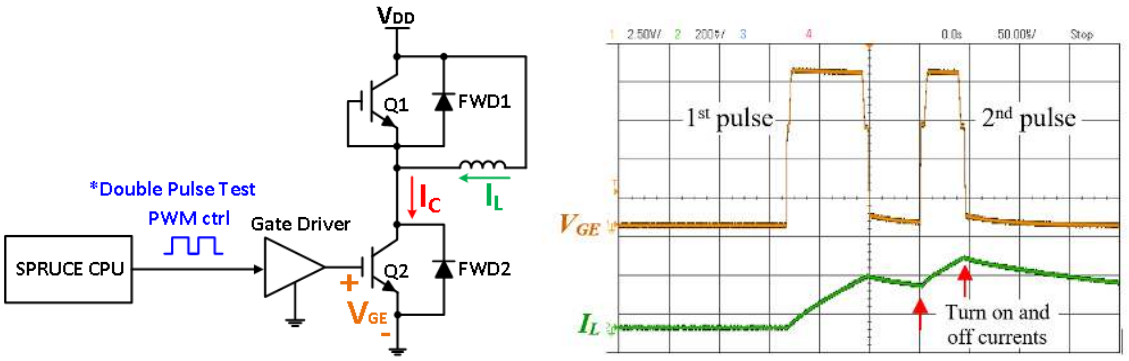
Table 4.1: Component List for the Gate Drive IC test PCB

Component	value	NO.	Model number	Description
Oscillator	10MHz	1	XLH335010.000000I	Sampling clock for the ADC
Oscillator	15MHz	1	SG-210STF 15.0000ML	I_C sensing circuit system clock
Oscillator	100MHz	1	KC3225A100.000C3GE00	SPRUCE CPU clock
LDO	1.8V		NCP1117ST18T3G	CPU and gate driver digital power supply
LDO	3.3V	3	NCP1117ST33T3GOSCT-ND	Gate driver power supply
				I_C sensing circuit analog power supply
				I_C sensing circuit digital power supply
LDO	2.5V	1	LD39015M25R	V_{REF+} for DSM
LDO	0.8V	1	LD39015M08R	V_{REF-} for DSM
LDO	Adjustable	4	LDCL015MR	V_{REF} for common mode voltage
				V_{REF} for comparator at turn-on
				V_{REF} for comparator at turn-off
				V_{REF+} for SC integrator
				V_{REF-} for SC integrator
LDO	5V	1	NCV4264-2ST50T3G	Power supply for the LED
LED	4-bit	1	LTM-8328PKR-04	4-bit LED display

The simplified test bench schematic is depicted in Figure 4.3 (a). The same double pulse test setup is used to turn the low side IGBT (device under test) on and off. The high side IGBT is always off. The current flows through the inductor and the high side FWD when the low side IGBT is off. The minimum turn-on current flowing through the low side IGBT is set by the first pulse width (for minimum turn-off I_C, the second pulse width also plays a role). The supply voltage V_{DD} is increased step by step until I_C reaches its full testing range. The measurements are performed at the rising and falling edges of the second gate pulse, as shown in Figure 4.3 (b).

Compared to the discrete implementation where the double pulse test was controlled by an external FPGA, all the digital programming for this test is provided by the internal SPRUCE unit. The basic timing diagram of the testing procedure at the turn-on of the IGBT is illustrated in Figure 4.4. First, the SPRUCE unit sets all the configuration bits for the I_C sensing circuitry. This is followed by the double pulse test. The turn-on Miller plateau sensing circuit generates a pulse that is inside the Miller plateau region and with a fixed pulse width. After the plateau sensing, the integrator integrates the voltage

difference between V_{DD} and V_{GE} during V_{SW}. After the second pulse, the SPRUCE unit takes the DSM output and performs digital filtering, and sends the output results to the LED display.



(a) (b)

Figure 4.3: (a) The double pulse test bench schematic, (b) Measured waveforms for V_{GE} and I_L during the double pulse test [V_{GE}: 2.5V/div, I_C: 2A/div].

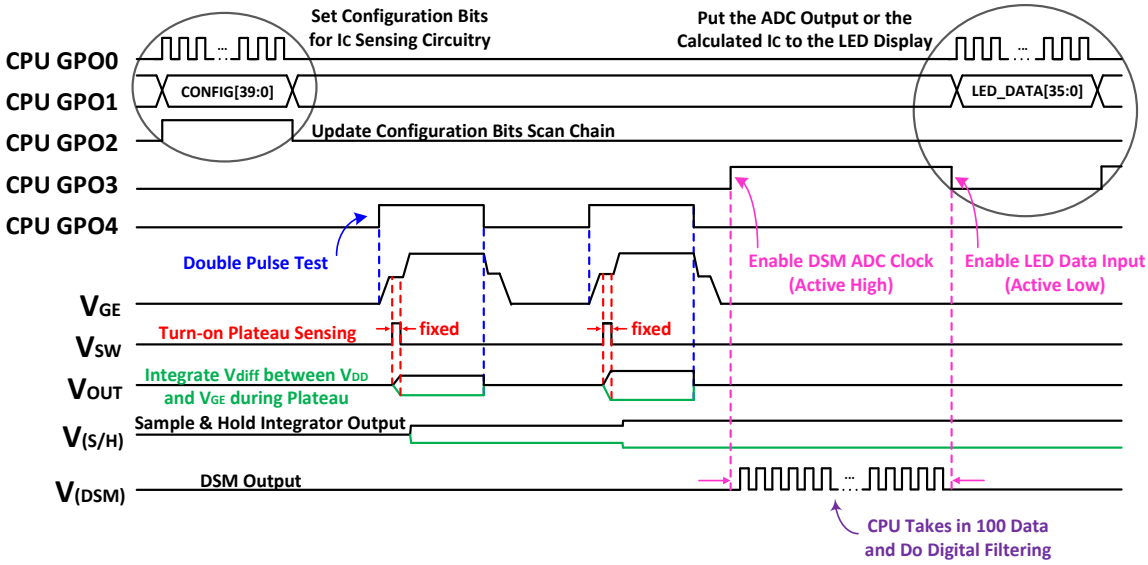


Figure 4.4: Timing diagram for the sensing of I_C during turn-on.

4.2. Functionality Test Results

The basic functional test for the IC chip is first performed at room temperature for simplicity. All the configuration bits are set properly for the test setup. The gate driver is designed with 8 output segments to provide different gate resistances, ranging from 0.35 to 41.9 Ω as listed in Table 3.2 in Section 3.3. The resistances for the pull-up and pull-down segments are selected to be 5.26 Ω and 13.99 Ω, respectively. The 13.99 Ω is obtained by turning on both the 21.0 Ω and 41.9 Ω segments which are connected in parallel. The selection for the gate driver segments is based on the requirement for the minimum plateau length during switching transients. With the selected segments, both the turn-on and turn-off plateau durations are around 2 µs.

Figure 4.5 shows the measured waveform of the IGBT gate node and the output waveform of the high voltage resistive divider. It can be seen that the voltage level is brought down from above 10 V to below 3.3 V for compatibility with the signal processing circuit for I_C sensing. With the default configuration of the resistive divider set to 0100 for RC<3:0>, the measured output to input ratio is around 0.266, less than the calculated ratio of 0.294. However, this kind of deviation is expected due to the large process variation for the typical n-well resistance and this would not impact the system performance.

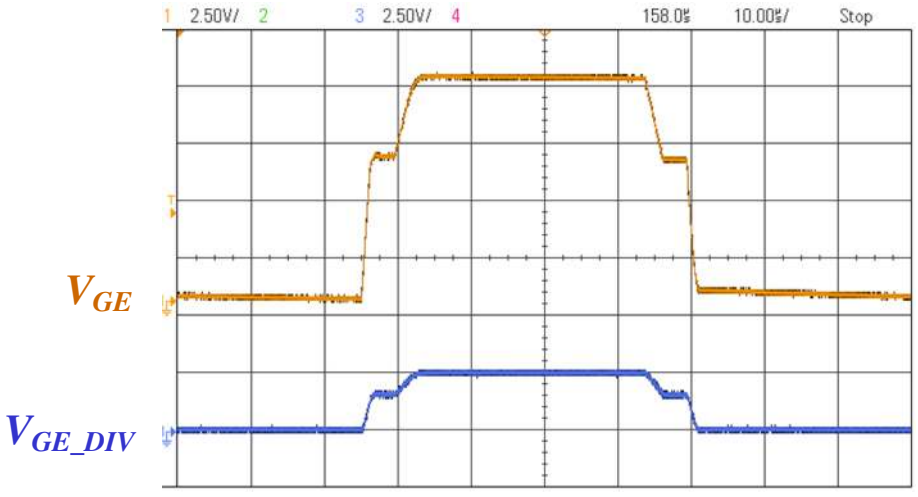


Figure 4.5: Measured waveforms for V_{GE} and the HV resistive divider output V_{GE_DIV} [V_{GE}: 2.5 V/div, V_{GE_DIV}: 2.5 V/div].

After the input resistive divider and buffer stage, the measured output waveforms for the SC filter are shown in Figure 4.6. The outputs are fully differential; with the time between the weak analog double pulses correspond to the Miller plateau region during turn-on and turn-off. The outputs are then fed to the comparators for the plateau sensing. The common mode voltage for the SC filter outputs is 1.65 V. It is the same for the subsequent fully differential stages.

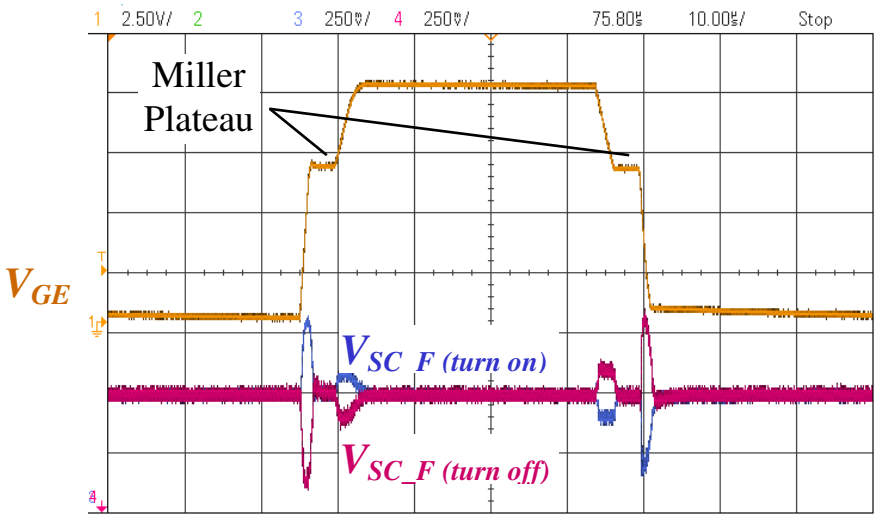


Figure 4.6: Measured waveforms for V_{GE} and the SC filter output V_{SC_F} [V_{GE}: 2.5 V/div, V_{SC_F}: 0.25 V/div].

The output waveforms from the comparators for turn-on and turn-off are shown in Figure 4.7 and Figure 4.8, respectively. It should be noted that V_{CMP} is a single pulse for turn-on while for turn-off it is a double pulse. This is because the reference voltage for the comparator is purposely set high for turn-on to increase the immunity to gate ringing at high current levels, as explained in Section 3.5.3. The measured waveforms match with the simulated results as well. The comparator V_{REF} for turn-on is set at 1.8V and for turn-off is set at 1.7V.

The logic block output V_{SW}, serves as the trigger signal for the SC integrator. It is clearly shown that the triggering signal is well within the plateau region for both turn-on and turn-off.

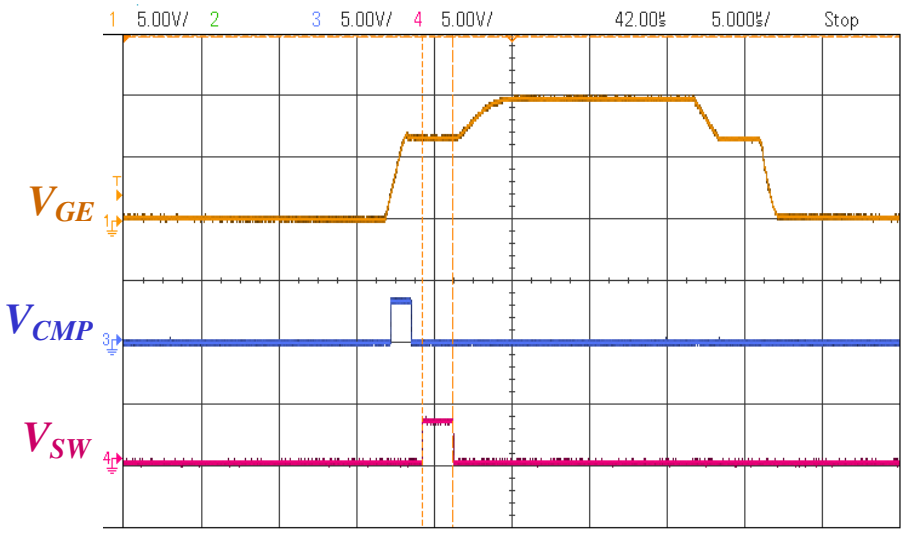


Figure 4.7: Waveforms for V_{GE}, the comparator output, V_{CMP} and the logic output, V_{SW} for turn-on transient [V_{GE}: 5 V/div, V_{CMP}: 5 V/div, V_{SW}: 5 V/div].

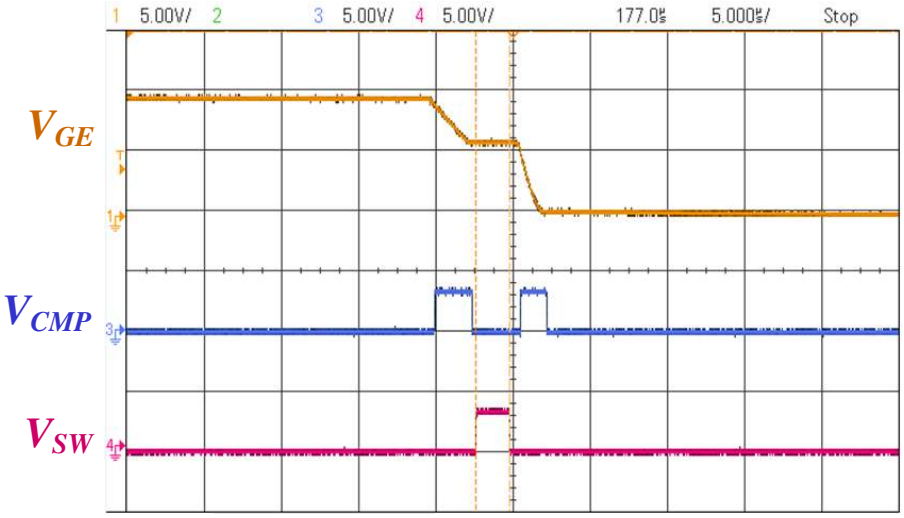


Figure 4.8: Waveforms for V_{GE}, the comparator output, V_{CMP} and the logic output, V_{SW} for turn-off transient [V_{GE}: 5 V/div, V_{CMP}: 5 V/div, V_{SW}: 5 V/div].

Figure 4.9 and Figure 4.10 show the waveforms at the integrator output for turn-on and turn-off. For the room temperature testing, the integration time is fixed at 2.1 µs, while the V_{REF_DIFF} of the integrator for turn-on is set to be 1.35 V and for turn-off is 1.85 V. This combination is to maximize the range of the integrator output to achieve better resolution. Meanwhile the outputs are still within the desired input range of the subsequent ADC stage.

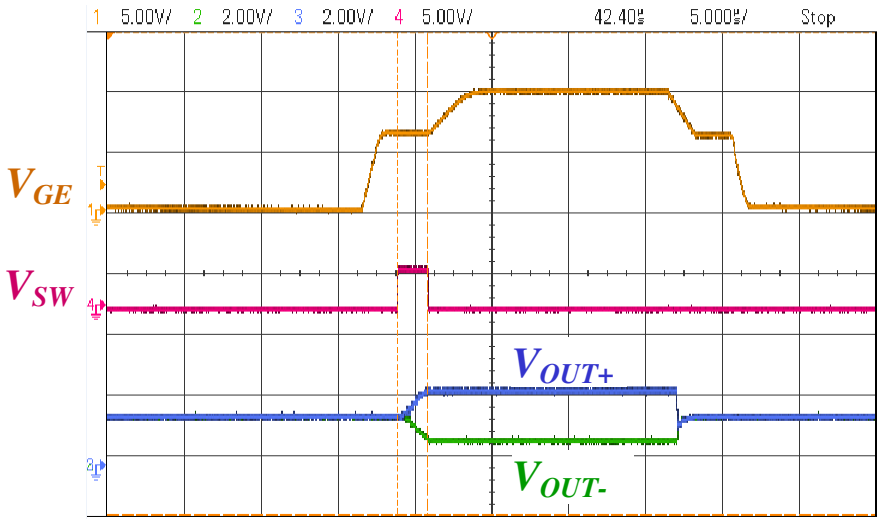


Figure 4.9: Waveforms for V_{GE}, V_{SW} and SC integrator outputs, V_{OUT+} and V_{OUT-} for turn-on transient [V_{GE}: 5 V/div, V_{SW}: 5 V/div, V_{OUT+} and V_{OUT-}: 2 V/div].

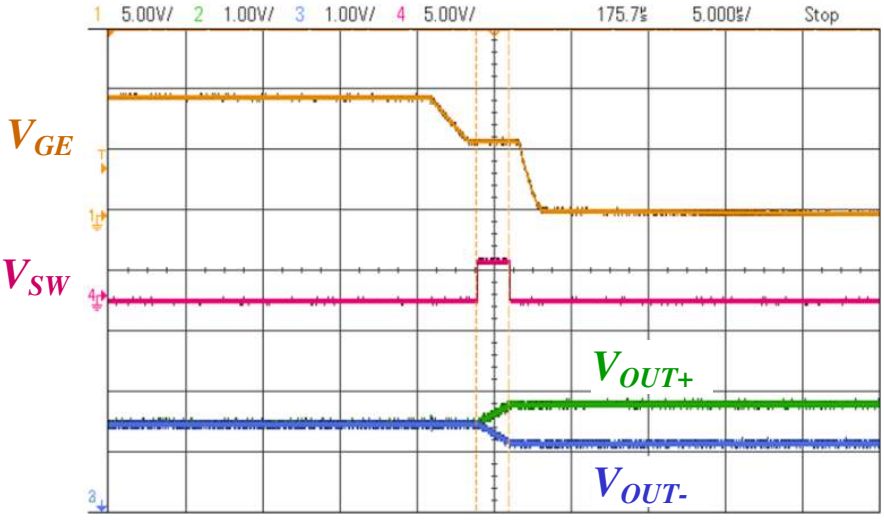


Figure 4.10: Waveforms for V_{GE}, V_{SW} and SC integrator outputs, V_{OUT+} and V_{OUT-} for turn-off transient [V_{GE}: 5 V/div, V_{SW}: 5 V/div, V_{OUT+} and V_{OUT-}: 2 V/div].

After the SC integrator stage, the sample-and-hold block maintains the integrator output until the next cycle. The DSM is enabled shortly after the sample-and-hold block settles. It keeps sampling the output and the last 100 bits of the quantizer output is fed back to the CPU. The CPU performs digital filtering and produces the final ADC output. The ADC outputs are displayed on the 4-digit LED, and are recorded as I_C is varied across the entire testing range. Figure 4.11 and Figure 4.12 show the ADC output codes as a function of I_C for turn-on and turn-off. The experiment is carried out using three different

IGBTs in the same IPM and the results exhibit a small device to device variation. A quadratic fit is used to compensate this variation as it is easy to implement in the on-chip stack-based CPU.

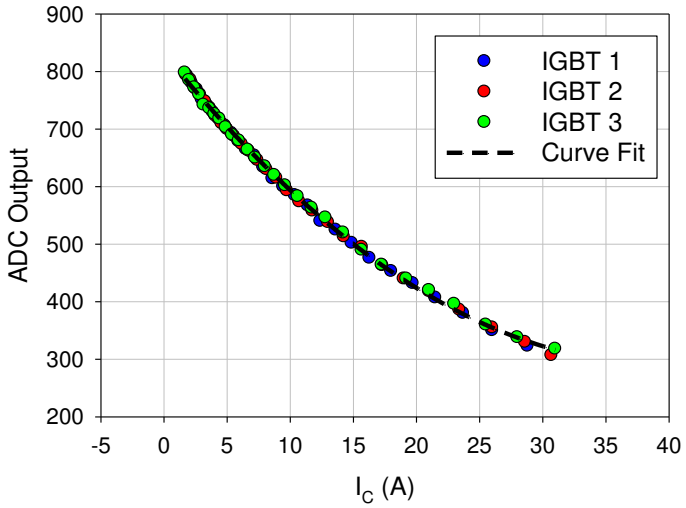


Figure 4.11: ADC output vs. I_C for three different IGBTs during turn-on at room temperature.

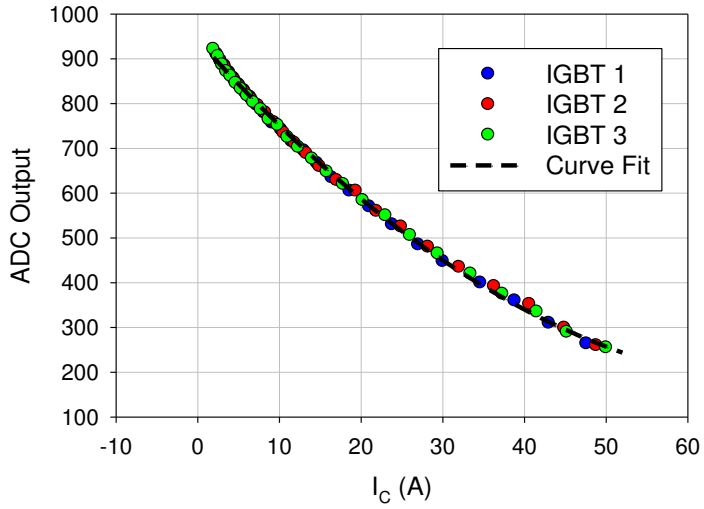


Figure 4.12: ADC output vs. I_C for three different IGBTs during turn-off at room temperature.

Repetitive double pulse testing on the three different IGBT devices is carried out to demonstrate the accuracy of this technique. As shown in Figure 4.13, the displayed I_C (on

the LED mounted on the PCB board) and the measured I_C (using the current probe) values are both recorded for the turn-on and turn-off transients. The deviation of the displayed I_C versus the measured I_C are well within ±0.9 A range for both turn-on and turn-off with 80 data samples for each condition. Therefore the targeted ±1 A accuracy is achieved within the current range of 1 to 30 A for turn-on and 1 to 50 A for turn-off.

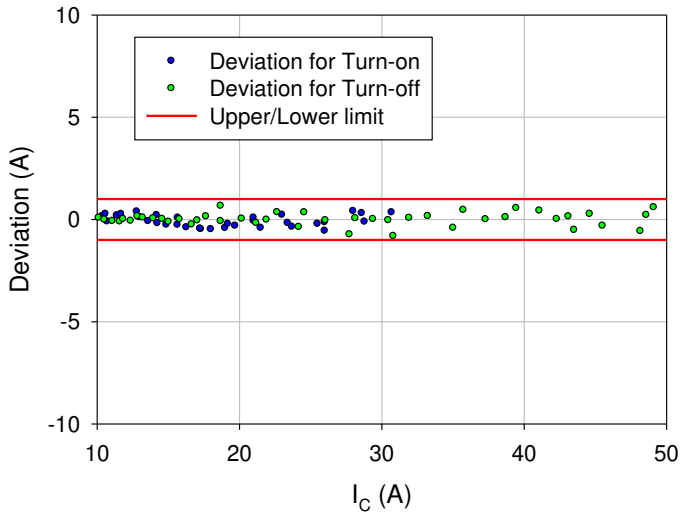


Figure 4.13: Deviation of the displayed I_C to the probed I_C.

In fact, the relationship between I_G and I_C (as described in equation (2.9) and (2.10) in Section 2.1.2) does not follow a second order polynomial relationship. Therefore, the resolution could be further improved if higher order of polynomial curve fitting is implemented. A lookup table of the I_C values versus the ADC codes with enough data points may also improve the accuracy substantially, and the SPRUCE unit has enough memory space to store the data. However, before too much effort has been made for data processing, the temperature sensitivity test for this technique needs to carried out and the temperature effect should be compensated first.

4.3. Temperature Testing and Compensation

As it is knows that the proposed current method is sensitive to temperature change. The IGBT module and driver board are put in a climate chamber for temperature sensitivity test, as shown in Figure 4.14. Beside the chamber, the remaining test setup is the same as in the room temperature functionality test. The testing procedure also remains the same. The Raspberry Pi is needed for the initial programming of the SPRUCE unit. However, the digital cables are not pulled off during the testing as it is difficult to pull the cables from the board inside the oven.

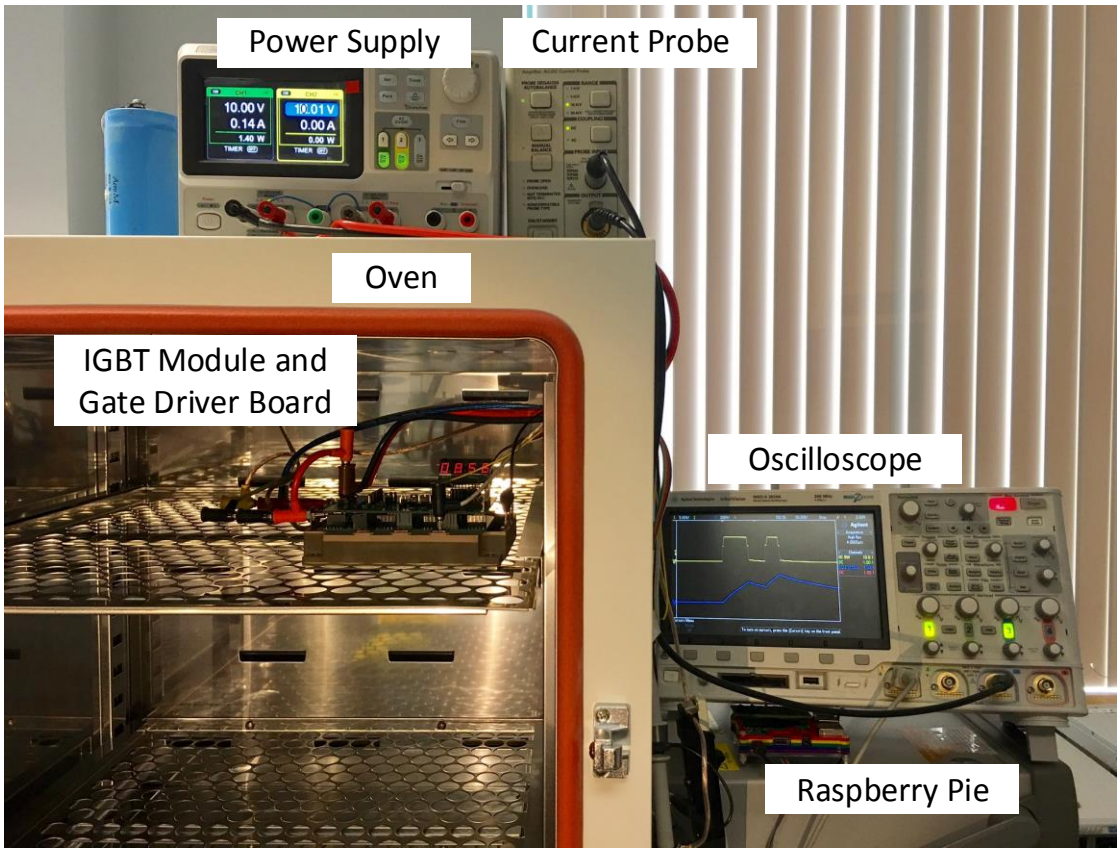


Figure 4.14: Experimental test setup for the gate driver IC in the oven.

The same double pulse test is performed at different temperatures. Slower pulsing rate is implemented (i.e., the interval between each double is more than one second) to avoid self-heating of the IGBT device. The fixed integration time is shortened to 1.33 µs compared to the previous 2.1 µs in the room temperature testing. In addition, the

V_{REF_DIFF} of the integrator for turn-on and turn-off are changed to 1.4 V and 1.8 V, respectively. This is mainly because the temperature effect would increase the integrator output range. The integration time and V_{REF} of the integrator are adjusted accordingly to make sure that the output of the integrator is within the desired ADC input range of ±1.2 V. Figure 4.15 and Figure 4.16 show the ADC output codes as a function of I_C for turn-on and turn-off transients at different ambient temperatures from 25 to 75 ^{o}C.

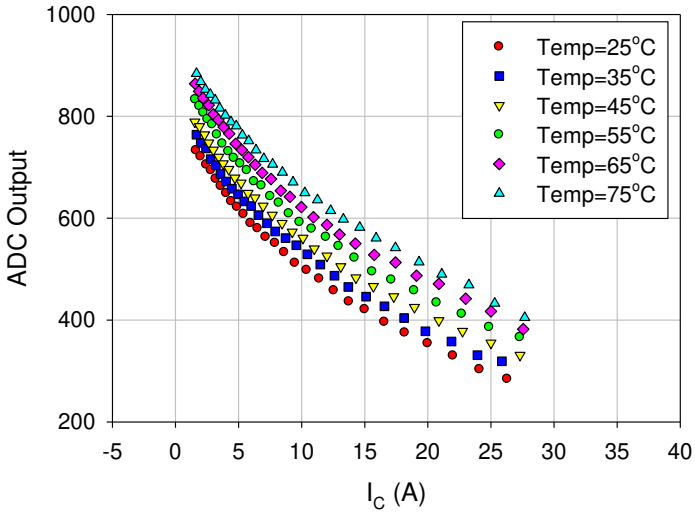


Figure 4.15: Measured ADC output vs. I_C at different ambient temperatures during turn-on.

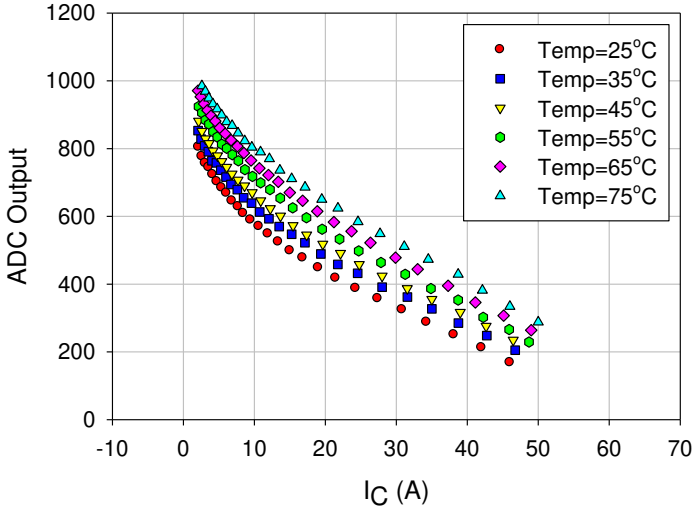


Figure 4.16: Measured ADC output vs. I_C at different ambient temperatures during turn-off.

The experiments are also carried out using three different IGBTs at different ambient temperatures (at 35, 55, and 75 ^{o}C), as shown in Figure 4.17 and Figure 4.18. The results exhibit a small device to device variation. However, it clearly shows that the proposed technique is sensitive to temperature variations.

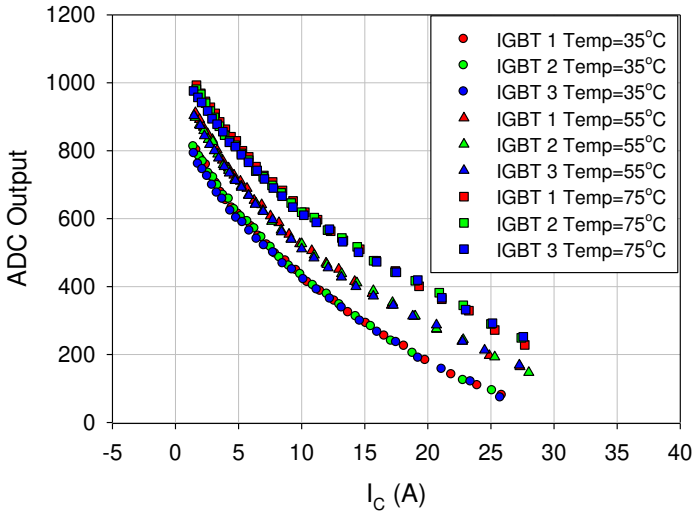


Figure 4.17: Measured ADC output vs. I_C at different ambient temperatures during turn-on for three different IGBTs.

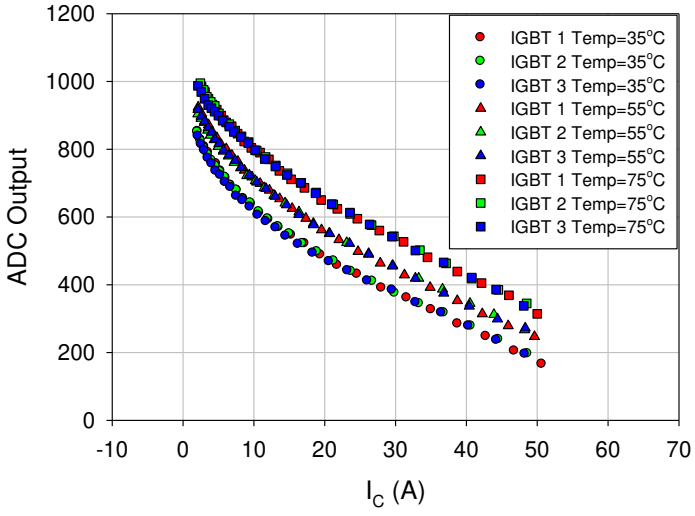


Figure 4.18: Measured ADC output vs. I_C at different ambient temperatures during turn-off for three different IGBTs.

Referring to Equation (2.9) and (2.10) in Section 2.1.2 which describe the relationship between I_G and I_C during turn-on and turn-off, both G_m and V_{th} of the IGBT are temperature sensitive parameters [95]. Therefore, the Miller plateau voltage value which corresponds to a specific I_C would change with temperature. Furthermore, the R_G realized using power MOSFETs segments are also subjected to temperature variation, this may also impact the driving strength of the IGBT and hence the Miller plateau voltage to certain extent.

Figure 4.19 and Figure 4.20 depict the extracted gate voltage in the Miller plateau versus I_C for turn-on and turn-off transients at different ambient temperatures. It demonstrates that the gate Miller plateau voltage changes with temperature for a given I_C value. This is the main reason for the variations of the ADC readouts versus I_C with temperature.

It is also verified that the relationship of the integrator outputs (Interpreted from the ADC readouts) and the Miller plateau voltages match Equation (3.10) in Section 3.6 (which describes the relationship between the Miller plateau voltage and the integrator outputs) quite well for both turn-on and turn-off transients.

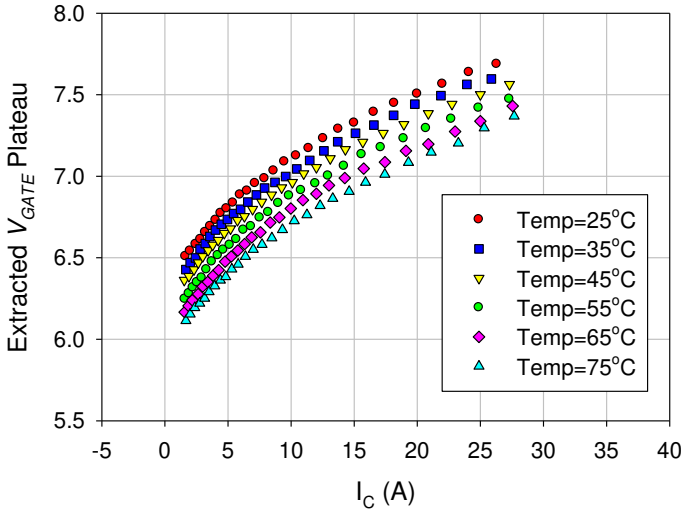


Figure 4.19: The extracted gate plateau voltage vs. I_C at different ambient temperatures during turn-on.

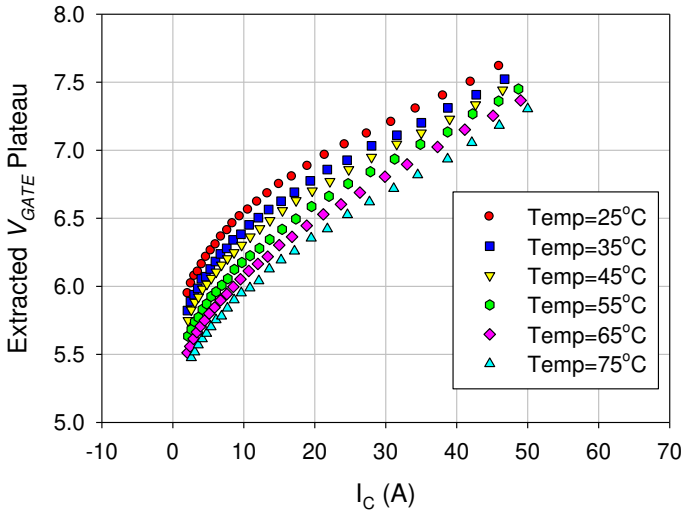


Figure 4.20: The extracted gate plateau voltage vs. I_C at different ambient temperatures during turn-off.

For the I_C sensing circuitry, the main circuit blocks are mostly switched capacitor circuits (filter, integrator and also DSM) that are insensitive to temperature change. Simulation results show that for a given Miller plateau voltage, the ADC outputs would change by less than 2% when temperature changes from 25 to 75 ^{o}C.

Considering the fact that IGBT is usually operating in high temperature conditions, temperature compensation is necessary for this current measurement technique. A 3rd order polynomial curve fitting is carried out using MATLAB for I_C versus ADC output codes and the ambient temperature, as depicted in Figure 4.21 and Figure 4.22. The residues across the full testing range are within ±0.5 A. Compared to the curve fitting for the room temperature test, there are two inputs (the ADC codes and ambient temperature). This makes the lookup table option impractical since too many measured data points are required to ensure proper accuracy. Therefore, polynomial curve fitting is preferred in this case. In addition, the on-chip SPRUCE unit can accept the digitized readout from any temperature sensor and perform the 3rd order polynomial curve fitting. Therefore, the temperature effect could be compensated internally on a single chip.

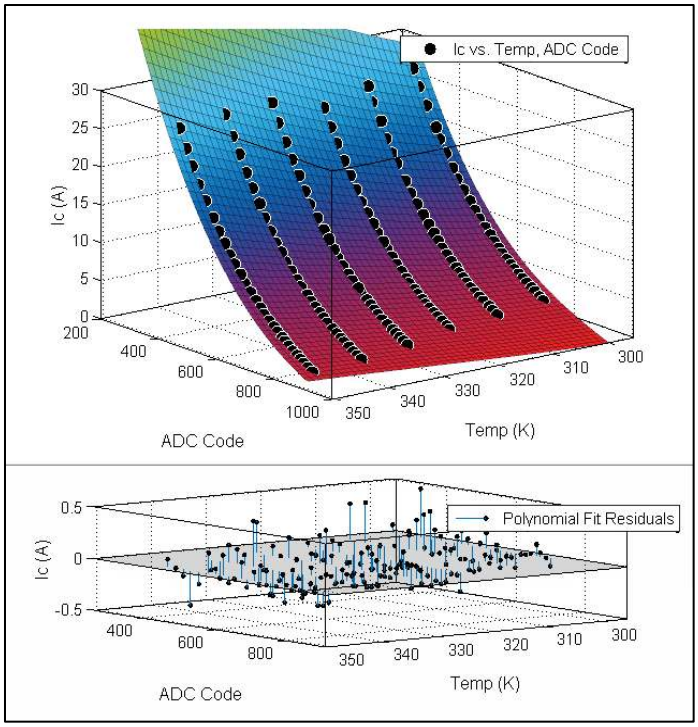


Figure 4.21: *Ic* vs. ADC output codes and temperature, and the 3rd order polynomial fit (Top). The polynomial fit residues plot (Bottom). (For IGBT Turn-on).

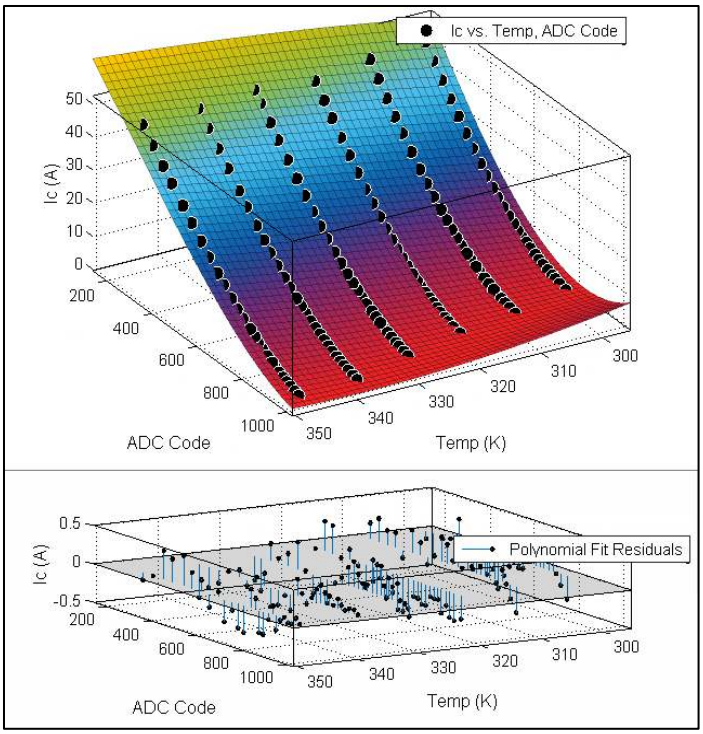


Figure 4.22: *Ic* vs. ADC output codes and temperature, and the 3rd order polynomial fit (Top). The polynomial fit residues plot (Bottom). (For IGBT Turn-off).

4.4. Chapter Summary

A summary of the chip performance is presented in Table 4.2. The chip performance is mainly limited by two considerations: the package and the SPRUCE CPU.

Table 4.2: Chip performance summary.

Technology [µm]		0.18
V_{DD} [V]		3.3
Chip Size	Total [mm×mm]	5×5
	CPU [mm×mm]	0.8×3.6
	Gate Driver Size [mm×mm]	1.2×2.7
	I_C Sensing Circuitry [mm×mm]	1.5×4
Power Consumption	CPU [mW]	36
	Gate Driver [mW]	320
	I_C Sensing Circuitry [mW]	113
IGBT Switching Frequency [Hz]		20K
I_C Sensing Testing Range [A]		0-50
I_C Sensing Testing Temperature Range [^{o}C]		25-75
I_C Sensing Accuracy [A]		±0.5A

The package used for this chip (QFN100) is oversized due to the pins needed for the reference voltages, debugging purpose and functional tests, as shown previously in Figure 3.71. However, since all the signals are processed internally with fully differential processing architecture throughout the signal path, the overall chip performance is still acceptable. Nevertheless, it is expected that if the current testing range is further expanded, the accuracy would be deteriorated greatly due to the EMI effect. Especially for the turn-on current sensing, due to the excessive ringing on the gate node, the plateau sensing may not even be functional. For the same design, if a much smaller package could be used, the current testing accuracy could be further improved and the current measurement range could be further extended.

The SPRUCE unit in this application provides intelligent on-chip digital processing. However, it was not a good ideal to implement the digital filtering using the SPRUCE unit. This is because only one stack is available for the all the basic operations.

Meanwhile a large amount of arithmetic operations are needed for the digital filter. Therefore, the implemented digital filter is extremely slow. The measured processing time for the digital filter is around 2 ms. This means that the current readout cannot be obtained within one switching cycle. A simple solution is to synthesize a stand-alone digital filter block using Verilog. ModelSim simulations have been carried out for the same filter presented in Section 3.8.4. With a clock frequency of 100 MHz, the digital processing time is well within 5 μs. Considering the switching frequency of the IGBT is 20 kHz, the current reading could certainly be achieved within one cycle.

The digital filter implemented in this thesis is unconventional for a DSM, since the outputs are chopped to 100 data per group, and every 100 data is converted to one digital output. While a conventional digital filter for any DSM would process the output continuously (usually way more than 100 continuous data points), decimate and filter them at the same time. The data stream is only chopped at the output of the filter to convert to the final digital output. Much higher ENOB could be achieved easily in this way. However, in this particular design, the CPU only provides 5 shift registers to store 100 continuous data points. The digital filter must operate under this limitation to achieve the desired the ENOB.

Chapter 5

Conclusion and Future Work

5.1. Conclusions

The main contribution of this thesis it that is proposes a new method to measure the IGBT collector current (I_C). This technique indirectly estimates the I_C using the gate current (I_G) during the Miller Plateau of the IGBT switching transients. The physical relationship between I_G and I_C during the Miller plateau is theoretically verified through basic device modeling. This relationship is unique for a particular IGBT structure and is only affected by temperature and process variations. Physical experiments demonstrated that the proposed technique could be used for voltage up to 250 V and currents up to 30 A with 2 % inaccuracy.

Compared to conventional collector current sensing techniques for IGBTs, this technique only utilizes low voltage signal at the gate side. There is no need to access the high voltage IGBT collector and the load. Therefore, this technique can be fully integrated into the gate driver I_C to realize on-chip current regulation without any extra discrete components. Furthermore, this technique is immune to the load voltage fluctuations, as higher load V_{DD} would only increase the V_{GE} or I_G plateau length without changing the plateau level.

The main limitation of this technique is that it can only estimate the current during the plateau region. Therefore, for current regulation purpose, this technique would be more suitable for applications in constant load or slow changing load conditions such as constant speed motor drives. In addition, this method cannot be used for over current protection or short circuit protection. Supplementary circuitry will be needed for protection purposes.

An automatic gate current sensing system which utilizes this technique is first implemented using discrete components. The Miller plateau region during the turn-on and turn-off phase of the IGBT is automatically sensed. I_G is integrated and digitized using an ADC during the plateau region. A regression analysis is performed on the actual I_C and the ADC outputs. It shows the maximum deviation is less than 0.8 A for both turn-on and turn-off over the current range of 1~25 A for turn-on and 1~30 A for turn-off.

The automatic current sensing system is then integrated into a gate driver IC. This smart gate driver IC also has a highly configurable output driver and an on-chip SPRUCE unit for all the digital processing. The current testing range is further extended to 50 A, and a polynomial curve fitting is used to predict I_C based on the digitized I_G value. At room temperature, a 2^{nd} order polynomial curve fitting can ensure an accuracy of ±1 A across the testing range between 1 to 30 A for turn-on and 1 to 50 A for turn-off. After the temperature effect is analyzed and factored in, a 3^{rd} order polynomial curve fitting is implemented, an estimated accuracy of ±0.5 A could be achieved within the current range of 1 to 30 A for turn-on and 1 to 50 A for turn-off from 25 to 75 ^{o}C.

The on-chip CPU code named SPRUCE is area and power efficient. It provides the required functionality such that any general closed loop control of an SMPS could be achieved. However, since it is single stack based, it is not suitable for applications involve extensive arithmetic operations due to speed limitation. Nevertheless, it is still capable of handling complicated controls and operations for low switching frequency application. Therefore, we envisage that many other types of driver ICs could be developed with novel use of the integrated CPU or with different types of integrated sensors in the near future. It is also possible to integrate several different sensors into the

same chip. Together with the on-chip CPU and configurable driver, it will soon be a common place to see fully-integrated smart gate drivers with closed loop local controls.

The proposed current measurement technique is applicable across different types of IGBTs and even power MOSFETs as long as there are Miller plateaus during turn-on and turn-off transients. But it should be noted that different devices may have different relationships between the Miller plateau voltages and the load currents, and also different thermal sensitivity. Curve fitting needs to be customized for each type of devices. In addition, re-calibration for each single device is needed if it exhibits large device to device variations for the IV transfer characteristics: the I_C vs V_{GE} relationship, which is the fundamental of the proposed current sensing technique. This transfer characteristic is normally described by the threshold voltage V_{th} and the transconductance G_m. Currently for majority of the commercial discrete IGBTs and IGBT modules, only the V_{th} of the IGBT device is specified with its minimum and max values. The variations can range from 5% to 30%. While G_m is usually specified as a single value at a typical current and temperature condition, and most of the time the G_m and even the transfer curves are not available from the device datasheets. Referring to Equation (2.9) and (2.10), the I_G versus I_C relationship is more dependent on G_m, and V_{th} only introduces an offset. Therefore, if G_m could be well controlled then the calibration procedure only involves measuring V_{th} and compensating the curve fitting with the calculated offsets. However, if G_m also exhibits large variations across different devices then re-calibration is needed for each IGBT device or IGBT module in order to achieve higher current sensing accuracy. Considering that the transfer curve characteristics may vary to different extends across different temperature conditions, the calibration procedure would be complicated and tedious. The transfer curves in full current range may need to be tested in step of 10 to 20^{o}C in order to obtain the set of data (as presented in Figure 4.21 and Figure 4.22) to do the customised curve fitting.

However, consider the emerging trend of Internet of Things (IoT) and artificial intelligence (AI) in the whole high technology industry, it would bring major changes in the power electronic industry and possibly create a new generation of power electronics. In this new IoT and AI era, massive sensors will be embedded in the power system and

the measured data will be transmitted to the device manufacturer though internet. The manufacturers and users are directly connected on-line. The manufacturers can monitor the real operating conditions of the device and provide customer-tailored services for each user [96]. For example, users can enjoy customer-tailored calibrations through optimized tuning of all the parameters in the programmable hardware. In order to realize this IoT and AI-assisted power electronics, the integrated sensors, the programmable hardware and intelligent controller would be of great importance. In this case, the proposed current sensor and fully integrated smart power IC with intelligent on-chip CPU control may found wide applications in the future.

5.2. Future Work

5.2.1. Accuracy Improvement

Future work could focus on how to further improve the accuracy of the proposed current sensing method. First thing is to employ on-chip LDOs for the reference voltages and eliminate unnecessary functionality test pins. In addition, the clocks used for the I_C sensing system and the ΔΣ ADC could be provided by the CPU DPWM block instead of supplied through external pins. Then a much smaller package could be chosen with much shorter bonding wires. This could greatly suppress the EMI effect when the switching current level is high.

Other than the packaging, the thermal modeling for this technique could be further refined. The temperature effect testing and compensation in this work is referenced to the ambient temperature. However, it is known that in the real applications, the junction temperature of the IGBT can be much higher than the ambient temperature. The embedded temperature sensor on the IGBT device (usually the PN diode) can be used to obtain the real junction temperature of the IGBT. The results can be digitized and fed back to the on-chip CPU to compensate the temperature effect for the proposed current sensing technique.

Another focus could be further improving the circuit performance especially the I_C sensing circuitry, as it implements basic textbook style analog circuits to realize all the functions. For example, the MOD2 Delta Sigma ADC could be replaced by an incremental converter, which is more suitable for applications with DC input voltages and higher accuracy could be achieved.

With the further improved measurement accuracy. The current measurement range could be certainly further extended. A more accurate ADC may be needed when the range goes further. In this case for a 2nd order DSM, a better digital filter could possibly provide 14-15 ENOB. Nevertheless, more attention should be paid to the EMI effect exerting on the system when the current becomes exceedingly high.

5.2.2. Closed-loop Current Regulation

The general purpose of the current measurement for power devices is for regulation or protection. Since the proposed technique could only have a current reading during the turn-on and turn-off phase of the IGBT. Therefore, this technique is not suitable for over current or short circuit protection. The typical short circuit withstand time of an IGBT is around 10 μs and the plateau region may not even exist when the device is under load fault condition.

However, this technique is well-suited for current regulation since the digitized current reading is readily available from the on-chip CPU. The CPU can also control the gate driver's duty cycle and dead time. Therefore, the on-chip current regulation could be easily realized through different kinds of algorithms that can be implemented on chip.

Nevertheless, as discussed in Section 4.4, the current digital filter implemented by the CPU is slow. The processing time is too long for current regulation purpose. The filter should be re-designed and synthesized to make sure the current readout could be obtained within each cycle for any future applications of this technique.

5.2.3. Zero Current Crossing Detection

The proposed current sensing method could also be used for zero current crossing detection for zero current switching. Since the embedded SPRUCE unit controls the PWM signal of the gate driver, it keeps track of the turn-on and turn-off times of the power device. In addition, it can record all the digitized current of the power device during the turn-on and turn-off transients. Simple and efficient algorithms can be implemented by the CPU to predict the zero current crossing point.

5.2.4. Incorporate Active Gate Driving

Since the proposed current sensing method is dependent on the Miller effect which has a minimum requirement for the Miller plateau length. Therefore, the gate resistance should not be lower than certain value. This would potentially increase the turn-on and turn-off switching time, hence increase the switching loss. One solution is to incorporate this method with active gate driving techniques such as the segmented gate driving [44]. The gate resistance can be changed to larger value around the plateau region, then the current sensing could be performed during the plateau region meanwhile the I_C over-shoot during turn-on could be suppresses and the switching loss can be reduced. And in this case, I_G vs I_C relationship always stands for the same R_G during the plateau region.

In fact, this proposed technique could be incorporated into the gate driver IC without conflicting with any existing adaptive gate driving circuits such as duty cycle control, dead time control and gate driver segmentation. It only senses the gate current during the plateau region, and it would not interfere with the gate signal with the added analog buffers.

Reference

[1] B. J. Baliga, "Introduction," in *The IGBT Device,* 1st ed. Raleigh, NC, USA: Elsevier Inc, 2015.

[2] N. Iwamuro and T. Laska, "IGBT History, State-of-the-Art, and Future Prospects," *IEEE Transactions on Electron Devices,* vol. 64, no. 3, pp. 741-752, 2017.

[3] "Chapter 1: Structure and Features," in *Fuji IGBT Application Manual*, ed: http://w5jgv.com/hv-ps1/pdf/fuji_igbt_application_manual(REH984).pdf.

[4] B. J. Baliga, "IGBT Structure and Operation," in *The IGBT Device,* 1st ed. Raleigh, NC, USA: Elsevier Inc, 2015, pp. 22-23.

[5] J. F. D. E. R. Motto, H. Takahashi, M. Tabata and H. Iwamoto, "Characteristics of a 1200 V PT IGBT with trench gate and local life time control," presented at the *Conference Record of 1998 IEEE Industry Applications Conference. Thirty-Third IAS Annual Meeting*, St. Louis, MO, USA.

[6] A. Alessandria and L. Fragapane, "A robust top structure design in a field-stop emitter-implant trench-gate IGBT for improved short circuit ruggedness," in *Proceedings of the 14th European Conference on Power Electronics and Applications*, 2011, pp. 1-8.

[7] A. Yu, L. Min-Zhi, L. Xiao-Yong, Z. Lin-Qing, W. Jun, and W. Peng-Fei, "A Dynamic Carrier-Storage trench-gate IGBT with low switching loss," in *13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, 2016, pp. 1071-1073.

[8] K. Ohi *et al.*, "Ultra low miller capacitance trench-gate IGBT with the split gate structure," in *IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2015, pp. 25-28.

[9] B. J. Baliga, "Package and Module Design," in *The IGBT Device,* 1st ed. Raleigh, NC, USA: Elsevier Inc, 2015.

[10] M. Otsuki, M. Watanabe, and A. Nishiura, "Trends and opportunities in intelligent power modules (IPM)," in *IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2015, pp. 317-320.

[11] B. J. Baliga, "Basic Power Module," in *The IGBT Device,* 1st ed. Raleigh, NC, USA: Elsevier Inc, 2015.

[12] A. Lindemann and G. Strauch, "Properties of Direct Aluminum Bonded Substrates for Power Semiconductor Components," *IEEE Transactions on Power Electronics,* vol. 22, no. 2, pp. 384-391, 2007.

[13] X. Bie, F. Qin, T. An, J. Zhao, and C. Fang, "Numerical simulation of the wire bonding reliability of IGBT module under power cycling," in *18th International Conference on Electronic Packaging Technology (ICEPT)*, 2017, pp. 1396-1401.

[14] C. F. Bayer, U. Waltrich, A. Soueidan, R. Schneider, E. Baer, and A. Schletz, "Enhancement of the partial discharge inception voltage of DBCs by adjusting the permittivity of the encapsulation," in *CIPS 9th International Conference on Integrated Power Electronics Systems*, 2016, pp. 1-5.

[15] G. Majumdar, T. Oi, T. Terashima, S. Idaka, D. Nakajima, and Y. Goto, "Review of Integration Trends in Power Electronics Systems and Devices," in *CIPS 9th International Conference on Integrated Power Electronics Systems*, 2016, pp. 1-10.

[16] B. J. Baliga, "Packages and Module Design," in *The IGBT Device,* 1st ed. Raleigh, NC, USA: Elsevier Inc, 2015, pp. 187-188.

[17] H. Iwamoto, E. Motto, J. Achhammer, M. Iwasaki, M. Seo, and T. Iwagami, "New intelligent power modules for appliance motor control," in *APEC 16th Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181)*, 2001, vol. 2, pp. 1051-1056.

[18] Hussein, Majurndar, Yoshida, and Maekawa, "IPMs solving major reliability issues in automotive applications [intelligent power module]," in *Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs*, 2004, pp. 89-92.

[19] B. J. Baliga, "IGBT Applications: Transportation," in *The IGBT Device*1st ed. Raleigh, NC, USA: Elsevier Inc, 2015.

[20] B. J. Baliga, "IGBT Applications: Industrial," in *The IGBT Device,* 1st ed. Raleigh, NC, USA: Elsevier Inc, 2015.

[21] B. J. Baliga, "IGBT Applications: Lighting," in *The IGBT Device,* 1st ed. Raleigh, NC, USA: Elsevier Inc, 2015.

[22] B. J. Baliga, "IGBT Applications: Consumer," in *The IGBT Device,* 1st ed. Raleigh, NC, USA: Elsevier Inc, 2015.

[23] B. J. Baliga, "IGBT Applications: Medical," in *The IGBT Device,* 1st ed. Raleigh, NC, USA: Elsevier Inc, 2015.

[24] B. J. Baliga, "Gate Drive Circuit Design," in *The IGBT Device,* 1st ed. Raleigh, NC, USA: lsevier Inc, 2015, pp. 193-202.

[25] J. T. Strydom, M. A. d. Rooij, and J. D. v. Wyk, "A comparison of fundamental gate-driver topologies for high frequency applications," in *Applied Power Electronics Conference and Exposition 19th Annual IEEE*, 2004, vol. 2, pp. 1045-1052.

[26] D. Maksimovic, "A MOS gate drive with resonant transitions," in *Power Electronics Specialists Conference, 22nd Annual IEEE*, 1991, pp. 527-532.

[27] J. V. P. S. Chennu and R. Maheshwari, "Study on Resonant Gate Driver circuits for high frequency applications," in *IEEE 6th International Conference on Power Systems (ICPS)*, 2016, pp. 1-6.

[28] P. Shihong and T. M. Jahns, "Flexible *dv/dt* and *di/dt* control method for insulated gate power switches," *IEEE Transactions on Industry Applications,* vol. 39, no. 3, pp. 657-664, 2003.

[29] Z. Wang, X. Shi, L. M. Tolbert, F, and B. J. Blalock, "A *di/dt* Feedback-Based Active Gate Driver for Smart Switching and Fast Overcurrent Protection of IGBT Modules," *IEEE Transactions on Power Electronics,* vol. 29, no. 7, pp. 3720-3732, 2014.

[30] L. Shu, J. Zhang, F. Peng, and Z. Chen, "Active Current Source IGBT Gate Drive With Closed-Loop *di/dt* and *dv/dt* Control," *IEEE Transactions on Power Electronics,* vol. 32, no. 5, pp. 3787-3796, 2017.

[31] L. Michel, X. Boucher, A. Cheriti, P. Sicard, and F. Sirois, "FPGA Implementation of an Optimal IGBT Gate Driver Based on Posicast Control," *IEEE Transactions on Power Electronics,* vol. 28, no. 5, pp. 2569-2575, 2013.

[32] M. Blank, T. Glück, A. Kugi, and H. P. Kreuter, "Slew rate control strategies for smart power ICs based on iterative learning control," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2014, pp. 2860-2866.

[33] L. Dang, H. Kuhn, and A. Mertens, "Digital Adaptive Driving Strategies for High-Voltage IGBTs," *IEEE Transactions on Industry Applications,* vol. 49, no. 4, pp. 1628-1636, 2013.

[34] N. Idir, R. Bausiere, and J. J. Franchaud, "Active gate voltage control of turn-on *di/dt* and turn-off *dv/dt* in insulated gate transistors," *IEEE Transactions on Power Electronics,* vol. 21, no. 4, pp. 849-855, 2006.

[35] J. Groeger, B. Wicht, and K. Norling, "Dynamic stability of a closed-loop gate driver enabling digitally controlled slope shaping," in *13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, 2017, pp. 61-64.

[36] B. J. Baliga, "Chip Design, Protection, and Fabrication," in *The IGBT Device,* 1st ed. Raleigh, NC, USA: Elsevier Inc, 2015, pp. 155-162.

[37] S. Hain and M. M. Bakran, "New Ultra Fast Short Circuit Detection Method Without Using the Desaturation Process of the Power Semiconductor," in *PCIM Europe; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2016, pp. 1-8.

[38] H. Niu and R. D. Lorenz, "Sensing IGBT junction temperature using gate drive output transient properties," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 2492-2499.

[39] J. Chen, A. Shorten, M. Sasaki, T. Kawashima, H. Nishio, and W. T. Ng, "An Automatic IGBT Collector Current Sensing Technique via the Gate Node," in *PCIM Europe; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2016, pp. 1-8.

[40] D. Bortis, J. Biela, and J. W. Kolar, "Active Gate Control for Current Balancing of Parallel-Connected IGBT Modules in Solid-State Modulators," *IEEE Transactions on Plasma Science,* vol. 36, no. 5, pp. 2632-2637, 2008.

[41] C. Lihua, F. Z. Peng, and C. Dong, "A smart gate drive with self-diagnosis for power MOSFETs and IGBTs," in *23rdAnnual IEEE Applied Power Electronics Conference and Exposition*, 2008, pp. 1602-1607.

[42] J. S. Yu, W. J. Zhang, and W. T. Ng, "A segmented output stage H-bridge IC with tunable gate driver," in *IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2014, pp. 205-208.

[43] A. Shorten, W. T. Ng, M. Sasaki, T. Kawashima, and H. Nishio, "A segmented gate driver IC for the reduction of IGBT collector current over-shoot at turn-on," in *25th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2013, pp. 73-76.

[44] A. A. Fomani, W. T. Ng, and A. Shorten, "An integrated segmented gate driver with adjustable driving capability," in *IEEE Energy Conversion Congress and Exposition*, 2010, pp. 2430-2433.

[45] K. Miyazaki, M. Takamiya, and T. Sakurai, "Automatic optimization of IGBT gate driving waveform using simulated annealing for programmable gate driver IC," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1-6.

[46] A. Perez, X. Jorda, P. Godignon, M. Vellvehi, J. L. Galvez, and J. Millan, "An IGBT gate driver integrated circuit with full-bridge output stage and short circuit protections," in *International Semiconductor Conference. CAS 2003 Proceedings (IEEE Cat. No.03TH8676)*, vol. 2, pp. 1-248.

[47] G. Pasetti, S. Saponara, F. Tinfena, R. Serventi, P. D. Abramo, and L. Fanucci, "An integrated smart driver for inductive loads with self-monitoring/diagnostic capability," in *International Symposium on Power Electronics Power Electronics, Electrical Drives, Automation and Motion*, 2012, pp. 1007-1011.

[48] J. B. Lee and D. S. Hyun, "Gate Voltage Pattern Analyze for Short-Circuit Protection in IGBT Inverters," in *IEEE Power Electronics Specialists Conference*, 2007, pp. 1913-1917.

[49] T. Horiguchi *et al.*, "A short circuit protection method based on a gate charge characteristic," in *International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, pp. 2290-2296.

[50] K. Y. K. Hasegawa, H. Yoshida, K. Hamada, M. Tsukuda, I. Omura, "Short-circuit protection for an IGBT with detecting the gate voltage and gate charge," *Microelectronics Reliability,* vol. 54, no. 9-10, pp. 1897-1900, 2014.

[51] P. Sun *et al.*, "Online junction temperature extraction with turn-off delay time for high power IGBTs," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 4016-4021.

[52] X. Zeng *et al.*, "Gate sensed method of load current imbalance measuring for paralleling IGBT devices," in *28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2016, pp. 407-410.

[53] M. Rose and H. J. Bergveld, "Integration Trends in Monolithic Power ICs: Application and Technology Challenges," *IEEE Journal of Solid-State Circuits,* vol. 51, no. 9, pp. 1965-1974, 2016.

[54] P. Wessels, "Smart power technologies on SOI," in *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, 2015, pp. 1-2.

[55] B. Vogler, R. Herzer, M. Dienstbier, and S. Buetow, "Fully integrated high voltage high current gate driver for MOSFET-inverters," in *29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, 2017, pp. 271-274.

[56] S. Ziegler, R. C. Woodward, H. H. C. Iu, and L. J. Borle, "Current Sensing Techniques: A Review," *IEEE Sensors Journal,* vol. 9, no. 4, pp. 354-376, 2009.

[57] X. Chucheng, Z. Lingyin, T. Asada, W. G. Odendaal, and J. D. v. Wyk, "An overview of integratable current sensor technologies," in *38th IAS Annual Meeting on Conference Record of the Industry Applications Conference*, 2003, vol. 2, pp. 1251-1258.

[58] A. M. Patel and M. Ferdowsi, "Advanced Current Sensing Techniques for Power Electronic Converters," in *IEEE Vehicle Power and Propulsion Conference*, 2007, pp. 524-530.

[59] Z. Zhang, D. Leggate, and T. Matsuo, "Industrial Inverter Current Sensing With Three Shunt Resistors: Limitations and Solutions," *IEEE Transactions on Power Electronics,* vol. 32, no. 6, pp. 4577-4586, 2017.

[60] K. H. S.Tabata, M.Tsukuda, I.Omura, "New Power Module Integrating Output Current Measurement Function" presented at the ISPSD, Sapporo, 2017.

[61] L. Xu, Q. Chen, X. Ren, S. C. Wong, and C. K. Tse, "Self-Oscillating Resonant Converter With Contactless Power Transfer and Integrated Current Sensing Transformer," *IEEE Transactions on Power Electronics,* vol. 32, no. 6, pp. 4839-4851, 2017.

[62] B. J. Baliga, "Chip Design, Protection, and Fabrication," in *The IGBT Device,* 1st ed. Raleigh, NC, USA: Elsevier Inc, 2015, pp. 154-155.

[63] F. Castelli, "The flat strap sandwich shunt," *IEEE Transactions on Instrumentation and Measurement,* vol. 48, no. 5, pp. 894-898, 1999.

[64] M. Sanoh, A. Mikata, K. Tokuno, M. Hanazawa, and H. Kakitani, "A calibration method for a commercial coaxial shunt at high pulse current," in *29th Conference on Precision Electromagnetic Measurements (CPEM)*, 2014, pp. 630-631.

[65] J. A. Ferreira, W. A. Cronje, and W. A. Relihan, "Integration of high frequency current shunts in power electronic circuits," in *Power Electronics Specialists Conference, 23rd Annual IEEE*, 1992, pp. 1284-1290 vol.2.

[66] S. Chakrabarti, T. M. Jahns, and R. D. Lorenz, "A current reconstruction algorithm for three-phase inverters using integrated current sensors in the low-side switches," in *38th IAS Annual Meeting on Conference Record of the Industry Applications Conference,* 2003, vol. 2, pp. 925-932.

[67] M. Kudoh, Y. Hoshi, S. Momota, T. Fujihira, and K. Sakurai, "Current sensing IGBT for future intelligent power module," in *Power Semiconductor Devices and ICs Proceedings*, 1996, pp. 303-306.

[68] S. Yuvarajan and L. Wang, "Performance analysis and signal processing in a current sensing power MOSFET (SENSEFET)," in *Conference Record of the IEEE Industry Applications Society Annual Meeting*, 1991, pp. 1445-1450 vol.2.

[69] T. P. Chow, Z. Shen, D. N. Pattanayak, E. J. Wildi, M. S. Adler, and B. J. Baliga, "Modelling and analysis of current sensors for N-channel, vertical IGBTs," in *Electron Devices Meeting. Technical Digest., International*, 1992, pp. 253-256.

[70] S. P. Robb, A. A. Taomoto, and S. L. Tu, "Current sensing in IGBTs for short-circuit protection," in *Proceedings of the 6th International Symposium on Power Semiconductor Devices and Ics*, 1994, pp. 81-85.

[71] M. Kudoh *et al.*, "Current sensing IGBT structure with improved accuracy," in *Power Semiconductor Devices and ICs,* 1995, pp. 119-122.

[72] H. Yamagiwa, T. Saji, S. Kaneko, S. Takahashi, T. Uno, and K. Sawada, "Sense Device Structure in Hybrid IGBT with Constant Current Sense Ratio for Entire Collector Current Range," in *ISPSD 2008*, pp. 217-220.

[73] "IGBT Sense Emitter Current Measurement Using the Keysight B1505A ", August 4, 2014.

[74] R. S. Chokhawala, J. Catt, and B. R. Pelly, "Gate drive considerations for IGBT modules," *IEEE Transactions on Industry Applications,* vol. 31, no. 3, pp. 603-611, 1995.

[75] H. Lavric and R. Fiser, "Lossless current sensing technique on MOSFET $R_{DS(on)}$ with improved accuracy," *Electronics Letters,* vol. 46, no. 5, pp. 370-371, 2010.

[76] T. Ribarich, "Enhancing switching-mode power performance with $R_{DS(on)}$ current sensing," ed: Power System Design: Empowering Global Innovation, 2014.

[77] R. Herzer, "Integrated gate driver circuit solutions," in *6th International Conference on Integrated Power Electronics Systems*, 2010, pp. 1-10.

[78] A. Shorten and W. T. Ng, "SPRUCE, an Embedded Compact Stack Machine for IGBT Power Modules," in *IEEE 46th International Symposium on Multiple-Valued Logic (ISMVL)*, 2016, pp. 172-176.

[79] R. Chokhawala, J. Catt, and B. Pelly, "Gate drive considerations for IGBT modules," in *Industry Applications Society Annual Meeting*, 1992, pp. 1186-1195 vol.1.

[80] J. Karlsson, "The concept of IGBT modeling and the evaluation of the PSPICE IGBT model," Master Thesis, Conducted at ALSTOM Power, Växjö, 2002.

[81] B. J. Baliga, "IGBT Structural Design," in *The IGBT Device,* 1st ed. Raleigh, NC, USA: Elsevier Inc, 2015.

[82] K. Gauen, "The effects of MOSFET output capacitance in high frequency applications," in *Industry Applications Society Annual Meeting,* 1989, pp. 1227-1234, vol.2.

[83] B. J. Baliga, "Insulated Gate Bipolar Transistors," in *Fundamentals of Power Semiconductor Devices,* Raleigh, NC, USA: Springer Science, 2008, pp. 816-819.

[84] V. K. Khanna, "Physics and Modeling of IGBT," in *The Insulated Gate Bipolar Transistor IGBT Theory and Design*New Jersey: John Wiley & Sons Inc, 2003, p. 244.

[85] B. J. Baliga, "Power MOSFETs" in *Fundamentals of Power Semiconductor Devices,* Raleigh, NC, USA: Springer Science, 2008, pp. 417-419.

[86] J. Yu, "A Segmented Output Stage H-Bridge IC with Tunable Gate Driver " Master of Applied Science, Graduate Department of Electrical and Computer Engineering, University of Toronto, 2014.

[87] D. A. J. Tony Chan Carusone, Kenneth W. Martin, "Switched Capacitor Circuits," in *Analog Integrated Circuit Design,* 2nd ed, John Wiley & Sons, Inc, 2011.

[88] T. Y. Goh, "SINGLE-INDUCTOR 4-OUTPUT DC/DC BUCK CONVERTER WITH COMPARATOR-BASED FIXED-FREQUENCY SINGLE-DISCHARGE CONTROL," Master of Applied Science, Graduate Department of Electrical and Computer Engineering, University of Toronto, 2016.

[89] K. Bult and A. Buchwald, "An embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm^2," *IEEE Journal of Solid-State Circuits,* vol. 32, no. 12, pp. 1887-1895, 1997.

[90] D. A. J. Tony Chan Carusone, Kenneth W. Martin, "Sample-and-Hold and Translinear Circuits," in *Analog Integrated Circuit Design,* 2nd ed, John Wiley & Sons, Inc, 2011.

[91] R. S. a. G. C. Temes, "Higher-Order Delta-Sigma Modulation " in *Understanding Delta-Sigma Data Converters,* 1st ed. Hoboken, New Jersey: A JOHN WILEY & SONS, INC, 2005, p. 125.

[92] R. S. a. B. C.Temes, "Appendix B, The Delta-Sigma Toolbox," in *Understanding Delta-Sigma Data Converters,* 1st ed. Hoboken, NewJersey: A JOHN WILEY & SONS, INC, 2005, pp. 399-426.

[93] A. Yukawa, "A CMOS 8-Bit High-Speed A/D Converter IC," *IEEE Journal of Solid-State Circuits,* vol. 20, no. 3, pp. 775-779, 1985.

[94] B. Nikolic, V. G. Oklobdzija, V. Stojanovic, J. Wenyan, C. James Kar-Shing, and M. M.-T. Leung, "Improved sense-amplifier-based flip-flop: design and measurements," *IEEE Journal of Solid-State Circuits,* vol. 35, no. 6, pp. 876-884, 2000.

[95] B. J. Baliga, "IGBT Models," in *The IGBT Device,* 1st ed. Raleigh, NC, USA: Elsevier Inc, 2015, pp. 205-211.

[96] M. Takamiya, K. Miyazaki, H. Obara, T. Sai, K. Wada, and T. Sakurai, "Power electronics 2.0: IoT-connected and Al-controlled power electronics operating optimally for each user," in *29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, 2017, pp. 29-32.

Appendix A

Memory Map of the SPRUCE CPU

The memory of the CPU is composed of 1067 20-bit shift registers. The main memory address is from 0 to 1024. The rest are all memory mapped modules. They are the DPWMs, the gate driver and current sensing circuitry configuration bits, 20 GPI registers and 20 GPO registers for I/O interfaces, and a 100 bits shift register to temporarily store the DSM outputs for digital processing.

	Function																				
Address	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Block
0->1024	R/W																				General Memory
1025	Unused																			START	SAR ADC
1026	Unused																			READY	SAR ADC
1027	Unused										Data Out										SAR ADC
1028	Unused												MODE2	MODE1	P2_EN	N2_EN	P1_EN	N1_EN	LINK	EN	DPWM 1
1029	Unused																P2	N2	P1	N1	DPWM 1
1030	Unused										Duty 1										DPWM 1
1031	Unused										Duty 2										DPWM 1
1032	Unused										Dead Time Rising 1										DPWM 1
1033	Unused										Dead Time Falling 1										DPWM 1
1034	Unused										Dead Time Rising 2										DPWM 1
1035	Unused										Dead Time Falling 2										DPWM 1
1036	Unused										Speed 1										DPWM 1
1037	Unused												MODE2	MODE1	P4_EN	N4_EN	P3_EN	N3_EN	LINK	EN	DPWM 2
1038	Unused																P4	N4	P3	N3	DPWM 2
1039	Unused										Duty 3										DPWM 2
1040	Unused										Duty 4										DPWM 2
1041	Unused										Dead Time Rising 3										DPWM 2
1042	Unused										Dead Time Falling 3										DPWM 2
1043	Unused										Dead Time Rising 4										DPWM 2
1044	Unused										Dead Time Falling 4										DPWM 2
1045	Unused										Speed 2										DPWM 2
Address	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Block
1046	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	ON[1]	OFF[1]	EN[1]	D0[8]	D0[7]	D0[6]	D0[5]	D0[4]	D0[3]	D0[2]	D0[1]	D0[0]	ON[0]	OFF[0]	EN[0]	LS Output Stage
1047	Unused	ON[3]	OFF[3]	EN[3]	D2[8]	D2[7]	D2[6]	D2[5]	D2[4]	D2[3]	D2[2]	D2[1]	D2[0]	ON[2]	OFF[2]	EN[2]	D1[8]	D1[7]	D1[6]	D1[5]	
1048	Unused									ON[4]	OFF[4]	EN[4]	Unused							OSC_EN	
1049	Unused					ON[6]	OFF[6]	EN[6]	Unused									ON[5]	OFF[5]	EN[5]	
1050	Unused		HS_OSC	G_CTRL	Unused									ON[7]	OFF[7]	EN[7]	Unused				
1051	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	ON[1]	OFF[1]	EN[1]	D0[8]	D0[7]	D0[6]	D0[5]	D0[4]	D0[3]	D0[2]	D0[1]	D0[0]	ON[0]	OFF[0]	EN[0]	HS Output Stage
1052	Unused	ON[3]	OFF[3]	EN[3]	D2[8]	D2[7]	D2[6]	D2[5]	D2[4]	D2[3]	D2[2]	D2[1]	D2[0]	ON[2]	OFF[2]	EN[2]	D1[8]	D1[7]	D1[6]	D1[5]	
1053	Unused									ON[4]	OFF[4]	EN[4]	Unused							OSC_EN	
1054	Unused					ON[6]	OFF[6]	EN[6]	Unused									ON[5]	OFF[5]	EN[5]	
1055	Unused													ON[7]	OFF[7]	EN[7]	Unused				
1056	Unused		Delay[8:0]									Unused	DAC[5:0]						Unused		J-Config
1057	Unused																				J-Config
1058	Rsense[8:0]									din_sel	Unused										J-Config
1059	S[2:0]			OFF_EN	ON_EN	EN_PA[1:0]		CB[3:0]				Unused									X-Config
1060	Unused		ADC_S1	ADC_S0	EN_BUF	RC[3:0]				MUX[3:0]			SW_EN[3:0]				S[5:3]				X-Config
1061	Unused									GPO[9:0]											GPO
1062	Unused									GPI[9:0]											GPI
1063	Store the 100 bits DSM output																				DS ADC
1064																					DS ADC
1065																					DS ADC
1066																					DS ADC
1067																					DS ADC
Address	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Block

Figure A: Complete memory map for the SPRUCE CPU in the gate driver IC.

Appendix B

Publication List

[1] J. Chen, A. Shorten, and W. T. Ng, "IGBT Collector Current Sensing Using Gate Current," *12th International Seminar on Power Semiconductors* (*ISPS*), Prague, Czech Republic, 2014

[2] J. Chen, A. Shorten, M. Sasaki, T. Kawashima, H. Nishio, and W. T. Ng, "An Automatic IGBT Collector Current Sensing Technique via the Gate Node," *PCIM Europe*, Nuremberg, Germany, 2016

[3] J. Chen, W. Zhang, A. Shorten, J.Yu. M. Sasaki, T. Kawashima, H. Nishio, and W. T. Ng, "An IGBT Gate Driver IC with Collector Current Sensing," *Proc. International Symp. Power Devices and ICs (ISPSD)*, Sapporo, Japan, 2017

[4] J. Chen, and W. T. Ng, " Design Trends in Smart Gate Driver ICs for Power MOSFETs and IGBTs," *IEEE 12th International Conference on ASIC (ASICON)*, Gui Yang, China, 2017