

# A snapback-free and fast-switching planar-gate SOI LIGBT with three electron extracting channels

Yuying Wang<sup>1</sup>, Aohang Zhang<sup>1</sup>, Peng Jian<sup>1</sup>, and Wensuo Chen<sup>1, a)</sup>

**Abstract** In this paper, a snapback-free and fast-switching SOI LIGBT with three electron extracting channels (TEC) is proposed and investigated. Compared with SBM LIGBT, the trench gate of n-MOS is changed to a planar gate, and a P- region is added to prevent N+ short circuit while providing electron extracting channel. Simulation results show that TEC decreases  $E_{OFF}$  by 15% at  $V_{ON} = 1.8$  V relative to SBM when all three channels are open, while TEC still decreases  $E_{OFF}$  by 10% at  $V_{ON} = 1.55$  V relative to SBM when only two channels are available. The device achieves the same breakdown voltage level of 603 V as SBM without additional trench etch process required.

**Keywords:** fast-switching, snapback-free, silicon-on-insulator lateral insulated gate bipolar transistor (SOI LIGBT), three electron extracting channels, planar gate

**Classification:** Power devices and circuits

## 1. Introduction

The silicon-on-insulator lateral insulated gate bipolar transistor (SOI LIGBT) has the advantages of large input resistance and low drive energy loss, and is widely used in intelligent power integrated circuits [1, 2, 3, 4, 5, 6, 7, 8]. Compared with unipolar devices, both the electrons and holes of LIGBT are involved in conduction in the on-state, which leads to a relatively lower forward conduction voltage drop ( $V_{ON}$ ), but also leads to a long tail of turn-off current resulting in a high turn-off loss ( $E_{OFF}$ ) when the excess carriers can only disappear through recombination [9, 10, 11, 12, 13]. The turn-off loss can be reduced by reducing the hole injection efficiency of P+ anode, but this will also reduce the conductivity modulation effect and increase  $V_{ON}$ , so it is difficult to take both into account [14, 15, 16, 17]. A better tradeoff can be achieved by changing the internal structure of the device, such as adding additional NPN electron extraction channels during turnoff [18, 19, 20]. In addition, researchers proposed the short-anode LIGBT (SA-LIGBT) [21, 22, 23, 24] to provide an electron extraction path to reduce  $E_{OFF}$ . However, an undesirable snapback is caused during the forward conduction characteristic. The separated shorted-anode LIGBT (SSA-LIGBT) [25] uses a large equivalent resistance formed by the drift region between the anode N+ and P+ anode to suppress the snapback, but eliminating

the snapback requires a long drift region, resulting in a large waste of chip area. Adding an auxiliary gate [26, 27] to the anode can dynamically control the holes injection of anode and achieve fast turn-off without snapback, but the extra control signal greatly increases the complexity of the whole circuit system. Adding an insulating oxide pillar to the anode to increase the flow path of electrons can also achieve snapback-free, but this also increases the process complexity of the device [28, 29]. To this end, A snapback-free fast-switching IGBT with an embedded self-biased n-MOS (SBM) [30] is proposed, which can easily achieve snapback-free without extra control circuit and provides the built-in electron extraction path to reduce the  $E_{OFF}$ . However, additional trench etch process is required, which is incompatible with CMOS process and is not easily integrated.

In this paper, a fast-switching planar-gate SOI-LIGBT with three electron extraction channels (TEC) is proposed. Channel I is planar gate self-biased n-MOS, channel II is N+/p-well/N-buffer electron extraction channel, and channel III is a longitudinal N+/P-/N-buffer electron extraction channel. The P region of the two NPN electron extraction channels is directly connected. The key parameters and performance of the structure were evaluated and tested in detail by simulation, and compared with CON and SBM LIGBT. The simulation results show that the proposed structure without trench etch process can realize snapback-free in forward conduction, has a superior  $E_{OFF}$ - $V_{ON}$  tradeoff relationship, and achieve the same breakdown voltage under the same device parameters.

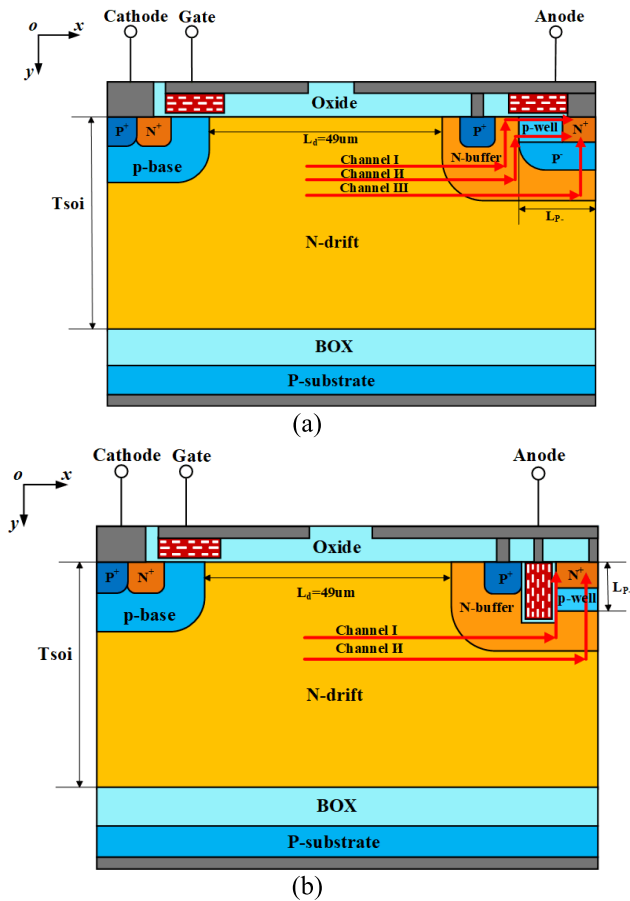
## 2. Device structure and mechanism

Fig. 1 shows the 2-D cross-section views of the proposed TEC LIGBT, the conventional LIGBT (Con.) and the SBM LIGBT. Based on SBM LIGBT, the trench gate self-biased of n-MOS is changed to a planar gate, and a P<sup>-</sup> region is added to prevent N<sup>+</sup> short circuit while providing the third electron extraction channel. The N<sup>+</sup> anode, the p-well, the N-buffer, and the planar gate act as the drain, the p-body, the source, and the gate of the n-MOS, respectively. The key parameters used in the simulation of three structures are listed in Table I, where  $D_{p-}$  and  $D_{p-well}$  are the doping concentration of P<sup>-</sup> region and p-well respectively,  $L_{p-}$  is the junction depth along the channel direction of P<sup>-</sup> region.

At the initial conduction stage, the anode voltage is too low to turn the P<sup>+</sup>/N-buffer and n-MOS on, LIGBT operated in unipolar mode. At this time p-well and P<sup>-</sup> provided

<sup>1</sup> State Key Lab of Power Transmission Equipment & System Security and New Technology, School of Electrical Engineering, Chongqing University, Chongqing 400044, China

<sup>a)</sup> wensuochen@cqu.edu.cn



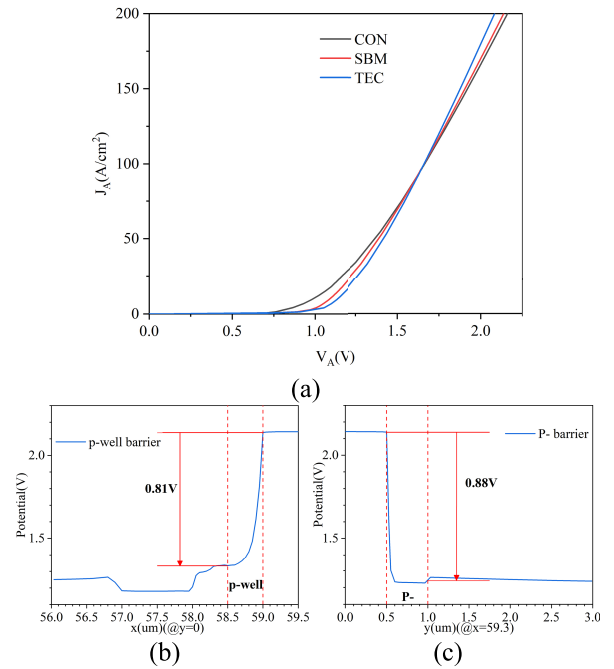
**Figure 1** Schematic cross-sectional views of (a) proposed TEC LIGBT, (b) SBM LIGBT.

**Table I** Key parameters for IGBTs.

Parameters	TEC	SBM	CON
N-drift length, $L_d$ ( $\mu\text{m}$ )	49	49	49
SOI layer thickness, $T_{\text{soi}}$ ( $\mu\text{m}$ )	25	25	25
Buried oxide thickness, $T_{\text{box}}$ ( $\mu\text{m}$ )	3	3	3
N-drift doping, $D_{N\text{-drift}}$ ( $\text{cm}^{-3}$ )	$2.8 \times 10^{14}$	$2.8 \times 10^{14}$	$2.8 \times 10^{14}$
N-buffer doping, $D_{N\text{-buffer}}$ ( $\text{cm}^{-3}$ )	$5 \times 10^{16}$	$5 \times 10^{16}$	$5 \times 10^{16}$
Cathode Gate oxide thickness, $t_{\text{ox,c}}$ (nm)	50	50	50
Junction depth along channel direction of P-, $L_p$ ( $\mu\text{m}$ )	1	1	1

suitable electronic barrier to avoid the phenomenon of snapback. When the anode voltage increases gradually, due to the opening of the P<sup>+</sup>/N-buffer junction, the conductivity modulation effect appears in the drift region, and the device works in bipolar mode. It can be seen from Fig. 2(a) and (b) that p-well and P<sup>-</sup> provide electronic barriers of 0.81 V and 0.88 V respectively, so snapback can be eliminated by setting suitable electronic barriers provided by p-well and P<sup>-</sup>.

When the device changes from the on-state to the off-state, the anode voltage rises to the bus voltage, and electrons flow into the anode through channel I, II and III respectively. Because there is no barrier from the trench gate, electrons can be extracted more easily through n-MOS, and channel I and II are also easier to extract electron. In addition, the low  $D_{P-}$  makes it easy to extract electrons for channel III. The three electron flow paths accelerate the recombination



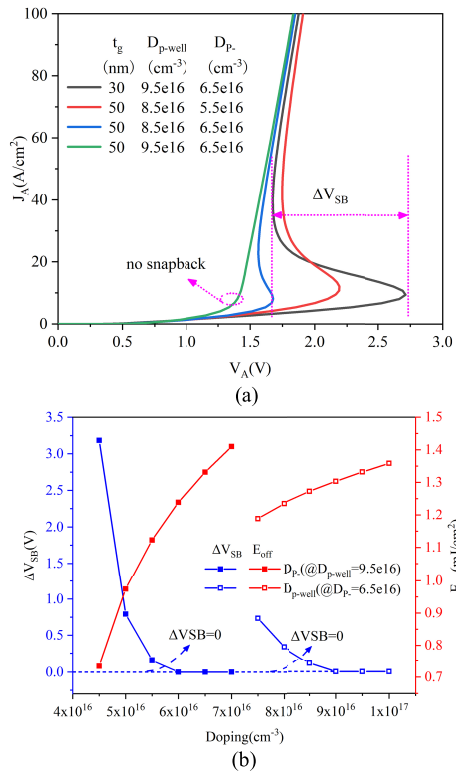
**Figure 2** (a) Forward conduction characteristics of the Con, SBM and TEC LIGBTs, electron barrier provided by (b) p-well and (c) P<sup>-</sup>.

of excess carriers, which greatly shortens the turn-off time of the device, thus realizing the fast switching of the device.

### 3. Results and discussion

Fig. 3(a) and (b) show the effects of  $t_g$ ,  $D_{p\text{-well}}$  and  $D_{P-}$  on forward conduction characteristics of TEC IGBT, where  $t_g$  is the thickness of gate oxide layer in anode. As shown in Fig. 3(a), with the increase of  $D_{p\text{-well}}$ , both the  $\Delta V_{\text{SB}}$  and the voltage at the time of snapback are reduced. This is because the increase of  $D_{p\text{-well}}$  makes the electron barrier it provides larger, thus realize snapback-free. It should be noted that in the case of a certain  $D_{p\text{-well}}$  and  $D_{P-}$ , too small  $t_g$  will reduce the threshold voltage of n-MOS, making it open before the P<sup>+</sup>/N-buffer junction, resulting in the snapback. It can be seen the increasing of  $D_{P-}$  can also suppress snapback because the larger the  $D_{P-}$ , the higher electron barrier it provides. As shown in Fig. 3(b), when  $D_{p\text{-well}} = 9.5 \times 10^{16} \text{ cm}^{-3}$ , the snapback effect can be eliminated with  $D_{P-} = 6 \times 10^{16} \text{ cm}^{-3}$ ; when  $D_{P-} = 6.5 \times 10^{16} \text{ cm}^{-3}$ , the snapback effect can be eliminated with  $D_{p\text{-well}} = 9 \times 10^{16} \text{ cm}^{-3}$ . But it can also be seen that with the increase of  $D_{p\text{-well}}$  and  $D_{P-}$ , the  $E_{\text{OFF}}$  gradually increases. Therefore, the electrical properties of the device can reach the optimal condition when the snapback phenomenon just disappears.

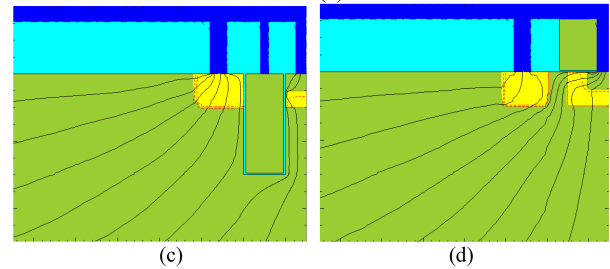
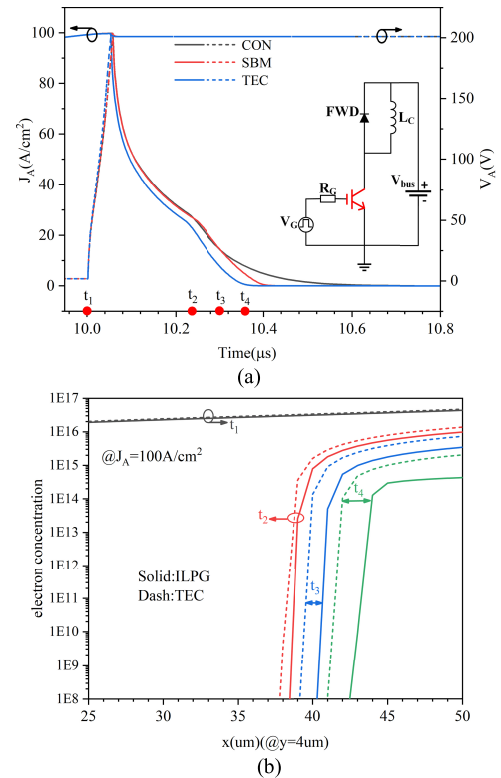
Fig. 4(a) and (b) show the switching characteristics with inductive load circuits for three LIGBTs under the condition of the same  $V_{\text{ON}}$  and no snapback. As can be seen in Fig. 4(a), CON has a long trailing current because it has no electron extraction channel, and it has the longest turn-off time. The turn-off time of SBM is in the middle because it has channels I and II for electron extraction. The proposed device uses the least turn-off time because in addition to channels I and II similar to SBM, there is an additional channel III for electron extraction. Fig. 4(b) shows the elec-



**Figure 3** (a) Effects of the  $D_{p\text{-well}}$  and  $D_{p-}$  on forward conduction characteristics of TEC IGBT. (b) Effects of the  $D_{p\text{-well}}$  and  $D_{p-}$  on  $\Delta V_{SB}$  and  $E_{OFF}$ .

tron distribution of TEC and SBM LIGBT in the N-drift from  $t_1$  to  $t_4$  ( $y=4\ \mu\text{m}$ ) [marked in Fig. 4(a)]. It is obvious that the electron density of TEC LIGBT is significantly lower than that of SBM LIGBT at the same time. Fig. 4(c) and (d) respectively show the current flowlines of SBM and TEC LIGBT during turn-off. It can be seen that although there are two electron extraction channels in SBM, only a small number of electrons are extracted through n-MOS channel I due to the blocking effect of the trench gate, and the electron extraction effect of  $N^+$ /p-well/N-buffer channel II is even minimal. In contrast, a large number of electrons were extracted through channel I and channel II in TEC LIGBT, and a small number of electrons were extracted through  $N^+$ /P-/N-buffer channels III. Therefore, TEC LIGBT achieved a faster switching than SBM LIGBT.

The  $E_{OFF}$ - $V_{ON}$  tradeoff performances of CON, SBM LIGBT and ILPGM LIGBT are shown in Fig. 5, where the thickness of gate oxide layer in anode is 50 nm. CON and SBM can obtain different  $V_{ON}$  by changing the anodic  $P^+$  concentration, while TEC can obtain different  $V_{ON}$  by changing  $D_{p-}$ . As can be seen from the figure, as the  $V_{ON}$  increases, the curves of SBM and CON get closer and closer. This is because when the  $P^+$  concentration decreases, the holes injected into N-buffer also decrease, and the corresponding excess carriers in the turn-off also decrease, and the effect of switching speed increasing brought by the electronic extraction channel gradually weakens. At the same time, it can be seen that the proposed LIGBT achieves the best tradeoff between  $E_{OFF}$  and  $V_{ON}$ . Compared with SBM LIGBT, TEC LIGBT reduces  $E_{OFF}$  by 15% at  $V_{ON} = 1.8\ \text{V}$ . When  $D_{p-}$  is increased to reduce  $V_{ON}$ , channel III is gradu-



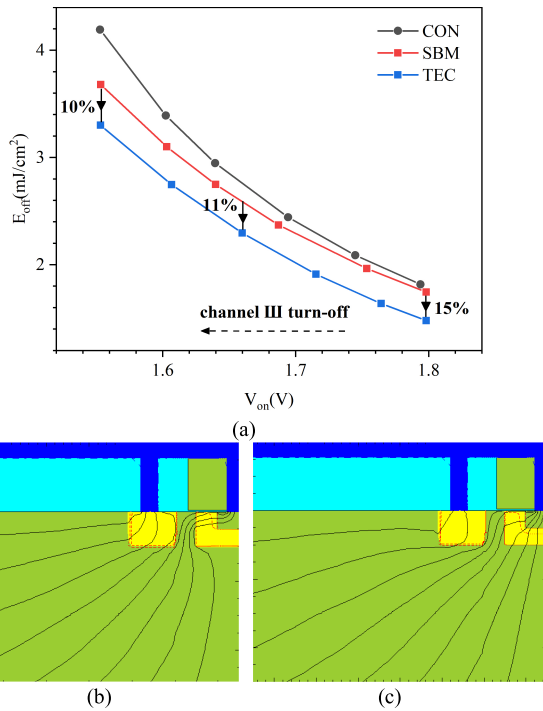
**Figure 4** Switching characteristics. (a) Inductive turn-off waveforms. The bus voltage  $V_{bus}$ ,  $R_G$ , load inductance  $L_C$  are 200 V, 10  $\Omega$  and 1 mH. (b) Electron distribution of SBM and TEC LIGBT at different times [labeled in (a)]. Current flowlines of (c) SBM and (d) TEC during turn-off.

ally closed, and the  $E_{OFF}$  reduction effect of TEC is gradually weakened. However, since there is no barrier of the trench gate, channel I and channel II of TEC are easier to extract electrons. Therefore, when only channel I and channel II are available, TEC still reduces  $E_{OFF}$  by 10% compared with SBM. Fig. 5(b) and (c) are current flowlines of TEC during turn-off when  $V_{ON} = 1.55\ \text{V}$  and  $V_{ON} = 1.8\ \text{V}$  respectively. It can be clearly seen that the channel III is turn-off in (b) and turn-on in (c).

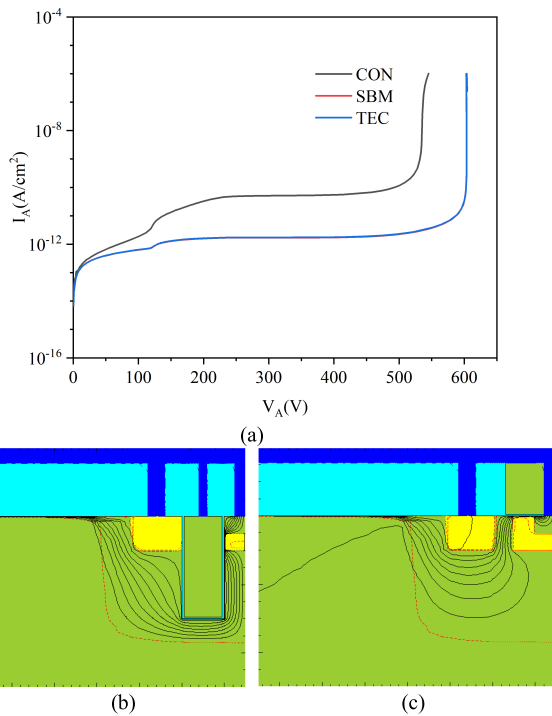
Fig. 6(a) shows the breakdown characteristics of CON LIGBT, SBM LIGBT and TEC LIGBT. It can be seen from the figure that TEC achieves the same breakdown voltage level of 603 V as SBM. As can be seen from Fig. 6(b), similar to SBM, TEC leakage current also flows to  $N^+$  anode rather than  $P^+$  anode through MOS channel, which is similar to the blocking mechanism of MOS.

#### 4. Conclusion

The proposed TEC LIGBT changes the trench gate of self-biased n-MOS in SBM to a planar gate, does not require additional trench etch process, and adds a P- region to suppress



**Figure 5** (a) Tradeoff performance between  $E_{OFF}$  and  $V_{ON}$  of CON, SBM and TEC LIGBTs at on-state current density of  $100 \text{ A/cm}^2$ . Current flowlines of TEC during turn-off when (b)  $V_{ON} = 1.55 \text{ V}$  and (c)  $V_{ON} = 1.8 \text{ V}$ .



**Figure 6** (a) Breakdown characteristic waveforms of different LIGBTs. Electron leakage current flowlines of (b) SBM and (c) TEC at breakdown.

the snapback phenomenon while providing a third electron extraction channel. When reaching the same breakdown voltage level as the SBM, TEC can completely eliminate the snapback phenomenon and achieve a better tradeoff than the SBM. Under the same  $J_A = 100 \text{ A/cm}^2$  condition, TEC reduces the  $E_{OFF}$  by 15% relative to SBM at  $V_{ON} = 1.8 \text{ V}$  when all three channels are active, and 10% relative to SBM

at  $V_{ON} = 1.55 \text{ V}$  when only channel I and channel II are available due to the absence of blocking effect trench gate provided.

## Acknowledgments

This work was supported by Science and Technology on Analog Integrated Circuit Laboratory (6142802200510), Project of Chongqing Natural Science Foundation (cstc2020jcyj-msxmX0572) and Project No.2020CDJ-LHZZ-076 Supported by the Fundamental Research Funds for the Central Universities.

## References

- [1] K. Hara, *et al.*: “600 V single chip inverter IC with new SOI technology,” ISPSD (2014) 418 (DOI: 10.1109/ispsd.2014.6856065).
- [2] T. Letavic, *et al.*: “650 V SOI LIGBT for switch-mode power supply application,” ISPSD (2006) 357 (DOI: 10.1109/ispsd.2006.1666145).
- [3] H. Wang, *et al.*: “Novel fast-switching LIGBT with P-buried layer and partial SOI\*,” Chin. Phys. B **30** (2021) 027302 (DOI: 10.1088/1674-1056/abcf3e).
- [4] S. Li, *et al.*: “A high-speed SOI-LIGBT with electric potential modulation trench and low-doped buried layer,” ISPSD (2018) 323 (DOI: 10.1109/ispsd.2018.8393668).
- [5] D. Disney, *et al.*: “High-voltage integrated circuits: history, state of the art, and future prospects,” IEEE Trans. Electron Devices **64** (2017) 659 (DOI: 10.1109/TEDE.2016.2631125).
- [6] L. Sun, *et al.*: “Novel SOI LIGBT with fast-switching by the electric field modulation,” Micro Nano Lett. **15** (2020) 155 (DOI: 10.1049/mnl.2019.0424).
- [7] L. Zhang, *et al.*: “Optimization of  $V_{CE}$  plateau for deep-oxide trench SOI lateral IGBT during inductive load turn-off,” IEEE Trans. Electron Devices **65** (2018) 3862 (DOI: 10.1109/TEDE.2018.2857838).
- [8] W.W.T. Chan, *et al.*: “An effective cross-talk isolation structure for power IC applications,” Proc. IEDM (1995) 971 (DOI: 10.1109/IEDM.1995.499378).
- [9] J. Li, *et al.*: “Fabrication and investigation of a lateral insulated gate-bipolar-transistor with ultrafast turn-off speed,” IEEE Electron Device Lett. **41** (2020) 573 (DOI: 10.1109/LED.2020.2972804).
- [10] W. Chen, *et al.*: “A snapback-free RC-LIGBT with separated LDMOS and LIGBT by the L-shaped SiO<sub>2</sub> layer,” IEICE Electron. Express **16** (2019) 20190445 (DOI: 10.1587/lelex.16.20190445).
- [11] S. Li, *et al.*: “Snapback-free shorted anode LIGBT with controlled anode barrier and resistance,” Chin. Phys. B **30** (2021) 028501 (DOI: 10.1088/1674-1056/abb7fc).
- [12] Y. Zou, *et al.*: “Low-loss SOI-LIGBT with assistant-depletion trench and partial P-type buried-layer,” IEEE International Conference on Electron Devices and Solid-State Circuits (2019) 1 (DOI: 10.1109/EDSSC.2019.8754119).
- [13] J. Wu, *et al.*: “An ultralow turn-off loss SOI-LIGBT with a high-voltage p-i-n diode integrated on field oxide,” IEEE Trans. Electron Devices **66** (2019) 1831 (DOI: 10.1109/TEDE.2019.2898232).
- [14] H. Hu, *et al.*: “A novel double-RESURF SOI-LIGBT with improved V-ON-E-OFF tradeoff and low saturation current,” IEEE Trans. Electron Devices **67** (2020) 1059 (DOI: 10.1109/TEDE.2020.2964944).
- [15] S. Cao, *et al.*: “Impact of depletion in substrate on turn-off characteristic of superjunction SOI-LIGBT,” IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC) (2019) 1 (DOI: 10.1109/EDSSC.2019.8753989).
- [16] L. Sun, *et al.*: “Analysis of the fast-switching LIGBT with double gates and integrated schottky barrier diode,” IEEE Trans. Electron Devices **66** (2019) 2675 (DOI: 10.1109/TEDE.2019.2912207).
- [17] H. Hu, *et al.*: “A novel low turn-off loss and snapback-free reverse-conducting SOI-LIGBT with integrated polysilicon diodes,” IEEE Trans. Electron Devices **66** (2019) 4296 (DOI: 10.1109/TEDE.2019.2936515).
- [18] W. Chen, *et al.*: “Area-efficient fast-speed lateral IGBT with a 3-D n-region-controlled anode,” IEEE Electron Device Lett. **31** (2010)

- 467 (DOI: [10.1109/LED.2010.2043638](https://doi.org/10.1109/LED.2010.2043638)).
- [19] S. Hardikar, *et al.*: “A fast switching segmented anode NPN controlled LIGBT,” IEEE Electron Device Lett. **24** (2003) 701 (DOI: [10.1109/LED.2003.819270](https://doi.org/10.1109/LED.2003.819270)).
- [20] C. Wang, *et al.*: “A snapback-free and high-speed SOI LIGBT with double trenches and embedded fully NPN structure,” Journal of Semiconductors **41** (2020) 102402 (DOI: [10.1088/1674-4926/41/10/102402](https://doi.org/10.1088/1674-4926/41/10/102402)).
- [21] M.R. Simpson: “Analysis of negative differential resistance in the I-V-characteristics of shorted-anode LIGBTs,” IEEE Trans. Electron Devices **38** (1991) 1633 (DOI: [10.1109/16.85160](https://doi.org/10.1109/16.85160)).
- [22] L. Sun, *et al.*: “Novel snapback-free SOI LIGBT with shorted anode and trench barriers,” IEEE Trans. Electron Devices **68** (2021) 2408 (DOI: [10.1109/TED.2021.3064790](https://doi.org/10.1109/TED.2021.3064790)).
- [23] B.H. Lee, *et al.*: “Dual-gate shorted-anode LIGBT with p(+) injector eliminating the negative resistance regime,” ISPSD (1998) 269 (DOI: [10.1109/ispsd.1998.702685](https://doi.org/10.1109/ispsd.1998.702685)).
- [24] X. Luo, *et al.*: “A snapback-free and low-loss shorted-anode SOI LIGBT with self-adaptive resistance,” IEEE Trans. Electron Devices **66** (2019) 1390 (DOI: [10.1109/TED.2019.2892068](https://doi.org/10.1109/TED.2019.2892068)).
- [25] D.S. Byeon, *et al.*: “The separated shorted-anode insulated gate bipolar transistor with the suppressed negative differential resistance regime,” Microelectron. Journal **30** (1999) 571 (DOI: [10.1016/S0026-2692\(98\)00180-3](https://doi.org/10.1016/S0026-2692(98)00180-3)).
- [26] L. Zhang, *et al.*: “Mechanism and novel structure for di/dt controllability in U-shaped channel silicon-on-insulator lateral IGBTs,” IEEE Electron Device Lett. **40** (2019) 1658 (DOI: [10.1109/LED.2019.2937399](https://doi.org/10.1109/LED.2019.2937399)).
- [27] J. Wu, *et al.*: “A snapback-free and low turn-off loss reverse-conducting SOI-LIGBT with embedded diode and MOSFET,” IEEE J. Electron Devices Soc. **7** (2019) 1013 (DOI: [10.1109/JEDS.2019.2939223](https://doi.org/10.1109/JEDS.2019.2939223)).
- [28] L. Sun, *et al.*: “Fast-switching lateral IGBT with trench/planar gate and integrated schottky barrier diode (SBD),” ISPSD (2019) 379 (DOI: [10.1109/ispsd.2019.8757596](https://doi.org/10.1109/ispsd.2019.8757596)).
- [29] H. Hu, *et al.*: “A novel diode-clamped carrier-stored SOI lateral superjunction IGBT with ultralow turn-off loss and saturation current,” IEEE International Conference on Power Electronics and Drive Systems (2019) 1 (DOI: [10.1109/PEDS44367.2019.8998773](https://doi.org/10.1109/PEDS44367.2019.8998773)).
- [30] X.R. Luo, *et al.*: “A snapback-free fast-switching SOI LIGBT with an embedded self-biased n-MOS,” IEEE Trans. Electron Devices **65** (2018) 3572 (DOI: [10.1109/TED.2018.2842092](https://doi.org/10.1109/TED.2018.2842092)).