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LETTER

A snapback-free RC-LIGBT with separated LDMOS and LIGBT by the L-shaped SiO_2 layer

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Abstract A RC-LIGBT with separated LDMOS and LIGBT by the L-shaped SiO_2 layer is proposed and investigated. The L-shaped SiO_2 layer enhances the bulk electric field remarkably and decreases the surface electric field substantially in the breakdown state. At the forward conduction, the current is dominated by the unipolar mode (LDMOS) before point A and bipolar mode (LIGBT) after point B, the snapback is eliminated between point A and B due to the conductivity modulation is restricted at the LIGBT region. The Free-Wheeling diode (FWD) is realized by the LDMOS region at reverse conduction state. Compared with the conventional RC-LIGBT, the proposed device shows snapback-free property and it increases the BV by 107% at the same time.
Keywords: RC-LIGBT, breakdown voltage, snapback phenomenon
Classification: Electron devices, circuits and modules

1. Introduction

The Reverse Conduction Lateral Insulated-Gate Bipolar Transistor (RC-LIGBT) plays the leading role in power integrated circuits due to the integration of the LIGBT and the Free-Wheeling diode (FWD) in a monolithic chip [1, 2, 3, 4, 5, 6, 7, 8]. However, a snapback phenomenon with abrupt current is observed at the forward conduction. Many advanced structures especially with oxide trench technology have been proposed to address the issue in the previous work [9, 10, 11, 12, 13, 14]. In ref [15], a dielectric trench and a floating P-region are introduced at the collector region (TFP RC-IGBT) to eliminate the snapback by the increase of the collector resistance. In ref [16, 17], an oxide plug and P-float have been introduced in the collector as an electron barrier in the unipolar mode to suppress the snapback by the increase of the V_{PN} between the P-Collector/N-buffer junction. Additionally, the Trench Oxide Layer (TOL) technology with (Enhanced Bulk Field) ENBULF theory [18, 19, 20, 21] and the (Reduced Surface Field) RESURF [22, 23, 24, 24, 25, 26] theory is widely applied to increase the breakdown voltage (BV) by the modulation of the electric field between the bulk and the surface [27, 28, 29, 30].

2. Device structure and parameters

The key parameters of the devices are given in the Table I:

Table I. Parameters of devices

Parameters	Proposed	Conventional
W_D	17 μm	17 μm
Length	27.3 μm	27.3 μm
SiO_2 layer (horizontal)	1 μm × 10.8 μm	—
SiO_2 layer (vertical)	19 μm × 0.5 μm	—
T_2	0.3 μm	0.3 μm
T_3	2 μm	2 μm
N-substrate	8×10^{14} cm^{-3}	8×10^{14} cm^{-3}
P-body	1×10^{16} cm^{-3}	8×10^{16} cm^{-3}
N-collector	1×10^{19} cm^{-3}	1×10^{20} cm^{-3}
P-collector	1×10^{19} cm^{-3}	1×10^{20} cm^{-3}
N^+ emitter	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}
N_d	1×10^{14} cm^{-3}	1×10^{14} cm^{-3}
N-buffer	1×10^{16} cm^{-3}	1×10^{15} cm^{-3}
Total of drift region	2	1
Area of drift region	S_1: 237.5 & S_2: 172.5	425
Depletion Layer	Lateral & Vertical	Vertical
Snapback	0	1.1 V

Fig. 1 shows the mechanism and structure of the proposed device, a L-shaped SiO_2 layer with ENBULF theory is inserted in the N-drift, and the N-drift is divided into LDMOS region (S_1) and LIGBT region (S_2).

3. The electric field characteristics

Fig. 2 shows the corresponding electric field at the breakdown state of the devices. Fig. 2(a) investigates the surface electric field peak $E_{.max}$ for the SiO_2/Si interface at Y = 0, and the $E_{.max}$ are 2.2×10^6 V/μm, 1.1×10^6 V/μm and 0.68×10^6 V/μm for the conventional LDMOS, LIGBT and RC-LIGBT, which are much higher than the proposed RC-LIGBT with 0.27×10^6 V/μm. Moreover, the shape of electric field are triangle distributed for the conventional devices and trapezoid distributed for the proposed at the surface P-body/N-drift junction (Y = 0.5 μm), meanwhile, the $E_{.max}$ transferred from Point E_1 (8.1×10^4 V/μm) to E_2 (2.8×10^5 V/μm), thus the BV for the proposed is increased remarkably. Fig. 2(b) shows the bulk electric field distribution for devices at Y = 15 μm. Compared to the

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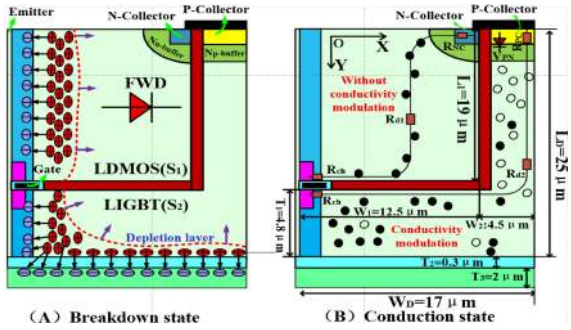

Fig. 1. The mechanism and structure of the proposed RC-LIGBT (a) the depletion and charge compensation at the breakdown state (b) the unipolar of the S_1 and the bipolar of the S_2 region at the conduction state.

conventional devices, the electric field in the N-drift for the proposed RC-LIGBT is increased by 4–5 times due to the introduction of L-shaped Si/SiO_2 junction. The BV is 206.5 V for the proposed RC-LIGBT, which is increased by 50.9% compared with the conventional RC-LIGBT (99.49 V).

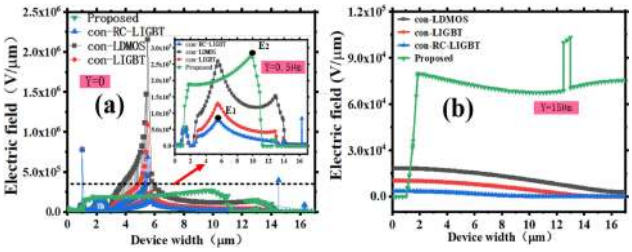

Fig. 2. The electric field distribution for the devices at the N_d 1×10^{14} cm^{-3} (a) surface electric distribution (b) bulk electric distribution.

4. Forward current characteristics

Fig. 3 shows the I-V curves and current distribution for the devices at the forward conduction state. For the conventional RC-LIGBT, when the V_{PN} of the P-collector/N-buffer as illustrated in Fig. 1(a) reaches to 0.6 V at point D, then the device starts to shift from unipolar mode to bipolar mode, thus the snapback phenomenon is observed. For the proposed RC-LIGBT at point A ($V_{PN} < 0.6$ V), the S_1 region conducts with unipolar mode. At point B, the P-collector begins to inject holes, and the S_2 region conducts with bipolar mode. Moreover, the unipolar mode and the bipolar mode are separated and conducted independently by the L-shaped SiO_2.

5. The effect of ratio on BV and V_{on}

Fig. 4(A) shows the influence of BV on Ratio when the N_d increases from 1×10^{13} cm^{-3} to 2×10^{14} cm^{-3}. The Ratio is defined as S_1/S_2, the S_1 and S_2 are the area for the independent LDMOS and LIGBT region. The simulation result shows that the LDMOS has a superior breakdown property than the LIGBT with parasitic PNP transistor. The BV will increase with the increase of the Ratio, and whether N_d is 1×10^{13} cm^{-3}, 5×10^{13} cm^{-3} or 1×10^{14} cm^{-3} the maximum value is reached at Ratio 2:1.

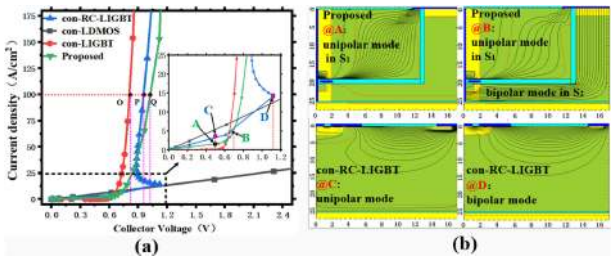

Fig. 3. The forward conduction characteristics for the devices (a) the I-V curves (b) the corresponding current distribution, unipolar at point A for the proposed, unipolar and bipolar at point B for the proposed, unipolar at point C for the conventional, bipolar at point D for the conventional.

Fig. 4(B) gives the influence of V_{on} on Ratio when the N_d is 1×10^{14} cm^{-3}. It shows that the V_{on} decreases from 1.46 V (point P) to 0.82 V (point M) with the Ratio decreasing from 2.5:1 to 1:3 when the current density is 100 A/cm^2, because the current density of the bipolar mode for the S_2 region (LIGBT) is much higher than the unipolar mode for the S_1 region (LDMOS).

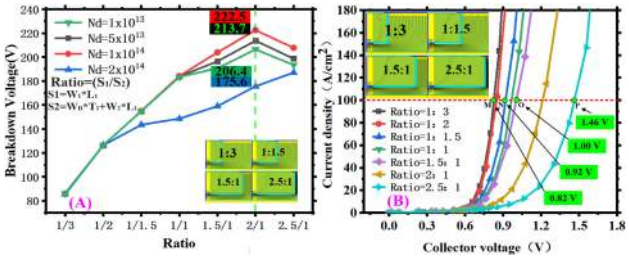

Fig. 4. The dependence of (A) BV and (B) V_{on} on Ratio of the proposed RC-LIGBT. (W_1, L_1, W_d, T_1 and W_2 are shown in the Fig. 1. (B))

6. Reverse characteristics

Fig. 5 gives the reverse conduction characteristics and current distribution for the devices. There is an anti-parallel FWD for each of the conventional LDMOS, RC-LIGBT and the proposed RC-LIGBT. Furthermore, the P-body acts as the anode and the N-collector acts as the cathode of the PIN diode. The current density will exponentially increase when the collector voltage is −0.59 V. However, the conventional LIGBT can not conduct the reverse current because of the inner PNP transistor (P-body/N-drift/P-collector).

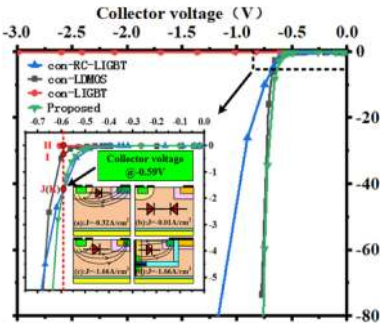

Fig. 5. The reverse conduction characteristics and current density distribution for (a) conventional LDMOS (b) the conventional LIGBT (c) conventional RC-LIGBT (d) the proposed RC-LIGBT.

Fig. 6 gives the key processes of the proposed device. Pictures a∼d and e∼h show the processes of forming channel and N-drift region for LIGBT and LDMOS regions respectively on the epitaxial layer by boron and phosphorus injection, silicon filling, chemical etching and oxidation. Pictures i∼j show the processes of forming collector and electrode respectively by multiple injection in LDMOS and LIGBT.

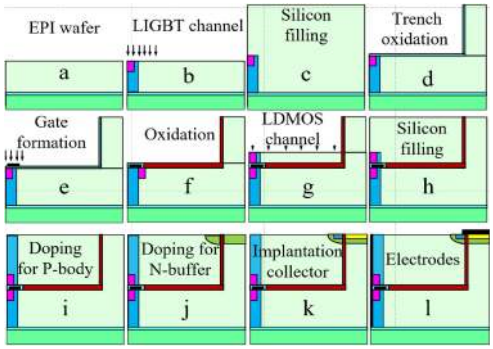

Fig. 6. The key process flow chart of the proposed RC-LIGBT.

7. Conclusion

A novel RC-LIGBT with L-shaped SiO_2 layer is proposed, and the device is divided into separate LIGBT and LDMOS regions. The results show that the BV is 107% higher than that of the conventional RC-LIGBT by the optimization of the surface and bulk electric field at the breakdown state. Furthermore, the Snapback phenomenon is completely eliminated by the restriction of the conductivity modulation in S_2 LIGBT region at the forward conduction state. Additionally, the anti-parallel FWD is integrated in the S_1 LDMOS region, thus the reverse current can be conducted.

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References

[1] W. Sun, *et al.*: "A novel silicon-on-insulator lateral insulated-gate bipolar transistor with dual trenches for three-phase single chip inverter ICs," IEEE Electron Device Lett. **36** (2015) 693 (DOI: 10.1109/LED.2015.2434611).
[2] D. Daniel: U.S. Patent 8729914 (2014).
[3] T. Yoshida, *et al.*: "The second-generation 600 V RC-IGBT with optimized FWD," ISPSD (2016) 159 (DOI: 10.1109/ISPSD.2016.7520802).
[4] K. Kenj: U.S. Patent 8299539 (2012).
[5] N. Iwamuro, *et al.*: "A chip design concept for an extremely low on-state voltage 1200 V FS-IGBT/FWD with high withstand capability for the MERS configuration," ISPSD (2009) 160 (DOI: 10.1109/ISPSD.2009.5158026).
[6] K. Yamada: U.S. Patent 10186609 (2019).
[7] H. Takahashi, *et al.*: "1200 V reverse conducting IGBT," ISPSD (2004) 133 (DOI: 10.1109/WCT.2004.239844).
[8] T. Naito: U.S. Patent 2018366548 (2018).
[9] K. Arjun: U.S. Patent 2016372193 (2016).
[10] L. Zhu, *et al.*: "An investigation of a novel snapback-free reverse-conducting IGBT and with dual gates," IEEE Trans. Electron Devices **59** (2012) 3048 (DOI: 10.1109/TED.2012.2215039).
[11] C. Park: U.S. Patent 9673314 (2017).
[12] T. Takahashi: U.S. Patent 9601485 (2017).
[13] L. Zhu and X. Chen: "Theoretical calculation of the p-emitter length for snapback-free reverse-conducting IGBT," J. Semicond. **35** (2014) 064009 (DOI: 10.1088/1674-4926/35/6/064009).
[14] K. P. Sung: U.S. Patent 9324800 (2016).
[15] H. Jiang, *et al.*: "A snapback suppressed reverse-conducting IGBT with a floating p-region in trench collector," IEEE Electron Device Lett. **33** (2012) 417 (DOI: 10.1109/LED.2011.2180357).
[16] W. Chen, *et al.*: "A high reliable reverse-conducting IGBT with a floating P-plug," ISPSD (2013) 265 (DOI: 10.1109/ISPSD.2013.6694437).
[17] W.-Z. Chen, *et al.*: "A snapback suppressed reverse-conducting IGBT with uniform temperature distribution," Chin. Phys. B **23** (2014) 018505 (DOI: 10.1088/1674-1056/23/1/018505).
[18] W. Zhang, *et al.*: "Ultra-low specific on-resistance SOI high voltage trench LDMOS with dielectric field enhancement based on ENBULF concept," ISPSD (2013) 329 (DOI: 10.1109/ISPSD.2013.6694415).
[19] C. Park: U.S. Patent 2017271498 (2017).
[20] W. Chen, *et al.*: "A snapback-free TOL-RC-LIGBT with vertical P-collector and N-buffer design," Chin. Phys. B **27** (2018) 088501 (DOI: 10.1088/1674-1056/27/8/088501).
[21] S. Yamazaki: U.S. Patent 10263118 (2019).
[22] X. Lin: U.S. Patent 9496333 (2016).
[23] A. Sadovnikov: U.S. Patent 9640611 (2017).
[24] W. Chen, *et al.*: "A snapback suppressed reverse-conducting IGBT with soft reverse recovery characteristic," Superlattices Microstruct. **61** (2013) 59 (DOI: 10.1016/j.spmi.2013.06.012).
[25] L. Zhu, *et al.*: "An investigation of a novel snapback-free reverse-conducting IGBT and with dual gates," IEEE Trans. Electron Devices **59** (2012) 3048 (DOI: 10.1109/TED.2012.2215039).
[26] B. Duan, *et al.*: "Analysis of the novel snapback-free LIGBT with fast-switching and improved latch-up immunity by TCAD simulation," IEEE Electron Device Lett. **40** (2019) 63 (DOI: 10.1109/LED.2018.2881289).
[27] S. Li, *et al.*: "A high-speed SOI-LIGBT with electric potential modulation trench and low-doped buried layer," ISPSD (2018) 323 (DOI: 10.1109/ISPSD.2018.8393668).
[28] G. Deng, *et al.*: "A snapback-free RC-IGBT with alternating N/P buffers," IISPSD (2017) 127 (DOI: 10.23919/ISPSD.2017.7988943).
[29] M. Antoniou, *et al.*: "The semi-superjunction IGBT," IEEE Electron Device Lett. **31** (2010) 591 (DOI: 10.1109/LED.2010.2046132).
[30] X. Xu, *et al.*: "Gate field plate IGBT with trench accumulation layer for extreme injection enhancement," Superlattices Microstruct. **104** (2017) 54 (DOI: 10.1016/j.spmi.2017.01.046).