# A SPAD-Based QVGA Image Sensor for Single-Photon Counting and Quanta Imaging

# A SPAD-based QVGA Image Sensor for Single Photon Counting and Quanta Imaging

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***Abstract*— A CMOS SPAD-based QVGA image sensor with 8µm pixel pitch and 26.8% fill factor is presented. The combination of analogue pixel electronics and scalable shared-well SPAD devices facilitate high resolution, high fill-factor SPAD imaging arrays exhibiting photon shot noise limited statistics. The SPAD has 47CPS dark count rate at 1.5V excess bias (EB), 39.5% photon detection probability at 480nm and minimum 1.1ns dead time at 1V EB. Analogue single photon counting imaging is demonstrated with maximum 14.2mV/SPAD event sensitivity and 0.06e- minimum equivalent read noise. Binary Quanta Image Sensor (QIS) 16kFPS real-time oversampling is shown, verifying single photon QIS theory with 4.6x over-exposure latitude and 0.168e- read noise.**

***Index Terms*— CMOS single photon avalanche diode (SPAD), charge transfer amplifier (CTA) counter, quanta image sensor (QIS), single photon counting (SPC), switched current source (SCS) counter.**

## I. INTRODUCTION

CMOS SPAD-based sensors capture optical signals with single photon sensitivity and picosecond temporal resolution. Applications of these devices include Time of Flight (ToF) 3D vision and LIDAR [1], [2], Fluorescence Lifetime Imaging Microscopy (FLIM) [3], Positron Emission Tomography (PET) [4], and imaging of ultra-fast physical processes such as light in flight [5]. Despite the single photon sensitivity of individual SPAD devices, it has hitherto been challenging to assemble SPAD pixel arrays with sufficient resolution and fill-factor to realize low-light CMOS Image Sensors (CIS). Meanwhile, consumer and scientific CIS have made steady progress, towards the photon counting regime, through increasing pixel conversion gain and optimized readout schemes [6]. Although CIS with sub one electron (1e-) noise have been reported recently [7], [8], the conditions for single photon counting (read noise of 0.3e- [9] down to 0.15e- [6]) have yet to be achieved. In 2005, Fossum projected these CIS trends of sub-electron read noise, sub-micron pixel pitch, multi-megapixel resolution and highly oversampled frame rates towards a Quanta Image Sensor (QIS) [10]. The pixel concept of the QIS ("jot") demands a nano-scale single photon sensitive device exhibiting a binary state. Although SPADs were considered as jot candidates, device scaling issues towards nanometre pitch precluded further investigation [9].

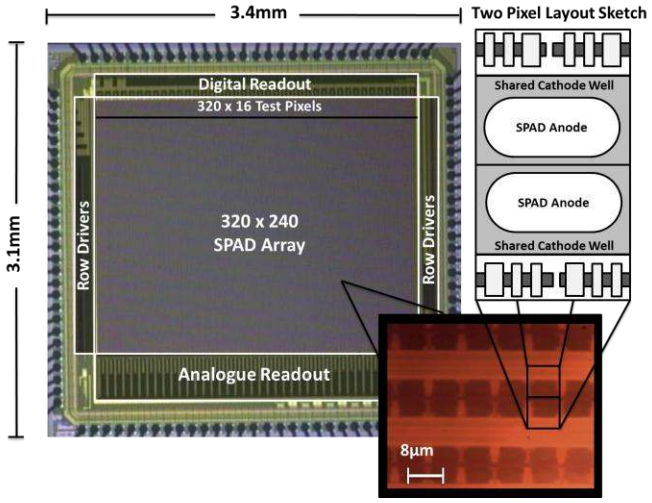


Fig. 1. Photomicrograph of the SPAD-based QVGA imager with inset zoom of the pixel array and layout sketch of the shared-well SPAD structure.

In this paper we demonstrate that analogue pixel electronics and scalable shared-well SPAD devices can be combined to assemble high resolution, high fill-factor pixel arrays exhibiting photon shot noise limited statistics. In a binary operation mode the pixel array offers a look-ahead to the properties of future QIS and a number of recent theoretical results are confirmed experimentally [9]. We present a detailed overview of a 320x240, 8µm pitch, 26.8% fill factor SPAD-based image sensor fabricated in ST Microelectronics 130nm imaging CMOS technology (Fig. 1). In this paper we provide a more detailed treatment to the sensor than first presented in [11]. We begin with a review of SPAD-based image sensors and explain the dual modes of operation of this sensor's SPAD pixel as both an analogue counter and a single bit memory. The device architecture and operation of the readout are described. Finally, single photon counting results are shown along with fast QIS image capture.

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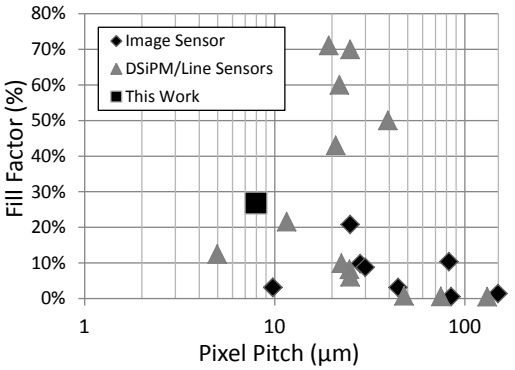


Fig 2. Pixel pitch versus optical fill factor for CMOS SPAD-based image sensor and DSiPM/line sensor pixels.

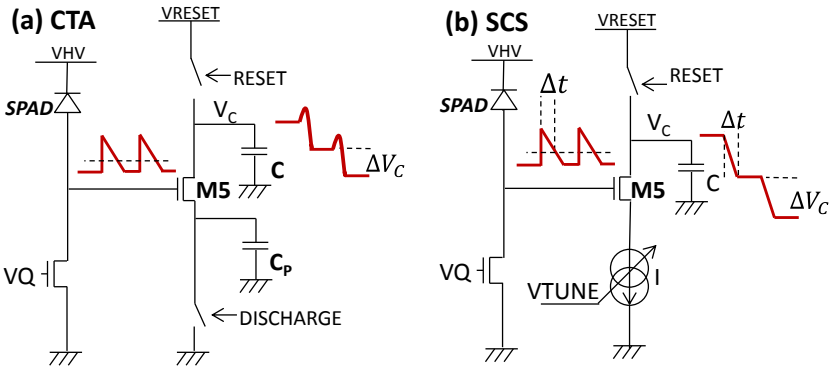


Fig. 3. Simplified circuit diagrams of the operation of two analogue counter implementations: (a) the charge transfer amplifier and (b) the switched current source.

## II. SPAD Image Sensor Pixels

Rochas et al. first reported SPADs in CMOS and subsequently the first fully integrated CMOS SPAD array [12], [13]. Many SPAD sensor architectures have been demonstrated since, in different forms (single point detectors, line sensors, large array photo-multipliers and image sensors) with a plethora of pixel designs. Unlike CISs with the APS-based readout, no single SPAD-based pixel architecture has become dominant. Such image sensors have a different set of design constraints to SPAD-based Digital Silicon Photo-Multipliers (DSiPM) or line sensors. All DSiPM pixels and some line sensor pixels have high fill factor arrays by placing only quench/recharge and addressing circuitry in pixel, such as [14]–[17] and so these are not further considered in this paper. We consider SPAD-based image or line sensors that have the additional in-pixel capability to capture, measure and store a photonic event. A review of the three categories of SPAD imager pixels follows: all-digital, single-bit memory, and analogue. The pixels highlighted in this section are graphed in Fig. 2 in terms of Pixel Pitch (PP) versus Fill Factor (FF) against this work. A range of SiPM pixels are plotted alongside for comparison.

### *A. All-Digital SPAD Pixels*

SPADs, when connected through an inverter, become a true digital imaging pixel with an application specific time conversion or counting circuit; each photon immediately represented as a digital pulse whose leading edge signals the photon's time of arrival with picosecond precision. The first demonstrated was a flash Time to Digital Converter (TDC) pixel with a bump-bonded discrete SPAD [18]. The first fully monolithically integrated all-digital pixel for TOF was in a 60x48 array with 85µm PP and 0.5% FF with two 8-bit up/down counters [19]. Three architectures of digital SPAD pixel for time-resolved FLIM were developed concurrently [20]–[22]: a flash Time to Digital Converter (TDC), a Time to Analogue Converter (TAC) and analogue counter with in-pixel single-slope ramp ADC, and a gated ring oscillator TDC. All three comprise a 32x32 array at 50µm PP with 1.6% FF, with maximum 488 photons/pixel/sec. The array was expanded to 160x128 in [23]. The first in-pixel delta-sigma TDC was implemented in a 44.65µm PP at 3.1% FF for ITOF 3D ranging at 128x96 resolution [2]. A number of TDC-based and counter pixels have recently been demonstrated at 150µm pixel pitch with maximum 4% fill factor and low dark count rate (DCR) noise [24]–[27]. In a monolithic image sensor, the area overhead of the in-pixel digital logic significantly limits the FF of these SPAD-based image sensors to a few percent. This low FF can be partially mitigated by micro-lensing [28] yet the large pitch still remains, which precludes high spatial resolution imaging arrays. Chip-stacking technology offers a promising solution to this limitation [29].

### *B. Single Bit Memory Pixels*

The minimum digital in-pixel logic to capture one SPAD event, is a single bit dynamic or static memory. A SPAD event switches the state of the in-pixel memory within a time-gated exposure window. However, this limits the full well of the pixel to one event (a photon or a dark event) and requires an external frame store to build up a digital image. Such SPAD pixels offer the first practical step toward realising the digital film sensor or QIS concept proposed in [9], [10]. The first example of this time-gated binary pixel architecture combines a SPAD, an inverter, a time gate and a static memory cell for time-gated FLIM in a 128x128 array at 25µm pitch [30] and scaled to a 512x128 array [31]. The 12T NMOS-only pixel uses a NMOS SRAM to avoid hot well spacing rules. The downside is static power consumption during operation. The SRAM consumption scales linearly with array size making it impractical for very high resolution imaging arrays.

### *C. Analogue Pixels*

Recent research has investigated two analogue pixel approaches for high resolution SPAD-based image sensors: TAC pixels for Time Correlated Single Photon Counting (TCSPC) imagers and analogue counters for time-gated Single Photon Counting (SPC) imagers [32], [33]. Fig. 3 illustrates the two different methods of analogue counting: Switched Current Source (SCS) and Charge Transfer Amplifier (CTA). A time gated SPAD pixel using a SCS analogue counter was reported for ITOF [34]. The pixel was implemented in a line sensor format of 64x1 pixels, at a PP of 38x180µm, 0.3% FF, with 25 CMOS transistors. The first example with ≤ 10T in pixel using a SCS counter achieved ~140mV per SPAD event in 30µm PP with 8.7% FF [35] [36]. Although the use of three PMOS in the pixel limits attaining a higher fill factor. In a

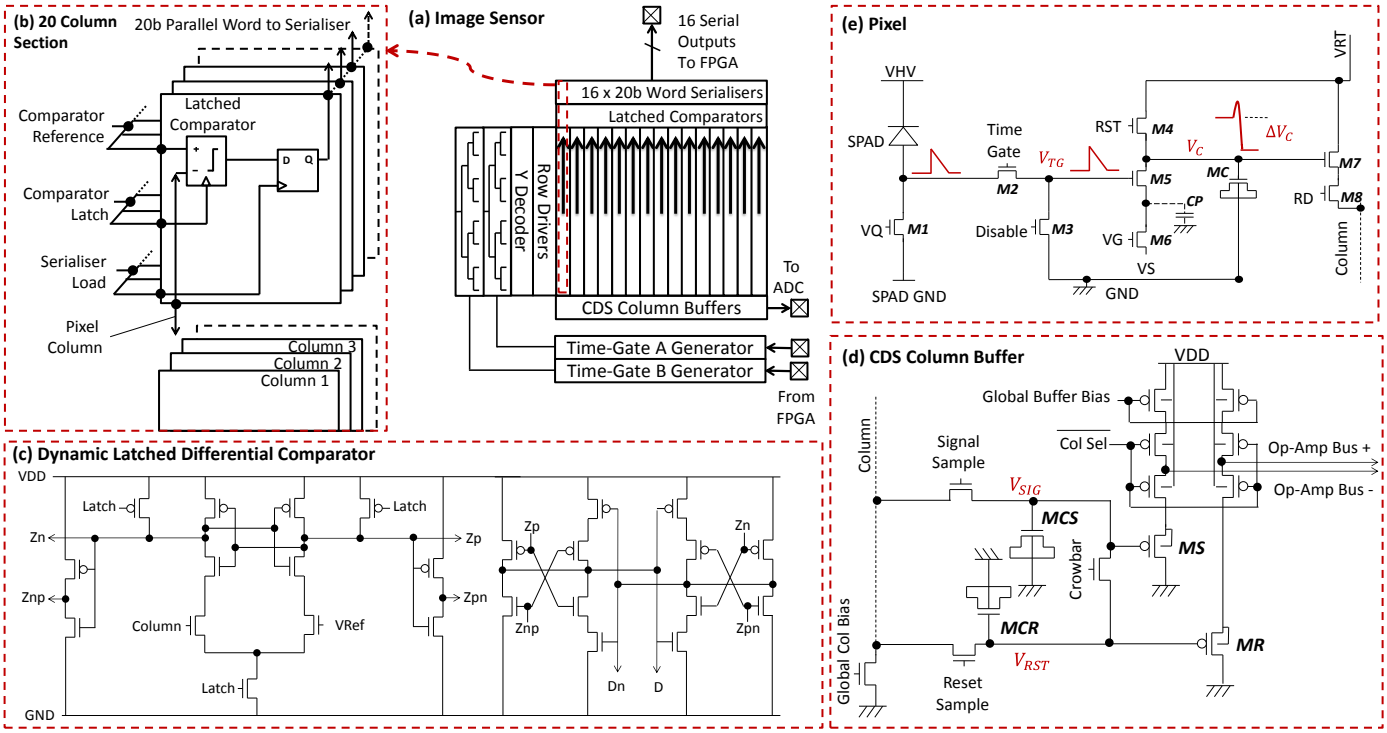


Fig. 4. (a) Image sensor block diagram. (b) Binary column parallel readout diagram. (c) Comparator schematic from binary readout. (d) Analogue CDS column buffer. (e) 9T NMOS-only SPAD-based pixel schematic.

further example, a 32x32 array was implemented with 25µm pitch SCS single photon counting pixels at a notable 20.8% FF [37][38]. The 12T pixel circuit was the first example of a pixel employing only NMOS-only transistors to achieve high FF. A front end gating circuit generates a picosecond duration input pulse removing the SCS dependence on SPAD dead time. An NMOS-only inverter has static power consumption making it unsuitable for a scaling to larger arrays. This same group published 40 pixel linear test arrays with both SCS and CTA trials, replacing the NMOS inverter with CMOS devices in [39], [40]. The PP and FF are estimated at 40x20µm at 10% FF. As a pre-cursor to this work, an NMOS-only 11T hybrid counter architecture combining a CTA and SCS was presented in [32] achieving 9.8µm pitch at 3.1% FF. That CTA pixel is redesigned here, reducing to 9T and implementing SPAD well sharing to achieve 8µm PP at 26.8% FF. Individually [32], and [39], [40] all conclude that CTAs have lower variability reporting ≤2% PRNU, versus SCS ≥8% PRNU.

## III. Image Sensor Overview

### A. SPAD-based Pixel

This section details the operation of the hybrid CTA and SCS analogue counter pixel shown in Fig 4(e). The SPC operation is intended to function in either CTA mode, with small voltages steps (µV to mV range) and a resulting large full well, or SCS mode with large voltage steps (100's mV to V's) and a small full well. In CTA mode, the pixel counter response is bias controllable (as detailed in [32]) using the $V_S$ bias voltage and can be expressed as follows:

$$\Delta V_C = \left(\frac{C_P}{C_T}\right).(V_{EB} - V_S - V_{TM5}) \quad \text{(Eq.1)}$$

Where $C_P$ is the parasitic capacitance between M5 and M6, $C_T$ is the total capacitance of the capacitor MC and $V_{EB}$ is the excess bias of the SPAD (assuming that across the time gate switch M2, $V_{EB} < V_{TIMEGATE} - V_{TM2}$). By the propagation of errors theorem, the pixel to pixel variability is:

$$\frac{\sigma_{\Delta V}}{\Delta V} = \sqrt{\left(\frac{\sigma_{CP}}{CP}\right)^2 + \left(\frac{\sigma_{CT}}{CT}\right)^2 + \left(\frac{\sqrt{(\sigma_{VEB})^2 + (\sigma_{VTM5})^2}}{V_{EB} - V_S - V_{TM5}}\right)^2} \quad \text{(Eq.2)}$$

Where $V_S$ is assumed to be a constant. In SCS mode, M5 is a source follower and M6 is a current source, both here considered only in the saturation region. The equation for the voltage step to first order is:

$$\Delta V_C = \left(\frac{\tau_D}{C_T}\right).\left(\frac{\beta M5}{2}.(V_{GSM5} - V_{TM5})^2.(1 + \lambda V_{DSM5})\right) \quad \text{(Eq.3)}$$

Where the dead time $\tau_D$ is expressed as:

$$\tau_D = \left(\tau_Q + \frac{C_{SPAD}.V_{EB}}{\frac{\beta M1}{2}.(V_Q - V_{TM1})^2}\right) \quad \text{(Eq.4)}$$

Where $\tau_Q$ is the rise time or quenching period of the SPAD avalanche. On the other hand, the SCS pixel to pixel variability is described in the following expressions:

$$\frac{\sigma_{\Delta V}}{\Delta V} = \sqrt{\left(\frac{\sigma_{CT}}{CT}\right)^2 + \left(\frac{\sigma_{IDSM5}}{I_{DSM5}}\right)^2 + \left(\frac{\sigma_{\tau D}}{\tau_D}\right)^2} \quad \text{(Eq.5)}$$

Where the second two terms are expanded as:

$$\frac{\sigma_{IDSM5}}{I_{DSM5}} = \frac{\sigma_{\beta M5}{}^2}{\beta M5} + \frac{\sigma_{VEB}{}^2}{V_{EB}} + \frac{\sigma_{VTM5}{}^2}{V_{TM7}} \quad \text{(Eq.6)}$$

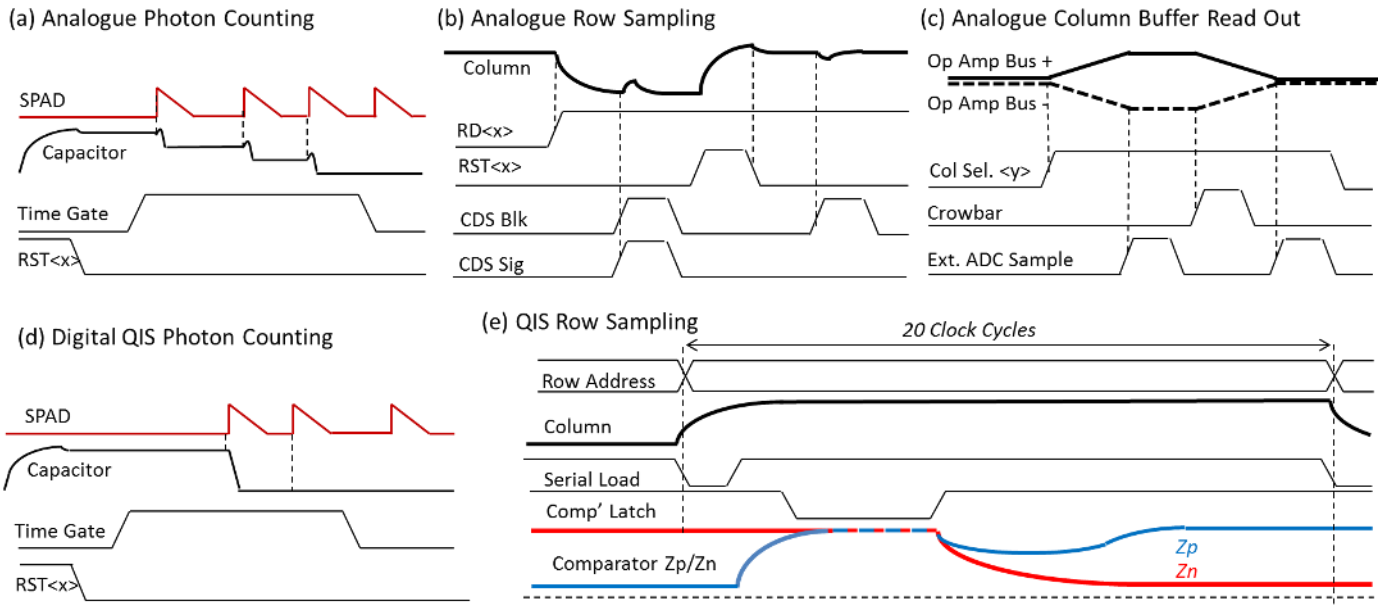


Fig. 5. Timing diagrams: (a) – (c) Analogue single photon counting readout. (d) – (e) Digital 1b 'QIS' readout.

$$\frac{\sigma_{\tau D}}{\tau_D} = \sqrt{\left(\frac{\sigma_{CSPAD}}{C_{SPAD}}\right)^2 + \left(\frac{\sigma_{VEB}}{V_{EB}}\right)^2 + \ldots \left(\sqrt{\left(\frac{\sigma_{\beta}}{\beta_{M1}}\right)^2 + \left(\frac{\sigma_{VTM1}}{V_{TM1}}\right)^2}\right)^2} \quad \text{(Eq.7)}$$

It is apparent from these expressions that the SCS mode inherently suffers from greater variability, yet with a higher achievable voltage step range (with control of either SPAD dead time or $V_{GSM5}$). As a result, the SCS is used only as a dynamic memory for digital single bit operation and the CTA mode for analogue single photon counting. The use of NMOS dynamic memory removes the scalability limit and static power consumption of NMOS-only SRAM.

*B. Image Sensor*

Fig. 4 illustrates the image sensor, pixel, and readout. The pixel (Fig.4(e)) analogue integrator structure consists of M5 dynamic source follower, discharge transistor M6 and poly capacitor (cap) MC. The counter voltage is output via the conventional NMOS CIS APS readout of M7 source follower, M8 read select and M4 reset, the 3T structure proposed in [41] following Noble's classic array readout paper [42]. The image sensor has two distinct readout mechanisms: single channel sequential-read analogue CDS, and column parallel single bit flash A/D conversion. Column parallel CDS sample and hold stages (Fig.4(d)) perform conventional APS row-wise sampling. Each of these CDS column buffers is sequentially scanned out using a single channel analogue bus through two single-ended op-amp buffers to an off-chip differential ADC. The buffer crowbar switch implements the delta-difference sampling (DDS) VFPN minimization technique described in [41].

Furthermore, the single bit digital readout is designed to operate the sensor, as a digitally oversampled binary image sensor, continuously at kFPS. The column-parallel coarse flash conversion and single bit digital readout are intended to function with the pixel biased in SCS mode with the highest counter step size. This operates the pixel as a time-gated

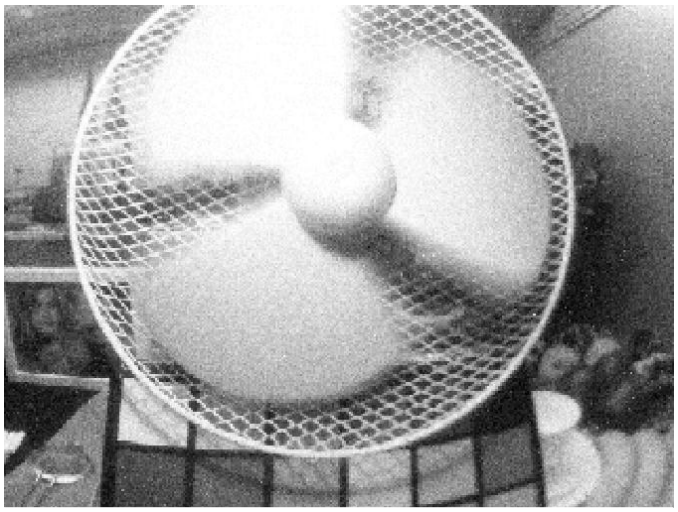

Fig. 6. Five bit QIS frame image consisting of 32 oversampled field images.

photon triggered dynamic memory. In this condition, the noise mechanisms and offsets (kT/C noise, source follower 1/f noise, source follower Vt variation, etc) are much lower in magnitude than the signal, and once input referred, these transistor based noise sources are rendered insignificant. Hence the need for CDS is removed and the data conversion is performed in a single step. Single flash sampling (with no reset sample) allows the row line time to be much shorter than conventional CIS line timing in the region of 100's of ns, as the column does not need to settle twice per row plus the reset time. Incomplete settling of the column lines is permissible, although may lead to higher conversion errors. The schematic of the differential single bit dynamic latched comparator is shown in Fig. 4(c). The column bus is connected directly to the positive side of the NMOS input differential pair. A global voltage reference, from an off-chip DAC, is connected to the negative input of the comparator and is common to all columns. The single-bit comparator output is sampled into a 20b-length serialiser (Fig.4(b)). Each single bit binary image read out from the sensor is referred to as a field image. The

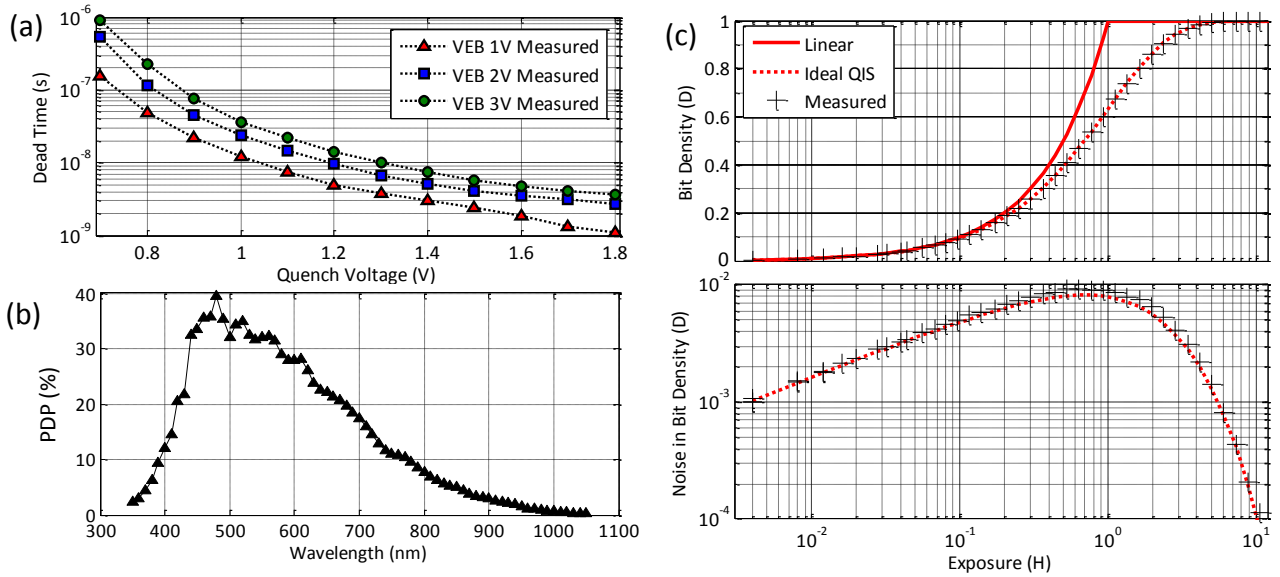


Fig. 7 (a) SPAD dead time versus quench bias. (b) SPAD photon detection probability. (c) QIS normalised density 'D' and noise versus normalised exposure 'H'.

field image is streamed out across 16 serial outputs in 4800 clock cycles. Using a 76.8MHz clock, a field image is therefore transferred in 62.5µs with the sensor operating at 16kFPS with an output data rate of 1.22Gbps.

A nanosecond electronic shutter is created by one of two time-gate pulse generators. Two timing-balanced clock H-trees connect to the time gate row drivers. This row driver circuit selects one of the two time-gate pulses to drive onto each row of the imaging array. Other row drivers handle the row select and read signals, the pixel reset, and the time-gate disable function. Both the X and Y (row and column) addressing decoders are binary to 'one hot' thermometer code converters. The sensor is controlled by an FPGA which handles exposure control, pixel addressing, readout timing, QIS oversampling and manages the data pipeline to PC. Fig. 5 details timing diagrams of the two sensor modes from pixel to readout.

## IV. QIS Image Formation

As described by Fossum in [10], the QIS is an imaging array of photo- sensitive sites with single bit output, each site referred to as 'a jot'. Binary field images (or jot bit planes) are oversampled, either spatially or temporally, to form a multi-bit intensity frame image, where each pixel is composed of a summation of jots. Aggregation is performed in a frame store, summing jot bit planes with a memory location per pixel to the required output bit depth – every doubling of bit depth halves the output frame rate. This has been shown through software post processing in [43], [44] and in a real time FPGA implementation using this image sensor in [11]. To capture the image in Fig. 6, 32 field images are continuously captured each with 2µs exposure time and temporally oversampled to form the shown image with 5-bit depth. It highlights the global shuttering of the field capture where blurring on the edge of the moving fan blades emanates from the temporal summation. It demonstrates that fast moving objects in a scene can be captured continuously using the 16kFPS frame rate single bit capture in conjunction with real-time oversampling.

## V. Experimental Results

### A. SPAD Characterisation

The P-Well to shared Deep N-Well substrate-isolated SPAD is characterised in terms of dark noise, dead time, PDP and temporal jitter. The median Dark Count Rate (DCR) of the image sensor at room temperature is 47 Counts Per Second (CPS) median at 1.5V Excess Bias (EB), this has been improved from previous results in [11] by process improvement. The recharge time of the SPAD after an avalanche event is known as the SPAD 'dead time' as it is un-responsive to subsequent photons during this period. This is an intrinsic pile-up distortion mechanism and must be minimised. The advantage of low pixel pitch SPADs are that the diode capacitance is small, and fast recharge is attainable. The recorded dead-time data for three EBs, are plotted in Fig. 7(a) indicating that 1.1ns dead time is achieved with 1V EB. The Photon Detection Probability (PDP), the SPAD-equivalent of Intrinsic Quantum Efficiency (IQE), is measured and plotted in Fig. 7(b). The PDP is in keeping with previously published results with 39.5% peak at 480nm [45]. The integrated jitter with an 80ps 425nm laser impulse is 184.6ps FWHM, and subtracting the quoted laser driver jitter in quadrature yields 166.4ps FWHM.

### B. Quanta Image Sensor Characterisation

The quanta imaging performance is captured with the sensor exposed to uniform constant illumination with 1V EB at VQ=1V (12ns dead time). The recorded bit plane density ('D') is calculated as those pixels registering a SPAD event, and normalized. Also, the exposure time 'H' is normalized using 3.7µs field exposure α 1.0H. Fig.7(c) displays the measured 'D' versus 'H', and plotted alongside are the ideal 'DlogH' QIS line and an ideal linear line. The overexposure latitude is calculated at 4.6x, which matches QIS theory [9]. The lower graph shows the noise versus exposure, highlighting at lower exposures the sensor is photon shot noise limited, and at higher noise the shot noise is compressed as

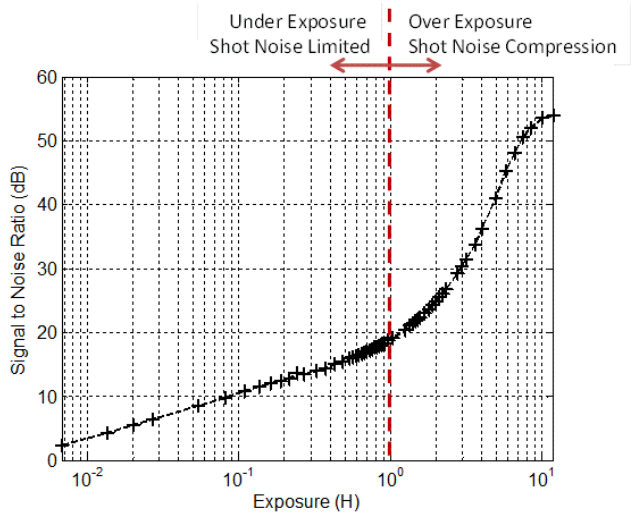


Fig. 8. Measured QIS Signal to Noise Ratio

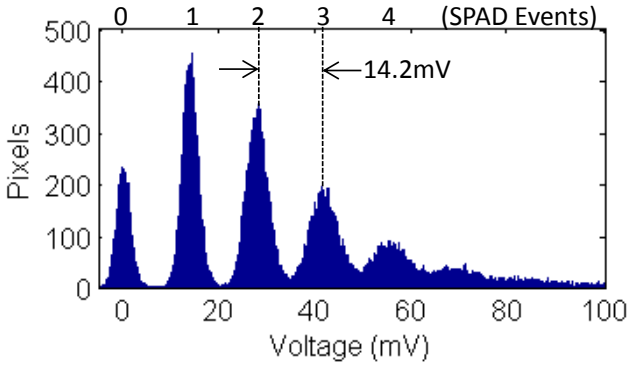


Fig. 9. Image sensor histogram at maximum CTA sensitivity 14.2mV per SPAD event, with 0.06e- equivalent read noise.

expected in a QIS. On average the sensor measures 0.17% higher noise than the ideal, representing a BER of 0.0017 and an equivalent read noise of 0.168e- using the equation in [10]. Fig. 8 demonstrates the measured Signal to Noise Ratio (SNR) of the sensor with 18dB SNR at 1.0H and 54dB SNR peak at 10.0H indicating the shot noise limited performance in the under-exposure region <1.0H and shot noise compression in the overexposure region >1.0H as predicted by QIS theory.

### *C. Single Photon Imaging*

The off-chip 14b ADC temporal noise is measured as 167.3μV RMS. Read noise is measured at 916μV RMS. The dark FPN (1σ) of the sensor is 91μV HFPN, 80.6 μV VFPN, and 99μV PPFPN. The maximum sensitivity in CTA mode is measured at 14.2mV per SPAD event and the histogram of the image sensor output in this condition is shown in Fig 9. The counter step size is bias controllable and the step size can be reduced to attain a higher maximum counting capability, or effectively a higher full well. However, this is to the detriment of read noise. Teranishi [6] describes the condition required for true electron counting at a maximum of 0.15e- read noise. Fossum [9] promotes that photon counting can be achieved with maximum 0.3e- read noise. With higher read noise, discrete single photon peaks cannot be accurately resolved. At the maximum sensitivity the effective full well is approximately 68 SPAD events with 0.06e- read noise. SPC imaging is achieved with this sensor at the 0.15e- input-referred read noise limit with 6.1mV per SPAD event sensitivity or higher, with an effective full well of 163 counts. Moreover, a 0.3e- read noise limit is attained at 3.05mV per SPAD event or higher, with a higher effective full well of 327 counts.

To demonstrate single photon counting image capture of a calibration chart, the pixel array is biased in CTA mode, VS=0.15V and VG=0.7V, and 3V EB with 5μs and 20μs exposure time in Fig. 10(a) and (b) respectively. The histograms of these images are shown below, indicating the discrete peaks of photon counting. To demonstrate global shutter imaging, a fast moving fan is captured under 400 and 5 lux illumination in Fig.10(c) and (d) respectively. The contrast of the four images has been scaled independently and they are captured with a 90º FOV, F#2.0 lens. The large FOV creates a fish eye distortion of the calibration chart in the images.

## VI. Conclusion

This work demonstrates that compact layout of CMOS SPADs with analogue pixel electronics achieves a high spatial resolution image sensor with the highest fill factor of a SPAD-based image sensor pixel to date. The pixel design is scalable to megapixel arrays and is a candidate for the realization of stacked SPAD image sensors. Single photon sensitive imaging is realised in a hybrid of two imaging modalities: in a QIS mode with single photon full well at high frame rate, and with multi-photon full well with analogue counting.

The time-domain characterisation of the time-gating or shuttering will be reported in a future publication. The maximum frame-rate achievable with this sensor will be able to increase to an extent through timing optimization but is fundamentally limited by the number of IO channels. Greater numbers of output channels will increase the frame rate although the scaling of power consumption is a major concern in the QIS paradigm.

In binary image sensor operation, theoretical QIS DLogH intensity and noise characteristics are confirmed experimentally. Furthermore, images are shown, which demonstrate single photon counting imaging, with sub 0.15e- read noise and shot-noise limited statistics. In [9], [46] the concept of multi-photon QIS emerged and it is envisaged that the analogue CTA-based single photon counting in conjunction with fast binary readout will be employed to demonstrate this in future work.

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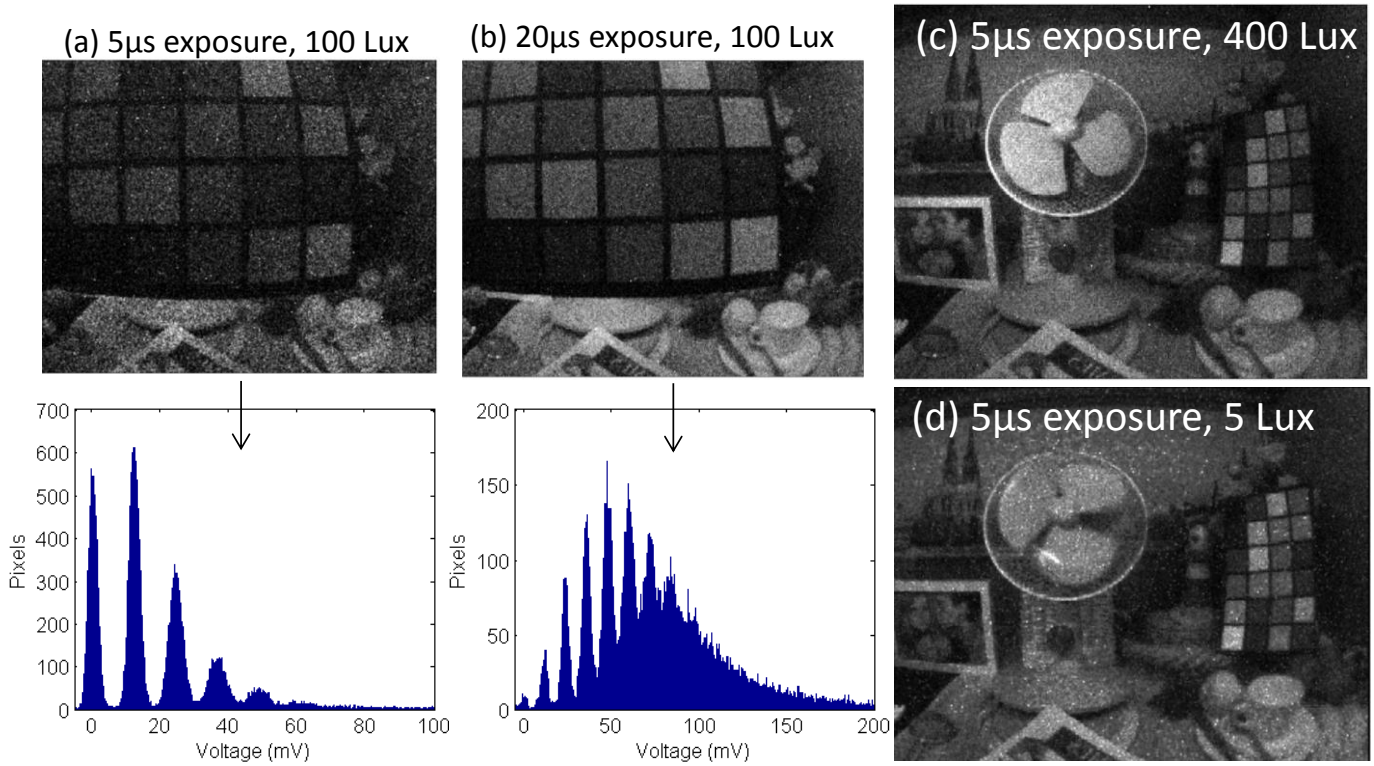


Fig. 10 (a),(b) SPC images and histograms with lower than 0.15e- read noise. (c),(d) Global shutter images are captured at 400 and 5 lux. The contrast of the four images is scaled independently. Defect correction has been applied to image (d).

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