A Study of Digital and Analog Automatic-Amplitude Control Circuitry for Voltage-Controlled Oscillators

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***Abstract*—This paper presents both analog and digital automatic-amplitude control techniques for voltage-controlled oscillators (VCOs). These feedback mechanisms help to keep the VCOs at optimum amplitude over temperature, process, and voltage variations. The VCOs were fabricated in a 50-GHz SiGe BiCMOS process. They use MOS varactors and achieve a 600-MHz tuning range in the 2-GHz band. The phase noise of the VCO with analog control was measured to be −99 dBc/Hz at 100-kHz offset from the carrier. The digital loop allows for a more optimized VCO core that achieves a phase noise of −108.5 dBc/Hz at 100-kHz offset in a low-gain mode. Techniques for suppressing the phase noise in regions of high gain are also presented. The VCOs draw between 4 and 8 mA from a 3.3-V supply.**

***Index Terms*—Broad-band communications, phase noise, radio-frequency integrated circuits, SiGe, voltage-controlled oscillators (VCO).**

I. Introduction

RECENTLY, there has been much interest in the prospect of combining voice-over-IP (VOIP) services with cable television and internet access. This means that consistent operation meeting Data-Over-Cable Service Interface Specification (DOCSIS) over a wide range of operating temperatures (−40 °C to +85 °C) will be the driving specification for any telecommunications chips that will be used in these systems.

This has led to much interest in doing highly integrated cable tuner receivers, capable of delivering high-quality 256 QAM demodulated signals to the baseband processor. Target specifications for phase noise in these systems is usually better than −100 dBc/Hz at 100-kHz offset. Thus, the voltage-controlled oscillator (VCO) in the system must be of good quality. Also, since cable is broadband (47–870 MHz), these VCOs must be tunable over a broad range (1.897–2.72 GHz for an intermediate frequency of 1.85 GHz) and, even so, several VCOs may be necessary to cover the whole range. Automatic-amplitude control is desired because without an adaptive loop it would be impossible for the designer to set the VCO current at an optimal level over all conditions [1]. In this brief, the design of two VCOs with two different approaches to this will be presented.

II. General VCO Design Considerations

The purpose of this design was to create a VCO with a wide tuning range, good phase noise, and very robust performance over process and temperature variations. The requirement for as much tuning range as possible makes the cross-coupled $-G_m$ oscillator topology the only viable option. The current and, therefore, the amplitude in the VCO is set by the current source. In this work, the current source is implemented using either a transistor [Fig. 1(a)] or a resistor with transistor switch (Fig. 2). Transistors $Q1$ and $Q2$ form the negative resistance across the *LC* tank formed by variable capacitors and the inductor. Coupling capacitors C_{cp} are included so that the bases of $Q1$ and $Q2$ can be biased at a dc voltage less than the collector's dc voltage $(V_{\rm ref})$. This allows the voltage swing at the collectors to grow to an acceptable level without saturating the transistors. Simulations have shown that this is a very important design consideration, as once these transistors start to enter saturation at the top and bottom of the oscillation swing, the phase-noise performance of the oscillator is greatly reduced. However, the value of $V_{\rm ref}$ must also be made high enough in order to ensure

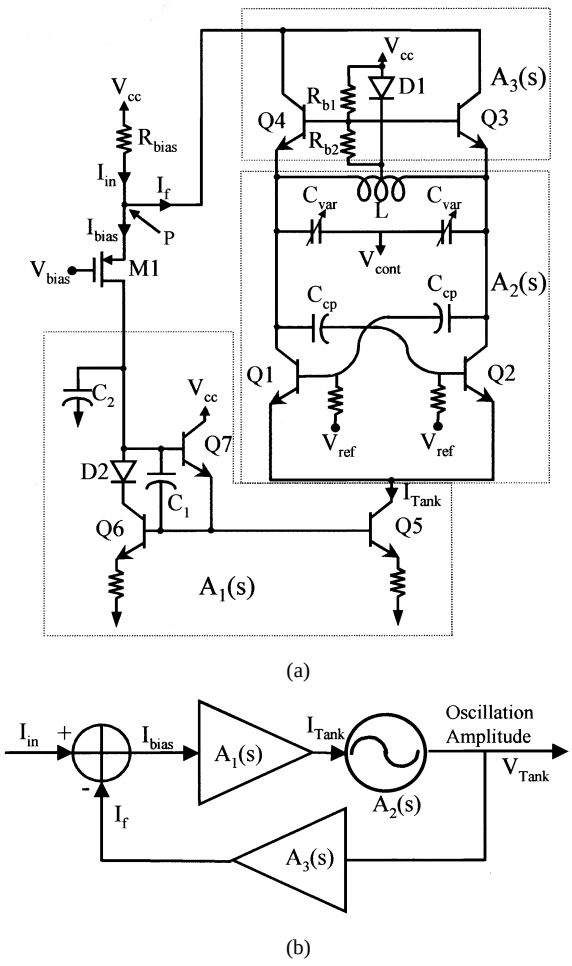

Fig. 1. VCO topology with analog control loop. (a) Circuit diagram. (b) Loop shown conceptually.

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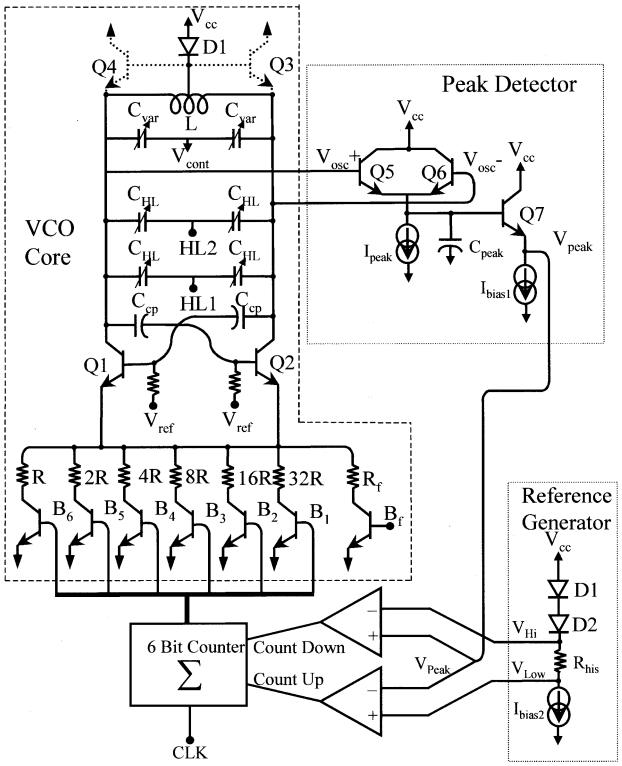

Fig. 2. VCO topology with adjustable degeneration resistors placed in a digital automatic-amplitude control loop.

proper operation of the current source. This can be as low as one V_{BE} plus a few hundred millivolts in the case of a resistor (Fig. 2), but should be on the order of one V_{BE} plus 1 V in the case of a transistor used as a current source [Fig. 1(a)]. Note that there is a large second harmonic signal present at the emitters of $Q1$ and $Q2$, thus, in Fig. 1(a), the voltage at the emitters of $Q1$ and $Q2$ must be higher than $V_{CE\mathrm{sat}}$ to ensure that $Q5$ stays out of saturation for the entire oscillation cycle. For this reason, the resistor option for the current source is more desirable, as it gives the VCO more headroom to develop a larger swing; however, this means that the resistor must be adjustable, as shown in Fig. 2.

The inductor in the tank was implemented using a differential geometry [2]. The varactors themselves were implemented using MOS varactors [3], [4] because these structures feature a high tuning ratio and high Q. Diode D1 is included to reduce the voltage at the tank to allow the varactors to take full advantage of their tuning range. The MOS varactor's C–V curve is centered around 0 V and the full capacitance range is achieved by applying ± 1 V to the device.

III. VCO With Analog Control Loop

In the VCO with the analog control loop shown in Fig. 1(a), transistors $Q3$ and $Q4$ are used to limit the swing of the oscillator to slightly more than 1 V_{BE}. Once the oscillation gets this large, these transistors start to turn on briefly at the top and bottom of the oscillator's swing, loading the tank. This will effectively de-Q the circuit and prevent the signal from growing any larger. Note that having amplitude stabilization mechanisms is important especially in high-gain VCOs, because noise can cause variations in the VCO amplitude and this could modulate the varactors and translate into phase noise [5].

The transistors $Q3$ and $Q4$ limit the amplitude of the oscillation directly, but are also the basis for the second mechanism that is used to make sure that the VCO is operating at an optimal level. Once these transistors start to turn on, they start to draw current I_f. Their collectors are connected back to the source of the pMOS device M1. $Q3$ and $Q4$ then steal current away from M1, causing the current in $Q6$ to be reduced. This, in turn, reduces the current in the VCO, which reduces the amplitude of the VCO until the transistors $Q3$ and $Q4$ just barely turn on. This ensures that the VCO always draws just enough current to turn on these transistors and no more, even though the reference currents may vary. The reference current through M1 must, therefore, be set higher than the optimum, as the loop can only work to reduce the current through the oscillator, but can never make it higher.

The loop can be drawn conceptually as shown in Fig. 1(b). The point P shown in Fig. 1(a) acts as a summing node for the three currents I_{in}, I_{bias}, and I_f. The current mirror amplifies this current and produces the tank current, which is taken by the VCO core and produces an output voltage proportional to the input tank current. The limiting transistors at the top of the tank convert the VCO amplitude into a current that is fed back to the input of the loop.

C_2 has been placed in the circuit to limit the frequency response, and it creates one dominant pole in the system. The transfer function for this part of the loop is given by

$$A_1(s) = \frac{I_{\mathrm{tank}}(s)}{I_{\mathrm{bias}}(s)} \approx \frac{\frac{g_{m6}}{C_2}\left(s + \frac{g_{m7}}{C_1}\right)}{s^2 + \left(\frac{g_{m7}}{C_1} + \frac{g_{m6}}{C_2}\right)s + \frac{g_{m6}g_{m7}}{C_1C_2}}. \tag{1}$$

This equation has a dominant pole $P_1 \approx g_{m6}/C_2$.

The oscillator itself forms the second block in the loop. It can be shown using a method similar to the one presented in [6] that for a VCO with parallel tank resistance of R_T, the peak voltage developed across the tank differentially will be given by

$$V_{\mathrm{tank}} = \frac{2}{\pi} I_{\mathrm{tank}} R_T. \tag{2}$$

This formula has obvious limitations in describing certain aspects of oscillator performance. Specifically, for large amplitudes the oscillation amplitude will cease to grow with increasing current, and for low current, the VCO will not start. More importantly, this expression also fails to capture the frequency response of the oscillator amplitude. If the oscillator tank is treated as a resonator with a pulse of current applied to it by transistors $Q1$ and $Q2$ each half cycle, then from this simple model the transient behavior of the circuit can be determined. The resonator forms a time constant $R_T C_{\mathrm{var}}$ that is equivalent to a pole in the response of the oscillation amplitude versus bias

current. This pole can be used to give frequency dependence to (2)

$$A_2(s) = \frac{V_{\text{tank}}(s)}{I_{\text{tank}}(s)} = \frac{2}{\pi C_{\text{var}}} \left(\frac{1}{s + \dfrac{1}{R_T C_{\text{var}}}} \right) = \frac{2}{\pi C_{\text{var}}} \left(\frac{1}{s + \dfrac{\omega_{\text{osc}}}{2Q}} \right). \quad (3)$$

This forms the second dominant pole $P_2 = \omega_{\text{osc}}/2Q$. It is interesting to note that a tank with higher Q will respond slower and, therefore, have a lower frequency pole than a low-Q oscillator. This makes intuitive sense because it is up to the losses in the tank to cause a change in amplitude.

The last part of the loop consists of the limiting transistors. This is the hardest part of the loop to characterize because by their very nature, the limiters are very nonlinear. The transistor base is essentially grounded while the emitter is attached to the tank of the oscillator. In the scheme that has been shown, the base is connected to a voltage higher than the tank voltage. For any reasonable applied tank voltage, the current will form narrow pulses with large peak amplitude. Thus, this current will have strong harmonic content. This harmonic content will lead to a nonzero dc current, which is the property of interest. For fairly large $V_{\text{tank}}/2V_T$

$$I_{C\_\text{AVE}} = \frac{1}{2\pi} \int_0^{2\pi} I_S e^{(V_{\text{tank}}/2V_T)\sin(\theta) + (V_{BEQL}/V_T)}\, d\theta = I_S e^{V_{BEQL}/V_T} I_O \left(\frac{V_{\text{tank}}}{2V_T} \right) \approx \frac{I_S e^{V_{BEQL}/V_T} \cdot e^{V_{\text{tank}}/2V_T}}{\sqrt{2\pi \dfrac{V_{\text{tank}}}{2V_T}}} \quad (4)$$

where $I_O(x)$ is a modified Bessel function of the first kind of order zero, V_{BEQL} is the quiescent bias voltage of the limiters, and I_S is the saturation current. Thus, the gain of this part of the loop is

$$A_3(s) = 2\frac{\partial I_{C\_\text{AVE}}}{\partial V_{\text{tank}}} = \frac{I_S e^{V_{BEQL}/V_T} \cdot e^{V_{\text{tank}}/2V_T}}{\sqrt{\pi V_T V_{\text{tank}}}} - \frac{I_S e^{V_{BEQL}/V_T} \cdot e^{V_{\text{tank}}/2V_T}}{\sqrt{\dfrac{\pi}{V_T}}\, V_{\text{tank}}^{3/2}}. \quad (5)$$

Here, it is assumed that this part of the loop has poles at significantly higher frequency than the one in the VCO and the one in the mirror.

These equations can be used to design the loop and demonstrate its stability. The capacitor C_2 is placed in the circuit to create a dominant and controllable pole P_1 significantly below the other pole P_2. Generally, the frequency of P_2 and gain of $A_2(s)$ are set by the oscillator requirements and are not adjustable. For more stability, the loop gain can be adjusted by either changing the gain in $A_1(s)$ or by adjusting the gain of $A_3(s)$. (This can be done by changing the size of the limiting transistors $Q3$ and $Q4$.) Reducing the gain of the loop is a less desirable alternative than adjusting P_1 because as the loop gain is reduced so is its ability to settle to an exact final value.

IV. VCO With Digital Control Loop

The VCO core for the digital loop is shown in Fig. 2. It uses degeneration resistors; thus, the amplitude of the VCO can be allowed to grow to almost twice the value in the previous design. To make the current adjustable, a set of six weighted resistors with transistor switches was used in this design. Note that in this design bipolar switches were used, but CMOS switches would have worked just as well, and both require less than 100 mV to operate properly. The switches provide 64 possible settings for the value of the degeneration resistance. Thus, if the signals that drive the switches are considered digital bits, then the resistance is chosen with a 6-bit digital word. One nonswitched resistor R_f is also included to avoid a state where all resistors are open. With $R = 200\ \Omega$ and $R_f = 450$, the resulting final design has effective resistor values from 82 to 450 Ω. As well, in this design two sets of identical varactors are included which are connected to a digital control signal. Thus, there are three selectable frequency bands for this design. This was done in an effort to keep the K_{VCO} smaller, which, in general, reduces phase noise and has other beneficial implications on the phase-locked-loop design.

A peak detector was designed and used to detect the amplitude of the VCO as shown in Fig. 2. Since the tank dc level is 1 V_{BE} less than V_{cc} and the desired swing is 2 V_{BE}, the peak voltage on one side of the tank is V_{cc} when the VCO is operating at the proper level. Thus, the desired output from the peak detector is $V_{cc} - 2V_{BE}$. Two references are generated which are compared to the peak detector output. The reference level generator produces two voltages separated by an offset V_{high} and V_{low}. The offset compensates for the fact the VCO amplitude cannot be set with infinite precision with only 6 bits.

The peak detector output is fed into two comparators, which are used to produce two digital signals—countup and countdown. These are then fed into a 6-bit counter which responds to these two signals and produces an output between 0 and 63. This output is then used to make adjustments in the VCO.

Unlike the analog loop, instability due to the system poles is not really a concern in this design, as the clock frequency creates a dominant and very low-frequency pole at $1/f_{\text{clk}}$. Of more concern is whether or not the loop will be able to find a final value. There must be a value of degeneration that will allow the peak detector to put out a value between V_{high} and V_{low}. If there is insufficient resolution, then the loop could "hunt" between two adjacent counts continuously. The other problem with this loop is that, provided that the amplitude of the VCO does not cross one of the threshold levels, there is no feedback. Until the amplitude is changed by some finite amount, the loop does not act to compensate for the change. Thus, noise that causes small amplitude fluctuations cannot be suppressed by this loop. Therefore, two versions of this VCO were built. One had limiters on the VCO tank to suppress these fluctuations, while the other did not. The addition of limiters does make the countdown more challenging to design. Fortunately, as the limiters start to turn on

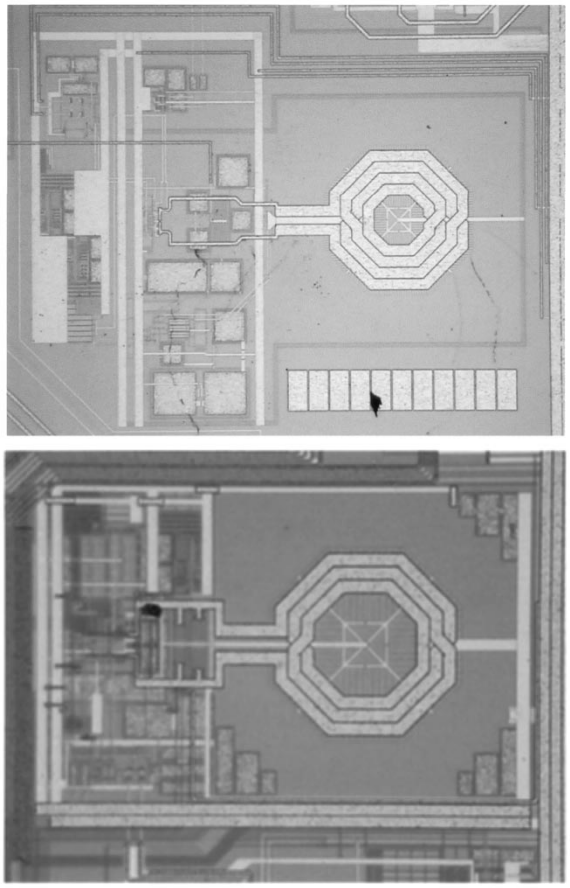

Fig. 3. Photomicrographs of the VCOs.

they slow down the rate of amplitude increase rather than stop it suddenly. Therefore, provided the upper reference is not set too high, the loop can still work in both directions even with the limiters added.

V. Experimental Results

All VCOs were built in a 50-GHz 0.35-μm BiCMOS process. The process had five metal layers and the top-level metal was 3-μm aluminum. A photomicrograph of each VCO is shown in Fig. 3. They use differential octagonal spiral inductors with a patterned ground shields that have a measured differential Q of 15 at 2.4 GHz. The chip area used by the VCOs was 1.2 mm $\times$ 0.8 mm and 1.0 mm $\times$ 0.6 mm, respectively.

Measurements reported here are on the raw performance of VCOs; however, they have also been demonstrated in a synthesizer. The circuits ran off a 3.3-V supply, drew 4 mA in the case of the analog loop (designed for a swing of 0.9 V) and 8 mA of current in the case of the digitally controlled loop (designed for a swing of 1.8 V). The output power of the VCO varied slightly across the operating band; however, this was due to the frequency response of certain elements in the signal path on the board. The tuning characteristic of both VCOs versus control voltage is shown in Fig. 4(a). Note that most of the tuning range is achieved between 2 and 3.3 V. This is due to the tuning characteristic of the varactors in this process. However, these varactors do produce a linear curve, which is good for the synthesizer design. The $K_{\rm VCO}$ as measured from this graph is about

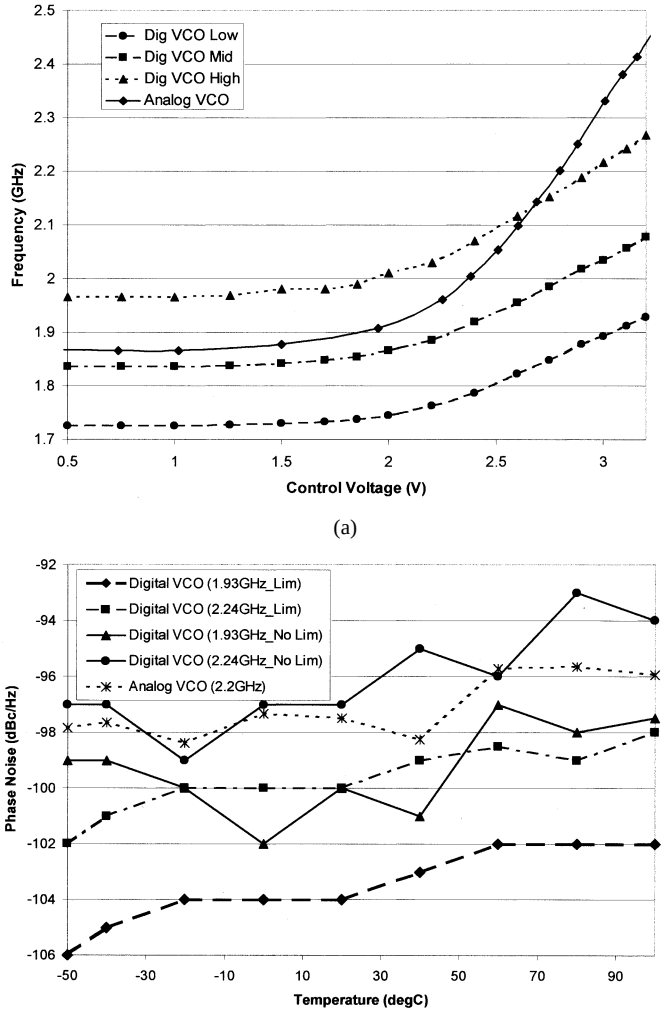

Fig. 4. Plots of some VCO measurements. (a) Frequency versus tuning voltage. (b) VCO phase noise at 100-kHz offset versus temperature.

500 MHz/V. The use of digitally controlled banks of varactors in the case of the digital VCO allowed the $K_{\rm VCO}$ to be reduced in this design while maintaining about the same tuning range. In this case, the low tuning band had a $K_{\rm VCO}$ of 180 MHz/V, the midband had a $K_{\rm VCO}$ of 200 MHz/V, and the high band had a $K_{\rm VCO}$ of 250 MHz/V.

Multiple samples of each version of the circuit were measured at different points in the tuning range. The phase noise of each version was found to vary by no more than a couple of decibels for all samples tested. The best performance of -108.5 dBc/Hz was achieved with the digitally controlled VCO without limiters in the low-gain mode. Table I shows the phase-noise performance of the three designs at various carrier frequencies. Note that the analog-controlled loop has the worst performance due to its reduced amplitude. It measures between -97 and -99 dBc/Hz. The digitally controlled loop without limiters gives the best number of -108.5 dBc/Hz, but the phase noise becomes worse at higher frequencies and is -96 dBc/Hz right at the top. The digital loop with limiters gives the best overall results with a constant -104 dBc/Hz except in the very high-gain region. This demonstrates the importance of suppressing amplitude fluctuations in VCOs with high gain,

TABLE I
PHASE NOISE FOR THE DIFFERENT VCOS UNDER DIFFERENT OPERATING CONDITIONS (FOR HL1 AND HL2, SEE FIG. 2)

VCO AAC Type	Frequency (GHz)	K_{VCO} (MHz/V)	HL1 (V)	HL2 (V)	Phase Noise @100kHz offset (dBc/Hz)
Analog	2.0	0	N/A	N/A	-99
	2.2	500	N/A	N/A	-97
	2.4	500	N/A	N/A	-97
Digital with no Limiters	1.736	0	0	0	-108.5
	1.935	180	0	0	-102
	1.935	0	3.3	0	-100
	2.088	200	3.3	0	-99
	1.998	0	3.3	3.3	-100.5
	2.088	0	3.3	3.3	-100
	2.188	250	3.3	3.3	-98
	2.238	250	3.3	3.3	-96
Digital with Limiters	1.716	0	0	0	-104.5
	1.945	180	0	0	-104
	1.945	0	3.3	0	-104
	2.04	200	3.3	0	-104
	1.988	0	3.3	3.3	-104
	2.24	250	3.3	3.3	-100

even though in low gain, this may degrade phase noise. VCOs without limiters and amplitude control loops were not built; however, simulations showed that without these additions to the circuit, phase-noise variations of as much as 15 dB or more could be expected over all conditions.

The phase noise was also measured over a -50 °C to $+100$ °C temperature range. The phase noise was found to be almost constant over this range, changing by only a couple of decibels. This residual variation is due to changes in the V_{BE} with temperature and the fact that noise sources increase in magnitude with increasing temperature. The result of this measurement is shown in Fig. 4(b). Observations of the counter in digital loop confirmed that it was adapting the current for these changes in temperature.

VI. CONCLUSION

This paper has presented VCOs with both analog and digital automatic-amplitude control loops. A best phase noise of -108.5 dBc/Hz at 100-kHz offset was achieved with the digital loop in a low-gain mode. The VCOs had a very wide tuning range, and using banks of varactors was found to reduce the $K_{\rm VCO}$ without affecting overall tuning range. The phase noise was almost constant over a temperature range of -50 °C to $+100$ °C. The design of the feedback automatic-amplitude control circuitry that helps to achieve this performance has been discussed.

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