

Efficient Approaches for Designing Quantum Costs of Various Reversible Gates

M. Surekha

*Assistant professor, Department of ECE
Visvodaya Engineering College, Kavali, India.*

Abstract

Over the last few decades, research in reversible logic has increasingly become very popular and it is gaining greater momentum in the present world. Reversible logic has started finding concert applications in quantum computing, optical computing, nano-technology based system, low-power CMOS design, VLSI design. The principal objective of this work is to argue for quantum implementation of various reversible logic gates by using C-NOT, Controlled-V and Controlled-V⁺ gates. The present work presents parallel adder/subtractor (with over flow detection), as well as Binary coded decimal adder (BCD) in terms of number of gates, garbage outputs, quantum cost, delay and hardware complexity compared to existing design.

Keywords: Parallel adder/subtractor, Quantum cost, Reversible logic, and Reversible BCD adder.

INTRODUCTION

The process of moving forward in high-level integration and fabrication process has emerged in superior logic circuits and energy loss has also been significantly reduced over the last decades. This inclination of decrease of heat in computation as well as its physical limit are achieved. According to Landauer [1, 2], in logic computation all bits of information loss generates $KT\ln 2$ joules of heat energy where K is Boltzmann's constants of 1.38×10^{-23} J/K and T is absolute temperature of the environment. At room temperature, the dissipating heat is around 2.9×10^{-21} J. Energy loss due to Landauer limit is also important as it is probable that the increase of heat production causing information loss will be perceptible in future.

Reversible circuits are essentially dissimilar from conventionally irreversible ones. In reversible logic, no information is lost, i.e. the circuit that does not lose information is reversible. Bennett [3] showed that zero energy dissipation would be likely if the system consists of reversible gates only. As a result, reversibility will be a necessary for the future circuit design. Quantum computation is also acquiring reputation as some exponentially hard problems can be solved in polynomial time [4]. It is known that the quantum computation is reversible. Therefore, research throughout reversible logic is useful for the improvement of future technologies; it has the possible to methods of quantum circuit construction resulting in more powerful computers. Quantum Technology is not only one, where reversibility is used.

There are a number of existing reversible gates such as the Feynman gate (FG), Double Feynman gate, Fredkin gate (FRG), Toffoli gate (TG), Peres gate (PG) or New Toffoli gate (NTG), New gate (NG), HNG gate, HNFG gate, OTG gate, TSG gate, MTSG gate, MIG gate, TR gate, NFT gate, NCT gate, R-gate, BVF gate, IG gate, RMF gate, MKG gate. Reversible logic has extensive applications in futuristic technologies such as Quantum computing, Quantum dot cellular automata, Nano technology, Optical computing, Ultra low power VLSI design, Low power CMOS circuits, DNA technology etc.

A very significant application of reversible logic is quantum computers. A quantum computer will be viewed as a quantum network (or a family of quantum networks), it is a group of quantum logic gates; each gate performing an elementary unitary operation on one, two or more than two-state quantum systems called qubit. Every elementary unit of information is potentially represented by qubit, corresponding to the classical bit values 0 and 1. Any unitary function is reversible and for this reason, quantum networks are required to be built from reversible logic components [5, 6].

The reversible logic circuits are designed based on the quantum cost, delay, and the number of garbage outputs. Garbage outputs do not perform any useful operations; they are not utilized in outputs in reversible circuits which exist just to maintain reversibility.

A reversible logic circuit must have the following characteristics [7]:

- Use minimum constant inputs.
- Use minimum number of reversible gates.
- Use minimum number of garbage outputs.
- Keep the length of the cascading gate minimum.

Before going to find the quantum cost of reversible gates, it is important to understand how to measure quantum cost of reversible gates. A reversible gate is an M-input and M-output i.e. it can produce unique output vector [8,9] from each input vector and vice versa. Therefore reversible gates are circuits in which the number of outputs is equal to the number inputs. Quantum cost can be calculated as a total number of 2x2 gates and 1x1 gates. 2x2 gates such as C-NOT, V-gate, V⁺-gate and 1x1 gate is a NOT gate.

PRIMITIVE GATES:

Inverter (NOT), C-NOT, V and V⁺ are called primitive gates

NOT gate: A NOT gate is a 1x1 gate is shown in Fig.1. A single qubit is inverted quantum cost of NOT gate is 0 (zero) [10].



Fig.1. NOT gate

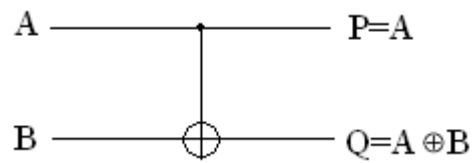


Fig.2. C- NOT gate

Controlled-NOT gate: C-NOT gate is shown in Fig.2. If the control qubit is one, then the target bit is inverted. It is a 2x2 gate; quantum cost of C-NOT gate is 1.

Controlled -V gate: Controlled -V gate [11] is shown in Fig.3(a). If the control signal A=0, then the Q-bit B will be passed through the controlled part without any change, i.e. Q=B. While the control signal A=1 then the unitary operation $V = \frac{i+1}{2} \begin{pmatrix} 1 & -i \\ -i & 1 \end{pmatrix}$ is applied to the input B, i.e., V(B). Quantum cost of Controlled-V gate is 1.

Controlled- V⁺ gate: The controlled V⁺ gate [11] is shown in Fig.3(b). The V⁺ gate performs the inverse operation of the V gate and is also a square root of NOT. If the control signal A=0 then the Q-bit B will be passed through the controlled part without any change, i.e. Q=B. While the control signal A=1 then the unitary operation $V^+ = V^{-1}$ is applied to the input B, i.e., Q=V⁺(B). Quantum cost of Controlled-V⁺ gate is 1.

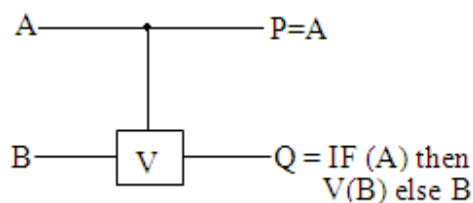


Fig.3(a). Controlled V gate

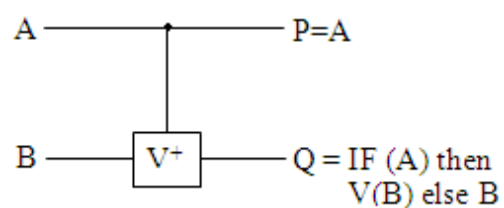


Fig.3(b). Controlled V⁺ gate

The V and V⁺ Quantum gates contain the following properties

$$V \times V^+ = V^+ \times V = I$$

$$V \times V = \text{NOT}$$

$$V^+ \times V^+ = \text{NOT}$$

Based on the above discussion, two controlled V gates (or) two controlled V⁺ gates can be connected in series as shown in Fig.4(a) and Fig.4(b) which is equal to inverter (NOT). If one controlled V gates and one controlled V⁺ gates are connected in series (or) one controlled V⁺ gates and one controlled V gates are connected series as shown in Fig.4(c) and Fig.4(d) which is equal to (identity matrix) identical value (or) simply acts as BUFFER gate [12].

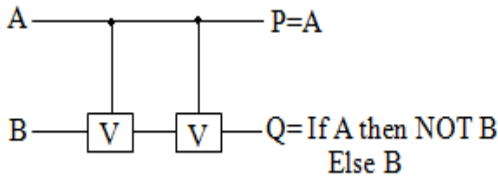


Fig.4(a). V-gates are in series

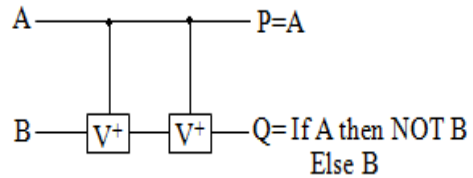


Fig.4(b). V⁺-gates are in series

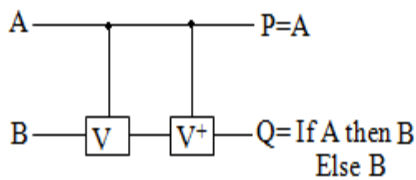


Fig.4(c). V gate and V⁺-gates are in series

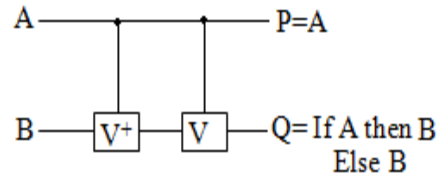


Fig.4(d). V⁺ gate and V-gates are in series

SWAP gate: SWAP gate is also one type of reversible gate. SWAP gate simply exchanges the bits which it has received is shown in Fig.5(a). Quantum implementation of the SWAP gate is constructed in two ways, in the first way, the SWAP gate is constructed by using C-NOT gate, that results quantum cost of 3 is shown in Fig.5(b). In the second way, integrated qubit [13] are used to construct SWAP gate as shown in Fig.5(c), then it's quantum cost is reduced by 1 compared to SWAP gate by Integrated Qubit gate (resulting quantum cost is 2)

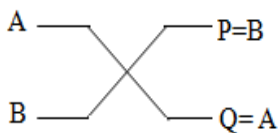


Fig.5(a). SWAP gate

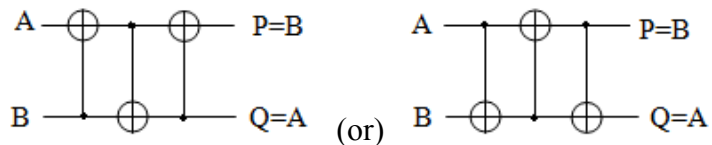


Fig.5(b). SWAP gate by C-NOT

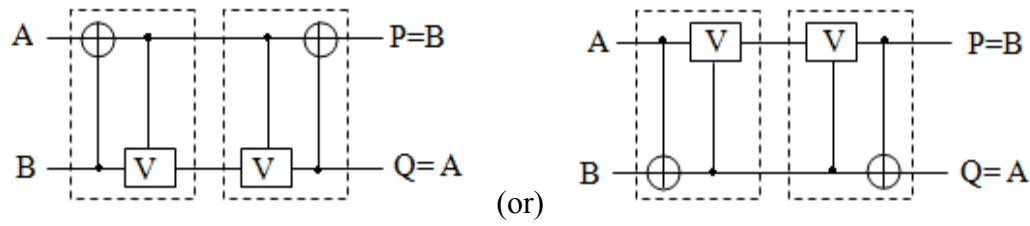


Fig.5(c).SWAP gate by Integrated Qubit

BASIC TERMS OF REVERSIBLE LOGIC :

There are many parameters for determining the performance and complexity of the circuits.

Quantum Cost: The cost of the circuit in terms of the number of primitive gates (1x1, 2x2) is referred as its quantum cost.

Garbage Outputs: The number of unused outputs presented in a reversible logic circuit cannot be avoided. Therefore, these are essential to maintain the reversibility and are referred as garbage outputs.

Constant Inputs: The numbers of inputs that are to be maintained constant at either 0 or 1 in order to synthesis the given logic function.

Delay: Delay of reversible circuit is defined as delay of critical path. Critical path states that maximum number of gates is used between input and output in the circuit.

Total logical calculations: The total logical calculations of reversible logic specify the number of XOR gates, NOT gates, and AND gates in the circuits. Consequently the Total logical calculations can be determined using the following equation;

$$T = \alpha + \beta + \delta \quad (1)$$

Where

T = Total logical calculation

δ = A NOT calculation

β = A two input AND gate calculation

α = A two input EX-OR gate calculation

VARIOUS REVERSIBLE LOGIC GATES AND THEIR QUANTUM COST:

Many reversible gates and their quantum costs are presented in the literature. They are, Feynman gate (FG) [14], Double Feynman gate [15], Fredkin gate (FRG) [16], Toffoli gate (TG) [17], Peres gate (PG) or New Toffoli gate (NTG) [18], New gate (NG) [19], HNG gate [20], HNFG gate [20], OTG gate [21], TSG gate [22, 23], MTSG gate [24], MIG gate [25], TR gate [26], NFT gate [27], NCT gate [28], R-gate

[29], BVF gate[30,31], IG gate [32], RMF gate [33], MKG gate [34]. All gates have an equal number of input and output lines. The gates are designed in such a way that there is unique input and output combination.

Reversible NOT Gate: Reversible NOT gate is 1x1 gate i.e. one input and one output as shown in Fig.6(a). Let us consider the input as A and output as P. Individually the output is $P=A'$. The implementation of NOT gate involves the quantum cost of 0(zero).Quantum equivalent circuit of reversible NOT gate is shown in Fig.6(b). Overall logical computation is $T=1\delta$.

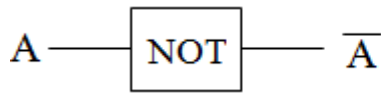


Fig.6(a): Reversible NOT gate

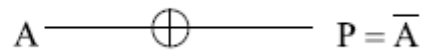


Fig.6(b): Quantum equivalent NOT gate

Feynman Gate (FG) (or) Controlled NOT Gate: Fig 7(a) represents a 2x2 Feynman gate also called as Controlled NOT gate (CNOT). Consider the inputs A and B and the outputs are P and Q. Individually the outputs are $P=A$; $Q=A \oplus B$. It is used as single copying of gate when $B=0$ as shown in Fig.7(b). If $B=1$, the FG gate acts as inverter as shown in Fig.7(c). The implementation of FG results the quantum cost of one. Quantum equivalent circuit of FG gate is shown in Fig.7(d). Overall logical computation is found to be $T=1\alpha$.

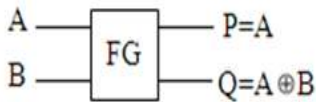


Fig.7(a): FG gate

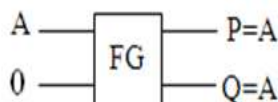


Fig.7(b): FG as single copying gate

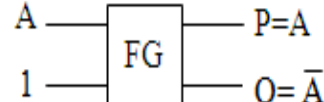


Fig.7(c): FG gate as inverter

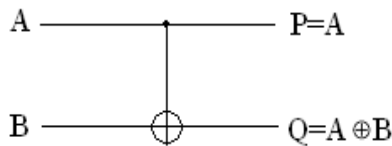


Fig.7(d): Quantum equivalent of FG gate

Double Feynman Gate: Cascading of two FG gates can be called a Double FG gate is shown in Fig.8(a). Let us consider the inputs are A, B and C and the outputs are P, Q and R. Individually the outputs $P=A$; $Q=A \oplus B$; $R=A \oplus C$. It is also used as double copying of gate when $B=C=0$ as shown in Fig.8(b). The implementation of double

Feynman gate results the quantum cost of 2. Quantum equivalent circuit of double FG gate is shown in Fig.8(c). Overall logical computation is found to be $T= 2\alpha$

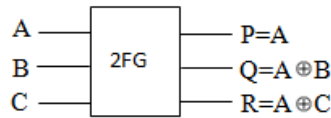


Fig.8(a): Double FG gate

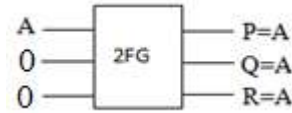


Fig.8(b): Double FG gate as double copying gate

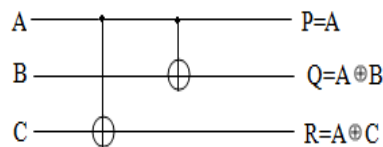


Fig.8(c): Quantum equivalent of double FG gate

Toffoli Gate: A 3x3 Toffoli gate is shown in Fig.9(a). Let us consider the inputs are A, B and C and the outputs are P, Q and R. Individually the outputs $P=A$; $Q=B$; $R=AB \oplus C$. Toffoli gate plays a very important role in the reversible gate. Any boolean function can be implemented by using TG gate, therefore it is also called universal gate. The implementation of Toffoli gate involves the quantum cost of 5. Quantum equivalent circuit of TG gate is shown in Fig.9(b). Overall logical computation is found to be $T= 1\alpha + 1\beta$.

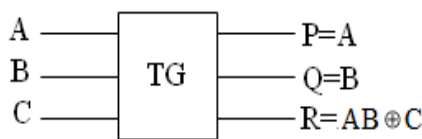


Fig.9(a): TG gate

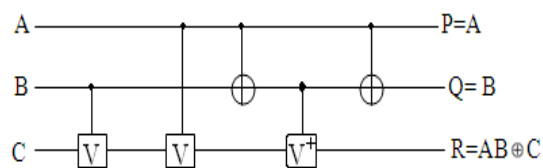


Fig.9(b): Quantum equivalent of TG gate

Fredkin Gate (FRG): A 3x3 Fredkin gate is shown in Fig.10(a). Let us consider the inputs are A, B and C and the outputs are P, Q and R. Individually the outputs are $P=A$; $Q=A'B \oplus AC$; $R=A'C \oplus AB$. Quantum cost of each dotted rectangular box as shown in Fig.10(b) is one. Therefore implementation of Fredkin gate involves the quantum cost of 5. Quantum equivalent circuit of FRG gate is shown in Fig.10(b). Overall logical computation is found to be $T= 2\alpha+4\beta+1\delta$.

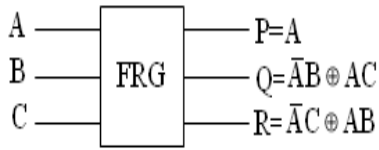


Fig.10(a): FRG gate

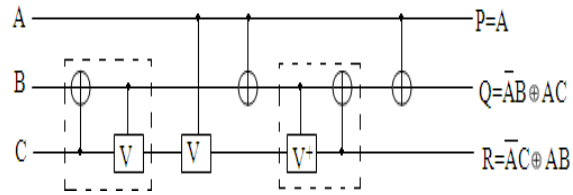


Fig.10(b): Quantum equivalent of FRG gate

New Toffoli Gate (or) Peres Gate: A 3x3 NTG gate is shown in Fig.11(a). Peres gate is the combination of FG and TG gate. Let us consider the inputs are A, B and C and the outputs are P, Q and R. Individually the outputs are $P=A$, $Q=A \oplus B$, $R=AB \oplus C$. The implementation of Peres gate involves the quantum cost of 4. Quantum equivalent circuit of NTG gate is shown in Fig.11(b). Overall logical computation is found to be $T= 2\alpha + 1\beta$.

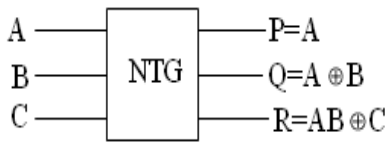


Fig.11(a): NTG gate

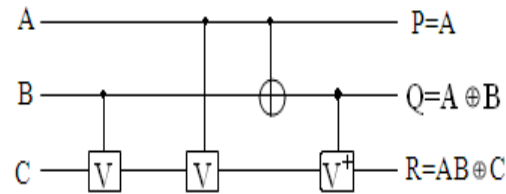


Fig.11(b): Quantum equivalent of NTG gate

New Gate: A 3x3 NG gate is shown in Fig.12(a). Let us consider the inputs are A, B and C and the outputs are P, Q and R. Individually the outputs are $P=A$, $Q=AB \oplus C$, $R=A'C' \oplus B'$. Quantum cost of each dotted rectangular box as shown in Fig.12(b) is one. Therefore the implementation of New gate involves quantum cost of 11. Quantum equivalent circuit of NG gate as shown in Fig.12(b). Overall logical computation is found to be $T= 2\alpha + 2\beta+3\delta$.

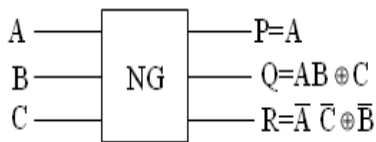


Fig.12(a): NG gate

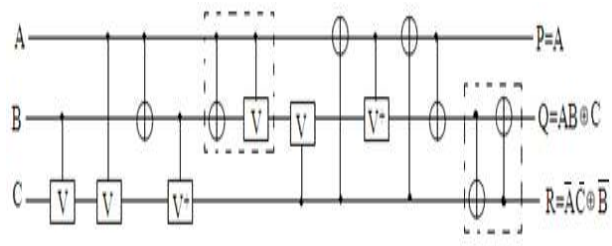


Fig.12(b): Quantum equivalent of NG gate

HNG Gate: A 4x4 HNG gate is shown in Fig.13(a). Let us consider the inputs are A, B, C and D and the outputs are P, Q, R and S. Individually the outputs $P=A$, $Q=B$, $R=A \oplus B \oplus C$, $S=(A \oplus B)C \oplus AB \oplus D$. HNG gate singly acts as full adder if $D=0$ as shown in Fig.13(b). The implementation of HNG gate involves quantum cost of 6.

Quantum equivalent circuit of HNG gate is shown in Fig.13(c). Overall logical computation is found to be $T=4\alpha + 2\beta$.

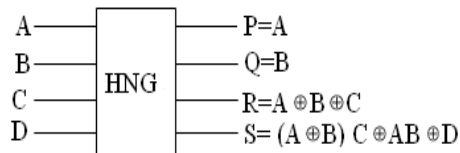


Fig.13(a):HNG gate

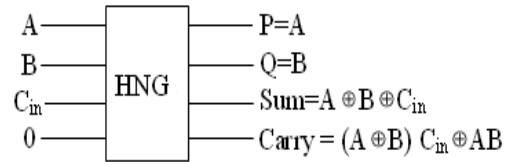


Fig.13(b):HNG gate as full-adder

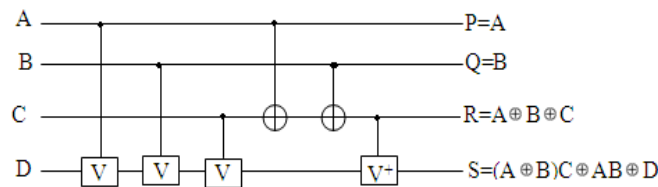


Fig.13(c): Quantum equivalent of HNG gate

HNFG Gate: A 4x4 HNFG gate is shown in Fig.14(a). Let us consider the inputs as A, B, C and D and the outputs P, Q, R and S. Individually the outputs are $P=A$, $Q=A \oplus C$; $R=B$; $S=B \oplus D$. HNFG gate is suitable for a single copy of two bits without any garbage output, If $C=D=0$ is shown in Fig.14(b). The implementation of HNFG gate involves quantum cost of 5 (by using C-NOT as swapping gate) as shown in Fig.14(c). Quantum cost is also reduced by using integrated Qubit gate as shown in Fig.14(d). is 4. Quantum equivalent circuit of HNFG gate is shown in Fig.14(c) and Fig.14(d). Overall logical computation is found to be $T=2\alpha$.

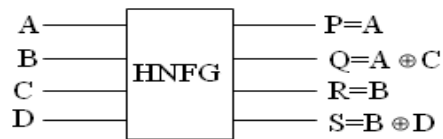


Fig.14(a): HNFG gate



Fig.14(b): HNFG gate as single copy of two bits

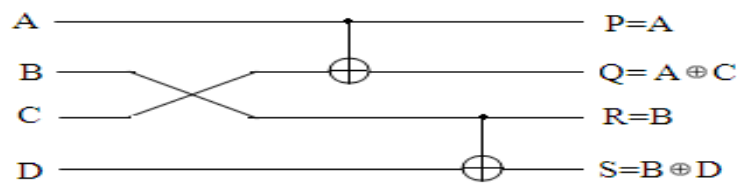


Fig.14(c): Quantum equivalent of HNFG gate

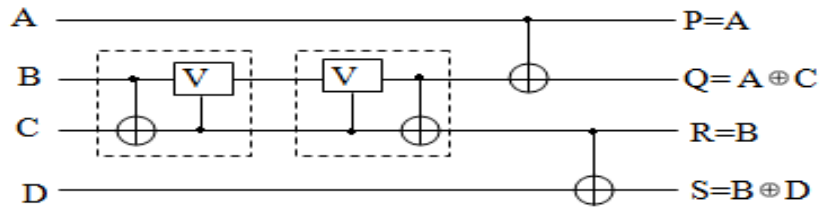


Fig.14(d): Quantum equivalent of HNFG gate

OTG Gate: OTG means Online Testable Gate. A 4x4 OTG gate is shown in Fig.15(a). It provides online testability in reversible logic circuits. Let us consider the inputs as A, B, C and D and the outputs are P, Q, R and S. Individually the outputs are $P=A$, $Q=A \oplus B$, $R=A \oplus B \oplus D$, $S=(A \oplus B)D \oplus AB \oplus C$. All Boolean functions can also be realized by using OTG gate and also work singly as a reversible full-adder if $C=0$ and $D=C_{in}$ as shown in Fig.15(b). the implementation of OTG gate involves quantum cost of 9 by using C-NOT as swapping gate as shown in Fig.15(c). or the implementation of OTG gate involves quantum cost of 8 by using integrated Qubit gate is shown in Fig.15(d). Quantum equivalent circuit of OTG gate is shown in Fig.15(c) and Fig.15(d). Overall logical computation is found to be $T= 4\alpha + 2\beta$.

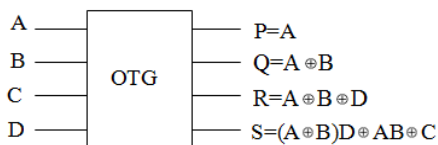


Fig.15(a): OTG gate

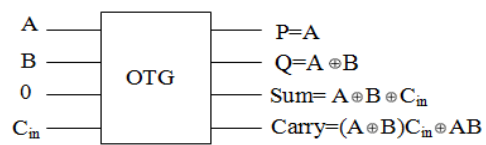


Fig.15(b): OTG gate as full-adder

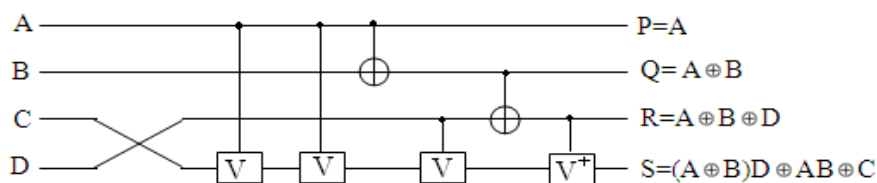


Fig.15(c): Quantum equivalent of OTG gate

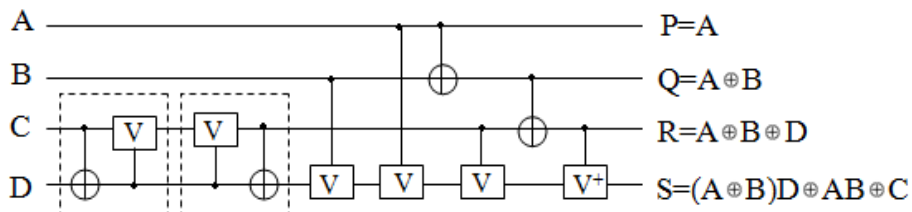


Fig.15(d): Quantum equivalent of OTG gate

TSG Gate: A 4x4 TSG gate is shown in Fig.16(a). Let us consider the inputs as A, B, C and D and the output are P, Q, R and S. Individually the outputs are $P=A$, $Q=A'C' \oplus B'$, $R=(A'C' \oplus B') \oplus D$, $S=(A'C' \oplus B')D \oplus AB \oplus C$. TSG gate is a universal gate because all Boolean functions can also be realized by using TSG gate and also work singly as a reversible full-adder with large reversible functions, if $C=0$ and $D=C_{in}$ as shown in Fig.16(b). The implementation of TSG gate involves quantum cost of 18 by using C-NOT as swapping gates is shown in Fig.16(c). or the implementation of TSG gate involves quantum cost of 17 by using integrated Qubit gate is shown in Fig.16(d). Quantum equivalent circuit of TSG gate is shown in Fig.16(c) and Fig.16(d). Overall logical computation is found to be $T= 4\alpha + 3\beta+3\delta$.

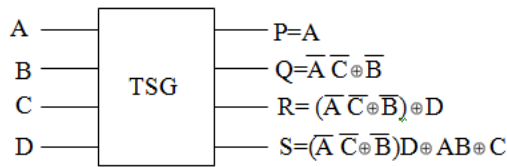


Fig.16(a): TSG gate

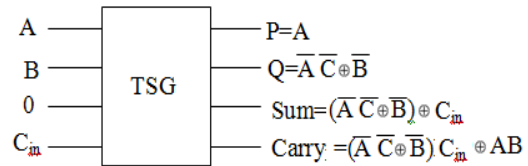


Fig.16(b): TSG gate as full-adder

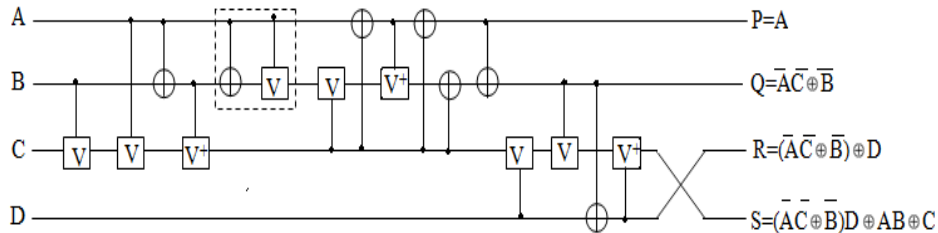


Fig.16(c): Quantum equivalent of TSG gate

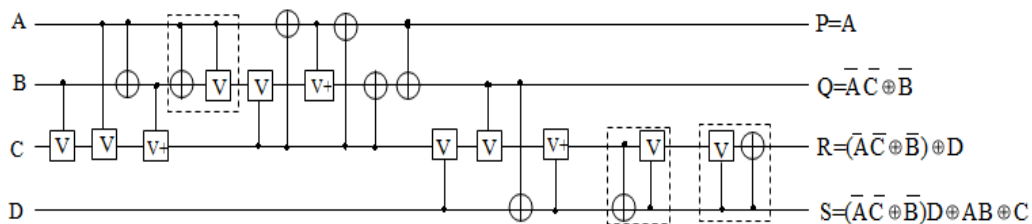


Fig.16(d): Quantum equivalent of TSG gate

MTSG Gate: A 4x4 MTSG gate is shown in Fig.17(a). The modified TSG gate is a MTSG gate. Let us consider the inputs as A, B, C and D and the outputs are P, Q, R and S. Individually the outputs are $P=A$, $Q=A \oplus B$, $R=A \oplus B \oplus C$, $S=(A \oplus B)C \oplus AB \oplus D$. MTSG gate singly acts as full adder, if $C=C_{in}$, $D=0$ as shown in Fig.17(b). The

implementation of MTSG gate involves quantum cost of 6. Quantum equivalent circuit of MTSG gate is shown in Fig.17(c). Overall logical computation is found to be $T= 4\alpha + 2\beta$.

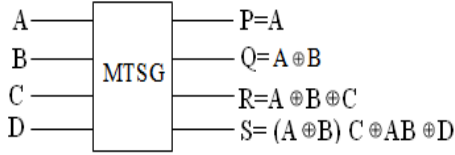


Fig.17(a): MTSG gate

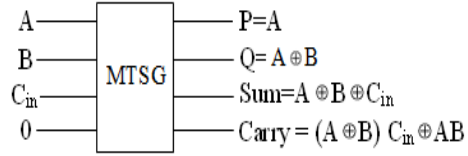


Fig.17(b): MTSG gate as full-adder

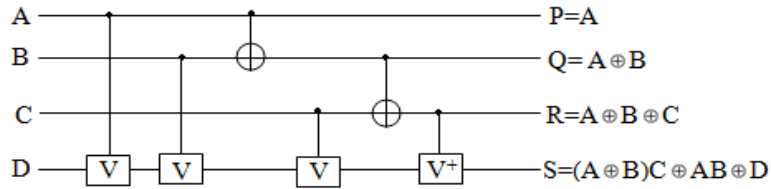


Fig.17(c): Quantum equivalent of MTSG gate

MIG Gate: A 4x4 MIG gate is shown in Fig.18(a). Let us consider the inputs as A, B, C and D and the outputs are P, Q, R and S. Individually the outputs are $P=A$, $Q=A \oplus B$, $R=AB \oplus C$, $S=AB' \oplus D$. Quantum cost of dotted rectangular box as shown in Fig.18(b). is one. Therefore the implementation of MIG gate involves quantum cost of 7. Quantum equivalent circuit of MIG gate is shown in Fig.18(b). Overall logical computation is found to be $T= 3\alpha + 2\beta+1\delta$.

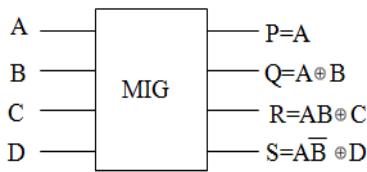


Fig.18(a): MIG gate

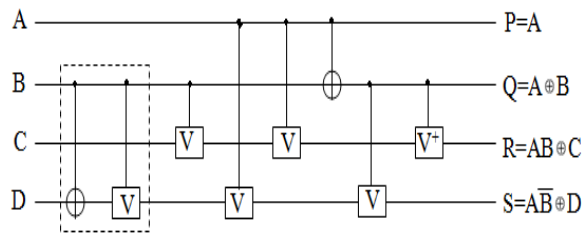


Fig.18(b): Quantum equivalent of MIG gate

TR Gate: A 3x3 TR gate is shown in Fig.19(a). Let us consider the inputs as A, B and C and the output are P, Q and R. Individually the outputs are $P=A$, $Q=A \oplus B$, $R=AB' \oplus C$. 1 is the quantum cost of each dotted rectangular box as shown in Fig.19(b). Therefore the implementation of TR gate results quantum cost of 4. Quantum equivalent circuit of TR gate is shown in Fig.19(b). Overall logical computation is found to be $T= 2\alpha +1\beta +1\delta$.

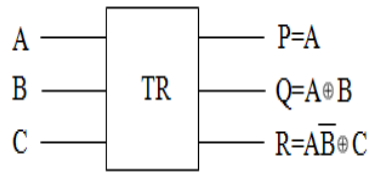


Fig.19(a): TR gate

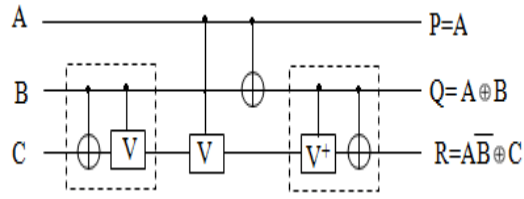


Fig.19(b): Quantum equivalent of TR gate

NEW FAULT TOLERANT (NFT) GATE:

A 3x3 NFT gate is shown in Fig.20(a). Let us consider the inputs as A, B and C and the output are P, Q and R. Individually the outputs are $P=A$, $Q=B'C \oplus AC'$, $R=BC \oplus AC'$. 1 is the quantum cost of each dotted rectangular box as shown in Fig.20(b). Therefore the implementation of NFT gate involves quantum cost of 7. Quantum equivalent circuit of NFT gate is shown in Fig.20(b). Overall logical computation is found to be $T= 2\alpha + 3\beta+2\delta$.

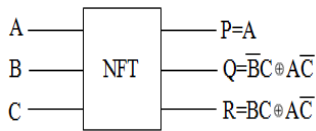


Fig.20(a): NFT gate

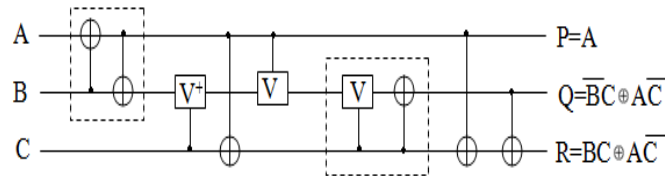


Fig.20(b): Quantum equivalent of NFT gate

NCT Gate: A 3x3 NCT gate is shown in Fig.21(a). Let us consider the inputs as A, B and C and the outputs are P, Q and R. Individually the outputs are $P=A$, $Q=B$, $R=A'B' \oplus C$. Therefore the implementation of NCT gate involves quantum cost of 5. Quantum equivalent circuit of NCT gate is shown in Fig.21(b). Overall logical computation is found to be $T= 1\alpha + 1\beta+2\delta$.

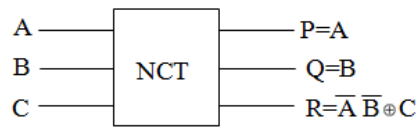


Fig.21(a): NCT gate

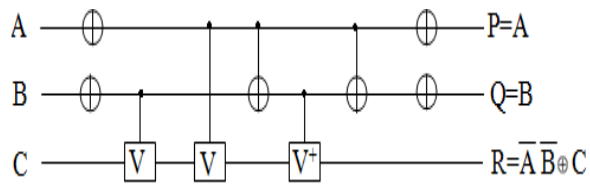


Fig.21(b): Quantum equivalent of NCT gate

R Gate: A 3x3 R gate is shown in Fig.22(a). Let us consider the inputs as A, B and C and the outputs are P, Q and R. Individually the outputs are $P=A \oplus B$, $Q=A$, $R=C' \oplus AB$. Therefore the implementation of R gate involves quantum cost of 5. Quantum equivalent circuit of R gate is shown in Fig.22(b). Overall logical computation is found to be $T= 2\alpha + 1\beta+1\delta$.

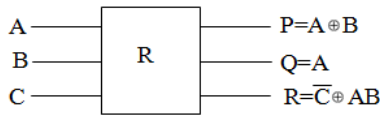


Fig.22(a): R gate

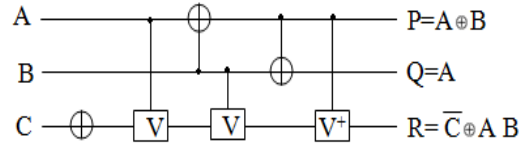


Fig.22(b): Quantum representation of R gate

BVF Gate: A 4x4 BVF gate is shown in Fig.23(a). Let us consider the inputs as A, B, C and D and the outputs are P, Q, R and S. Individually the outputs are $P=A$, $Q=A \oplus B$, $R=C$, $S=C \oplus D$. Therefore the implementation of BVF gate involves quantum cost of 2. Quantum equivalent circuit of BVF gate is shown in Fig.23(b). Overall logical computation is found to be $T=2\alpha$.

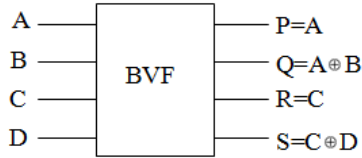


Fig.23(a): BVF gate

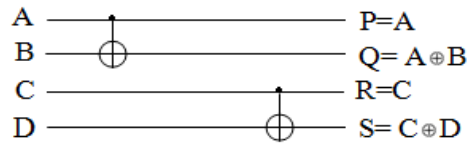


Fig.23(b): Quantum equivalent of BVF gate

RMF Gate: A 4x4 RMF gate is shown in Fig.24(a). Let us consider the inputs as A, B, C and D and the outputs are P, Q, R and S. Individually the outputs are $P=A$, $Q=A \oplus B$, $R=A \oplus B \oplus C$, $S=AB \oplus D$. Therefore the implementation of RMF gate involves quantum cost of 5. Quantum equivalent circuit of RMF gate is shown in Fig.24(b). Overall logical computation is found to be $T=4\alpha + 3\beta + 1\delta$.

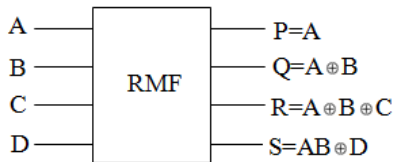


Fig.24(a): RMF gate

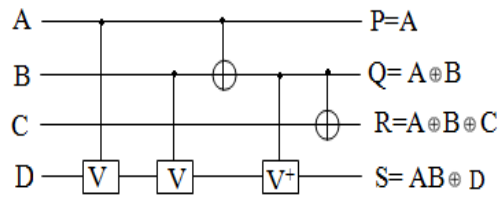


Fig.24(b): Quantum equivalent of RMF gate

IG Gate: A 4x4 IG gate is shown in Fig.25(a). Let us consider the inputs as A, B, C and D and the outputs are P, Q, R and S. Individually the outputs are $P=A$, $Q=A \oplus B$, $R=AB \oplus C$, $S=DB \oplus B'(A \oplus D)$. Modified version of MIG gate is IG gate. Therefore the implementation of IG gate involves quantum cost of 9. Quantum equivalent circuit of IG gate is shown in Fig.25(b). Overall logical computation is found to be $T=3\alpha + 3\beta + 1\delta$.

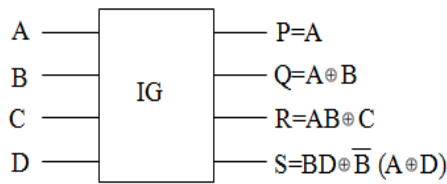


Fig.25(a): IG gate

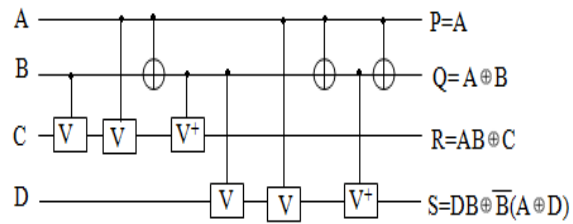


Fig.25(b): Quantum equivalent of IG gate

MKG Gate: A 4x4 MKG gate is shown in Fig.26(a). Let us consider the inputs as A, B, C and D and the outputs are P, Q, R and S. Individually the outputs are $P=A$, $Q=C$, $R=(A'D' \oplus B') \oplus C$, $S=(A'D' \oplus B')C \oplus (AB \oplus D)$. Therefore the implementation of MIG gate involves quantum cost of 16 by using C-NOT as swapping gate as shown in Fig.26(b). Or the implementation of MIG gate involves quantum cost of 15 by using integrated Qubit gate is shown in Fig.26(c). Quantum equivalent circuit of MKG gate is shown in Fig.26(b) and Fig.26(c). Overall logical computation is $T= 4\alpha + 3\beta+3\delta$.

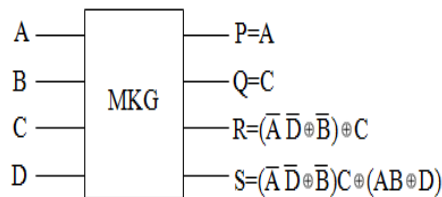


Fig.26(a): MKG gate

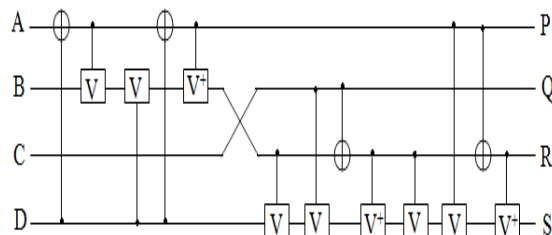


Fig.26(b): Quantum equivalent of MKG gate

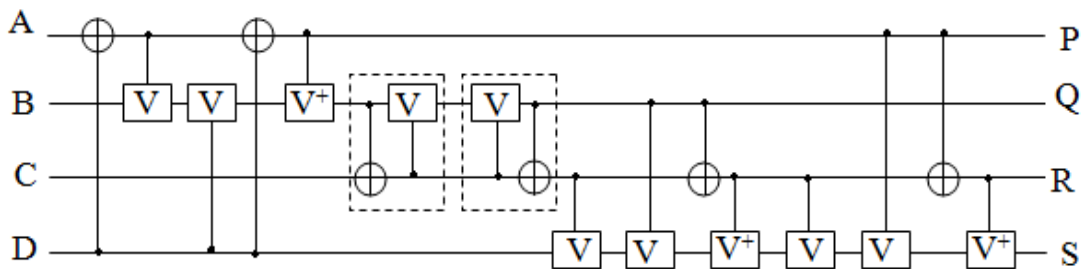


Fig.26(c): Quantum equivalent of MKG gate

DESIGN OF REVERSIBLE ADDERS

The design of reversible arithmetic adders, such as ripple carry adder, parallel adder/subtractor, and BCD adder plays very significant role in designing system hardware.

4-BIT RIPPLE CARRY ADDER:

The basic building block of ripple carry adder is the full adder. Binary adders are implemented to add two numbers. So 4 Full -Adders are required to add two 4-bit binary numbers. The reversible ripple carry adder can be designed by cascading the reversible full adder. In this work, 4-bit ripple carry is designed by cascading 4- HNG gates as shown in Fig.27. The output expressions for the ripple carry adder are:

$$S_i = A \oplus B \oplus C_i \quad (2)$$

$$\text{and } C_{i+1} = (A \oplus B) C_i \oplus AB \quad (3)$$

Where $(i=0, 1, 2 \dots)$

The ripple carry adder is designed with minimum number of reversible gates, garbage output, quantum cost and total logical calculations.

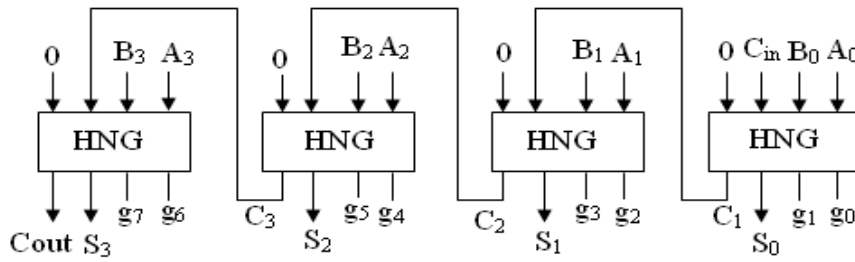


Fig.27. 4-bit Reversible Ripple carry adder

4-BIT PARALLEL ADDER/SUBTRACTOR (WITH OVERFLOW):

Computers need only one common hardware circuit to handle arithmetic operations like addition and subtraction. Therefore in the present work, we constructed 4-bit parallel adder/subtractor (with over flow) as shown in Fig.28. The addition and subtraction operations can be combined into one circuit through one common binary adder by adding an EX-OR gate into each full-adder. Reversible parallel adder/subtractor is constructed by using HNG and FG gates. Depending up on the mode (M) of operation, the circuit is either a 4-bit full adder or 4-bit full subtractor.

When $M=0$, the circuit is equivalent to adder i.e. $B_{(bit)} \text{ XOR } 0 = B_{(bit)}$ and the Carry bit =0, then the circuit performs the operation $A+B$ (addition).

When $M=1$, the circuit is equivalent to subtractor i.e. $B_{(bit)} \text{ XOR } 1 = \text{inverted } (B_{(bit)})$ and the carry bit =1, then the circuit performs the operation $A-B$ (subtraction).

Before performing any arithmetic operation, numbers are loaded into registers. For a number between 0 to 15 we use a register length 4-bits, when two 4-bit numbers are added/subtract and the result is greater than 4-bits then we get an overflow condition.

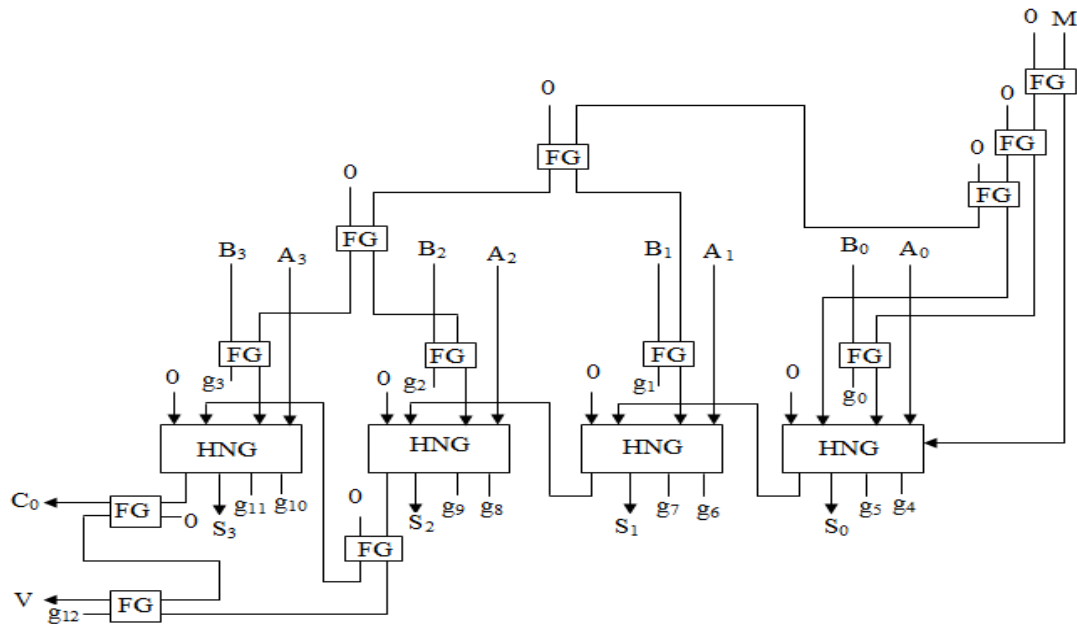


Fig.28. 4-bit Reversible parallel adder/subtractor (with overflow)

BCD ADDER:

If every digit of a decimal number is represented by its corresponding direct binary code, it is recognized as Binary Coded Decimal (BCD).

While we give two 4 bits BCD numbers to the 4 bit adders, the output exceeds the BCD range. When the output of the 4 bit adder is taken directly, then it will be an invalid representation. Therefore it requires some mechanism through which the output of the 4 bit adder can be adjusted into when it is a valid BCD representation.

To adjust the decimal position when it is greater than 1001(decimal 9), a combinational circuit for overflow detection is used in the BCD addition to adjust the decimal position

Overflow-detection algorithm:

The algorithm proposed below has S_1, S_2, S_3 and C_4 are the partial sums received from the parallel adder. Over flow detection bit is $F = (S_1 + S_2) S_3 \oplus C_4$. The expression shows that the resulting circuit contains at least two blocks as shown in Fig.29.

The first block contains S_1 and S_2 i.e. $(S_1 + S_2)$.

The second block contains S_3, C_4 and also output from first block is $(S_1 + S_2)$ i.e. $(S_1 + S_2) S_3 \oplus C_4$.

Therefore the result is $F = (S_1 + S_2) S_3 \oplus C_4$.

If these two carriers $(S_1 + S_2) S_3$ and C_4 are not equal, an overflow occurs.

If these two carriers $(S_1+S_2) S_3$ and C_4 are equal, an overflow does not occurs.

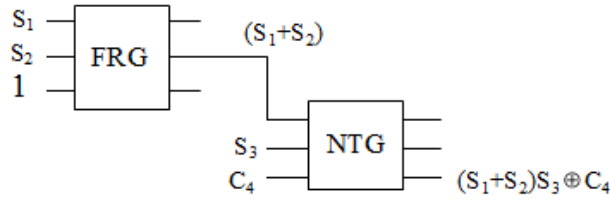


Fig.29. BCD adder's Overflow detection logic

Proposed BCD adder:

Adder adds the two BCD digits. A BCD adder uses a circuit which checks the result at the output of the first adder circuit when the result has exceeded 9 or a carry has been generated when the circuit determines any of the two error conditions that the circuit adds a 6 to the original result using the second Adder circuit. The output of the second Adder gives the correct BCD output. If the circuit finds the result of the first adder circuit to be a valid BCD number (between 0 and 9 no Carry have been generated), the circuit adds a zero to the valid BCD result using the second Adder. The output of the second Adder gives the same result. To The Proposed BCD adder is designed with 2-parallel adders, 5-FG gates, 1-FRG gate, and 1- NTG gate as shown in Fig.30. Then the quantum cost, garbage output, and number of gates required are found to be a minimum. Table-1. Shows that the proposed design is better than the existing reversible BCD adders and also construction is simple.

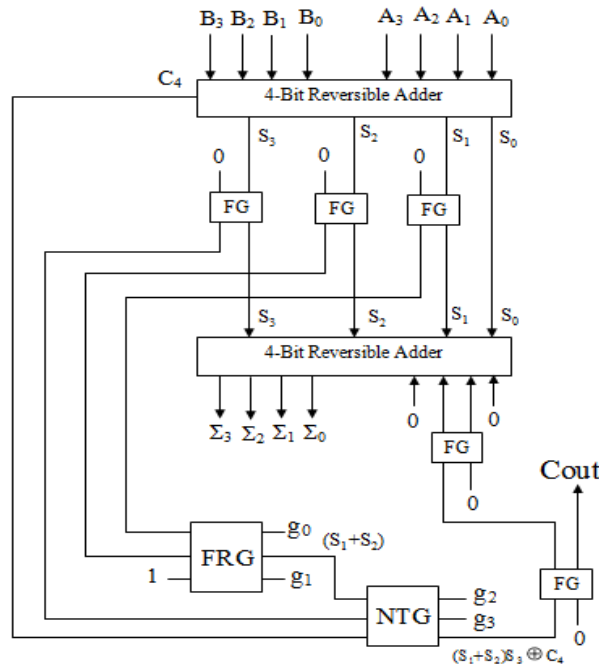


Fig.30. Proposed Reversible BCD Adder

Table-1: Relative Analysis of different reversible BCD adder

Parameters	Existing circuit[35]	Existing circuit[36]	Existing circuit[37]	Existing circuit[20]	Proposed circuit
Number of gates	$19+4FG=23$	$11+5FG=16$	$19+4FG=23$	$11+2FG+1HNFG=14$	$10+5FG=15$
No. of garbage o/p	22	22	22	22	20
Quantum cost	139	Not shown	Not shown	Not shown	62
Total logical calculations	$32\alpha+24\beta+24\delta$	$59\alpha+30\beta+33\delta$	$42\alpha+30\beta+33\delta$	$49\alpha+21\beta+6\delta$	$41\alpha+21\beta+\delta$

CONCLUSION

In this paper, the investigator presented the quantum cost of various reversible logic gates. The quantum cost of TSG gate is 17 which is less than the real quantum cost of TSG designed in references [38, 39]. Reversible computing has enormous potential to reduce the complexity of the digital circuits. Reversible computing has enormous potential to reduce the complexity of the digital circuits. Different reversible logic gates meant for this purpose have been introduced by different types of research. These gates we can be used in design of several combinational or sequential circuits with several advantages over conventional gates. The 4x4 reversible logic gates is HNG gate. HNG gate alone acts as reversible full-adder circuit and it produces two garbage outputs. The proposed reversible BCD adder circuit was designed with minimum quantum cost. This concept can be used in design of large reversible systems as reversible gates which are necessary for quantum computers, because all quantum computers are designed or built with reversible components. The proposed design has all the good features of reversible logic synthesis.

REFERENCES

- [1] R. Keyes, R. Landauer, Minimal energy dissipation in logic, IBM J. Res. Dev. 14(1970) 152–157.
- [2] R. Landauer, Irreversibility and heat generation in the computational process's, IBM J. Res. Dev. 5 (1961) 183–191.
- [3] C.H. Bennett, Logical reversibility of computation, IBM J. Res. Dev. 17 (1973) 525–532.
- [4] V.V. Shende , A.K. Prasad I.L. Markov, J.P. Hayes, Synthesis of reversible logic circuits, IEEE Trans, CAD 22(6) (2003) 723-729.
- [5] M. A. Nielsen and I. L. Chuang, Quantum Computation and Quantum Information. New York: Cambridge Univ. Press (2000).

- [6] V.Vendral, A. Barenco, and A.Ekert, "Quantum networks for elementary arithmetic operations", *Phys. Rev. A*, vol. 54, no. 1, pp. 147-153, Jul1996.
- [7] Perkowski, M. and P. Kerntopf, 2001. Reversible Logic. Invited tutorial, Proc. EURO-MICRO, Sept 2001, Warsaw, Poland.
- [8] H.M.H. Babu, M.R. Islam, A.R. Chowdhury, S.M.A. Chowdhury, Reversible logic synthesis for minimization of full-adder circuit, *IEEE Conf. Digital Syst.Des.(2003)* 50-54.
- [9] H.M.H. Babu, M.R. Islam, A.R. Chowdhury, S.M.A. Chowdhury, Synthesis of full-adder circuit, using reversible logic, in:17th International Conference on VLSI Design, 2004, pp.757-760.
- [10] M. Z. Moghadam, k. Navi, "Ultra- area-efficient reversible multiplier", *Microelectronic.J.* pp. 377-385, 2012.
- [11] Himanshu Thapliyal and Nagarajan Ranganathan, A New Design of The Reversible Subtractor Circuit. 2011 11th IEEE International Conference on Nanotechnology, Portland Marriott, august 15-18, 2011, Portland, Oregon, USA.
- [12] W. N. Hung, X. Song, G. Yang, and M. Perkowski, "Optimal synthesis by multiple output Boolean functions using a set of quantum gates by symbolic reachability analysis", *IEEE Trans. Computer-Aided Design*, vol.25, no.9, pp. 1652-1663, Sept. 2006.
- [13] Matthew Lewandowski, Nagarajan Ranganathan, and Matthew Morrison, 2013. Behavioural Model of Integrated Qubit Gates for Quantum Reversible Logic Design. VLSI(ISVLSI), 2013 IEEE computer society Annual symposium on 5-7 Aug 2013. DOI 10.1109/ISVLSI, 2013. 6654658. Natal, South Africa.
- [14] R.Feynman, Quantum mechanical computers, *Opt. News(1985)* 11-20.
- [15] B. Parhami, "Fault Tolerant reversible circuits", in *Proceedings of 40th Asimolar Conf. Signals, Systems, and Computers*, Pacific Grove, CA, pp.1726-1729,October 2006.
- [16] E. Fredkin, E. Toffoli, Conservative logic, *Int. J. Theor. Phys.*21(1983)219-253.
- [17] T. Toffoli, Reversible computing, Tech memo MIT/LCS/TM-151, MIT Lab for Computer science, 1980.
- [18] A. Peres, Reversible logic and quantum computers, *Phys. Rev.* (1985) 3266-3276.
- [19] M. H.A.Khan, M.A. Perkowski, Logic synthesis with cascades of new reversible gate families, in:6th International Symposium on Representation and Methodology of future Computing Technology(Reed-Muller), March 2003, pp.43-55.

- [20] Majid Haghparast, Keiven Navi. A Novel Reversible BCD adder For Nanotechnology Based systems. American Journal of Applied Sciences 5(3): 282-288, 2008: IISN 1546-9239.
- [21] H. Thapliyal, and A. P. Vinod, "Designing Efficient Online Testable Reversible Adders with New Reversible Gates", proc. ISCAS 2007, New Orleans, USA, May 2007 pp. 1085-1088.
- [22] H. Thapliyal, M.B. Srinivas, A new reversible TSG gate and its application for designing efficient adder circuits, in: 7th International Symposium on Representations and Methodology of Future Computing Technologies, 2005.
- [23] H. Thapliyal, M.B. Srinivas, Novel reversible TSG gate and its application for designing reversible carry look ahead adder and other adder architectures, in: 10th Asia-Pacific Computer Systems Architecture Conference, 2005.
- [24] Md. Mahmudul Hasan, A.K. Biswas, M. Hasan, A.R. Chowdhury, H.M.H. Babu, A novel approach to design BCD adder and Carry Skip BCD adder, in: 21st International Conference on VLSI Design, 4-8 January 2008, pp. 566-571.
- [25] M. S. Islam, M. M. Rahman, Z.bagam, M.Z. Hafiz, "Fault Tolerant Reversible logic synthesis: Carry look-head and carry-skip adders", In Proc. of IEEE International Conference on Advanced in Computational Tools for Engineering Applications , pp. 396-401, July 15-17, 2009.
- [26] Himanshu Thapliyal and Nagarajan Ranganathan, Design of Efficient Reversible Binary Subtractors Based on A New Reversible Gate, IEEE Computer Society Annual Symposium on VLSI.2009
- [27] M. Haghparast and K. Navi, "A.novel fault tolerant reversible gate for nanotechnology based systems", Am.J. of App.sci., vol. 5, no.5, pp. 519-523,2008.
- [28] Nagamini. A. N, Ashwin.S, Vinod Kumar Agrval, "Design of optimized reversible binary adder/subtractor and BCD adder". International Conference on Contemporary Computing and Informatics (IC31). 2014, pp: 774-779, DOI:10.1109/IC31.2014.7019664.
- [29] Dilip P. Vasudevan, Parag K. Lala, Fellow, IEEE, Jia Di, and J. Patrick Parkerson, "Reversible-Logic Design With Online Testability, IEEE Transactions on Instrumentation and Measurement, Vol. 55, No.2, April, 2006.
- [30] X.Susan Christina, M. Sangeetha Justine, K. Rekha, U. Subha and R.Sumathi, "Relization of BCd adder using Reversible Logic", International Journal of Computer Theroy and Engineering, Vol.2, No. 3, June, 2010, 1793-8201.
- [31] M. S. Islam, M. M. Rahman, Z.bagam, M.Z. Hafiz and A.A.Mahmud, "Synthesis of fault tolerant reversible logic circuits", In Proc. IEEE International Conference on Testing and Diagnosis Chengdu, China, 28-29 April, 2009.

- [32] M. S. Islam, Z. Begam, "Reversible logic Synthesis of fault tolerant carry skip BCD adder", Bangladesh Academy of Science Journal, vol.32, no. 2, pp. 193-200, 2008.
- [33] Himanshu Thapliyal and Sumedha K. Gupta, "Design of Noval Reversible Carry Look-ahead BCD Subtractor", 9th International Conference on Information Technology (ICIT'06) 0-7695-2635-7/06, 2006 IEEE.
- [34] M. Shams, M. Haghparast and K.Navi, "Noval Reversible Multiplier Circuit in Nanotechnology", World Applied sci. J., Vol. 3, pp 806-810, 2008.
- [35] H. M. H. Babu, Ahsan Raja Chowdhury, "Design of a Compact reversible Binary coded Decimal adder circuit", Elsevier J. syst. Archit. 52 (2006) 272-282.
- [36] Thapliyal H.S. Kotiyal, M.B. Srinivas, 2006. "Noval BCD adders and their reversible logic implementation for IEEE 754r format. Proceedings of the 19th International Conference on VLSI Design", 3-7 Jan 2006.
- [37] Hasan Babu Hafiz.Md. and Ahsan Raja Chowary, "Design of a reversible binary coded decimal adder by using reversible 4-bit parallel adder". VLSI Design 2005, Kolkata, India, pp 255-260.
- [38] Ashis Kumer Biswas, Md. Mahmudul Hasan, Ahsan Raja Chowdhury, Hafiz. Md. Hasan Babu, "Efficient approaches for desining reversible Binary Coded Decimal adders". Microelectronics Journal 39, 1693-1703 2008.
- [39] Rigui Zhou, Yang Shi, Jian Cao, Hui'an Wang, Comment on "Efficient approaches for desining reversible Binary Coded Decimal adders". Microelectronics Journal 41 (2010) 308-310.