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A Study of On-Chip Stacked Multiloop Spiral Inductors

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***Abstract*—This paper proposes a new differential topology that features a stacked multiloop inductor. Comparative studies of stacked one- to four-loop spiral inductors with and without patterned ground shields (PGSs) for silicon-based radio-frequency integrated circuits (RFICs) were conducted, and lumped-element circuit models were developed for these inductors. The partial-element equivalent-circuit method that can accurately analyze mutual inductive couplings among different spirals in these multiloop geometries was employed for capturing the frequency-dependent inductances and resistances of inductors at low frequencies. A good agreement between numerical results and measurements is obtained. It is demonstrated that a stacked multiloop spiral inductor with differential topology and PGS has a larger inductance and a higher Q-factor as compared with the same inductor without differential topology and PGS. This hybrid methodology could provide a promising technique for developing new silicon-based passive devices used in RFICs.**

***Index Terms*—Differential topology, inductance, partial-element equivalent-circuit (PEEC) method, patterned ground shields (PGSs), Q-factor, resistance, stacked multiloop spiral inductors.**

I. Introduction

In the past decade, CMOS silicon-based spiral inductors have drawn considerable attentions due to their wide applications in radio-frequency integrated circuits (RFICs). With respect to different geometries and layouts of single-spiral inductors, some frequency-dependent and frequency-independent lumped-element circuit models (LECMs) have been developed and further implemented in the design of circuits [1], [2]. For a silicon-based spiral inductor, the conductive loss of all metal tracks and the eddy-current loss in the silicon substrate [3] need to be reduced so as to increase its Q-factor. Differential spiral inductors have been successfully introduced and employed [4] to provide higher Q-factors in differential circuits.

In addition, in order to increase Q-factors, a patterned ground shield (PGS), first proposed in [5], can be implemented between the metal spiral and the silicon substrate [6]. More recently, Cheung and Long [7] studied shielding effects of different PGSs used for silicon-based monolithic microwave and millimeter-wave integrated circuits. The presence of a PGS may cause additional parasitic capacitance, resulting in the reduction of self-resonant frequency of the spiral inductor. Physically, it can be predicted that the combination of the differential topology and PGS technique may be a much better choice for enhancing the performance of most silicon-based passive devices. In circuit designs, on-chip spiral inductors with larger inductance and smaller area are always highly desired, and therefore, two- or multispiral stacked geometries may be considered [8]–[10].

In this paper, differential topology is applied to explore high-performance on-chip stacked multiloop inductors which were designed and fabricated using a 0.18-μm RF CMOS process. It is demonstrated that the differential topologies with PGS can be an efficient solution for enhancing the performance of multiloop inductors with the same structure.

II. Topologies of On-Chip Stacked Multiloop Spiral Inductors

Fig. 1(a) shows the stacked one-loop circular spiral inductor represented by S_1. Based on S_1, the on-chip stacked multiloop spiral inductors can be configured. This geometry is different from that studied in [10], where the central single via is used to connect the top and bottom spirals. According to Fig. 1(a), two- and three-loop circular spiral inductors can be easily formed, as shown in Fig. 1(b)–(e), respectively. We can categorize these geometries into two groups based on the current directions in different spirals. One is the two-directional (2-D) nondifferential ($\mathrm{S}_{2-\mathrm{NDIFF}}$ and $\mathrm{S}_{3-\mathrm{NDIFF}}$) topologies of the single spiral, and another is 2-D differential ($\mathrm{S}_{2-\mathrm{DIFF}}$ and $\mathrm{S}_{3-\mathrm{DIFF}}$) topologies. It must be mentioned that the concept of differential here only indicates the different current flowing directions.

It is evident that the directions of the flowing current shown in Fig. 1(b) and (c) or in Fig. 1(d) and (e) are different. Such differential topology in Fig. 1(c) or (e) can provide higher Q-factor over a broader range of frequencies than that of its nondifferential counterpart. In these topologies, the metal track

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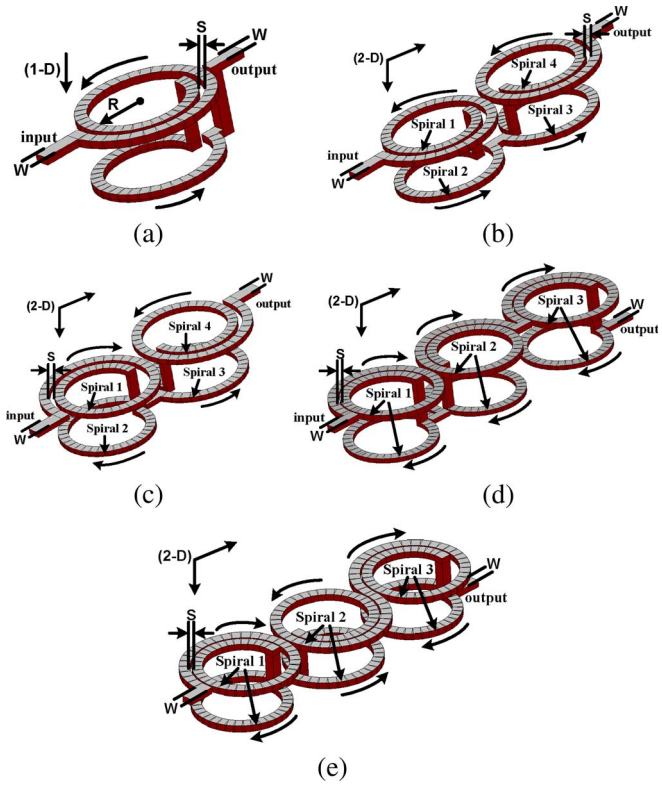

Fig. 1. Two-directional nondifferential and differential topologies of one- to three-loop stacked spiral inductors. (a) S_1. (b) $S_{2-NDIFF}$. (c) S_{2-DIFF}. (d) $S_{3-NDIFF}$. (e) S_{3-DIFF}.

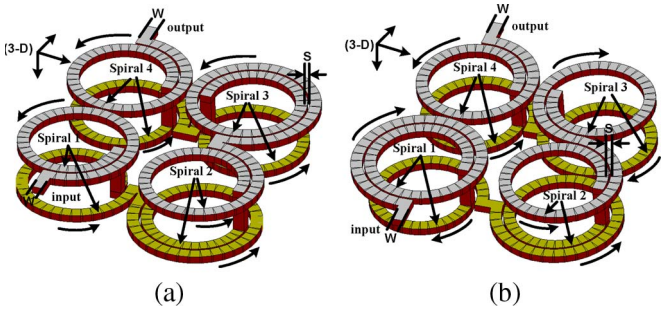

Fig. 2. Three-directional nondifferential and differential topologies of the stacked four-loop spiral inductors. (a) $S_{4-NDIFF}$. (b) S_{4-DIFF}.

width is W, track spacing is S, and inner radius denoted by R is exactly the same. On the other hand, following the similar way as shown in Fig. 1(c) and (e), the two- and three-loop differential topologies of stacked square and octagonal spiral inductors can also be constructed, but their geometries are not shown here.

Furthermore, Fig. 2(a) and (b) shows the three-directional (3-D) nondifferential ($S_{4-NDIFF}$) and differential (S_{4-DIFF}) topologies of stacked four-loop spiral inductors, respectively. The top and bottom spirals are also designed to have the same inner radius (R) as in Fig. 1(a)–(e) earlier. The current direction shown in Fig. 2(b) is just in a reverse direction as in Fig. 2(a), and such unique differential implementation will be useful for the enhancement in its Q-factor, which will be demonstrated experimentally as follows. Table I lists the area information of all the inductors studied.

TABLE I
COMPARISON OF THE AREA OF DIFFERENT INDUCTORS

	S_1	$S_{2\text{-DIFF}}$	$S_{2\text{-NDIFF}}$	$S_{4\text{-DIFF}}$	$S_{4\text{-NDIFF}}$
Area ($mm \times mm$)	0.0154	0.0308	0.0308	0.0616	0.0616

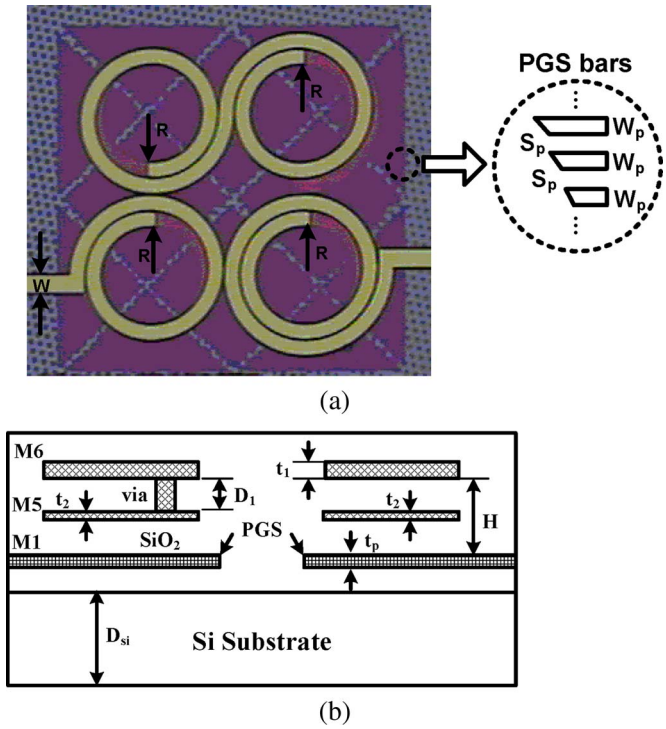

Fig. 3. (a) Top view of the fabricated on-chip stacked four-loop circular differential spiral inductor, where the PGS, bottom, and top spirals are placed at metal layers 1, 5, and 6, respectively. (b) Cross-sectional view of the fabricated samples with a PGS implemented.

The earlier stacked one- to four-loop spiral inductors were designed and fabricated using the 0.18-μm RF CMOS process, as shown in Fig. 3, with $R = 44\ \mu$m, $W = 12\ \mu$m, $S = 2\ \mu$m, $t_1 = 2\ \mu$m, $t_2 = 0.54\ \mu$m, $D_1 = 0.9\ \mu$m, $H = 6.7\ \mu$m, and $D_{si} = 350\ \mu$m. These topologies will suffer from both conductive and substrate losses and, in particular, at high frequencies. Therefore, a PGS, as proposed in [5], [6], and [7], was shown in Fig. 3(a) and (b), so as to reduce the silicon substrate loss. The width of all PGS metal bars (W_p) was designed to be the same as the bar spacing (S_p), i.e., $W_p = S_p = 0.4\ \mu$m.

III. MODELING OF MULTILOOP SPIRAL INDUCTORS

A circuit model is really necessary for us to design an inductor for specific requirements. At first, Fig. 4 shows the LECMs of the on-chip stacked one-loop spiral inductor (S_1) with and without a PGS, respectively. The elements R_{s1}, L_{s1}, R_{s2}, and L_{s2} in the LECMs represent the series resistances and inductances of the top and bottom spirals [1], respectively. The mutual inductance and capacitance between the top and bottom spirals in the LECMs are denoted by M_D^U, $C_{\text{couple 1}}$ and $C_{\text{couple 2}}$. Usually, $C_{\text{couple 1}}$ is much smaller than $C_{\text{couple 2}}$. The mutual inductance and capacitance, which decrease with the separation D_1, need to be calculated numerically. The networks involving C_{oxi}, R_{subi}, C_{PGSi}, and

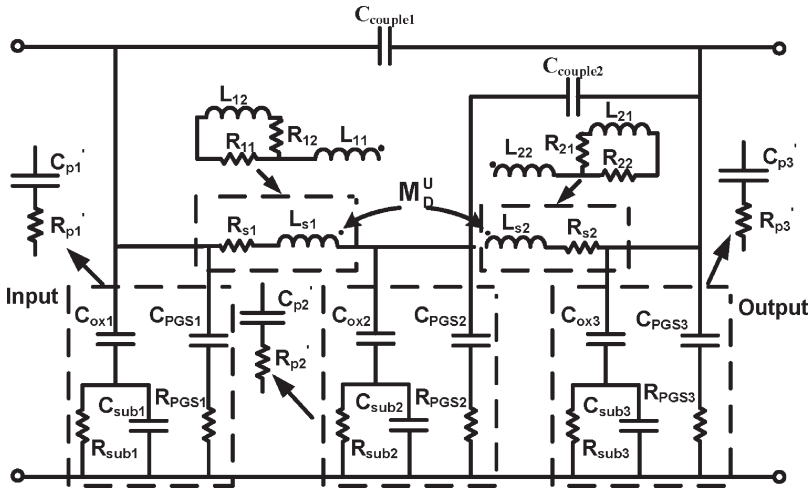

Fig. 4. LECM of the on-chip stacked one-loop spiral inductor (S_1) with a PGS.

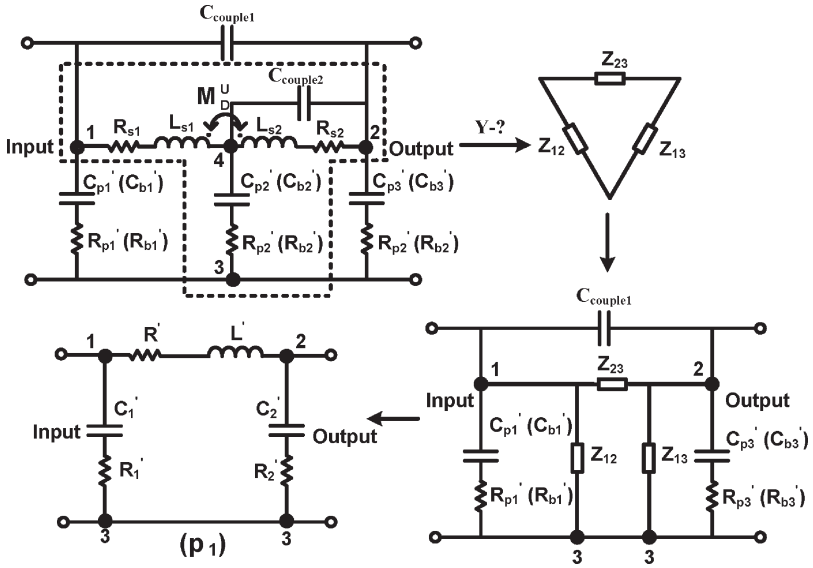

Fig. 5. Simplified π_1 model for the on-chip stacked one-loop spiral inductor (S_1) with or without PGS.

$R_{\mathrm{PGS}i}$ $(i = 1, 2$ and $3)$ in the LECM shown in Fig. 4 can be equivalently replaced by the networks only consisting of resistance R'_{pi} and capacitance C'_{pi}. They are given by

$$R'_{pi} = \frac{C_{\mathrm{oxi}}^2 R_{\mathrm{subi}} + C_{\mathrm{PGS}i}^2 R_{\mathrm{PGS}i}\left[e + (R_{\mathrm{PGS}i} + R_{\mathrm{subi}}) R_{\mathrm{subi}} C_{\mathrm{oxi}}^2 \omega^2\right]}{a + b + C_{\mathrm{oxi}}^2 (c+d)} \tag{1a}$$

$$C'_{pi} = \frac{a + b + C_{\mathrm{oxi}}^2 (c+d)}{a/C_{\mathrm{PGS}i} + f + C_{\mathrm{oxi}}(c + \omega^2 R_{\mathrm{PGS}i}^2 a)} \tag{1b}$$

with

$$a = C_{\mathrm{PGS}i}^2 \left[1 + (\omega C_{\mathrm{subi}} R_{\mathrm{subi}})^2\right] \tag{2a}$$

$$b = 2C_{\mathrm{oxi}} C_{\mathrm{PGS}i}\left[1 + (C_{\mathrm{PGS}i} + C_{\mathrm{subi}}) C_{\mathrm{subi}} R_{\mathrm{subi}}^2 \omega^2\right] \tag{2b}$$

$$c = 1 + (2C_{\mathrm{PGS}i} + C_{\mathrm{subi}}) C_{\mathrm{subi}} R_{\mathrm{subi}}^2 \omega^2 \tag{2c}$$

$$d = C_{\mathrm{PGS}i}^2 \omega^2 \left[(\omega C_{\mathrm{subi}} R_{\mathrm{subi}} R_{\mathrm{PGS}i})^2 + (R_{\mathrm{PGS}i} + R_{\mathrm{subi}})^2\right] \tag{2d}$$

$$e = 1 + (2C_{\mathrm{oxi}} + C_{\mathrm{subi}}) C_{\mathrm{subi}} R_{\mathrm{subi}}^2 \omega^2 \tag{2e}$$

$$f = C_{\mathrm{oxi}}^2 R_{\mathrm{subi}}^2 \omega^2 (C_{\mathrm{PGS}i} + C_{\mathrm{subi}} + C_{\mathrm{subi}} C_{\mathrm{PGS}i}^2 R_{\mathrm{PGS}i}^2 \omega^2). \tag{2f}$$

By taking the shunt branches consisting of $C_{\mathrm{PGS}i}$ and $R_{\mathrm{PGS}i}$ $(i = 1, 2,$ and $3)$ away in Fig. 4, the LECM of the one-loop spiral inductor (S_1) without PGS can be also obtained. Under such circumstances, the networks involving C_{oxi}, R_{subi}, and C_{subi} are equivalently replaced by the shunt branches only consisting of resistance R'_{bi} and capacitance C'_{bi}, and

$$R'_{bi} = \frac{R_{\mathrm{subi}}}{1 + (\omega C_{\mathrm{subi}} R_{\mathrm{subi}})^2} \tag{3a}$$

$$C'_{bi} = \frac{C_{\mathrm{oxi}}\left[1 + (\omega C_{\mathrm{subi}} R_{\mathrm{subi}})^2\right]}{1 + (\omega C_{\mathrm{subi}} R_{\mathrm{subi}})^2 + C_{\mathrm{oxi}} C_{\mathrm{subi}} (\omega R_{\mathrm{subi}})^2}. \tag{3b}$$

Fig. 4 can be simplified to the top-left circuit shown in Fig. 5. Using the $\mathrm{Y}-\Delta$ network transformation, the node 4 in the

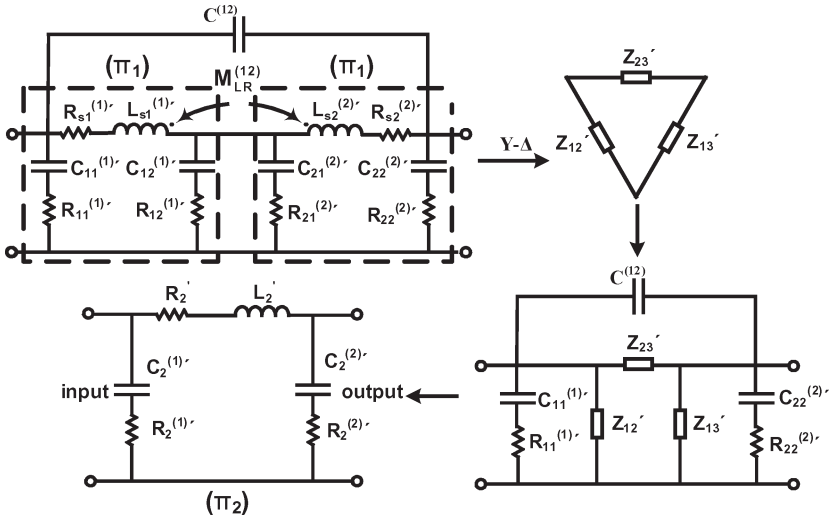

Fig. 6. Simplified π_2 model of the on-chip stacked two-loop spiral inductor with or without PGS.

top-left circuit is eliminated. Its following equivalent circuit is the bottom-right circuit which is transformed to a simplified π-type model denoted by π_1, and

$$R' = \mathrm{Re}\left\{\frac{Z_{23}}{1+j\omega C_{\mathrm{couple}\ 1} Z_{23}}\right\} \tag{4a}$$

$$L' = \frac{1}{\omega}\mathrm{Im}\left\{\frac{Z_{23}}{1+j\omega C_{\mathrm{couple}\ 1} Z_{23}}\right\} \tag{4b}$$

$$R'_1 = \mathrm{Re}\left\{\frac{(1+j\omega C'_{b1}R'_{b1})\,Z_{12}}{1+j\omega C'_{b1}\,(R'_{b1}+Z_{12})}\right\} \tag{4c}$$

$$\frac{1}{C'_1} = -\omega\mathrm{Im}\left\{\frac{(1+j\omega C'_{b1}R'_{b1})\,Z_{12}}{1+j\omega C'_{b1}\,(R'_{b1}+Z_{12})}\right\} \tag{4d}$$

$$R'_2 = \mathrm{Re}\left\{\frac{(1+j\omega C'_{b3}R'_{b3})\,Z_{13}}{1+j\omega C'_{b3}\,(R'_{b3}+Z_{13})}\right\} \tag{4e}$$

$$\frac{1}{C'_2} = -\omega\mathrm{Im}\left\{\frac{(1+j\omega C'_{b3}R'_{b3})\,Z_{13}}{1+j\omega C'_{b3}\,(R'_{b3}+Z_{13})}\right\} \tag{4f}$$

where $\mathrm{Re}\{\}$ and $\mathrm{Im}\{\}$ represent the real and imaginary parts of the variable, respectively, and

$$Z_1 = j\omega\left(M_D^U - \frac{1}{\omega^2 C_{b2}(C_{p2})}\right) + R_{b2}(R_{p2}) \tag{5a}$$

$$Z_2 = j\omega\left(L_{s1} - M_D^U\right) + R_{s1} \tag{5b}$$

$$Z_{12} = Z_1 + Z_2 + Z_1Z_2/Z_3 \tag{5c}$$

$$Z_{23} = Z_2 + Z_3 + Z_2Z_3/Z_1 \tag{5d}$$

$$Z_{13} = Z_1 + Z_3 + Z_1Z_3/Z_2 \tag{5e}$$

$$Z_3 = \frac{j\omega\left(L_{s2} - M_D^U\right) + R_{s2}}{1+j\omega C_{\mathrm{couple}\ 2}R_{s2} - \omega^2 C_{\mathrm{couple}\ 2}\left(L_{s2} - M_D^U\right)}. \tag{5f}$$

The final inductance L and Q-factor of the on-chip stacked one-loop spiral inductor (S_1) can be extracted by

$$L = \mathrm{Im}(1/Y_{11})/\omega \tag{6a}$$

$$Q = \mathrm{Im}\{Z_{11}\}/\mathrm{Re}\{Z_{11}\} \tag{6b}$$

where Y_{11} and Z_{11} can be easily obtained from (5a)–(5f).

Based on the model development for the one-loop geometry, one can further construct the LECM and transform it into a simplified π-type model for the on-chip stacked multiloop spiral inductor. Fig. 6 shows the LECM of two-loop geometry together with its simplified π-type model denoted by π_2. In its building, the elements of $\{R_{s1}^{(1)'}, L_{s1}^{(1')}, C_{11}^{(1)'}, C_{12}^{(1)'}, R_{11}^{(1)'}, R_{12}^{(1)'}\}$ and $\{R_{s2}^{(2)'}, L_{s2}^{(2')}, C_{21}^{(2)'}, C_{22}^{(2)'}, R_{21}^{(2)'}, R_{22}^{(2)'}\}$ are determined according to (5a)–(5f), where we have the following conditions.

1) $\{R_{s1}^{(1)'}, L_{s1}^{(1)'}\}$ and $\{R_{s2}^{(2)'}, L_{s2}^{(2)'}\}$ represent the series resistances and inductances of each loop (S_1) in the $\mathrm{S}_{2-\mathrm{DIFF}}$ [Fig. 1(c)], corresponding to $\{R', L'\}$ in Fig. 5, respectively.
2) $\{R_{11}^{(1)'}, C_{11}^{(1)'}, R_{12}^{(1)'}, C_{12}^{(1)'}\}$ and $\{R_{21}^{(2)'}, C_{21}^{(2)'}, R_{22}^{(2)'}, C_{22}^{(2)'}\}$ account for the hybrid lossy effects and capacitive coupling in the double-layer substrate, corresponding to $\{R'_1, C'_1, R'_2, C'_2\}$ in Fig. 5, respectively; $M_{LR}^{(12)}$ and $C^{(12)}$ are added to account for the magnetic and electric couplings between two adjacent loops.

Fig. 7 shows the equivalent LECM of the on-chip stacked four-loop spiral inductor and its simplified π_4 model, where we have the following conditions.

1) $\{R_{s12}^{(1)}, L_{s12}^{(1)}\}$ and $\{R_{s34}^{(2)}, L_{s34}^{(2)}\}$ are obtained based on the derived $\{R'_2, L'_2\}$ in the π_2 model in Fig. 6, respectively.
2) $\{R_{12}^{(1)}, C_{12}^{(1)}, R_{12}^{(2)}, C_{12}^{(2)}\}$ and $\{R_{34}^{(1)}, C_{34}^{(1)}, R_{34}^{(2)}, C_{34}^{(2)}\}$ are obtained according to the elements $\{R_2^{(1)'}, C_2^{(1)'}, R_2^{(2)'}, C_2^{(2)'}\}$, respectively.
3) $M_{(12)}^{(34)}$ and $C_{(12)}^{(34)}$ are added to account for the magnetic and electric couplings among four loops, and their values can be only calculated numerically.

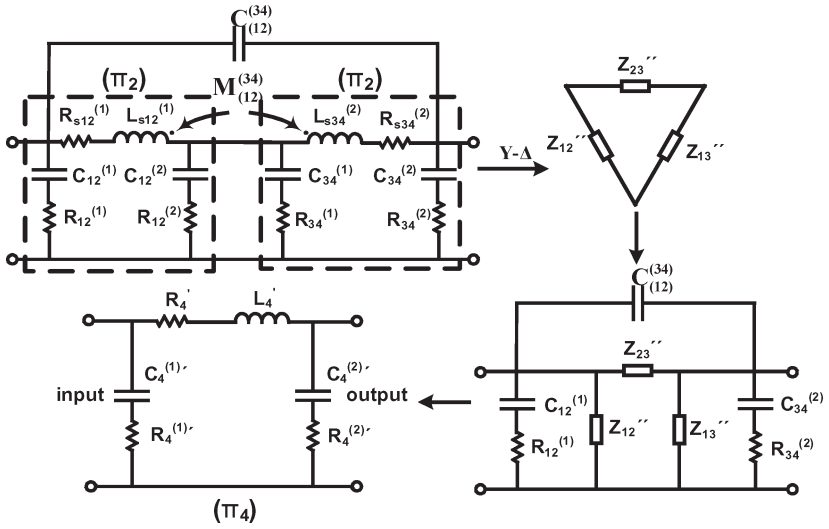

Fig. 7. Simplified π_4 model of the on-chip stacked four-loop spiral inductor with or without PGS.

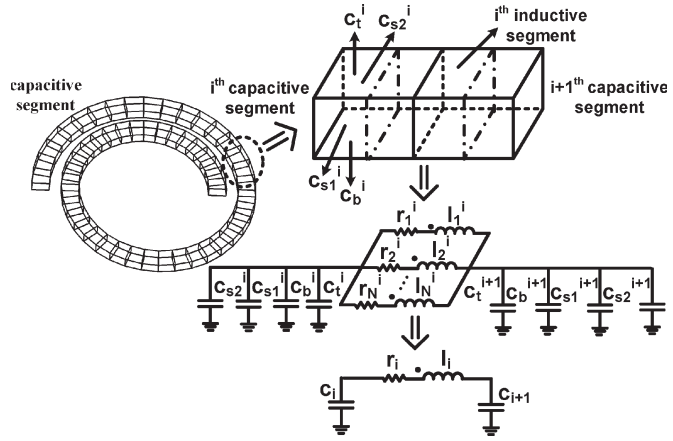

Fig. 8. Capacitive and inductive cells of a circular spiral; and the equivalent PEEC model consisting of an inductive and two capacitive cells.

IV. Numerical Implementation of the PEEC Method

The overall inductance of a single-spiral inductor can be determined using closed-form formula [11]. However, for the on-chip stacked one- to four-loop spiral inductors, no closed-form formulas are available to calculate their inductances or resistances, which will be calculated using the partial-element equivalent-circuit (PEEC) method [12]. The PEEC method is a numerical approach that divides metallic structures into a set of small segments and, then, solves the equation in a discrete manner. The equivalent PEEC model of two adjacent segments is shown in Fig. 8. In its implementation, some key points are explained as follows.

1) The circular spiral is treated as a regular polygon consisting of S hexahedron segments with the finite thickness and the finite conductivity. In order to get the balance between numerical accuracy and computational efficiency, the maximum segment numbers $(S_{\max})$ must be chosen appropriately.
2) Each quadrangle segment is divided into T filaments, and each filament is turned into a branch of series interconnect consisting of self-inductance l_{ij} and self-resistance r_{ij} $\{i = 1, \ldots, S_{\max}; j = 1, \ldots, T_{\max}\}$. The mutual inductances among different filaments are represented by M_{ij}.
3) Single inductive cell is divided into $\{12, 2\}$ filaments, i.e., $T_{\max} = 24$, which is validated as an appropriate number in the next part. The partial inductance between two hexahedral segments with an arbitrary orientation is calculated using the method as described in [13].
4) We notice that a capacitive-cell model is proposed in [14] to calculate the capacitance of some passive RF devices with finite metal thickness. Therefore, we extend it to be applicable for each segment with four surfaces. In Fig. 8, the capacitances C_t^i, C_b^i, C_{s1}^i, and C_{s2}^i represent the top-, bottom-, and side-surface capacitances of the ith segment, respectively.

According to the Ohm's law, the voltages and currents of all segments are expressed by

$$\begin{bmatrix} \mathbf{V}_1 \\ \mathbf{V}_2 \\ \vdots \\ \mathbf{V}_{\mathrm{S}} \end{bmatrix} = \begin{bmatrix} \mathbf{Z}_{11} & \mathbf{Z}_{12} & \cdots & \mathbf{Z}_{1\mathrm{S}} \\ \mathbf{Z}_{21} & \mathbf{Z}_{22} & \cdots & \mathbf{Z}_{2\mathrm{S}} \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{Z}_{\mathrm{S}1} & \mathbf{Z}_{\mathrm{S}2} & \cdots & \mathbf{Z}_{\mathrm{SS}} \end{bmatrix} \begin{bmatrix} \mathbf{I}_1 \\ \mathbf{I}_2 \\ \vdots \\ \mathbf{I}_{\mathrm{S}} \end{bmatrix} \tag{7}$$

where the T-dimensional vector $\mathbf{V_i}$ and $\mathbf{I_i}$ represent the voltage and current of the filaments in the ith segment; $\mathbf{Z_{ij}}$ is a $T \times T$ impedance matrix and given by

$$\mathbf{Z}_{\mathrm{ij}}(p,q) = \begin{cases} r_p^i + j\omega l_p^i, & (\mathrm{i} = \mathrm{j},\ \mathrm{p} = \mathrm{q}) \\ j\omega M_{pq}^{ij}, & \text{otherwise} \end{cases}$$
$$(1 \le p, q \le T_{\max}; 1 \le i, j \le S_{\max}) \tag{8}$$

where r_p^i and l_p^i represent the inductance and resistance of the pth filament in the ith segment, respectively; while M_{pq}^{ij} stands for the mutual inductance between the pth filament in the ith

segment and the qth filament in the jth segment. Equation (7) can be converted into

$$\begin{bmatrix}\mathbf{I}_1\\ \mathbf{I}_2\\ \vdots\\ \mathbf{I}_{\rm S}\end{bmatrix} = \begin{bmatrix}\mathbf{Z}_{11} & \mathbf{Z}_{12} & \cdots & \mathbf{Z}_{1{\rm S}}\\ \mathbf{Z}_{21} & \mathbf{Z}_{22} & \cdots & \mathbf{Z}_{2{\rm S}}\\ \vdots & \vdots & \ddots & \vdots\\ \mathbf{Z}_{{\rm S}1} & \mathbf{Z}_{{\rm S}2} & \cdots & \mathbf{Z}_{{\rm SS}}\end{bmatrix}^{-1}\begin{bmatrix}\mathbf{V}_1\\ \mathbf{V}_2\\ \vdots\\ \mathbf{V}_{\rm S}\end{bmatrix}$$

$$\equiv \begin{bmatrix}\mathbf{Y}_{11} & \mathbf{Y}_{12} & \cdots & \mathbf{Y}_{1{\rm S}}\\ \mathbf{Y}_{21} & \mathbf{Y}_{22} & \cdots & \mathbf{Y}_{2{\rm S}}\\ \vdots & \vdots & \ddots & \vdots\\ \mathbf{Y}_{{\rm S}1} & \mathbf{Y}_{{\rm S}2} & \cdots & \mathbf{Y}_{{\rm SS}}\end{bmatrix}\begin{bmatrix}\mathbf{V}_1\\ \mathbf{V}_2\\ \vdots\\ \mathbf{V}_{\rm S}\end{bmatrix}. \quad (9)$$

For each branch, we have

$$V_i = \mathbf{V}_{\rm i}(p) \quad (10a)$$

$$I_i = \sum_{p=1}^{T_{\max}} \mathbf{I}_{\rm i}(p) \quad (10b)$$

where V_i and I_i denote the voltage and current of the ith segment, respectively. Therefore, we further have

$$\begin{bmatrix}I_1\\ I_2\\ \vdots\\ I_S\end{bmatrix} = \begin{bmatrix}Y_{11} & Y_{12} & \cdots & Y_{1S}\\ Y_{21} & Y_{22} & \cdots & Y_{2S}\\ \vdots & \vdots & \ddots & \vdots\\ Y_{S1} & Y_{S2} & \cdots & Y_{SS}\end{bmatrix}\begin{bmatrix}V_1\\ V_2\\ \vdots\\ V_S\end{bmatrix} \quad (11)$$

$$Y_{ij} = \sum_{p=1}^{T_{\max}}\sum_{q=1}^{T_{\max}} \mathbf{Y}_{\rm ij}(p,q). \quad (12)$$

From (11), we can obtain all elements in the [**Z**]-matrix. The series resistance and inductance are thus calculated by

$$R_s = {\rm Re}\left\{\sum_{i=1}^{S_{\max}}\sum_{j=1}^{S_{\max}} Z_{ij}\right\} \quad (13a)$$

$$L_s = \frac{1}{\omega}{\rm Im}\left\{\sum_{i=1}^{S_{\max}}\sum_{j=1}^{S_{\max}} Z_{ij}\right\}. \quad (13b)$$

The mutual inductive coupling plays an important role in the enhancement of the total inductance earlier. Taking the four-loop geometry as an example, each spiral is divided into $S_{\max}$ segments. Thus, the mutual inductance between spirals p and q ($p, q = 1, 2, 3, 4$, and $p \neq q$) can be calculated by

$$M_{pq} = \frac{1}{\omega}{\rm Im}\left\{\sum_{i=1+(p-1)S_{\max}}^{pS_{\max}}\ \sum_{j=1+(q-1)S_{\max}}^{qS_{\max}} Z_{ij}\right\}. \quad (14)$$

To check the effectiveness of the earlier modified PEEC method, we developed a program to compute the performance parameters of multiloop stacked spiral inductors. At first, Fig. 9 shows the comparisons between the simulated and measured inductances and Q-factors of the geometries in Fig. 1(a)–(e), respectively. It is shown that good agreements are obtained for these parameters. Furthermore, we have

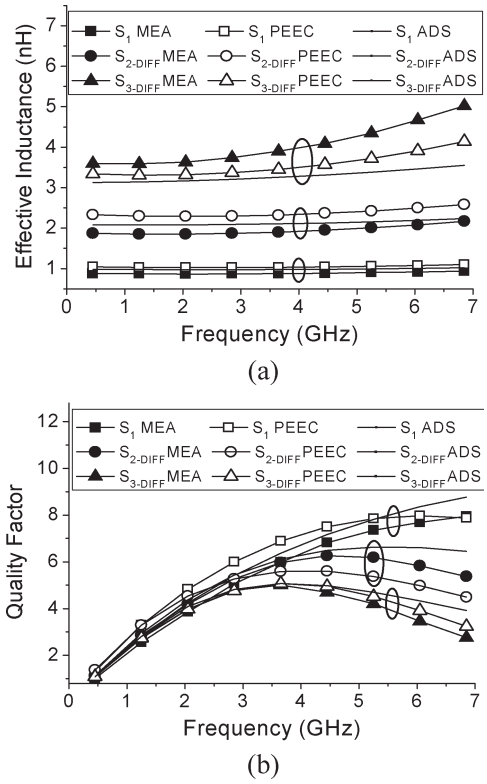

Fig. 9. Comparison in the simulated and measured frequency responses of stacked multiloop inductors. (a) Inductance. (b) Q-factor.

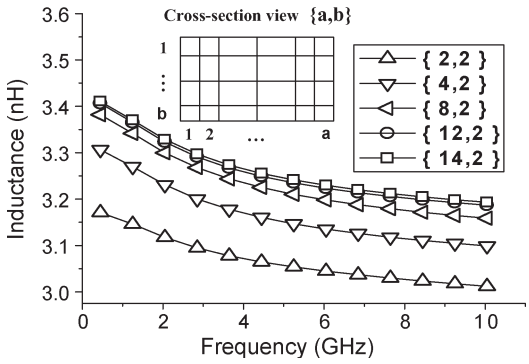

Fig. 10. Frequency-dependent series inductances of $\rm S_{3-DIFF}$ with different filaments chosen.

checked the convergence in the segmentation of all spirals, and Fig. 10 shows the frequency-dependent inductance of $\rm S_{3-DIFF}$ but with different number of the filaments of $\{a, b\} = \{2, 2\}, \{4, 2\}, \{8, 2\}, \{12, 2\}$, and $\{14, 2\}$ in the segmentation of the spirals, respectively. It is shown that fast convergence is obtained in the computed series inductance of $\rm S_{3-DIFF}$ as $\{a, b\}$ is increased from $\{12, 2\}$ and $\{14, 2\}$, respectively.

The current density distribution within the cross section of metal track at a given frequency can be described by a depth-dependent exponential function, which is approximated by a staircase function in the PEEC method instead. Therefore, the error between the exponential and the approximation of staircase function will be reduced. Correspondingly, the approximated current distribution will be more accurate when

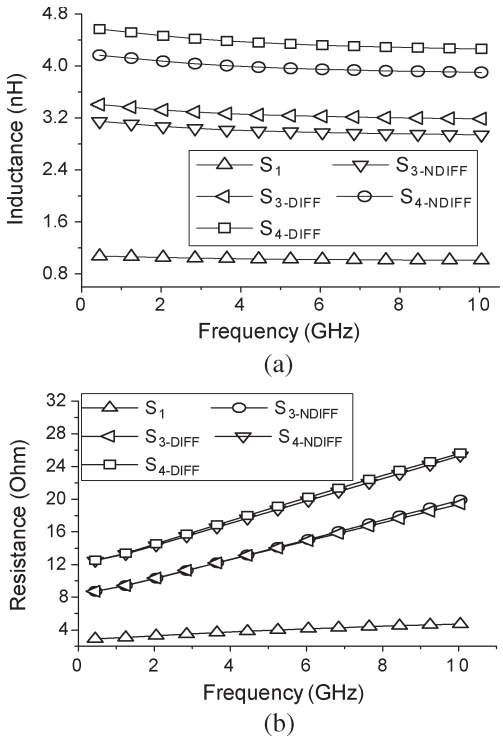

Fig. 11. Frequency-dependent inductances and resistances of the topologies S_1, $S_{3-(N)DIFF}$, and $S_{4-(N)DIFF}$ without a PGS implemented, respectively. (a) Inductances. (b) Resistances.

more filaments segmented are meshed. In our numerical computations, we keep $\{a, b\} = \{12, 2\}$ so as to capture frequency-dependent inductance and resistance of the multiloop stacked spiral inductors, as shown in Figs. 11–13 as follows.

Fig. 11 shows a comparison of the computed inductances and resistances as a function of frequency for the on-chip stacked one-, three-, and four-loop spiral inductors without PGS, respectively, and some phenomena can be observed.

1) The inductance increases with the loop number and so does the resistance. As expected, the inductances of the three- and four-loop geometries are three and four times larger than their one-loop counterpart.
2) Due to the skin effect, the inductance decreases with frequency slightly. However, the resistance increases with frequency significantly and, in particular, for the four-loop geometry.
3) The S_{4-DIFF} has the largest inductance among the five studied geometries, and the relative increase in inductance is defined by

$$RE^{(L)}_{(n)\text{diff}} = (L_{\text{diff}} - L_{\text{ndiff}})/L_{\text{ndiff}} \times 100\% \qquad (15)$$

where $RE^{(L)}_{(n)\text{diff}} = 8.26\%$ for S_{3-DIFF} and 9.55% for S_{4-DIFF} at 2.85 GHz, respectively. Most of the mutual inductances between different spirals in Figs. 1 and 2 are negative in nondifferential type, such as M_{S1-S2} and M_{S3-S4}; while they are positive in differential inductors, such as M_{S1-S2}, M_{S1-S3}, and M_{S1-S4}. Although some of the mutual inductances are positive in nondifferential type and negative in differential type, the values of these inductive coupling are smaller than those dominant mutual inductances. It leads the total inductances of the differential inductors larger than those of nondifferential counterparts.

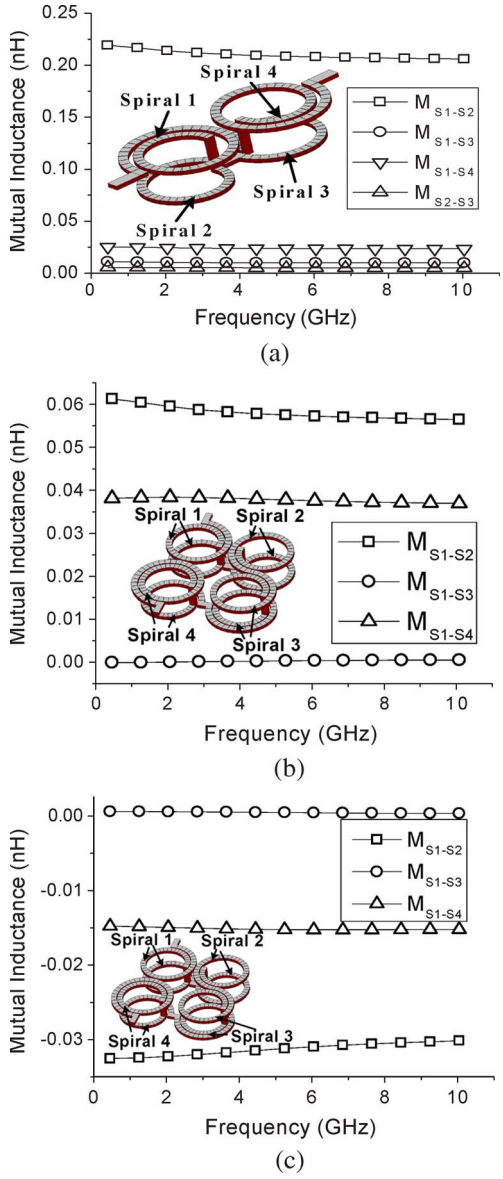

Fig. 12. Mutual inductances between different spiral partners in S_{2-DIFF}, S_{4-DIFF}, and $S_{4-NDIFF}$ versus frequency.

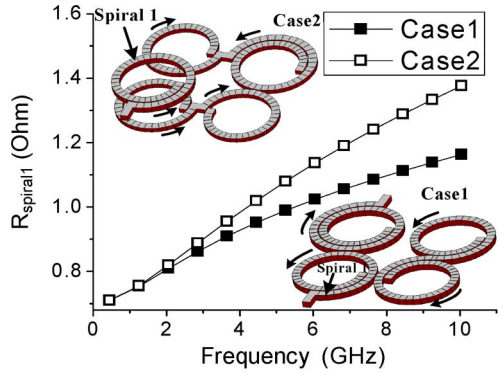

Fig. 13. Effects of proximity effect on the series resistance of single spiral.

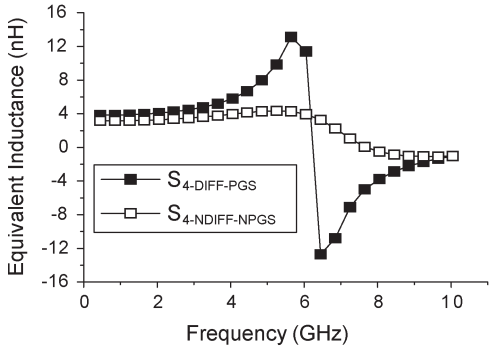

Fig. 14. Experimentally extracted equivalent inductance as a function of frequency for topologies of $S_{4-DIFF}^{(PGS)}$ and $S_{4-NDIFF}^{(NPGS)}$.

4) There is very little difference in the computed resistance between S_{3-DIFF} and $S_{3-NDIFF}$ or between S_{4-DIFF} and $S_{4-NDIFF}$ over a wide frequency range, because the overall metal-track length in the differential topology is nearly the same as that in its nondifferential counterpart.

Fig. 12(a) and (b) shows the computed mutual inductances between different spiral partners in S_{2-DIFF} and S_{4-DIFF}, respectively, where M_{Si-Sj} represents the mutual inductance between the spirals (i = 1 and 2) and (j = 3 and 4), as shown in Fig. 12. It is obvious that the mutual inductance between spirals one and two is much larger than those of other cases [Fig. 12(a)].

Fig. 13 shows the proximity effects on the frequency-dependent series resistance of single spiral denoted by Spiral 1 with neighborhoods of three spirals in Case 1 and four spirals in Case 2, respectively. The spirals are not physically connected in the inlets in Fig. 13. The arrows represent the fictitious current direction which are independent in different spirals.

It is evident that proximity effects on the series resistance cannot be excluded at high frequencies, and the relative increase in series resistance between Cases 1 and 2 is defined by

$$RE_R = (R_{\text{case 2}} - R_{\text{case 1}})/R_{\text{case 1}} \times 100\% \qquad (16)$$

where $RE_R = 9.15\%$ at $f = 4.85$ GHz and 18.39% at $f =$ 10.05 GHz approximately. With the increase in frequency, the proximity effect on the series resistance in Case 2 will be much more significant than that in Case 1. The main reason is that the mutual magnetic coupling between the vertically neighboring spirals is much larger than that between the laterally neighboring spirals. In Fig. 12(a), the mutual inductance between vertically neighboring spirals M_{S1-S2} is around ten times larger than those between lateral neighboring spirals, such as M_{S1-S4} and M_{S2-S3} in all frequencies. The more significant the mutual inductive coupling is, the more dominant the proximity effect will be.

V. Experimental Results and Discussions

As shown in Section II, several on-chip multiloop stacked inductors with and without a PGS were designed and fabricated. Measurements of their two-port S-parameters were carried out so as to capture their performance parameters, with an equivalent inductance and Q-factor extracted using (6a) and (6b), respectively. Fig. 14 shows the extracted inductance of

TABLE II
Comparison of the Maximum Q-Factors of Different Topologies With and Without a PGS, Respectively

	Maximum Q (no PGS)	Maximum Q (with a PGS at M1)	$I_Q^{(PGS)}$ (%)
S_1	8.06	10.40	29.03
$S_{2\text{-DIFF}}$	6.27	6.94	10.69
$S_{2\text{-NDIFF}}$	5.98	6.80	13.71
$S_{4\text{-DIFF}}$	3.59	4.39	22.28
$S_{4\text{-NDIFF}}$	3.19	3.66	14.73

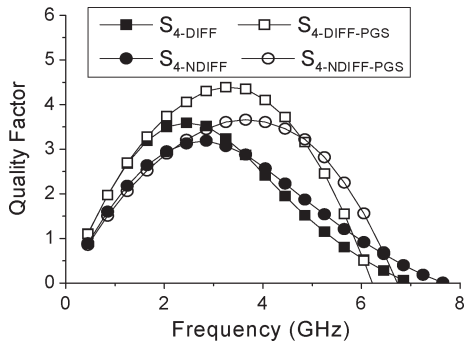

Fig. 15. Comparisons of the measured Q-factors versus frequency among different topologies with PGS and without PGS, respectively.

the topologies of $S_{4-DIFF}^{(PGS)}$ and $S_{4-NDIFF}^{(NPGS)}$, respectively. It is shown that the differential topology with a PGS implemented is effective for the increase in inductance. On the other hand, it is noted that its implementation will result in the decrease in self-resonance frequency of the spiral inductor slightly as a PGS will produce additional capacitive coupling between metal spirals and silicon substrate.

Table II shows the comparison of the maximum Q-factors for four pairs of nondifferential and differential topologies with and without a PGS, respectively, and the S_1 case is also included. The relative increase in the maximum Q-factor is defined by a set of equations as follows:

$$I_Q^{(\text{DIFF})} = \left[Q_{\max}^{(\text{DIFF})} - Q_{\max}^{(\text{NDIFF})}\right] \Big/ Q_{\max}^{(\text{NDIFF})} \times 100\% \qquad (17a)$$

$$I_Q^{(\text{PGS})} = \left[Q_{\max}^{(\text{PGS})} - Q_{\max}^{(\text{NPGS})}\right] \Big/ Q_{\max}^{(\text{PGS})} \times 100\%. \qquad (17b)$$

It is indicated that differential topology is also an effective way to enhance the Q-factor of a silicon-based inductor. For example, even for the case of no PGS implemented, $I_Q^{(\text{DIFF})} = 3.68\%$ for S_{3-DIFF} as compared with its counterpart $S_{3-NDIFF}$; and 12.5% for S_{4-DIFF} as compared with its counterpart $S_{4-NDIFF}$. Furthermore, when we have combined differential topology with a PGS, such as in $S_{4-DIFF}^{(PGS)}$, the enhancement in its maximum of the Q-factor is very significant, as shown in Fig. 15.

The negative effect caused by a PGS is mainly due to additional capacitive coupling. When the PGS is closer to the inductor, the loss effect is alleviated while the resonant frequency is lower. Therefore, its embedding depth in the silicon-oxide layer should be chosen appropriately.

VI. Conclusion

New differential multiloop topologies that features stacked structure were proposed first. A comparative study on one- to four-loop inductors with and without PGSs were conducted in this paper. To handle these multiloop stacked configurations, LECMs were developed for enhancing our analysis. Furthermore, PEEC method was employed for predicting the frequency-dependent inductances and resistances of these inductors. Good agreements between numerical results and on-chip measurements were observed. They showed that a differential multiloop stacked spiral inductor with a PGS can increase the inductance and Q-factor significantly and only reduce self-resonant frequency slightly. Therefore, the proposed differential multiloop stacked spiral inductors are very suitable for the design of RFICs with high quality.

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