A Study of Reduced-Terminal Models for System-Level SSO Noise Analysis

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***Abstract*—SSO noise modeling imposes significant challenges in signal integrity analysis as it requires a complex model which represents numerous signal, power, and ground conductors and planes. Even with effective macros modeling techniques, the resulting model is still complex due to a large number of external nodes which often represent data, power, and ground pins or pads. This paper discusses several options to reduce the number of external nodes for SSO simulation. Both signal and power nodes are reduced based on the worst case aggressor switching activities. Significance of placing supernode in reduction of signal nodes is discussed. Low power memory system is considered as a numerical example to demonstrate and compare the accuracy of each option.**

Keywords–signal intergrity;power integrity;SSO analysis; worst case analysis; model reduction

I. INTRODUCTION

The data rate of digital interface continues to increase. At high data rates over Gbps range, simultaneous switching output (SSO) noise introduced by output drivers is one of the major bottlenecks in the design of high speed channels [1]. Current peaks generated by simultaneously switching signals could result in a large amount of SSO noise when the impedance of the power distribution system is not sufficiently low.

Accurate simulation of SSO noise is quite challenging due to modeling complexity. On top of modeling many drivers and receivers, any nonlinearity of the output driver also needs to be modeled accurately, requiring a full transistor driver model. On the other hand, a need for small-form factor for mobile applications magnifies the impact of 3D power noise coupling in addition to the lack of a reliable power distribution network (PDN) due to limited space. Because of a large number of I/Os and complexity of design in such 3D package systems, SSO noise simulation for such systems introduces a remarkable challenge. For efficient channel analysis for these complex systems, it is highly desirable to reduce the channel model complexity.

Many methods have been introduced to reduce the complexity of the model. Macro modeling has been used widely to reduce the complexity of internal circuit representation [2, 3]. However, due to the large number of I/Os in 3D package systems, the reduction of internal complexity is not enough to efficiently simulate SSO noise of the system.

In this paper, a methodology for reducing even the external nodes of a channel model is discussed to save the simulation running time without compromising accuracy. In particular, equi-potential nodes such as common power and grounds can be merged into one representative node so that the number of external ports can be reduced. Further reduction is possible in the worst case SSO simulation by merging aggressor nodes into one representative supernode that have the same data pattern in the worst case scenario.

II. SI AND PI CO-SIMULATION METHODOLOGY

Analysis of the system-level margin degradation from power supply noise requires not only accurate power distribution network (PDN) model but also accurate current profiles exciting the network. For such accurate current profile, inclusion of accurate transistor-level transmitter and receiver models is desirable. At the same time, signal integrity (SI) and power integrity (PI) co-simulation enables us to model the coupling between signal and supply nets. However, it is very challenging to simulate the entire system with transistor-level driver and receiver models due to the vast computing resource requirement.

In this section, an SI and PI co-simulation methodology presented in [4, 5] is briefly reviewed using an x32 graphic memory system (GDDR) as a demonstration vehicle. Fig. 1 shows the flow of the overall methodology. First, a distributed RLGC models of PDN for PCB and package is generated. By reducing the number of internal nodes and merging the same power nets at the external nodes, the RLGC model is simplified to find an equivalent S-parameter model. S-parameter modeling and simulation have become standard features for modern simulation tools. SSO noise is severe for wirebond packages due to high inductance values. For such systems, using an equivalent RLGC matrix instead of complex S-parameter matrix can reduce the complexity of the model. The equivalent matrix can be obtained by approximating the S-parameter using a transmission line parameter [6].

Next, the PDN model for PCB and package is combined with on-chip power distribution model. The combined

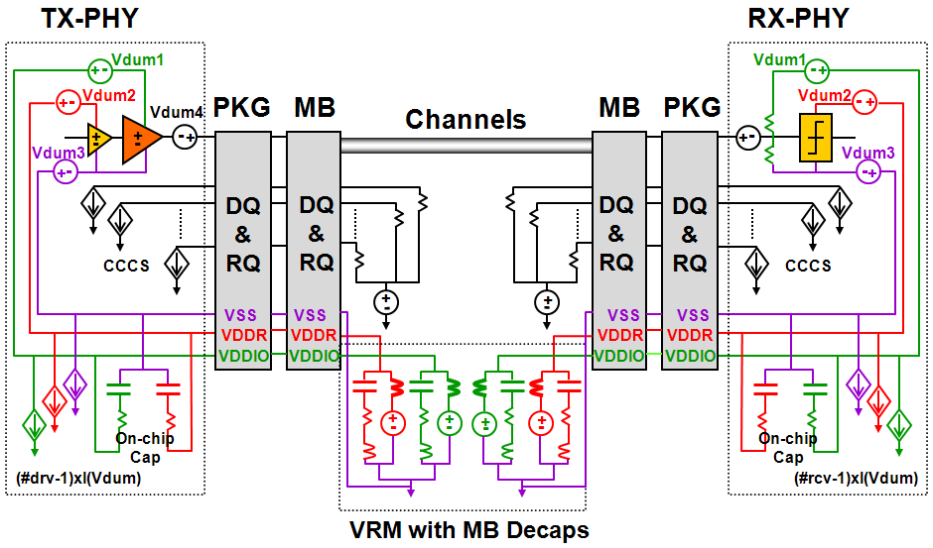


Figure 1. Efficient channel modeling for SI and PI co-simulation using current mirrors.

PDN model is merged with a channel model for signals. The package PDN should be modeled using a 3D EM solver including both power and signal nets in order to capture interaction between power and signal within a package accurately; as a result, the model can represent an accurate return path during pull-on and pull-down switching. On the other hand, PDN and channel models for PCB motherboard and on-chip trace can be built separately. The signal traces on PCB are usually modeled as transmission lines using a 2D field solver whereas other components such as vias and escape lines are modeled using a 3D EM solver. Finally, driver and receiver models are added. A small number of accurate transistor-level driver models are combined with current-controlled current sources in order to simulate accurate signal waveforms while maintaining the low complexity of the overall system model [4, 5].

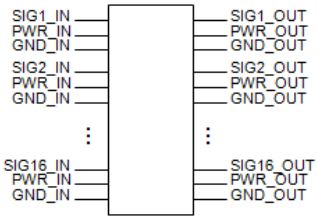
To avoid the excessive running time in simulation of the worst case noise excitation, a new simulation methodology is proposed in [5]. In the new approach, an independent simulation is done at the package resonance frequency to capture the impact of SSO noise. The voltage margin loss, obtained from this simulation, is then characterized as an additional input voltage requirement at the receiver on top of the conventional voltage requirement due to sampler sensitivity and power noise. Consequently, the effective input voltage requirement becomes a function of system configurations.

III. Merging Common Power, Ground, and Aggressor Signal Lines

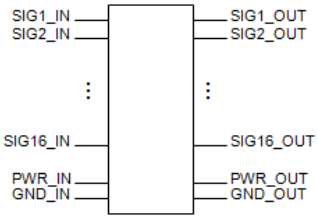
For the further reduction of complexity of channel model, while internal nodes are simplified by macro-modeling approach, decreasing the number of external ports leads to considerable reduction of model complexity. The concept of merging equi-potential external nodes was first described in [7, 8]. When ports are eligible to be assumed as equi-potential nodes, they can be merged into one representative port. As each common power and ground node is almost equi-potential, it can be merged into one as shown in Fig. 2 (b).

Additional reduction of the number of external ports can be made by merging signal lines if they are assumed to have the same data pattern. In SI and PI analysis, the worst case system performance with the worst case SSO noise is the main interest and, in such cases, we can assume that all aggressors have the same data pattern. Therefore, a number of ports for aggressor signal lines with the same data pattern can be merged in the worst case analysis. This will be discussed in detail in Section IV.

While model's external ports are merged and simplified, its internal model also needs to be simplified accordingly by simulation of the original model with merged ports. If the length of channel is sufficiently short compared to the wave length of signal's bandwidth, the RLGC model may be a suitable simplified model for the channel with merged



(a) Original model



(b) Reduced model

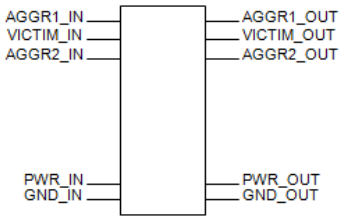
Figure 2. Reduction of external ports

external ports. However, if it is not, a cascaded model or a general model such as s-parameter are required for accurate modeling of the channel with merged ports.

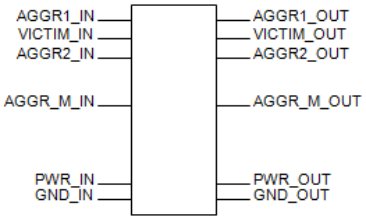
As mentioned in Section II, drivers can be replaced by current-controlled current sources to reduce the complexity in the SI/PI simulation. When dealing with a model with reduced external ports, the current source needs to be adjusted accordingly. For example, when *n* ports are merged into one representative port, the amount of current flowing into the one representative port should be multiplied by *n*. In particular, when signal nodes are merged, controlled current sources should be added not only to signal node itself but also power and ground nodes accordingly.

IV. Reduction of Aggressor Lines in Worst Case Analysis

In a typical SI analysis, a few adjacent aggressor lines to the victim line play a major role in deteriorating signal integrity on the victim line by causing crosstalk. To add SSO impact to the SI analysis, many other aggressors except the adjacent aggressor lines to the victim line can have the same data pattern generating large SSO noise for the worst case. However, after power and ground ports are merged, shown in Fig. 2(a) and (b), the impact of the SSO noise from the signal lines not included in the SI model will be missed as shown Fig. 3(a). In this approximation, signal current for the ignored aggressor lines is missed while return current for the ignored aggressors are still flowing through the merged power and ground. This approximation is unrealistic and violates Kirchhoff's current law. It results in an inaccuracy in estimating noise coupling between signal lines and supply nets as well as SSO noise impact at IO driver power supply.

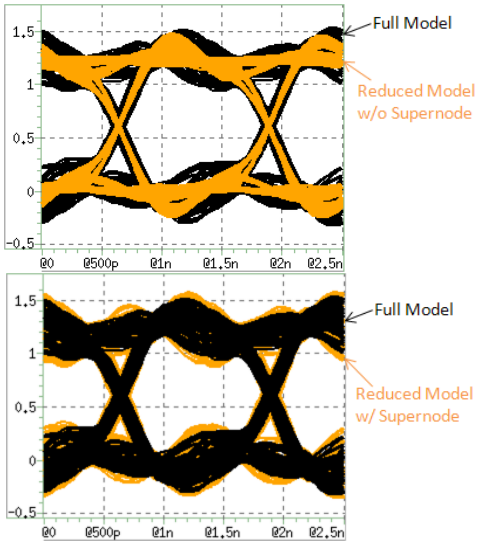


(a) Common mistake

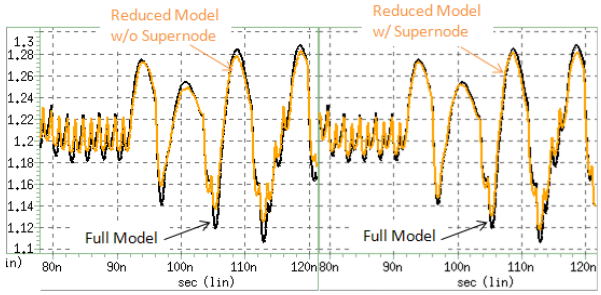


(b) Supernode added

Figure 3. Merging aggressor nodes in the worst case analysis.



(a) Eye of victim line



(b) SSO noise at VDDIO

Figure 4. Simulation result

For accurate modeling, not only do the adjacent aggressor lines remain, but also other non-adjacent aggressor lines must be included. In this paper, to simplify aggressor lines properly, the non-adjacent aggressor lines are replaced by a representative supernode that emulates all the omitted non-adjacent aggressor lines as shown in Fig. 3(b). It prevents the analysis from underestimating SI/PI performance.

To validate the significance of the supernode in the model reduction, the channel and PDN model for low power DDR2 (LPDDR2) system is modeled, reduced without a supernode as Fig. 3(a) and with a supernode as Fig. 3(b), and compared with a full model. In LPDDR2's Package-on-Package (PoP) structure, there are a large number of 3D interconnects including 61 signal lines, 14 power lines, and 14 ground lines between DRAM and Controller. To simplify the analysis, only wire bond model is considered in the modeling with open termination while package and pcb are assumed to be ideal.

A simulated eye diagram at the victim line and a time domain waveform of SSO noise at VDDIO are shown in Fig. 4(a) and (b), respectively. As shown in the figure, reduction of external ports with supernode provides fairly accurate results while modeling without the supernode produces inaccurate performance which results from the distortion of current path by wrong modeling.

V. Numerical Results

As a next step, the proposed reduction scheme in this paper is applied for a 3D Mobile memory system with a full model. The model is made up of PCB, power/ground/signal traces, wire-bonds, and transistor driver circuits, which are commonly used for the PoP system. The model was validated with open termination (LPDDR scheme), load termination to power and ground (SSTL scheme for the main memory system), and load termination to power (PODL scheme for graphic memory system). As an example, Fig. 5 shows the accuracy of the proposed method for the pseudo open-drain logic (PODL) scheme.

Channel and PDN models between DRAM and Controller are built as shown in Fig. 1. Among signal lines, one DQ line and its two adjacent DQ lines are chosen to be a victim and aggressors for crosstalk while all other signal lines are assumed to be aggressors for SSO. A channel model is reduced according to the proposed reduction scheme for the worst case eye and SSO noise analysis. By reducing external and internal nodes, simulation time shrinks by a factor of 85x.

Simulation results are compared to results from the full model without such external and internal node reduction. As shown in Fig. 5, accuracy level is well-maintained in spite of model reduction.

TABLE I. Nomalized simulation time comparison

	Full model	**Proposed model**
Simulation time	85x	1x

VI. Conclusion

While SSO noise modeling is a significant issue in signal integrity analysis, it is highly challenging due to the complexity of a model to be analyzed. Whereas macro modeling can be used to reduce internal complexity of model, a large number of external nodes for data, power, and ground pins or pads imposes still significant complexity on the model. Several options to reduce the number of external nodes for SSO noise simulation have been discussed in this paper. Reduction is available for both signal and power nodes based on the worst case aggressor switching activities. 3D package system has been shown as a numerical example to demonstrate the accuracy and improvement in the computation time by the proposed method.

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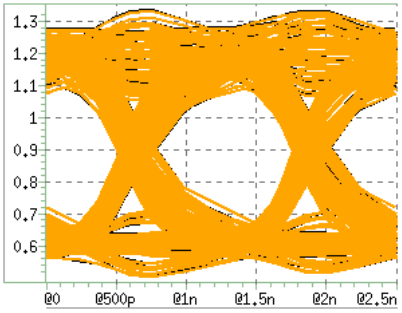
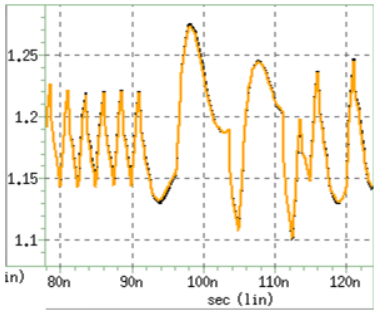


(a) Eye of victim line



(b) SSO noise at VDDIO

Figure 5. Simulation result (orange: proposed model, black: full model).

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