A Sub-μW Embedded CMOS Temperature Sensor for RFID Food Monitoring Application

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***Abstract*—An ultra-low power embedded CMOS temperature sensor based on serially connected subthreshold MOS operation is implemented in a 0.18 μm CMOS process for passive RFID food monitoring applications. Employing serially connected subthreshold MOS as sensing element enables reduced minimum supply voltage for further power reduction, which is of utmost importance in passive RFID applications. Both proportional-to-absolute-temperature (PTAT) and complimentary-to-absolute-temperature (CTAT) signals can be obtained through proper transistor sizing. With the sensor core working under 0.5 V and digital interfacing under 1 V, the sensor dissipates a measured total power of 119 nW at 333 samples/s and achieves an inaccuracy of +1/−0.8 °C from −10 °C to 30 °C after calibration. The sensor is embedded inside the fabricated passive UHF RFID tag. Measurement of the sensor performance at the system level is also carried out, illustrating proper sensing operation for passive RFID applications.**

***Index Terms*—CMOS temperature sensor, embedded sensor, passive RFID tag, ultra-low-power application.**

I. Introduction

UNLIKE traditional temperature sensors that utilize off-chip components, on-chip CMOS temperature sensors are well-known for their benefits of low production cost and easy interfacing with other electronic circuits. On-chip temperature sensors with small area and low power consumption are normally employed in thermal management applications in order to monitor system reliability and performance as a result of temperature variation. One popular use of embedded temperature sensors in VLSI implementation is to monitor excess on-chip heat dissipation resulting from higher and higher level of integration [1]. On the other hand, the emergence of RFID and wireless sensor network (WSN) applications has given rise to the development of embedded temperature sensors for wireless monitoring systems. For deployment in such applications, power consumption, instead of sensing range and accuracy requirements, is of utmost importance, especially for passive RFID tags. This is because passive RFID tags harvest power through rectification of the incoming RF signal, and the total energy available is limited. Typically, the total current budget for the whole tag can be as low as few μA [2]. The addition of an embedded sensor will inevitably increase the tag loading, and hence reduce the tag operating distance [3], [8].

On-chip temperature sensing is conventionally accomplished using BJT devices and digitized using analog-to-digital converters (ADCs) [4]. These sensors in general achieve good accuracy, with the penalties of increased circuit complexity and chip area. The corresponding power consumption is usually in μW range, and is therefore not applicable for passive RFID tag applications. On the other hand, the use of delay generated by inverter chains for temperature sensing with time-to-digital converters (TDCs) for digitizing temperature modulated pulse-width is also reported [5]. These time domain sensors, though having increased inaccuracy, usually outperform the ones utilizing ADCs in terms of power consumption and area.

Recently, various passive RFID tags embedded with temperature sensors with lower power consumptions have been reported. In [6], an on-chip temperature sensor based on BJT architecture with sigma-delta ADC is demonstrated. The tag consumes 2.4 μW and 12 μW (assuming a 1.2 V supply) for read and temperature measurement operations, respectively, while achieving an inaccuracy of $-1.8\,^{\circ}\mathrm{C}/+2.2\,^{\circ}\mathrm{C}$ from 0 to 100 °C after calibration at 40 °C. It can be noticed that the sensor requires much more power than the tag, and the addition of the sensor can significantly affect the normal tag operation. In [7], temperature is measured by charging an integrating capacitor up to the temperature dependent diode voltage V_{BE} through a reference current. The time required is then digitized using a reference clock. The sensor dissipates a total current of 1.6 μW, with a resolution of 0.8 °C and an inaccuracy of $\pm 2.4\,^{\circ}\mathrm{C}$ within the −10 to 80 °C sensing range. Even though the sensor consumed merely 1.6 μW, it is still significant when compared with the reported tag total power consumption of 5.1 μW. In [8], a standalone temperature sensor with only 220 nW power consumption is reported. In this implementation, both the temperature dependent and the reference currents are converted to frequency signals. The sensor exhibits a temperature inaccuracy of $-1.6/+3\,^{\circ}\mathrm{C}$ from 0 °C to 100 °C, while occupying an area of 0.05 mm^2. This demonstrates the feasibility of sub-μW CMOS temperature sensor implementation suitable for embedded passive RFID tag applications.

From the above discussions, it is noticed that existing solutions for embedded ultra-low power temperature sensors in passive RFID tags still consume considerable power when com-

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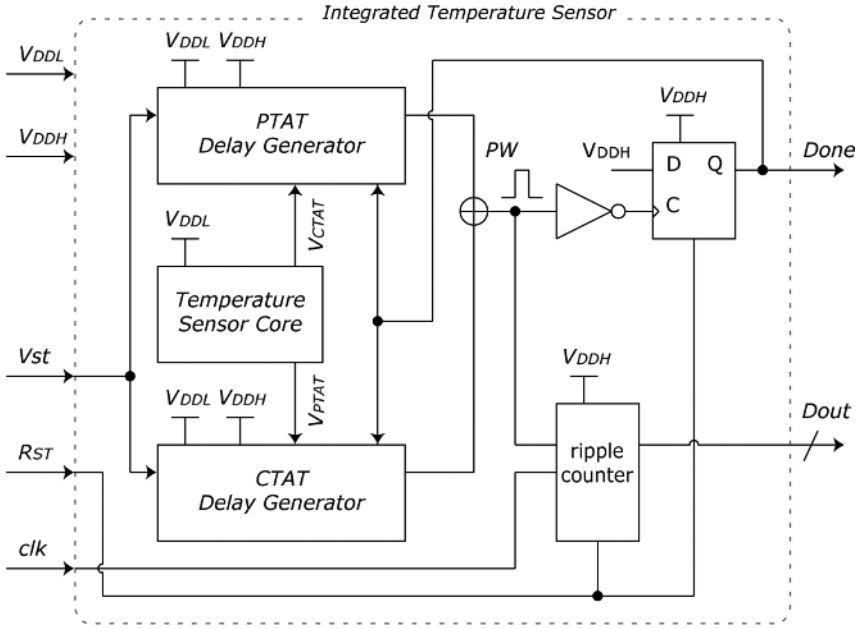

Fig. 1. Block diagram of the proposed temperature sensor with interfacing in the RFID tag system.

pared with the limited power available, which can greatly reduce the normal tag reading range. As an example, an increase in tag power by 30% through activating the sensor, as in the case of [7], can reduce the tag operating distance by almost 20% as deduced by the Friis Transmission Equation (assume other parameters to be constant). In that case, embedded temperature sensors should theoretically consume sub-microwatt power level, so as not to affect the overall tag operation. As demonstrated in the recent development of RFID tags, the tag power will inevitably fall in the future to extend the tag operating distance, making ultra-low power temperature sensing even more important in future designs.

In this paper, we present an ultra-low power integrated temperature sensor for passive UHF RFID tag implemented in TSMC 0.18 μm 1P6M CMOS process. A sensing range of $-10\,^{\circ}$C to $30\,^{\circ}$C is targeted, which is typically suitable for food quality control and monitoring applications, particularly those related to refrigerated and shelf storage [9]. Ultra-low power consumption is achieved through the use of subthreshold MOS sensor core with time domain readout. The system clock is utilized as the quantization clock to further reduce power and area overhead. The sensor consumes 119 nW with $+1/-0.8\,^{\circ}$C inaccuracy at a sampling frequency of 333 samples/s. This paper is organized as follows. Section II introduces our proposed temperature sensor design. Section III shows the measurement results of the proposed temperature sensor at both block level and RFID system level. The conclusion is presented in Section IV.

II. Proposed Temperature Sensor Design

Fig. 1 shows the block diagram of the proposed temperature sensor in the RFID tag. The proposed temperature sensor first generates the $V_{\rm PTAT}$ and $V_{\rm CTAT}$ signals from the sensor core utilizing MOS devices operating in subthreshold region. These signals are converted to delays through the corresponding delay generators. The resultant temperature modulated output pulse PW (refer to Fig. 1), which is level-shifted to 1 V swing for interfacing at the output of the delay generators, is further digitized using the clock signal. This time-domain readout scheme eliminates the use of power hungry ADC to reduce power consumption. For system level implementation, the sensor reuses the existing supply voltages and clock signals available in the tag to reduce the power and area overhead. The sensor supply voltages, $V_{\rm DDL} = 0.5$ V and $V_{\rm DDH} = 1$ V, are provided by the on-chip power management unit. The supply voltages are provided by LDOs with filtering to reduce both noise at the RF frequency and the ripple voltage, as required by the sensor and other building blocks to ensure robust tag operation. The clock generator generates the system clock, and this clock is utilized by the sensor for quantization. This quantization clock is generated through injection locking. In that case, its frequency is referenced to the incident RF input and should be weakly dependent to both process and temperature variation. The sensor control signals are generated and the digitized temperature data received by the digital baseband. In order to further reduce power consumption, a *Done* signal is exerted at the end of each conversion period to shut-down the analog building blocks and to acknowledge the baseband. The digital data *Dout* is then ready and can be read out.

A. Sensor Core Implementation

Fig. 2 shows the temperature sensing core implementation, which is constructed using serially connected MOS transistors operating in subthreshold region to generate the $V_{\rm PTAT}$ and $V_{\rm CTAT}$ signals in order to achieve both low voltage and low power operation. Note that $\rm M_{1-2}$ are required to provide proper biasing for $\rm M_{3-6}$. For a MOS transistor operating in subthreshold region, the drain current can be deduced by

$$I_{\rm sub} = \mu C_{\rm OX}\left(\frac{W}{L}\right)V_T^2 \exp\left(\frac{V_{\rm gs}-V_{\rm th}}{nV_T}\right)\left[1-\exp\left(-\frac{V_{\rm ds}}{V_T}\right)\right] \quad (1)$$

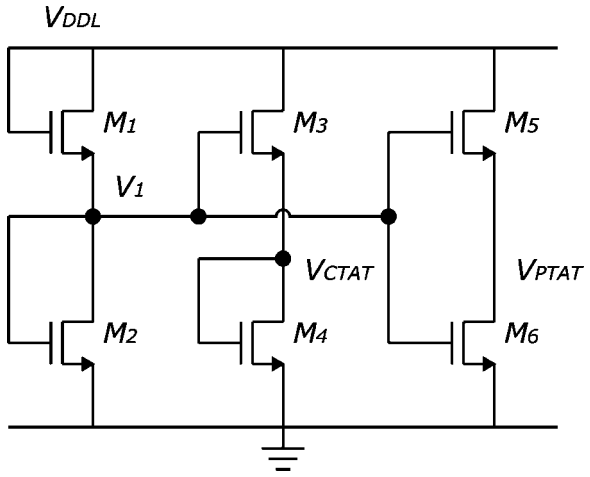

Fig. 2. Proposed serially connected subthreshold temperature sensor core.

where μ is the mobility, $C_{\rm OX}$ is the oxide capacitance, W/L is the transistor sizing, V_T is the thermal voltage kT/q and $V_{\rm th}$ is the transistor threshold voltage, respectively. Under the condition that $V_{\rm ds} >\sim 3V_T$, which is about 75 mV at room temperature, (1) can be reduced to

$$I_{\rm sub} \approx \mu C_{\rm OX}\left(\frac{W}{L}\right) V_T^2 \exp\left(\frac{V_{\rm gs}-V_{\rm th}}{nV_T}\right) \tag{2}$$

In our implementation, we biased the transistors so that $V_{\rm PTAT}(V_{\rm ds6})$ and $V_{\rm CTAT}(V_{\rm ds4})$ are both smaller than $3V_T$ ($\sim$30 mV) so that we can reduce the resistor by more than half in the subsequent V-I conversion stage (Section II-B) to achieve the same power budget. Using (1) and (2), in the case of $V_{\rm PTAT}$ (refer to Fig. 2), if we equate $I_{\rm D5} = I_{\rm D6}$, we obtain

$$\begin{aligned}
&\mu C_{\rm OX}\left(\frac{W}{L}\right)_5 V_T^2 \exp\left(\frac{V_1 - V_{\rm PTAT} - V_{\rm th5}}{nV_T}\right)\\
&\quad\approx \mu C_{\rm OX}\left(\frac{W}{L}\right)_6 V_T^2 \exp\left(\frac{V_1 - V_{\rm th6}}{nV_T}\right)\\
&\qquad\times\left[1-\exp\left(-\frac{V_{\rm PTAT}}{V_T}\right)\right]\\
&\Rightarrow V_{\rm PTAT} + nV_T \ln\left(1-\exp\left(-\frac{V_{\rm PTAT}}{V_T}\right)\right)\\
&\quad\approx nV_T \ln\frac{(W/L)_5}{(W/L)_6} - \Delta V_{\rm th5,6}.
\end{aligned} \tag{3}$$

Assuming the term $|\exp(-V_{\rm PTAT}/V_T)|$ is small, (3) can be reduced to

$$V_{\rm PTAT} \approx nV_T\left(\ln\frac{(W/L)_5}{(W/L)_6} + \exp\left(-\frac{V_{\rm PTAT}}{V_T}\right)\right) - \Delta V_{\rm th5,6} \tag{4}$$

where $\Delta V_{\rm th}$ is the difference in threshold voltages due to the body effect. Similarly, if we equate $I_{\rm D1} = I_{\rm D2}$ and $I_{\rm D3} = I_{\rm D4}$, the voltage V_1 and $V_{\rm CTAT}$ shown in Fig. 2 can be expressed as

$$V_1 \approx \frac{1}{2}\left(nV_T \ln\frac{(W/L)_1}{(W/L)_2} - \Delta V_{\rm th1,2} + V_{\rm DDL}\right) \tag{5}$$

$$\begin{aligned}
V_{\rm CTAT} \approx \frac{1}{2}\Bigg(&nV_T\left(\ln\frac{(W/L)_3}{(W/L)_4} + \exp\left(-\frac{V_{\rm CTAT}}{V_T}\right)\right)\\
&-\Delta V_{\rm th3,4} + V_1\Bigg).
\end{aligned} \tag{6}$$

For simplicity, we first assume that there is no body effect. In order to solve for $V_{\rm PTAT}$ in (4), we employed the Lambert-W function [10], which is typically used to solve equations involving exponentials. In that case, (4) can be further reduced to

$$V_{\rm PTAT} \approx V_T\left[n\ln\frac{(W/L)_5}{(W/L)_6} + G\left(n\cdot\exp\left(-n\ln\frac{(W/L)_5}{(W/L)_6}\right)\right)\right] \tag{7}$$

where G(.) is the Lambert-W function. For now, we further assume that $V_{\rm DDL}$ has negligible temperature dependency. Subsequently, (5) and (6) can be reduced to

$$\begin{aligned}
V_{\rm CTAT} \approx \frac{V_{\rm DDL}}{4} + V_T\Bigg(&\frac{n\ln(K)}{4}\\
&+G\left(\frac{n}{2}\exp\left(-\frac{1}{4}\left(\frac{V_{\rm DDL}}{V_T} + n\ln(K)\right)\right)\right)\Bigg)
\end{aligned} \tag{8}$$

where

$$K = \left(\frac{(W/L)_3}{(W/L)_4}\right)^2\left(\frac{(W/L)_1}{(W/L)_2}\right). \tag{9}$$

Fig. 3 shows the Matlab simulation results for the $V_{\rm PTAT}$ and $V_{\rm CTAT}$ signals predicted by (7), (8), and (9), using different transistor sizing ratios. It can be observed that the resultant PTAT and CTAT voltages achieve high linearity over the targeted sensing range, and their temperature dependencies can be adjusted by varying the corresponding transistor sizing. In particular, $V_{\rm PTAT}$ can be designed to have positive temperature dependency by sizing the transistor width of $\rm M_5$ to be larger than $\rm M_6$. Similarly, $V_{\rm CTAT}$ can be designed to have negative temperature dependency by properly sizing the transistors $\rm M_{1-4}$, with the width of $\rm M_2$ and $\rm M_4$ larger than $\rm M_1$ and $\rm M_3$, respectively. Also, it can be observed that the existence of a temperature dependent term V_T inside the Lambert-W function in (8) can affect the linearity of $V_{\rm CTAT}$ with respect to temperature. In that case, instead of having a temperature independent $V_{\rm DDL}$, better linearity in $V_{\rm CTAT}$ can be achieved if $V_{\rm DDL}$ is slightly positive temperature dependent for canceling the effect of V_T. This is confirmed in our study in variation in $V_{\rm DDL}$, as outlined in Section II-C.

With the consideration of the body effect, from the BSIM3v3 model, the threshold voltage of MOS transistor can be expressed as

$$\begin{aligned}
V_{\rm th}(T) = V_{\rm th}(T_0) + \left(K_{T1} + \frac{K_{tl1}}{L_{\rm eff}}\right)\left(\frac{T}{T_0}-1\right)\\
+K_{T2}V_{\rm bseff}\left(\frac{T}{T_0}-1\right)
\end{aligned} \tag{10}$$

where K_{T1}, K_{tl1}, and K_{T2} are process-dependent parameters, and $L_{\rm eff}$ and $V_{\rm bseff}$ are the effective channel length and body-source voltage, respectively. If we consider the difference of threshold voltages (assume the transistor lengths are matched), the first two terms can be cancelled, leaving only a $V_{\rm bs}$ dependent term. Taking into account that the lower transistors $\rm M_2$, $\rm M_4$, and $\rm M_6$ are connected to ground and hence have zero $V_{\rm bs}$, the following equation can be deduced:

$$\Delta V_{\rm th}(T) = K_{T2}V_{\rm bseff}\left(\frac{T}{T_0}-1\right). \tag{11}$$

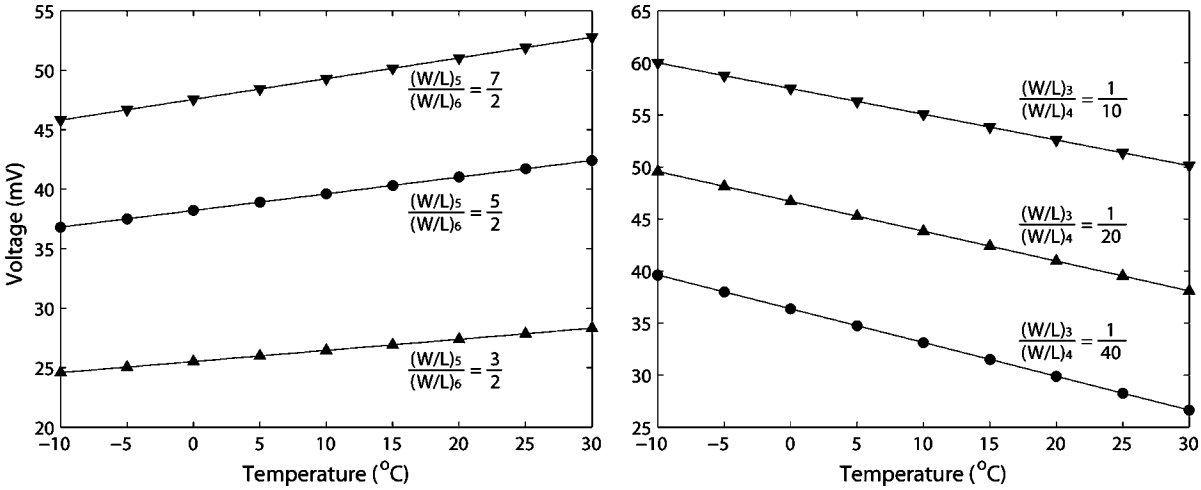

Fig. 3. Matlab simulation results of Eq. (7) (left) and Eq. (8) (right) using transistor sizing ratios as shown. The term $(W/L)_1/(W/L)_2$ is fixed to be 1/32 and V_{DD1} is set to 0.5.

TABLE I
SUMMARY OF TRANSISTOR SIZES AND RESISTOR AND CAPACITOR VALUES

Transistor	W/L (μm/μm)	Resistor	kΩ	Capacitor	pF
M1	2u/360n	R_{CT}	222.84	C_{CT}	3.36
M2	32*2u/360n	R_{PT}	311.89	C_{PT}	3.36
M3	4*2u/360n				
M4	160*2u/360n				
M5	50*2u/2.88u				
M6	20*2u/2.88u				

From (11), it can be observed that ΔV_{th} is dependent on V_{bseff}, which corresponds to the V_{PTAT} and V_{CTAT} signals. Notice that the temperature dependency of ΔV_{th} is scaled by the factor K_{T2}, which approximately equals -0.03 in our process. In order to verify how the body effect affects V_{PTAT} and V_{CTAT}, we performed simulations of the sensor core using the transistor sizing as shown in Table I. Fig. 4 shows the simulated waveform for V_{PTAT}, V_{CTAT}, $\Delta V_{\mathrm{th3,4}}$ and $\Delta V_{\mathrm{th5,6}}$ ($\Delta V_{\mathrm{th1,2}}$ is similar to $\Delta V_{\mathrm{th3,4}}$ and is not shown). It can be observed that both the V_{PTAT} and V_{CTAT} signals can be generated with good linearity with respect to temperature over the targeted sensing range, and are clearly exhibiting the same temperature dependency as compared to $\Delta V_{\mathrm{th5,6}}$ and $\Delta V_{\mathrm{th3,4}}$, respectively. This can also be deduced from (4), (5) and (6), considering the fact that the ΔV_{th} signals have a linear response to temperature as shown in Fig. 4.

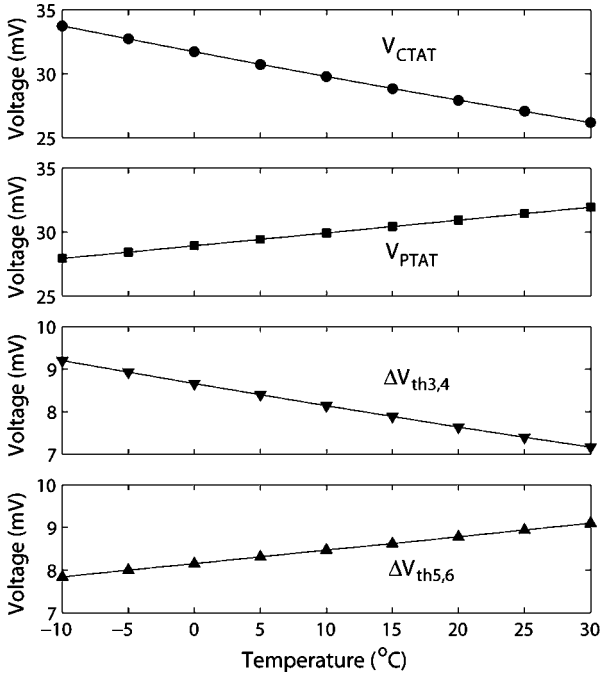

Fig. 4. Simulation results of the V_{PTAT}, V_{CTAT}, $\Delta V_{\mathrm{th3,4}}$ and $\Delta V_{\mathrm{th5,6}}$ dependence on temperature.

B. Delay Generator Implementation

In [5], the use of two delay lines for time-domain CMOS temperature sensor has been proposed. By introducing a second reference delay line, the offset introduced by the first temperature modulated delay line can be canceled. However, the addition of the second delay line will also increase the output noise power without contributing to the overall signal. Our proposed temperature sensor incorporates both the PTAT and CTAT delay lines to form a differential sensing architecture. In that case, the signal offset can be canceled without sacrificing the sensor output SNR, as even the noise power is increased due to the addition of a second delay line, the signal power is also increased to compensate for the loss.

Fig. 5 illustrates the PTAT and CTAT delay generators that convert the temperature modulated signal from voltage domain to time domain for simple and power efficient processing. Without loss of generality, we first consider the CTAT delay generator. Transistors $\mathrm{M_{P7-8}}$, together with the resistor $\mathrm{R_{PT}}$ and the amplifier, convert the input voltage V_{PTAT} into current I_{PTAT}. Low-voltage operation is sustained by implementing the amplifier using simple current mirror architecture. Stacking of transistors is avoided by having the amplifier output directly driving $\mathrm{M_{P7}}$. The scaled current from $\mathrm{M_{P8}}$ is mirrored through $\mathrm{M_{P9-10}}$. Transistors $\mathrm{M_{P10-15}}$ operate as a single-slope ADC,

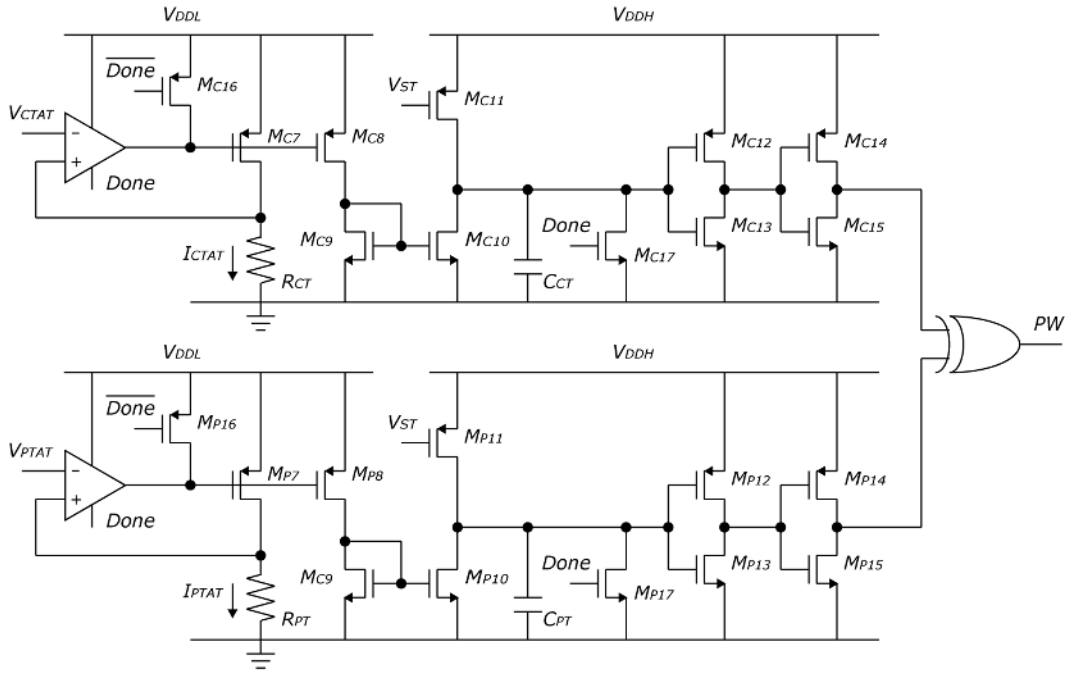

Fig. 5. Implementation of the PTAT (above) and CTAT (below) delay generators.

which also performs level-shifting from 0.5 V to 1 V for interfacing with other digital circuits. Similarly, the PTAT delay generator converts $V_{\rm CTAT}$ into $I_{\rm CTAT}$, followed by another single-slope ADC. At the start of each integration cycle, the signal $V_{\rm ST}$ is exerted, shutting down $\rm M_{P11}$ ($\rm M_{C11}$). The temperature modulated current signals (which is converted from $V_{\rm PTAT}$ or $V_{\rm CTAT}$) is integrated through capacitor $\rm C_{PT}$ ($\rm C_{CT}$). Upon reaching the switching threshold of $\rm M_{P12-13}$ ($\rm M_{C12-13}$), a rising edge is triggered and buffered by $\rm M_{P14-15}$ ($\rm M_{C14-15}$). As the discharging currents are temperature dependent, the delay between the two rising edges is also temperature dependent. The two rising edge signals from the CTAT and PTAT delay paths are XORed to generate a temperature modulated pulsewidth PW (Fig. 6) and then further quantized using the ripple counter and the system clock. The whole block is shut-down through the feedback signal (refer to Fig. 1), which also indicates the end of conversion.

As mentioned before, two rising edges are generated at the outputs of individual delay generator. For $I_{\rm CTAT}$ and $I_{\rm PTAT}$ are both linearly dependent to temperature, we assume that at a particular temperature T and reference temperature T_0, they can be expressed as

$$I_{\rm PTAT}(T) = I_{\rm PTAT}(T_0)\left[1 + k_P(T - T_0)\right] \tag{12}$$

$$I_{\rm CTAT}(T) = I_{\rm CTAT}(T_0)\left[1 - k_C(T - T_0)\right] \tag{13}$$

where k_P and k_C are the corresponding proportional constants. Without loss of generality, let us consider the case of PTAT delay generator. The temperature-dependent $I_{\rm CTAT}$, which is generated from $V_{\rm CTAT}$ of the sensor core in Fig. 2, is utilized to discharge the integrating capacitor ($\rm C_{PT} = C_{CT} = C$). The PTAT delay generated can be determined by the following equation:

$$t_{\rm PTAT}(T) = \frac{C\Delta V}{I_{\rm CTAT}(T)} \tag{14}$$

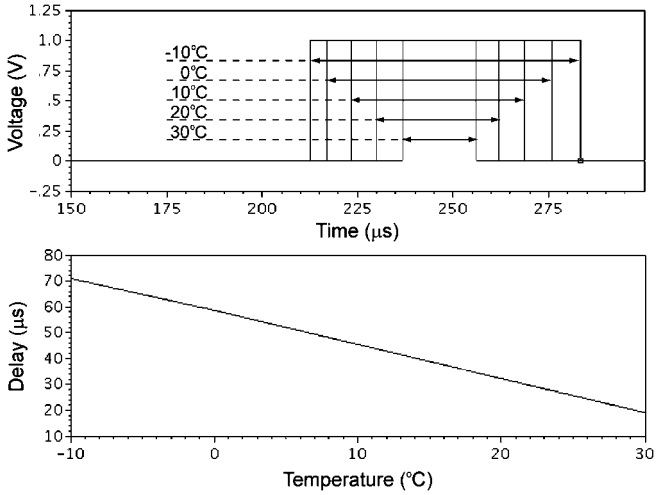

Fig. 6. Simulated temperature modulated pulsewidth from $-10\,^{\circ}$C to $30\,^{\circ}$C.

where ΔV is the difference between $V_{\rm DDH}$ and the threshold crossing determined by the corresponding transistors $\rm M_{C12-13}$ in the PTAT delay generator (refer to Fig. 5). By using (13), (14) can be approximated as

$$t_{\rm PTAT}(T) \approx \frac{C\Delta V}{I_{\rm CTAT}(T_0)}\left(1 + k_C(T - T_0) + k_C^2(T - T_0)^2\right). \tag{15}$$

Similarly, the CTAT delay generated can be expressed as

$$t_{\rm CTAT}(T) \approx \frac{C\Delta V}{I_{\rm PTAT}(T_0)}\left(1 - k_P(T - T_0) + k_P^2(T - T_0)^2\right). \tag{16}$$

For (15) and (16) to be valid, both $k_C(T - T_0)$ and $k_P(T - T_0)$ have to be small. In order to achieve this, we sized the transistors to obtain the corresponding k_C and k_P accordingly, as shown in Fig. 4. In our implementation, the

term k_C and k_P are approximately equal to 5.1 m/°C and 3.7 m/°C, respectively. Assume that the capacitor and the threshold crossings are matched between the two delay generators, the second-order terms of (15) and (16) can be cancelled if the following condition holds:

$$k_P^2 I_{\mathrm{CTAT}}(T_0) = k_C^2 I_{\mathrm{PTAT}}(T_0) \tag{17}$$

which can be accomplished in the design stage. After cancelling the second-order term, the temperature-modulated signal PW at the output of the XOR gate can be expressed as

$$t_{\mathrm{PW}}(T) \approx \left(\frac{C\Delta V}{I_{\mathrm{CTAT}}(T_0)} - \frac{C\Delta V}{I_{\mathrm{PTAT}}(T_0)}\right) + \left(\frac{C\Delta V k_C}{I_{\mathrm{CTAT}}(T_0)} - \frac{C\Delta V k_P}{I_{\mathrm{PTAT}}(T_0)}\right)(T - T_0). \tag{18}$$

Eq. (18) verifies that even though the outputs of individual delay generators are nonlinear, as predicted in (15) and (16), the resultant delay at the output of the XOR gate can still be linear. Note also that the coefficient of the temperature-dependent term is increased (as k_C is negative), meaning that the signal power is increased through differential sensing. Fig. 6 shows the simulated pulsewidth PW from $-10\,^{\circ}$C to $30\,^{\circ}$C. The nominal values for I_{CTAT} and I_{PTAT} at room temperature are 10.9 nA and 12.5 nA, respectively. With an increase in temperature, the output PW signal is reduced at both rising and falling edges through the use of the differential sensing architecture, and the resultant temperature dependency of t_{PW} is linear.

C. Process Variation

In fact, the linearity of the sensor is affected by mismatch between the two signal paths. Apart from the errors introduced by transistors M_{1-6} and amplifier offsets, resistors and capacitors used for V-I conversion and signal integration are also susceptible to process variation and mismatch. On-chip resistors and capacitors values can have $\pm 10\%$ to 15% variation. This effect on the sensor performance can be studied using (18). Notice that as both resistors are matched, I_{CTAT} and I_{PTAT} will vary with high correlation. In that case, the variation in resistors and capacitors will not significantly degrade the t_{PW} linearity. Instead, this will mainly affect the effective resolution of the sensor response. Fig. 7 shows the Monte Carlo simulation results (100 runs) of the sensor error without considering variations in resistors/capacitors after two-end-point calibration. The resultant sensor error over the targeted sensing range is $+0.9/-0.3\,^{\circ}$C. In order to estimate the effect on the sensor performance due to resistor/capacitor variation, we also performed Monte Carlo simulations with different resistor and capacitor process corners. In particular, we performed three separate Monte Carlo simulations. In each simulation, we choose one of the three corner models (SS, TT, FF) for resistor and capacitor. After combining the results of the three simulations, we get a set of data which also includes the corner variations of resistors and capacitors. The simulation results show that the sensor error is increased to $+1.4/-0.4\,^{\circ}$C over the specified temperature range after calibration.

As mentioned before, the accuracy of (15) and (16) rely on the fact that both $k_C(T - T0)$ and $k_P(T - T0)$ are small. For an extended sensing range, these assumptions become more inaccurate, making the linearity of t_{PW} to become worse. Note that our targeted sensing range is $40\,^{\circ}$C (from $-10\,^{\circ}$C to $30\,^{\circ}$C). From simulation, if we consider extending the temperature range from $40\,^{\circ}$C to $60\,^{\circ}$C, the sensor inaccuracy due to nonlinearity will be increased from $+0.9/-0.3\,^{\circ}$C to $+1.1/-0.8\,^{\circ}$C (without considering resistors and capacitors variations) after calibration.

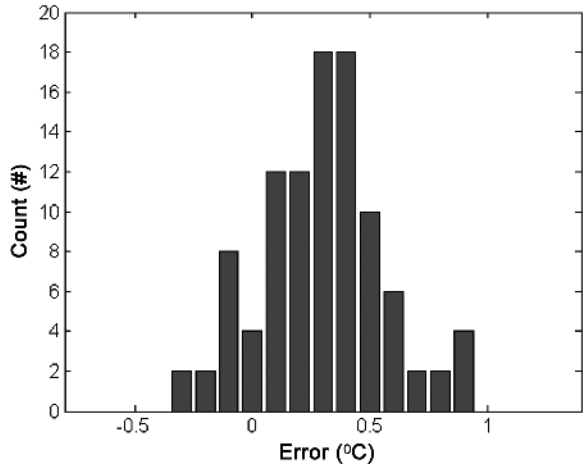

Fig. 7. Error due to nonlinearity from $-10\,^{\circ}$C to $30\,^{\circ}$C after calibration from 100 Monte Carlo simulation runs (without considering variations for resistors and capacitors).

In case of the supply voltage variation, it should be noted that due to process variation, on-chip implementation of LDO accuracy, which is limited by the on-chip bandgap, can have up to 4–5% part-to-part variation. In that case, it is possible that the resultant supply voltage is either under- or overcompensated, resulting in a characteristic of either PTAT or CTAT. As indicated in (8), the signal V_{CTAT} is dependent on V_{DDL}. In that case, the temperature dependency of V_{CTAT} is a combination of the transistor sizing and V_{DDL}. As a consequence, the change in V_{DDL} with respect to process and mismatch can affect the sensor performance. As discussed in Section II-A, the linearity of V_{CTAT} degrades when V_{DDL} is CTAT, and improves when V_{DDL} is PTAT. Fig. 8 shows the sensor maximum absolute error after two-end-point calibration and the resultant t_{PW} over the targeted sensing range with V_{DDL} having different temperature dependencies. In our implementation, V_{DDL} typically exhibits a PTAT behavior of about 50 ppm within the targeted sensing range. The bounds in Fig. 8 are set to reflect an approximately $\pm 5\%$ error in V_{DDL} due to process. It can be observed that the error due to linearity improves if V_{DDL} exhibits PTAT behavior, and the worst case increase in error when compared with the typical case (50 ppm) is approximately $0.1\,^{\circ}$C. In that case, the increase in sensor error due to variation in V_{DDL} is expected to be small after calibration.

III. Measurement Results

The proposed temperature sensor was implemented in a standard CMOS 0.18 μm one-poly-six-metal (1P6M) process. As shown in the chip micrograph in Fig. 9, the sensor occupies an active area of 0.0416 mm^2. Extensive matching is exercised

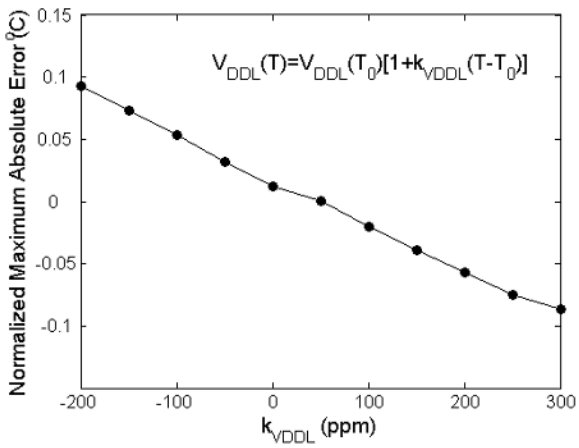

Fig. 8. Normalized maximum absolute error after two-end-point calibration over the targeted sensing range, with V_{DDL} having different temperature dependencies.

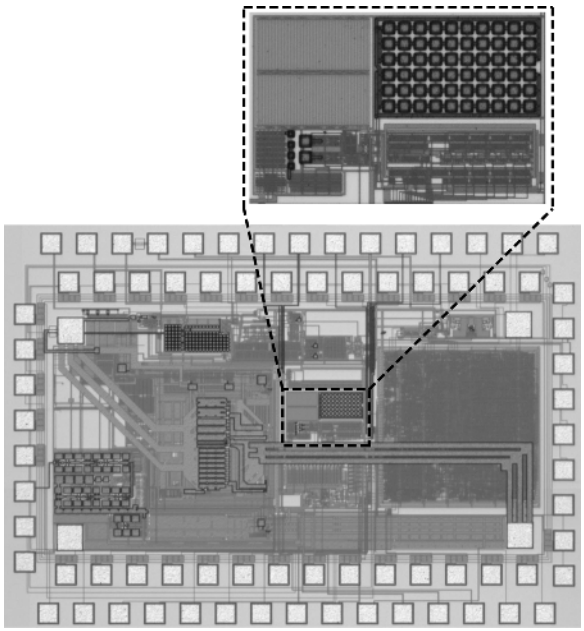

Fig. 9. Chip micrograph of the complete RFID tag with embedded temperature sensor. The sensor occupies an area of 0.0416 mm^2.

during the layout design stage in order to minimize the effect due to process variation and mismatch.

Power consumption is measured at room temperature using Agilent 3458A. With supply voltages at 0.5 V and 1 V and a conversion rate of 1 ksamples/s, the sensor dissipates a measured power of 119 nW (74 nW from 0.5 V supply and 45 nW from 1 V supply). From simulation, the power consumption breakdown for the sensor core, delay generators and digital circuitry are 17 nW, 55 nW, and 25 nW, respectively. In order to characterize the performance of the temperature sensor, the measurement is performed inside the temperature chamber THS-A KSON Instrument Technology, with a temperature step of 5 °C within the specified temperature range from −10 °C to 30 °C. In our first measurement setup, in order to fully characterize the sensor, Agilent Modular Logic Analysis System 16902B is used to generate the required control signals as well as analyze the sensor

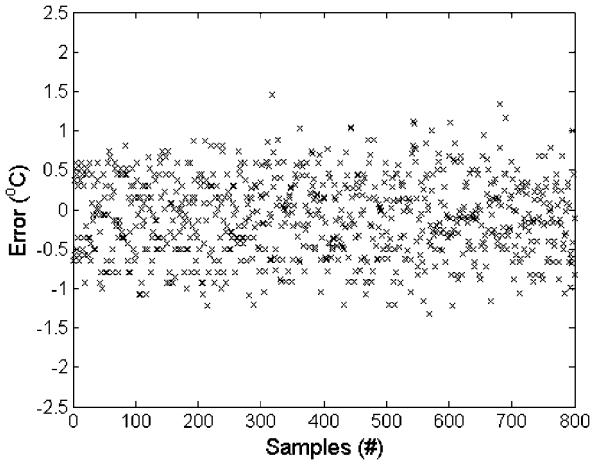

Fig. 10. Measured temperature inaccuracy (°C) over 800 samples at 1 ksamples/s from a single test chip showing a 3σ error of ±1.5 °C.

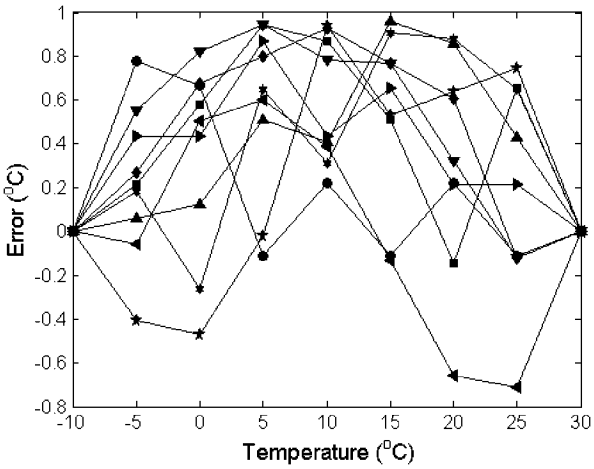

Fig. 11. Measured temperature inaccuracy (°C) after averaging and two-end-point calibration from −10 °C to 30 °C of nine evaluated samples.

outputs. The output pulse was quantized using an external clock. Calibration is performed by using simple straight line fitting between the results at two end temperature points as proposed in [5]. With $N_{T\min}$ and $N_{T\max}$ representing the digital outputs at the minimum and maximum temperature in the targeted sensing range, which are −10 and 30 °C, respectively, the effective resolution is defined as $(T_{\max} - T_{\min})/(N_{T\min} - N_{T\max})$. The sensor performance can then be obtained by comparing the interpolated value and the measured output. Fig. 10 shows the measured temperature error over measured output samples at 1 ksamples/s. It is observed that the 3σ error, which is mainly contributed by the readout noise, can be up to 1.5 °C. In order to improve the measured accuracy, a lower conversion rate is used so as to minimize the readout noise, and measured data are averaged at every 30 samples. Fig. 11 shows the resultant temperature error of nine evaluated chips from −10 °C to 30 °C after two-end-point calibration. With a temperature step of 5 °C, the measured temperature error is +1/−0.8 °C. Due to process variation, the effective resolution varies from chip to chip, ranging from 0.14 to 0.21 °C/LSB over nine measured samples.

Fig. 12 shows the overall architecture of UHF RFID Tag system with our proposed embedded temperature sensor. Apart

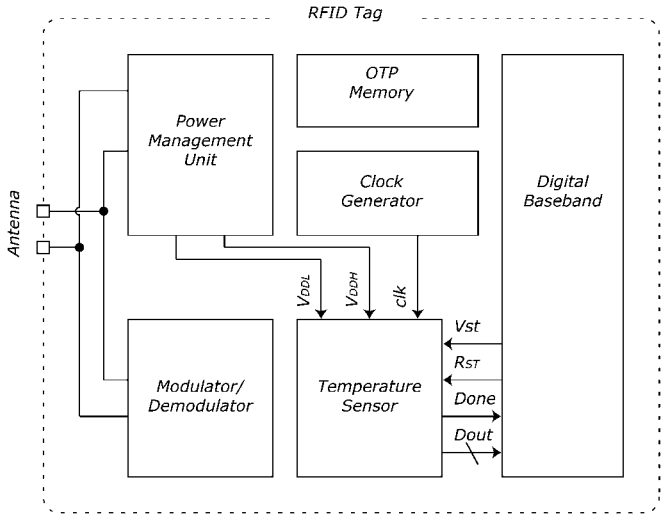

Fig. 12. Block diagram of the UHF RFID tag with embedded temperature sensor showing only input/output interfaces of the embedded sensor.

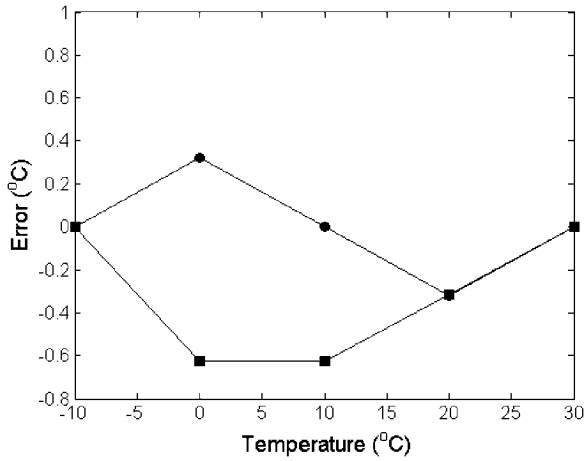

Fig. 13. Measured temperature inaccuracy (°C) under system level measurement after two-end-point calibration from −10 °C to 30 °C.

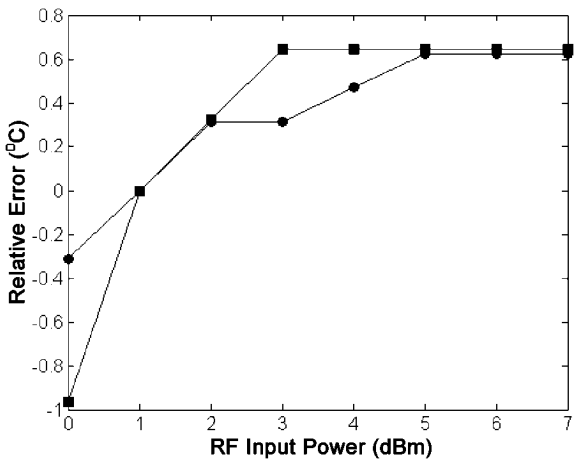

Fig. 14. Measured temperature inaccuracy (°C) over RF input power (dBm) over two measured samples.

from the sensor, it consists of a modulator/demodulator front-end, a power management unit, a clock generator, a digital baseband, and a one-time programmable (OTP) memory. As mentioned in Section II, the sensor supply voltages and the quantization clock are provided by the existing power management unit and the clock generator, respectively. Temperature sensing operation is activated after receiving an EPC Gen2 [11] compliant custom temperature sensing command. The sensor then uses the rectified power and the system clock to perform sensing and quantization. Upon sensing completion, the digitized temperature data is sent back to the reader for further processing and storage.

The major factors that determine the sensor performance are the supply voltages and the system clock. In that case, the embedded sensor performance is also tested in the RFID tag system to evaluate the system performance, where the power is supplied by the power management block and the injection-locked reference clock is supplied by the clock generator block. Similar to the previous setup, this test is also performed inside the temperature chamber, but with the external inputs changed to an input RF signal using Agilent E4433B. Two samples have been fully characterized experimentally and the measurement result is shown in Fig. 13. It can be observed that the measured sensor inaccuracy is still within the temperature inaccuracy of $+1/-0.8\,^{\circ}\mathrm{C}$ from the standalone sensor test, verifying the performance of the sensor in the system. Note that an increase in error is expected if more samples are measured.

Fig. 14 shows the error induced due to variations in the RF input power. At low RF input power, the sensor performance is degraded. This is mainly due to the fact that there is not enough power available for the building blocks and the supply voltages from the power management are not at their nominal values. A nominal power of 1 dBm is required to power up the system to its designed operating condition. This is due to the fact that there is impedance mismatch between the Agilent E4433B output and the tag input, and power is lost due to reflection. Due to a lack of power, the sensor fails to function with an input RF power below 0 dBm, which indicates the minimum input power for the embedded sensor to function. By further increasing the RF input power, the sensor error changes until it saturates, upon which there is no more effect in sensor error with further increase in RF input power. It can be observed that the sensor inaccuracy over the operating range due to varying input power, when compared with its nominal operating condition at 1 dBm, is within $+0.7/-1\,^{\circ}\mathrm{C}$ over two measured samples.

Table II compares the performance of our proposed temperature sensor with other low-power MOS-based temperature sensor designs recently reported in the literature [5]–[8]. One should note that the comparison of different temperature sensors is not obvious as typically the target performance is different for different designs, and therefore circuit complexities and specifications may vary significantly. In addition, some designs rely on externally powered control signals, which are not relevant to our application since all signals are generated internally from a passive RFID tag. Some other implementations only focus on the precision and temperature range while little attention is given to power consumption. In this work, since the energy available within the passive RFID tag is very limited, the focus is mainly on the power while trying to maintain reasonable

TABLE II
PERFORMANCE COMPARISON OF RECENTLY PUBLISHED LOW-POWER CMOS TEMPERATURE SENSORS

Sensor	Supply voltage (V)	Error (°C)	Area (mm^2)	Temp. Range (°C)	Power Consumption	Sampling Rate	Technology
[5]	3.3	+0.9/-0.7	0.175	0~100	10μW	2	0.35μm
[6]	N/A	+2.2/-1.8#	N/A	0~100	9.6μW#	2	N/A
[7]	2	+/-2.4#	0.03#	-10~80	1.6μW	N/A	0.35μm
[8]	1	+3/-1.6	0.0495	0~100	0.22μW	100	0.18μm
This work	**0.5, 1**	**+1/-0.8**	**0.0416**	**-10~30**	**0.119μW##**	**333**	**0.18μm**

Note: All errors indicated are not 3σ bounds.
Estimated data from the corresponding literature.
Excluding the power for generating the supply and clock.

accuracy, temperature range, and sampling frequency. For this reason, our comparison highlights recent designs with the main aim of low power with designs specifically targeted at wireless sensing applications [6]–[8]. It can be noted that our proposed sensor achieves the lowest possible power consumption and maintains reasonably good measured inaccuracy over the targeted temperature sensing range. The area of the proposed sensor is also small enough to be embedded on RFID tags, where cost is an important consideration.

IV. CONCLUSION

In this paper, we have proposed an ultra-low-power CMOS temperature sensor with 119 nW power consumption (excluding the power consumed by generating the supply and clock) at room temperature targeting at RFID food monitoring applications. Temperature sensing is performed through the V_{PTAT} and V_{CTAT} signals generated from serially connected MOS transistors operating in subthreshold region. As a consequence, supply voltage as low as 0.5 V can be used for sensing purposes. This can further reduce the power consumption overhead, which is one of the major concerns in embedded sensors for passive wireless applications. Differential sensing architecture is utilized so as to cancel the signal offset as well as increase the effective temperature signal power. Measurement results at both block level and system level show that a temperature inaccuracy of $+1/-0.8\,^{\circ}\mathrm{C}$ can be achieved at 333 samples/s within a targeted temperature range from $-10\,^{\circ}\mathrm{C}$ to $30\,^{\circ}\mathrm{C}$. A very interesting fact about our design is that temperature sensing is fully performed within a passive tag, where power is harvested from an RF source, thanks to the ultra-low-power feature of our proposed design. Moreover, the small silicon area achieved in this design makes it suitable for RFID applications, where cost is of primary importance.

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