A sub-Hertz nanopower low pass filter

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***Abstract*—This brief presents a first order low pass filter topology capable of providing cut-off frequencies down to 2 mHz with a power consumption of 5 nW. The circuit is intended for signal conditioning applications, particularly for use with very low frequency physiological signals in low power portable medical equipment. To achieve the low frequency cut-off the filter is based around the use of a clocked transconductor which provides a low transconductance while using a relatively high bias current level. The circuit is implemented in a 0.35 μm technology with a 1 V supply and has a measured 32 μV_{RMS} of noise and 64 dB dynamic range. In terms of power consumption and cut-off frequency the reported filter outperforms previous filters from the literature.**

***Index Terms*—Analog filtering, clocked transconductor, low power, biomedical signal conditioning.**

I. Introduction

SUB-Hertz low pass filters have many applications in sensor interfaces [1] and biomedical signal processing units [2]. Sensor interfaces are often applied to slowly varying phenomena such as flow rate, pressure, chemical concentration and temperature, and sub-Hertz filters are required for anti-aliasing filters, active gain controllers and isolation of the wanted signal in these applications. Similarly, biomedical signals are usually found in the 10 mHz to 100 Hz frequency range [3] and hence require sub-Hertz frequency filters to condition the signal before processing. For example, the filter presented here was designed as part of the breathing monitoring device presented in [4] (although it is not restricted to this use). In the system of [4], sub-Hertz frequency filters are used to smooth the signal after rectification and for finding the average of the signal. Sub-Hertz filters are used for a similar purpose in [5].

However, despite their utility, creating large time constant low pass filters on-chip is a challenging problem. To implement large time constants switched capacitor based topologies require large capacitor ratios [6], and a sufficiently high power supply must be used to achieve an acceptably low switch on-resistance [2].

In g_mC based topologies the cut-off frequency is generally determined by the ratio g_m/C, where C is the integrating capacitance present. However, area limitations restrict the maximum capacitance that can be present on-chip to pico-Farad values, limiting the minimum cut-off that can be achieved. Large off-chip capacitors can be used, but for a given cut-off frequency the required g_m value is decreased, decreasing the transconductor output current. On-chip currents down to femto-Amp levels are feasible, but moving off-chip the current is limited by the leakage currents in the bondpads to pico-Amp levels [7]. Larger g_m and C values must thus be used to keep the output current above this limit, but at the cost of power consumption.

For a fully on-chip solution, impedance scaling techniques, placing the capacitor across an inverting amplifier and utilising the Miller effect, can be used to increase the effective capacitance although this introduces increased complexity, power consumption and noise [8], [9]. More commonly, to achieve low frequency on-chip cut-offs the transconductor unit is modified to reduce the effective g_m value, and several techniques for this have been previously reported.

For example, floating gates can be added to the transconductor input transistors to capacitively attenuate the effective input voltage at the cost of increasing the input referred noise. [10] used this technique to achieve a 500 mHz cut-off low pass filter. Alternatively, [8], [11] made use of transistors in the triode region to perform the voltage-to-current conversion. [11] reported a 1.5 Hz cut-off low pass filter based upon this, but an additional feedback amplifier was required to keep the conversion transistors in the triode region. [12] used bulk driven (as opposed to gate driven) input transistors for the transconductor to take advantage of the generally lower g_{mb} transconductance. A 170 mHz cut-off was achieved, but at the expense of a reduced input impedance. Simultaneously, [12] made use of current division which is also used in [1], [8], [13], with [1] reporting a 53 mHz cut-off filter. The technique uses current mirrors or splitters to reduce the output current from the transconductor and hence the effective transconductance, but generally comes at the cost of circuit area. Current cancellation, where the transconductor current is reduced by adding input transistors of different sizes and cross connecting their drain terminals can also be used [14]. However, this use of partial positive feedback relies on very good matching for successful operation. Finally, [2], [15] cascaded transconductance amplifiers with transresistance amplifiers, each of differing value, such that the overall transconductance was reduced. [2] reported a 100 mHz cut-off integrator, but it is noticeable that reported circuits using this technique do not supply noise or distortion figures. These are likely to be poor since every section adds noise and distortion and cascading many times will result in low dynamic range.

This brief presents a new low pass filter topology based on a hybrid approach between switched capacitor and g_mC filters. Here a clocked transconductor is used to form the reduced transconductance g_m element in a g_mC filter. The duty cycle

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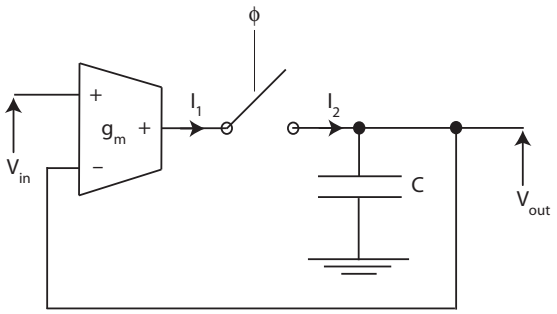

Fig. 1. Principle of operation of the proposed low pass filter. A standard first order g_mC filter is modified to include a switch between the transconductor output and the capacitor, reducing the effective transconductance.

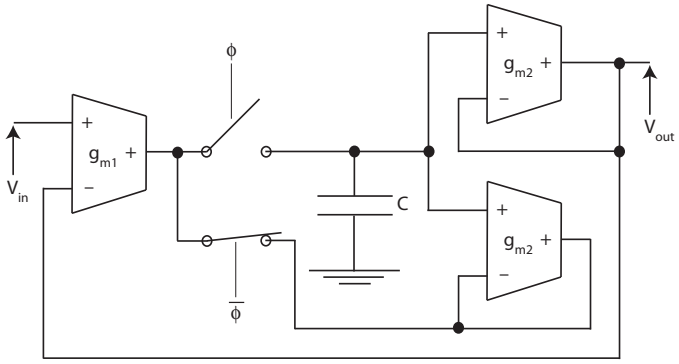

Fig. 2. The complete low pass filter incorporates two buffers to provide a path for the transconductor output current when the switch ϕ is open and to mitigate the effect of charge injection.

of the clock then determines the effective transconductance and allows easy digital control of the filter cut-off frequency. In this brief, Section II describes the operation and design of the new low pass filter topology. Experimental results are then presented and compared to other filters from the literature in Section III. Finally conclusions are given in Section IV.

II. The clocked transconductor filter

A. Principle of operation

Fig. 1 shows the basic principle of the proposed low pass filter topology: it is based around clocking the output of a standard transconductor element. A standard transconductor is placed in a feedback loop arrangement with a capacitor forming a first order g_mC low pass filter and a switch is then added between the output of the transconductor and the capacitor. This switch allows the output of the transconductor to be connected to and disconnected from the capacitor and feedback loop. As the output current from the transconductor, I_1, can only flow into the capacitor when the switch is closed the average current that flows into the capacitor, I_2, is reduced. If δ is the duty cycle of the switch ϕ, then

$$I_2 = \delta \times I_1. \tag{1}$$

As I_2, the effective output current of the transconductor is reduced, the effective transconductance of the transconductor is reduced by the same amount. Furthermore, this reduction in transconductance is achieved in the time domain and may be precisely controlled via the clock used to control the switching operation. This allows easy digital control of the transconductance and the filter cut-off frequency. For correct operation the clock frequency used must be sufficiently high so that the clock harmonics fall out of band. The precise clock frequency used is not important however, and this requirement is generally trivial to satisfy in a sub-Hertz filter where the passband frequencies may be orders of magnitude lower than the clock frequency.

The introduction of the switch in Fig. 1 also increases the effective output resistance of the transconductor. For a first order g_mC filter the time constant, τ, is given by

$$\tau = \frac{\mathrm{C}}{g_o + g_m} \tag{2}$$

where g_o is the transconductor's output conductance. For τ to be tunable via the bias current the g_m term in (2) must dominate over g_o, which can be problematic to achieve as the effective value of g_m is reduced. The proposed topology overcomes this as when the switch is open g_o does not affect the capacitor voltage since the two nets are isolated. The capacitor is only loaded by g_o when the switch is closed, and hence the effective output conductance of the transconductor also scales with the duty cycle. Since both g_m and g_o scale at the same rate, if the transconductor g_m dominates g_o when no duty cycle is present then it will still dominate in the proposed topology. No additional design of the transconductor for low g_o values is required.

B. The complete low pass filter

In reality the simplistic diagram of Fig. 1 does not obey Kirchoff's current law: when the switch is open the transconductor's output current has nowhere to flow. This would cause the output of the transconductor to saturate at (or near) the supply rails as no output current could be provided. To overcome this two buffer cells are introduced as shown in Fig. 2. The first buffer is placed between the capacitor and the output/feedback node, V_{out}, to isolate the capacitor node from the load. The second buffer is then placed between the output of the filter transconductor (g_{m1}) and the capacitor via a second switch, $\overline{\phi}$, in anti-phase to the main switch. This second buffer thus provides a path for the output current of g_{m1} when the ϕ switch is open. When ϕ is open, $\overline{\phi}$ is closed and the output of g_{m1} is fixed to the same voltage as the capacitor, but without any current from g_{m1} flowing into the capacitor. Thus the voltage at the output of g_{m1} stays approximately constant regardless of whether the current from it is flowing into the capacitor or not, preventing the output of the transconductor changing between the supply rail voltages and the voltage at the capacitor each time the switch is toggled.

This arrangement also reduces the effects of charge injected through the switches. When ϕ switches, charge is injected predominately into the capacitor C as this offers the lowest impedance. For low frequency operation C is generally large, and the resulting voltage spike produced is hence small. When $\overline{\phi}$ switches, charge is predominately injected into a buffer

connected in negative feedback. The load capacitance seen is thus both the buffer output capacitance and the input capacitance of the negative input, increasing the total capacitance present. Additionally, both switches can operate at frequencies much higher than the bandwidth of the filter and so remaining voltage ripple can be easily removed if required.

C. Implementation

For on-chip implementation a 39.8 pF poly-poly capacitor is used for C and the switches ϕ and $\overline{\phi}$ are implemented as single minimum sized NMOS FETs. Since the voltages across the switches are small and remain at approximately half the supply voltage the estimated 3 MΩ on-resistance of these is high, but sufficient for the application.

The transconductors used for g_{m1} and g_{m2} are shown in Fig. 3. The g_{m1} transconductor, Fig. 3(a), consists of two differential pairs connected in a doublet arrangement with input transistor width ratio 5:1. This ratio is chosen to maximise the differential input range for a Total Harmonic Distortion (THD) of 1% [16]. For nominal operation the bias current is set at 200 pA. The g_{m2} transconductors for the buffers, Fig. 3(b), consist of basic differential pairs with their outputs connected to the negative inputs for unity voltage gain. The bias current is set at 1 nA and since these buffers operate well below their bandwidth their inputs are approximately equal and they contribute little to distortion in the overall filter.

To bias the circuit an internal current mirror with current scaling is included on-chip so that only one external current source, set at 1 nA, needs to be applied. The designed transconductors are not temperature compensated and as such either PTAT (Proportional To Absolute Temperature) biasing or a temperature dependent duty cycle is required to give correct operation over large temperature changes. A suitable 2 nW current source is reported in [17], [18] but is not included here. For testing, the clock and bias current are generated off-chip using an HP8112A and Keithley 236 respectively and the filter output voltage is buffered to drive the test equipment. Neglecting the digital clock and bias generation the overall circuit thus draws approximately 5 nA from the 1 V supply.

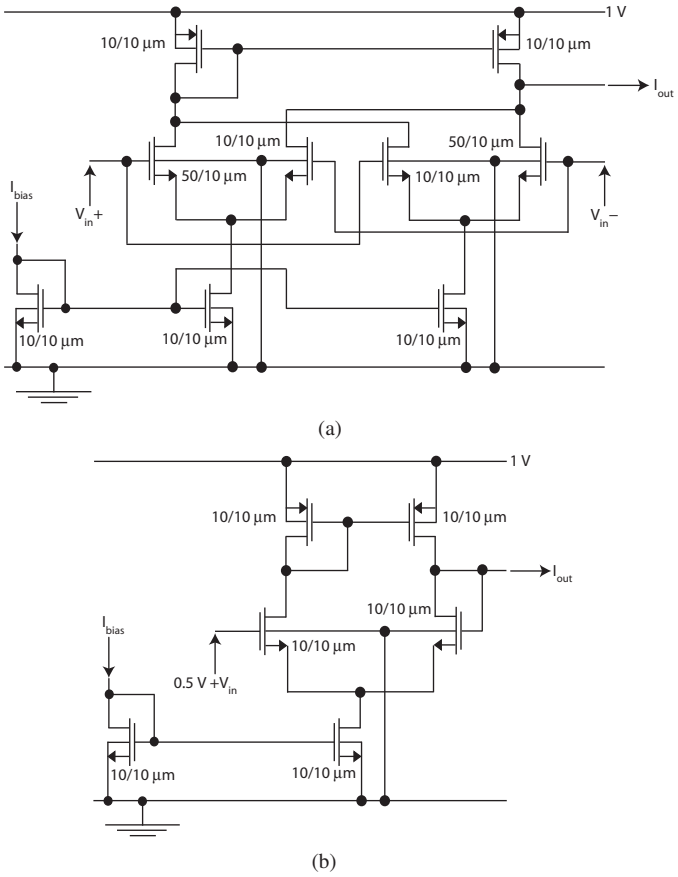

Fig. 3. Transconductors used for the filter implementation. (a) The filter transconductor (g_{m1}) uses a doublet arrangement with 5:1 width ratio. A 0.5 V common mode signal is required at the input for correct operation. (b) The buffer transconductors (g_{m2}) are differential pairs in a unity gain configuration.

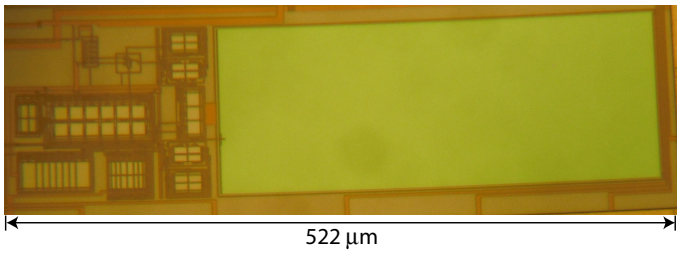

Fig. 4. Micro-photograph of the fabricated circuit.

III. Experimental results

The proposed clocked transconductor based low pass filter has been fabricated in the austriamicrosystems 0.35 μm, single well, 2 poly, 3 metal process, and a micro-photograph of the fabricated circuit is given in Fig. 4.

Fig. 5 then shows the Bode magnitude response from 10 measured samples using a 200 pA/1 nA bias, and 1 kHz clock with 10% duty cycle. This gives a relatively high 1 Hz cut-off frequency for increased measurement speed. Two readings from each chip are present to demonstrate the repeatable operation of the filter, with 10 averages taken per reading. The mean 3 dB cut-off frequency present is 1 Hz with a standard deviation of 0.06 Hz.

Under the same biasing conditions the output noise integrated between 20 mHz and 1 Hz has been measured as 32 μV_{RMS} and the largest in-band THD measured as 0.96% for a 140 mV_{pp} 1 Hz input signal. The filter dynamic range is thus in excess of 60 dB. These measured filter parameters are summarised in Table I.

The tuning range of the filter is illustrated in Fig. 6. Using the same bias conditions as above, decreasing the duty cycle to 0.0025% lowers the filter cut-off frequency to 2 mHz. 0.0025% is a low duty cycle, but from a 1 kHz clock the 25 ns clock high-time corresponds to a 20 MHz component, which is still feasible to implement. Alternatively, increasing the bias current to 4 nA/20 nA and the clock frequency to 20 kHz with a 50% duty cycle, a 90 Hz cut-off is achieved. Overall, a greater than a four decade range in tunablity is possible and the cut-off tuning curve is shown in Fig. 7. The topology is thus highly versatile for use in a range of applications.

Note, however, that a high frequency parasitic is present:

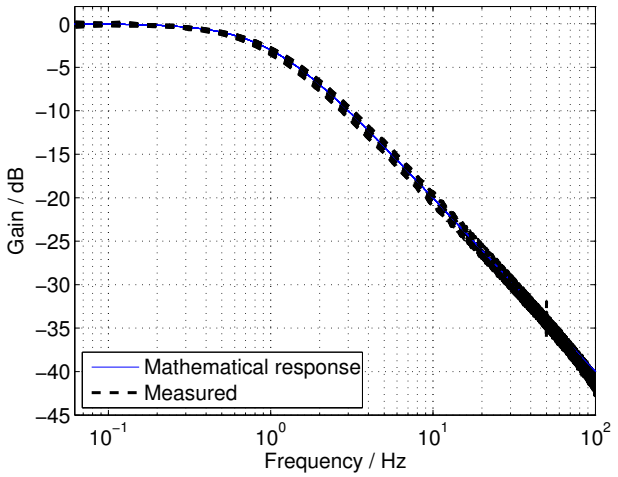

Fig. 5. Bode magnitude responses from 10 measured samples (2 measurements per sample) show robust low frequency operation of the filter.

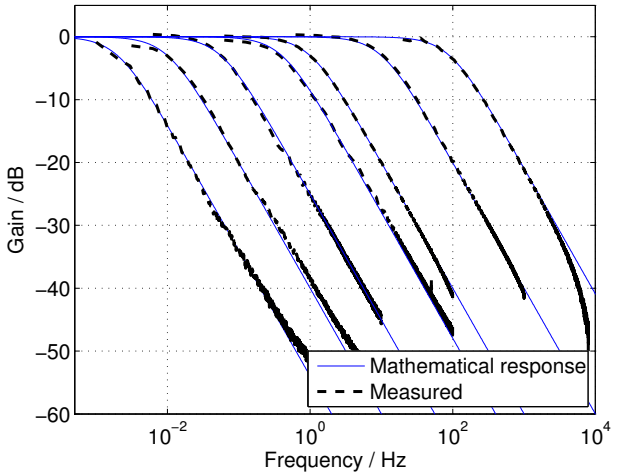

Fig. 6. Tuning range of the fabricated filter goes from 2 mHz to 90 Hz cut-offs. The following settings are used for these results in the format [Bias, Clock frequency, Duty cycle, Cut-off frequency]: [200 pA/1 nA, 1 kHz, 0.0025%, 2 mHz], [200 pA/1 nA, 1 kHz, 0.025%, 10 mHz], [200 pA/1 nA, 1 kHz, 10%, 1 Hz], [2 nA/10 nA, 10 kHz, 0.025%, 56 mHz], [2 nA/10 nA, 10 kHz, 0.25%, 400 mHz], [2 nA/10 nA, 10 kHz, 10%, 10 Hz], [4 nA/20 nA, 20 kHz, 50%, 90 Hz].

its effect can be seen at approximately 5 kHz for the 90 Hz cut-off filter in Fig. 6. Also, Fig. 8 illustrates the gain of the filter for input frequencies from the pass band to five times the clock frequency used. This shows that all input frequencies are attenuated, except at the clock frequency and harmonics of it. For correct operation the amplitude of inputs at these frequencies should thus be kept low. Since the clock frequency can be set to be much higher than the bandwidth of the signals typically encountered in low frequency applications this constraint is generally not difficult to satisfy.

Finally, Table II compares the results obtained here to other low frequency low pass filters and integrators reported in the literature. For conciseness only implementations with experimental results that have been reported since the year 2000 are included in this table. It can be seen that the filter

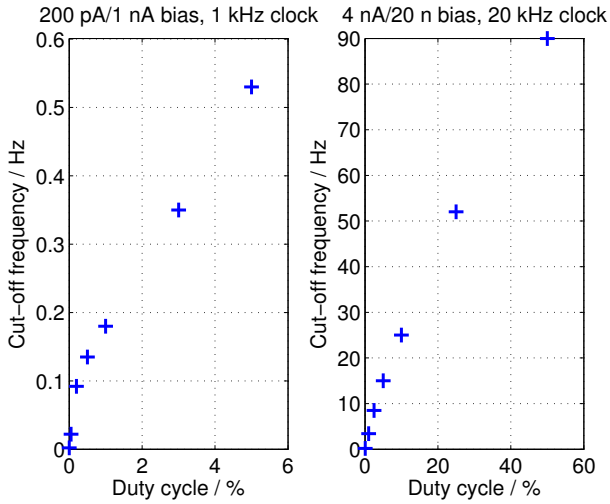

Fig. 7. Tuning curve showing how the filter cut-off frequency is controlled.

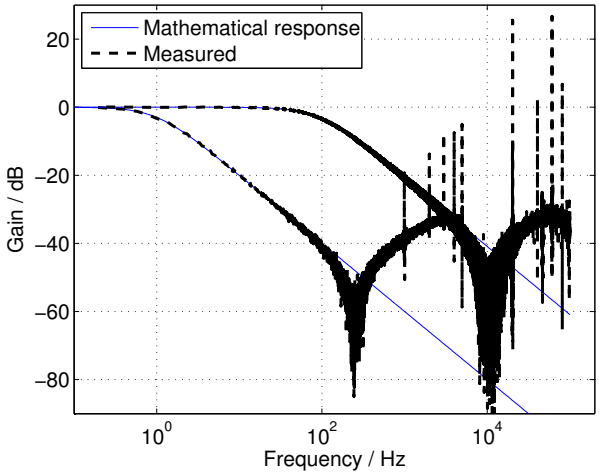

Fig. 8. Response of the filter to inputs at frequencies up to five times the clock frequency for the [200 pA/1 nA, 1 kHz, 10%, 1 Hz] and [4 nA/20 nA, 20 kHz, 50%, 90 Hz] bias conditions.

presented here has the lowest frequency cut-off, supply voltage and power consumption of all of the considered designs. This is achieved without a noticeable increase in area. The proposed clocked transconductor topology is thus highly suitable for use in low power, low voltage sensor interfaces and in portable medical instrumentation.

IV. Conclusions

A very low frequency, going down to sub-Hertz cut-offs, low pass filter topology has been presented showing excellent characteristics when compared with results in the literature. Operation is based upon using a switch at the output of a transconductor in a g_mC filter to decrease the value of the transconductance and to increase the output resistance. This allows very low transconductance values to be achieved, and the clock signal facilitates easy digital tuning. Measured results showing sub-Hertz operation with a current draw of 5 nA have been presented. In comparison to previous low pass filters from

TABLE II
COMPARISON OF PROPOSED TOPOLOGY PERFORMANCE WITH OTHER REPORTED LOW FREQUENCY LOW PASS FILTERS.

Ref.	CMOS process / μm	Minimum cut-off / Hz	Filter order	Power consumption / W	Supply voltage / V	Dynamic range / dB	Area / mm^2	Integrating capacitance per pole / F
[19]	0.35	35.0	1	–	3.2	–	0.025	25f
[8]	0.80	02.4	6	010μ	3.0	60	1	05p
[11]	0.35	01.5	2	165μ	3.3	60	0.336	52.5p
[10]	0.80	500m	2	002μ	1.5	70	–	–
[7]	0.35	500m	1	–	–	–	–	100f
[13]	0.80	302m	1	113n	–	65.4	0.2	50p
[20]	0.35	250m	2	–	3.0	40	–	29p
[21]	0.50	180m	1	77.4n	–	61.4	0.035	15p
[12]	1.20	170m	2	08.2μ	2.7	70.5	0.06	10n[a]
[2]	0.80	100m	1	230n	3.0	–	0.1	70p
[1]	1.00	075m	1	–	5.0	–	0.25	10p
This work	0.35	002m	1	005n	1.0	63.8	0.07	40p

[a]Off-chip

TABLE I
SUMMARY OF MEASURED CIRCUIT PERFORMANCE.

CMOS process technology	0.35 μm
Power supply	1 V
Area	0.07 mm^2
Nominal current consumption	5 nA
Output noise (20 mHz – 1 Hz)	32 μVrms
THD (1 Hz, 140 mV$_{pp}$ input)	0.96%
Dynamic range	63.8 dB
Input common mode range	400 mV – 550 mV
PSRR+ (1 Hz, 100 mV$_{pp}$ V$_{DD}$ input)	-55 dB
Cut-off tuning range	2 mHz – 90 Hz

the literature the proposed topology provides the lowest cut-off and power consumption seen, in addition to a very wide tuning range.

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