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A Subsampling UWB Impulse Radio Architecture Utilizing Analytic Signaling

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SUMMARY This paper describes a system architecture along with signal processing technique which allows a reduction in the complexity of a 3.1–10.6 GHz Ultra-Wideband radio. The proposed system transmits passband pulses using a pulser and antenna, and the receiver front-end down-converts the signal frequency by subsampling, thus, requiring substantially less hardware than a traditional narrowband approach. However, the simplified receiver front end shows a high sensitivity to timing offset. By proposing an analytic signal processing technique, the vulnerability of timing offset is mitigated; furthermore, a time resolution finer than the sampling period is achieved, which is useful for locationing or ranging applications. Analysis and simulations of system specifications are also provided in this paper.

key words: *UWB, subsampling, impulse radio, analytic signaling, wideband circuit*

1. Introduction

UWB technology was approved by the FCC in 2002 [1], and has since drawn considerable attention for a variety of applications, including imaging, surveillance, high-speed data communication and locationing. One of the most attractive applications is for indoor communication systems which are allowed to operate in the frequency band from 3.1 to 10.6 GHz. The interest in these indoor systems extends from high-speed and short- range systems to low data rate communications and precision ranging, as seen in the standard efforts of IEEE 802.15.3a/4a. Regardless of application, it is very crucial to design with low cost and low power; especially as many of these applications intend to deploy a large volume of inexpensive UWB mobile devices that must operate with the longest possible battery life.

The main goal of this work is to improve the efficiency of UWB implementation using signal processing techniques. In particular, an approach will be described that takes advantage of UWB pulses which are narrow in time (with a timescale on the order of a nano-second) to achieve a fine time resolution for ranging. The proposed system architecture [2] is compared to traditional heterodyne transceiver described in Sect. 2. Section 3 explains the challenges of implementing a subsampling front-end and the reasons why it is advantageous to UWB implementation. Digital analytic signal processing for synchronization, detection and ranging will be highlighted in Sect. 4. Section 5 describes the approach to determine system specification. System-level simulations using measured pulse shape and noise are performed to verify system specifications and tradeoffs in Sect. 6.

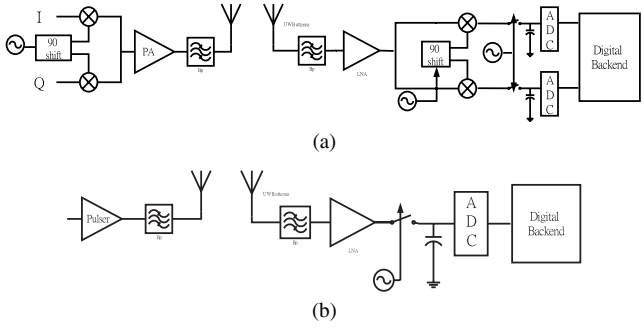

Fig. 1 Transceiver of (a) one-stage heterodyne (b) subsampling radio.

2. Transceiver Architecture Advantages

The proposed system follows the concept of impulse radio [3], [4] rather than heterodyne transceiver, the most popular architecture in existing narrowband systems. Shown in Fig. 1, a heterodyne transmitter modulates the baseband information onto a sinusoidal carrier through analog mixers. In contrast, an impulse radio simply uses a pulser to drive the antenna, and radiates a passband pulse (between 3.1–10.6 GHz) shaped by the impulse response of the wideband antenna. The hardware elimination of mixers and local oscillators required for mixing imply lower complexity implementations.

On the receiver side, the heterodyne system utilizes one or two mixing stages to down-convert the passband signal back to baseband prior to the ADC. The proposed receiver directly samples the incoming signal after amplification. The sampled data will be processed by a digital matched filter in order to reach the matched filter bound for optimal detection [5]. The proposed system avoids wideband analog processing by adding more processing to the digital backend, which results in a more efficient solution.

3. Analog: Subsampling Front End

In this section we will first review the fundamentals of subsampling theory and then discuss what makes it suitable for ultra-wideband systems.

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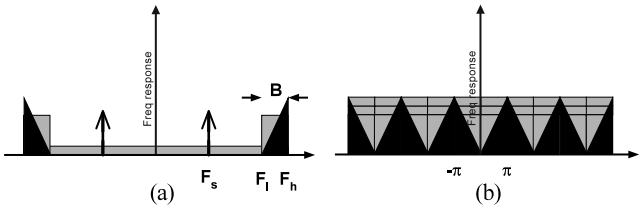

Fig. 2 Signal and noise spectrum (a) before and (b) after subsampling. The black color is wanted signal, and the gray one represents noise, assuming a sufficient out-of-band blocking.

3.1 Theory Background and Challenges

Subsampling front end directly samples the passband signal at twice the signal bandwidth instead of the maximum signal frequency. The signal is bandlimited from F_{l} to F_{h} (Hz), and the sampling frequency is F_{s} (Hz), as shown in Fig. 2. By carefully choosing F_{s}, F_{l} and F_{h}, a non-aliased sampled spectrum can be derived [6]. For example, if the lower or upper frequency bound, i.e. F_{l} and F_{h}, is a non-negative integer multiple of the signal bandwidth, B, the signal aliasing can be avoided at the minimal uniform sampling rate, $2B$,

$$F_l = n \cdot (F_h - F_l) = n \cdot B, \quad \text{where} \quad n \in N.$$

An undersampling ratio, K, is defined as, $\lfloor F_h/2B \rfloor$, the largest integer but smaller than $F_h/2B$. This ratio is a good indication of the amount of aliasing effect, which will be seen later.

There are several key challenges about subsampling that prohibit it from being popular in existing narrowband systems. First of all, the noise spectrum from $-F_{\mathrm{l}}$ to $+F_{\mathrm{l}}$ will alias into the signal band and thus deteriorate the passband SNR, assuming the receiver bandwidth is F_{h}. Even if the receiver can afford a perfect anti-aliasing filter, the circuits after the filter, such as the sample and hold or buffer stages, still contribute thermal noise. Therefore, if the receiver noise is dominated by these circuit noise sources, the passband SNR degradation is proportional to the undersampling ratio, K, which can be on the order of hundred's for a narrowband system. In reality, there is no perfect anti-aliasing filter. However, the higher the undersampling ratio, the harder it is to implement such a filter, which will be elaborated in the system specification section. Secondly, it is more difficult to design a good bandpass (anti-aliasing) filter at RF frequency band than IF or baseband. As mentioned earlier, insufficient attenuation of out of band noise causes more degradation in signal SNR. Traditionally, these high Q bandpass filters are implemented off-chip, which unavoidably increases the cost and power consumption. Finally, the incoming signal frequency is actually higher than the sampling frequency; therefore the receiver's tracking bandwidth needs to cover the maximum signal frequency range and sampling jitter causes even more degradation of the SNR. If one models the jitter-induced error as another noise source, the noise power increases with input signal frequency [7]. Therefore, directly sampling at RF frequency introduces more noise power than IF or baseband frequency.

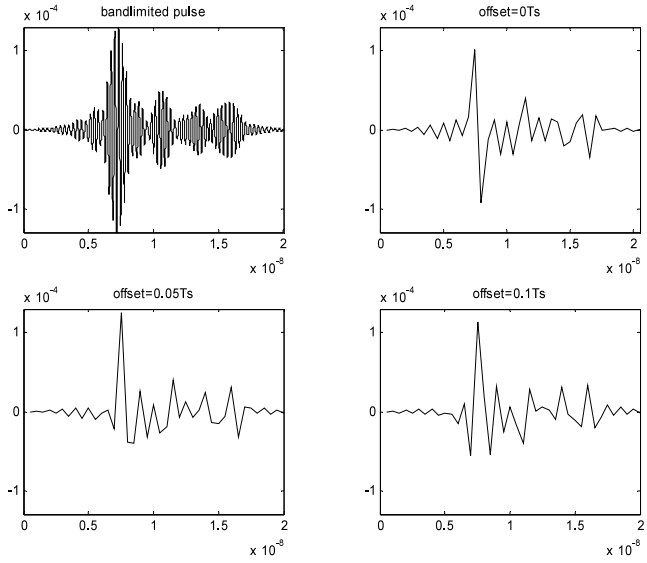

Fig. 3 Bandpass pulse (top left) and subsampled waveform with $0Ts$ (top right), $0.05Ts$ (bottom left), $0.1Ts$ (bottom right) sampling offset.

3.2 Subsampling for UWB

Interestingly, the challenge of subsampling is relaxed in the UWB case. For example, if a 1 GHz wide pulse is transmitted between 3 to 4 GHz, and sampled at 2 Gsa/s, then the undersampling ratio is only two, much smaller than a narrowband system. Moreover, as the UWB signal has such a wide bandwidth; at least 500 MHz by FCC regulations, the noise spectrum will be most likely dominated by in-band ambient noise and potential interference received from other wireless systems, as illustrated in Fig. 2. Therefore, the SNR degradation due to aliasing will be much smaller compared to narrowband systems. Next, the difficulty of implementing a RF bandpass filter is also relaxed by the lower filter Q, which is less than ten in UWB, enabling the integration of a CMOS implementation. Except, in the case of strong out-of-band interference close to the signal band, a high-Q notch filter can help improve system SNR. In the system specification section, we will have more discussions on bandpass filtering. Lastly, the lower ADC dynamic range due to large in-band noise and vulnerability to interference will reduce the sampling jitter constraint. Our system level simulations in Sect. 6 also verify the relatively lower dynamic range requirement.

3.3 Timing Sensitivity Issue

While most of the challenges of subsampling become feasible for UWB, the architecture still suffers from sampling offset, which can be introduced by frequency mismatch between the TX and RX oscillators or changes of pulse arrival times. The sampled waveform will change dramatically due to this sampling offset, which can deteriorate the

SNR of matched filter outputs because of the mismatch between the incoming pulse shape and matched filter response. The impact of the matched filtering mismatch on system performance was studied in [8] and showed a vulnerability to the sampling offset, which will be called timing sensitivity. In fact, the timing sensitivity is more significant in subsampling than Nyquist sampling given the same sampling frequency, since the variation in the waveform significantly complicates the design of digital matched filter. Using measured UWB pulses that are bandlimited to 3–4 GHz, the impact of sampling offset on sampled waveform is shown in Fig. 3. An analytic signaling approach described in the next section is thus proposed to alleviate this problem.

4. Digital: Analytic Signal Processing

The main functionality of the digital backend is to perform synchronization and data recovery. In narrowband communications, synchronization is comprised of timing recovery and carrier frequency compensation. Since there is no sinusoidal carrier in an impulse radio, the synchronization issue becomes only timing recovery. Timing recovery is typically done via oversampling or interpolation [9]. But, the cost of these approaches in UWB radio is very high due to the large bandwidths involved.

4.1 Proposed Baseband Processing

The first priority of digital backend is to solve the high timing sensitivity problem. By understanding the relationship between sampling offset and the sampled waveform, the solution to reduce timing sensitivity will become clear. If a bandlimited signal, $s(t)$, is sampled at $1/Ts$, any sampling offset, To, of the sampling sequence will transform into a phase shift in frequency domain, as seen,

$$s(t)\cdot\sum\delta(t-k\cdot Ts-To)\overset{\text{F.T.}}{\Leftrightarrow}S(\omega)$$
$$*\sum\delta\left(\omega-k\frac{2\pi}{Ts}\right)\cdot e^{-jk\frac{2\pi}{Ts}To}.$$

Since the timing offset corresponds to phase shift, a naïve approach is to eliminate the phase term by calculating the magnitude of signal's spectrum through FFT. In other words, a power spectral density (PSD) matched filter can be insensitive to the sampling offset. However, the scheme is far from optimum particularly when the sampling offset is small due to the loss of phase information. In fact, it cannot perform synchronization, phase demodulation or exploit any timing resolution that UWB potentially offers. Therefore, a better approach needs to be proposed for achieving both optimality and timing insensitivity.

Without the loss of signal information, energy detection can also be decoupled from the phase shift, if we formulate an analytic signal, $y(t)$. It can be generated through Hilbert transformer [10], as follows,

$$y(t)=s(t)+j\cdot\hat{s}(t),\quad\text{where}\quad\hat{s}(t)=s(t)*h_{\text{hilbert}}(t).$$

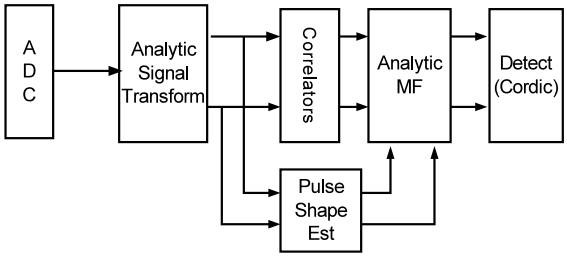

Fig. 4 Digital backend block diagram.

The Hilbert transformer is implemented in digital domain, and its ideal frequency response can be expressed as, $H_{\text{hilbert}}(\omega)=-j\cdot\text{sign}(\omega)$, where sign() is the signum function.

The most significant benefit of analytic signal lies in its real and imaginary parts being orthogonal, and the phase information can be studied on the Euler plane. As sampling offset varies, the signal energy moves between these two orthogonal dimensions. Later, we will show that with appropriate usage of the analytic signal, one can reduce the timing sensitivity or resolve timing information. Another benefit of formulating analytic signal is the possibility to halve digital clock rate after shifting $\pi/2$ in digital domain.

Figure 4 is the block diagram of the proposed digital backend. The main components are pulse shape estimator, analytic signal transformer, correlators, analytic matched filter, and detection block. The first task of signal detection is to determine the matched filter response through the pulse shape estimator. It requires a training sequence to learn the received pulse shape. Assuming the training period is within the channel coherence time, it is shown that doing a running average is the best unbiased linear estimator to estimate the mean of the received signals, i.e. the pulse shape, in the sense of minimizing mean square error [11]. The correlation block is used to provide additional processing gain or despread any possible coding that is modulated on the pulses.

The analytic matched filter response is similar to a real-valued matched filter except with complex conjugation on the time-reversed signal. The filter response is,

$$h_{\text{MF}}(t)=s^*(T-t).$$

Therefore, the analytic matched filter takes the pulse estimator results and convolves with the incoming analytic signals. The outputs of matched filter are then followed by a detection block, which is used for synchronization and data recovery. A Coordinate Rotation Digital Computer (Cordic) block can be used to calculate the phase and magnitude of the complex signal, which are essential for signal detection.

4.2 Performance Comparison

A system simulation is used to compare the proposed analytic signal processing with other alternative approaches and illustrate how to achieve synchronization, detection; and ranging capabilities based on the proposed system. More

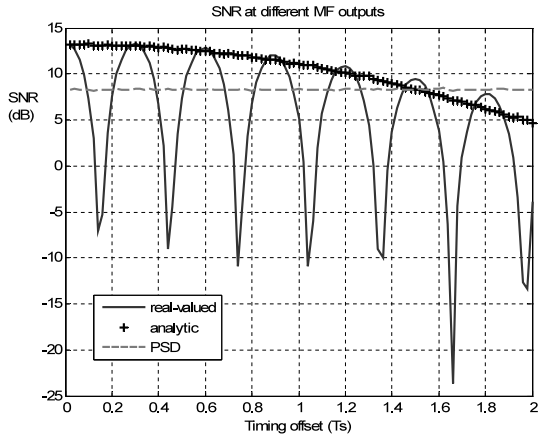

Fig. 5 SNR comparison of real-valued processing (solid), magnitude of analytic signal processing (+) and PSD processing (dashed) with 0 to $2Ts$ timing offset.

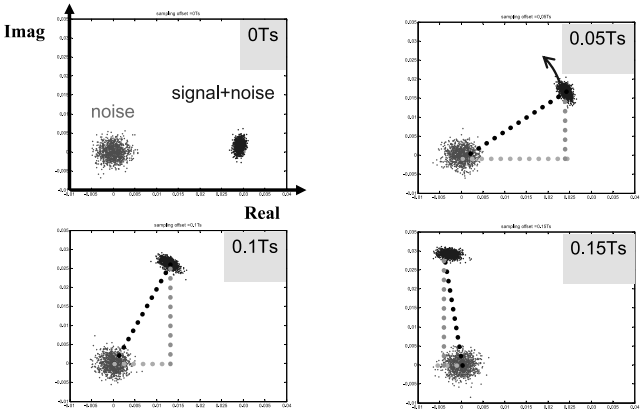

Fig. 6 Plots of analytic matched filter outputs corresponding to {0, 5, 10, 15}% of Ts timing offset.

details of system-level simulation are provided in Sect. 6.

As illustrated in Fig. 5, the output SNR of the real-valued matched filter has periodical null points as the timing offset increases. By utilizing the magnitude of the analytic and PSD matched filter, one can avoid null SNR points. Since PSD matched filter approach entirely throw away phase information, the SNR degradation is significant in the lower offset regime. Therefore, in order to reduce the vulnerability to the timing offset while approaching matched filter bound, analytic signal processing is essential to alleviate the limitations of using a subsampling front-end.

The result can be explained from Fig. 6, where the analytic matched filter outputs are plotted on Euler coordinates. 10,000 experiments were simulated with and without signal existence. Each graph differs only in sampling offset. The results show that an offset of even 5% of the sampling period could rotate the complex signal about 30 degrees. If a real-valued matched filter was used rather than an analytic one, the real-valued matched filter output is essentially the projection onto the real axis. The reason why timing sensitivity is particularly high for subsampling can be understood by the phase shift term, $\exp(-2\pi kTo/Ts)$. The rotation angle is proportional to the ratio of To/Ts, and undersampling ratio, k. In other words, the spacing between the nulls in Fig. 5 is inversely proportional to the ratio, k. Note that the Euclidean distance between the two clouds remains about the same, as opposed to the real axis projection always going to zero when the signal energy resides in imaginary component. Thus, the magnitude of analytic signal avoids nulls with respect to timing offset.

4.3 Extended Usage of Analytic Signal for Ranging Applications

For the purpose of synchronization or data recovery, the timing sensitivity should be kept as small as possible. However, for ranging purpose, the high sensitivity to timing offset implies a high time resolution for the system. As the timing offset can be caused by pulse delay, we may make use of this to measure the distance between transmitter and receiver. In order to determine the pulse delay, the receiver must learn the oscillator mismatch in the training sequence. Also note that the high time resolution is derived from the following: the wide bandwidth of UWB signal, the interpolation effect from the center oscillation frequency, and the phase information extracted from analytic signal processing. Therefore, the higher the frequency band or undersampling ratio, the finer the time resolution this system can achieve. Finally, the accuracy of ranging depends on how fine the receiver can resolve the angle, which is directly related to the SNR of analytic matched filter output. It implies a longer spreading code can help achieve finer resolution. In this particular example we used, 90-degree phase shift corresponds to about one-inch accuracy.

5. System Specifications Analysis

A first-order link budget analysis including circuit implementation loss will be provided for the entire receiver chain up to ADC. The analytical approach is to treat each individual non-ideality as an independent and additive noise source. The circuit specification of each block should be made to minimize the implementation loss, defined as the gap between output and received SNR. The received and output SNR can be expressed as:

$$SNR_{\text{received}} = \frac{P_{\text{signal}}}{P_{\text{ambient}}},$$

$$SNR_{\text{out}} = \frac{P_{\text{signal}}}{P_{\text{ambient}} + P_{\text{ckt}} + P_{\text{jitter}} + P_{\text{SH}} + P_{\text{adc}}}.$$

P_{signal}: received signal power;
P_{ambient}: received ambient thermal noise plus interference power within communication band;
P_{ckt}: input-referred thermal noise power caused by amplifiers and filters;
P_{jitter}: input-referred clock jitter induced sampling noise;
P_{SH}: input-referred sample and hold (subsampling mixer) noise;

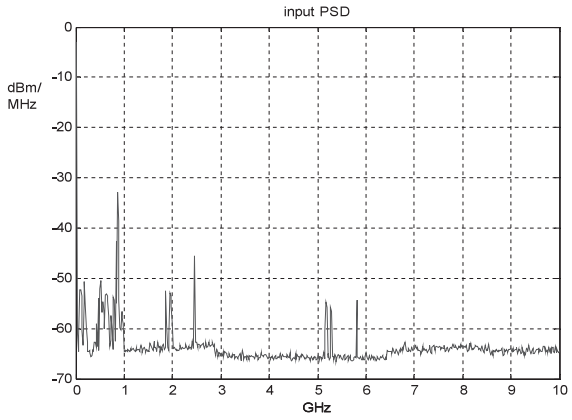

Fig. 7 Measured noise and interference using TEM horn antenna.

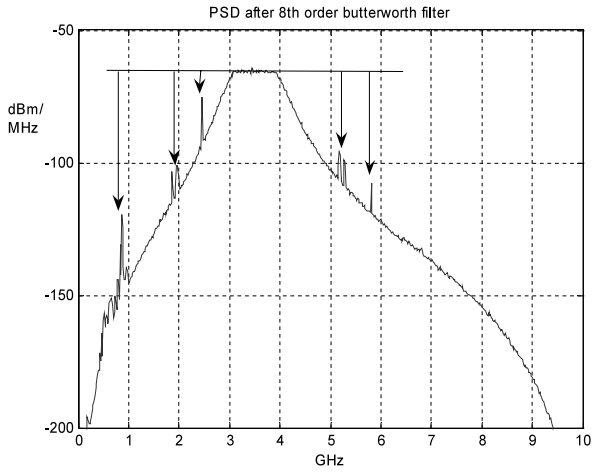

Fig. 8 Spectrum after 8th order Butterworth bandpass filter.

P_{adc}: input-referred quantization noise power of ADC.

The following analysis is based on transmitting a 1 GHz UWB pulse centered at 3.5 GHz with a sampling rate of 2 Gsa/s. However, one may easily apply this analytical approach to a different communication band and sampling frequency as long as there is no signal aliasing. Later, we will include these realistic circuit impairments into system-level simulations using measured noise and interference samples.

5.1 Received SNR

According to FCC regulation [1], the transmission power spectral density has to be under −41 dBm/MHz. Given a 1 GHz wide signal bandwidth, the maximum transmission power is −11 dBm. The received power however gets attenuated through the wireless channel. According to our S21 measurements using spiral and elliptical wideband antennas [12] as well as literature reports [13], [14], the path loss can be 40 to 60 dB from 1 to 10 meters between transmitter and receiver. Therefore, the expected received signal power in the following analysis is within −51 to −71 dBm range.

The ambient noise level is strongly coupled with the operation environment. Figure 7 shows a noise spectrum measured by TEM horn antenna and spectrum analyzer (HP 8563E) in the lab of Berkeley Wireless Research Center (BWRC), USA. The measured data was recorded one whole day with maximum and hold, which represents the worst-case scenario. Most of the interference comes from < 1 GHz, the 1.9 GHz PCS band, and the 2.4 GHz ISM band. Note that due to the popularity of WiFi systems, we also measured interference from the 5 GHz UNI band. From the measurement results, received interference power can vary from −50 to −30 dBm. The received thermal noise power under a power matched front-end is −174 dBm/Hz [15]. For 1 GHz bandwidth and ideal bandpass filtering, the total thermal noise power is −84 dBm, which sets the minimum bound on noise level.

5.2 Bandpass Filter Response

The aggregate receiver response, including antenna, matching network, amplifiers and filters, requires a bandpass response for image rejection and channel selection if a multiband operation is desired. As mentioned earlier, due to the wideband nature (low Q) of UWB, the requirement of bandpass filtering is largely relaxed as opposed to narrowband system. From thermal noise perspective, the undersampling ratio (less than 10) determines the required stop band attenuation in order to suppress the aliased out-of-band thermal noise well below in-band noise level. Nevertheless, the real requirement of stop band attenuation depends on out-of-band interferers in Fig. 7. The unfiltered out-of-band interference will alias back to the signal band and corrupt the SNR. The proposed bandpass response attenuates any out-of-band interference at least 10 dB below in-band thermal noise level. Shown in Fig. 8, an 8th order Butterworth bandpass filter between 3 to 4 GHz meets the requirement. Note that one may relax the order of bandpass response if additional notch filter is used to block high interference band.

5.3 Gain

Sufficient gain is required to amplify the input received level to the full swing of the ADC in order to fully utilize its dynamic range. On the other hand, the gain should be limited to avoid saturating front end. Saturation of receiver will cause large distortion as well as enhancing noise power. Not only is it difficult to perform good matched filtering in the digital domain, but we also lose the ability to reject in-band interference by any digital signal processing technique. As described in Sect. 5.1, the input received power is within −51 dBm to −71 dBm. If a passband UWB pulse in Fig. 2 is used, the peak signal level varies from 100's μV to a couple mV, assuming there is no further duty cycling. According to FCC's regulation, one may increase the pulse energy by lowering pulse repetition rate up to 20 dB. If a system adopts

duty cycling, one should further reduce receiver gain.

On the noise side, considering 1 GHz thermal noise (−84 dBm) plus 20 dB margin for noise figure of receiver front-end, aliased noise power and insertion loss of matching network, the standard deviation is about 200 μV on 50 ohm input impedance. Since the signal and noise are independent, the total received signal variance is the summation of the two. For the pulse shape we measured, the total received signal standard deviation is around 1 mV. Using three-sigma rule, the input-referred single-ended swing is about 3 mV for 0.3% probability of saturation. As the supply voltage of CMOS process keeps scaling down, the input full swing of ADC is reduced to the order of 100's mV, especially for high-speed operation. This implies the gain should not exceed 40 dB. Note that this analysis does not consider AGC loop in order to reduce the receiver complexity.

5.4 Sampling Clock

The only oscillator required in the subsampling front-end is the sampling clock. The two most important specifications of clocking are precision and jitter. As illustrated in Fig. 6, the sampling offset will rotate the analytic matched filter output, which in turn limits the number of pulses that can be used for pulse shape estimation. The proposed specification on clock precision constrains the sampling offset to at most 1% of the sampling period during the channel estimation phase, which is about a 6 degree rotation. For example, a 10 ppm, 100 MHz oscillator can tolerate about 50 pulses for channel estimation, calculated by the following equation:

$$\frac{1}{f_{\text{osc}}} \cdot \frac{P_{\text{off}}}{10^6} \cdot (\#\ \text{cycle/pulse}) \cdot (\#\ \text{pulses}) \leq T_s \cdot 1\%$$

f_{osc}: oscillator frequency
P_{off}: clock frequency offset measured in part per million (ppm)
cycle/pulse: number of oscillator cycles within a pulse repetition period
pulses: number of pulses required for channel estimation

Another critical specification of the clock is jitter, especially for a subsampling receiver. In a traditional worst-case jitter analysis, the clock is assumed to sample at the sharpest edge. Jitter is constrained such that it contributes negligible noise compared to one LSB of ADC. For example, a 4-bit ADC sampling 5-GHz sine wave requires jitter less than 4 pico-seconds. However, for a UWB signal, the energy is distributed over a wide frequency band. Thus, a worst-case analysis is too pessimistic. A noise modeling considering the input signal spectrum is more appropriate [16].

$$P_{\text{jitter}} = \int_{-\infty}^{\infty} |S(j\omega)|^2 \left(1 - e^{\frac{-\omega^2\sigma_j^2}{2}}\right) d\omega$$

$S(j\omega)$ is the signal spectrum and ω_j is the RMS jitter.

Once the UWB pulse is known, one may calculate the jitter induced noise power for the link budget analysis. In the next section, we will perform system simulations to get more insights on the impact of clock jitter.

5.5 Subsampling Mixer and ADC

Conventionally, quantization noise power contributed from ADC is modeled as $\text{LSB}^2/12$ assuming quantization noise is uniformly distributed [10]. As bit resolution decreases, this noise modeling becomes less accurate. Therefore, we will determine the ADC resolution in system simulations. In a back of envelope calculation, the quantization noise power of a 4-bit ADC is about the same as ambient noise given in Sect. 5.3.

The sample and hold circuit (subsampling mixer) can be modeled as an RC lowpass network. All the thermal noise contributed from this stage will entirely alias back to the signal band, and the total power is the well-known kT/C noise, where C is the sampling capacitance. Interestingly, this aliased thermal noise power does not degrade the overall system performance given the resolution of ADC targeted for this system. For example, a sampling capacitance larger than 10's fF has negligible thermal noise for 8-bit ADC. Note that the tracking bandwidth of sample and hold block has to cover entire frequency band, which benefits from technology scaling.

6. System Simulations

While the previous section provides an analytical approach of designing the proposed system, we now include these circuit non-idealities into system-level simulations using measured noise samples. The simulation takes measured pulses generated from a pulser and TEM horn antenna, whose frequency response is flat between 3 to 10 GHz. For interference and noise, sixty million samples were acquired by the TEM horn antenna and Agilent DSO (54855A), which is capable of sampling at 20 Gsa/s. The measured pulse shape and noise samples were post-processed in Matlab. The pulse is bandlimited to 3–4 GHz and subsampled at 2 Gsa/s.

Figure 9 shows the simulation framework. Signal and noise are each oversampled at higher rates and filtered by the same bandpass (anti-aliasing) filter. A random jitter can be introduced while downsampling to 2 Gsa/s. The system simulation allows us to investigate input sensitivity, clock jitter, bandpass filter response, gain, ADC bits along with the whole digital signal processing blocks. For the time being, we will focus only on the specifications of analog blocks, while keeping all the digital blocks in floating point. Digital implementation can be easily built upon

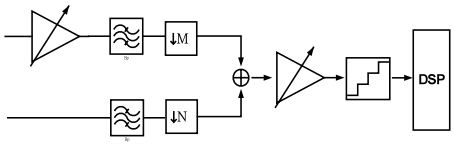

Fig. 9 Block diagrams of system simulation framework.

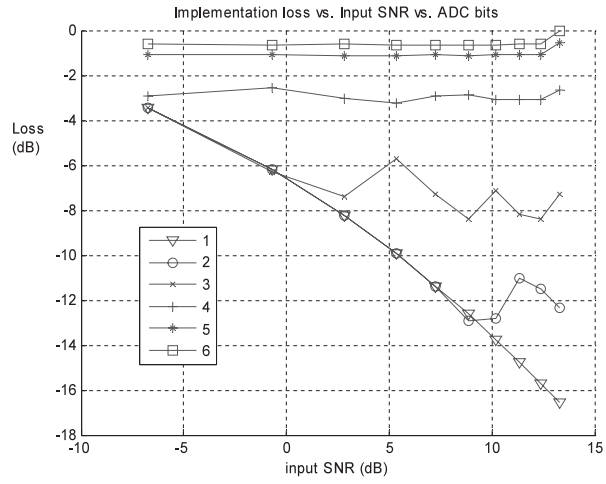

Fig. 10 Implementation loss versus input SNR and ADC bits.

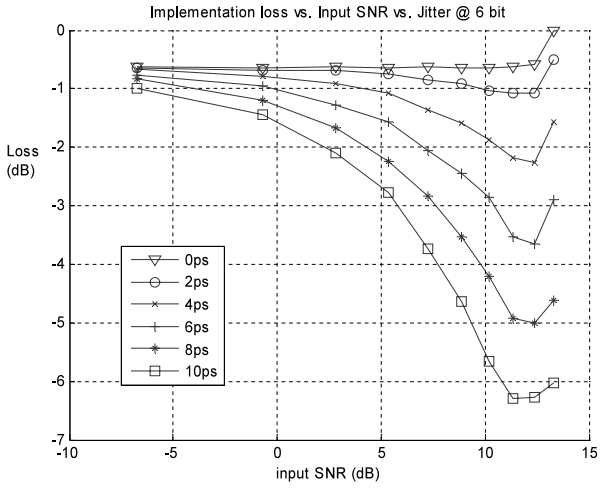

Fig. 11 Implementation loss versus input SNR and Jitter.

this Matlab/Simulink framework using our in-house digital FPGA/ASIC design flow [17], [18]. A previously designed UWB digital baseband for DC-1 GHz band is one example of using this fast silicon prototyping approach [19].

The figure of merit of the proposed design methodology is implementation loss between input (received) SNR and analytic matched filter output SNR, which is measured without any sampling offset or channel estimation error. Next, the relationship between implementation loss and critical system parameters, such as ADC bits, jitter, in-band interference level, and input SNR, will be examined.

• ADC Quantization effect

The input signal level is scaled from −51 dBm to −71 dBm as explained in Sect. 5.1. Shown in Fig. 10, more than 4-bit quantization is sufficient to keep implementation loss within 3 dB for all input SNR. This is fairly close to hand analysis results. Note that, in the low SNR region, 1-bit ADC does not degrade system performance by much.

• Jitter

In the jitter simulation, a 6-bit ADC is used and RMS jitter varies from 0 to 10 picoseconds. Figure 11 shows that a jitter greater than 6 picoseconds can cause more than 3 dB implementation loss. The jitter requirement is relatively stringent; however a fixed frequency clock tends to produce less phase noise than a tunable frequency one [20]. We can also conclude that jitter induced noise dominates the total noise power in high SNR region.

• In-band interference Immunity

Depending on the operating environment, UWB is highly vulnerable to the in-band interference. Therefore, we purposely inject an in-band sine wave to investigate the interference immunity. The simulation results do not include any interference cancellation that can be potentially incorporated into the system. Observing from Fig. 12, larger than −40 dBm interference power in general degrades system performance more than 3 dB, because the input-referred saturation level is set around 3 mV (amplitude of −40 dBm interference on 50 ohm impedance). Therefore, input-referred

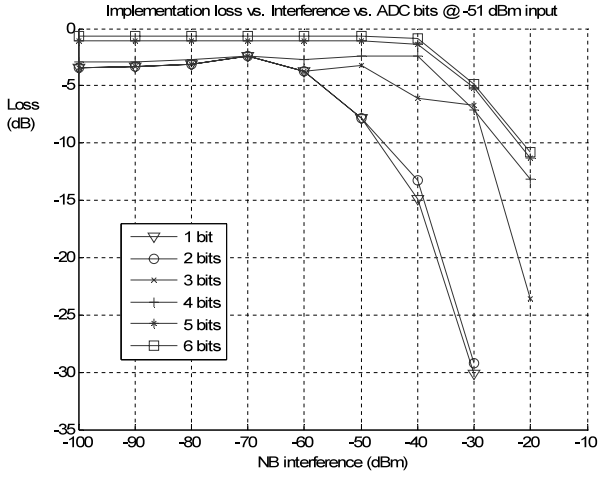

Fig. 12 Implementation loss versus in-band interference level and ADC bits.

saturation level is a trade-off between interference immunity and quantization noise. We can also observe that more than 3-bit ADC shows a better in-band interference immunity.

7. Conclusion

A subsampling analog front-end combined with analytic signal processing has been proposed for passband UWB communications. The architecture minimizes the building blocks for a low-complexity implementation with the potential for full CMOS integration. By exploiting the analytic matched filter output, timing recovery can be done without oversampling or interpolation. The proposed system also achieves a high time resolution, which implies high accuracy ranging capability. A first-order link budget analysis including circuit impairments is provided. The specifications of the critical blocks are verified by both hand analysis and system-level simulations. Following the presented design approach, one may determine the optimal circuit specifications of the proposed radio architecture for different ap-

plications, such as low-rate ranging system or high-speed data communications.

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