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A Subthreshold Cross-Coupled Hybrid Charge Pump for 50-mV Cold-Start

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ABSTRACT In this paper, a fully-integrated switched-capacitor DC-DC converter based on a Dickson charge pump able to work with input voltage levels that force the transistors working in subthreshold region is presented. The proposed topology exploits resistors in the charge transfer switch in order to overcome the limits of conventional solutions when working in the subthreshold regime. Post-layout simulations using a 28-nm FD-SOI technology show that the CP can boost an input voltage as low as 50 mV to a maximum output voltage of 270 mV, keeping a settling time about 25X lower than the conventional dual-branch cross-coupled charge pump and a voltage conversion efficiency higher than 76%. The proposed topology is particularly suited for the start-up of power management units supplied by thermoelectric generators.

INDEX TERMS Charge Pump (CP); Dickson charge pump; Energy harvesting; Power management; Switched-capacitor boost converter; thermoelectric generator.

I. INTRODUCTION

Energy Harvesting (EH) from available ambient energy sources is arousing great interest in the engineering world. With the specific role to energetically sustain circuit operations in autonomous electronic systems, EH is continuously exploited in a wide range of applications such as wearable devices, implantable medical devices, and wireless sensor nodes for Internet of Things (IoT) and Body Area Networks (BANs) [1]–[10].

Among the various types of energy sources, thermal energy (TE) scavenged by means of thermoelectric generators (TEGs) is very suitable for applications, like body-worn electronics, where other sources like solar cells and vibrational transducers may show lower performance due to unpredictable change of environmental conditions (i.e., light intensity and acceleration). TE conversion process is based on the Seebeck effect, for which electricity can be generated from the temperature gradient across two conductors connected together [11].

A TEG consists of small legs of n and p type semiconductor materials, also called pellets, connected thermally in parallel and electrically in series. When a temperature difference is continuously applied between the two plates of the TEG, the electrons and holes move from the hotter surface to cooler surface, resulting in a voltage difference at the TEG terminals [12]. Limited by the device size and the accounted temperature difference (e.g. that between the human skin and the ambient air ranging from 2°C to 5°C on average) the voltage generated by TEGs in practical application scenarios results to be often as low as several tens or a few hundreds of milli-volts [12]–[15]. Moreover, to extract the maximum power from the TEG, its output voltage must be set to half of its open circuit value. Consequently, the typical voltage levels at the output of a TEG are unsuitable to feed directly the analog and/or digital circuits. Therefore, a Power Management Unit (PMU) is mandatory to boost and efficiently adapt the output voltage of the TEG to that required by the various functional blocks of the overall electronic system.

As an example, let us consider Fig. 1, which depicts one of the simplified block diagram of a typical PMU [16]–[24]. The input voltage, V_{IN}, provided by the external TEG, feeds the auxiliary circuitry which is geared toward the cold start of the primary boost converter. The first amount of harvested energy is conveyed to an intermediate accumulation element (capacitor CINT) and, after its voltage has reached a target value (typically above the transistor threshold voltage), the stored charge is successively used to start-up the primary converter, switching-on the input source and enabling the gate control signals. In order to enable startup with low-voltage levels provided by the external energy source, a cold-start circuit, also referred in literature as kick-starter, is required [25]–[27].

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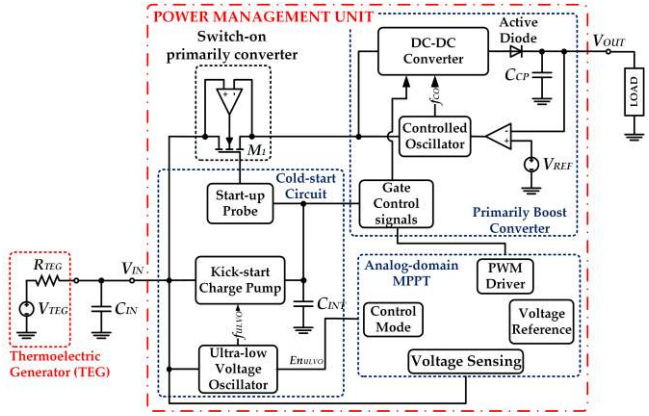

FIGURE 1. Simplified block diagram of an energy harvesting PMU.

The DC-DC converter in Fig. 1 can be implemented using switched inductor (SI) or switched capacitor (SC) topologies. SI converters are suitable for applications requiring high power but requires bulky off-chip components (inductors and/or transformers), resulting in a cost increase of the entire system. On the other hand, in low-power low-area applications, SC converters represents a better alternative since they are amenable for full on-chip integration [28]–[34], although characterized by a lower power conversion efficiency as compared to SI converters.

SC converters with a voltage gain higher than one are referred in literature as voltage multipliers or charge pumps (CPs). CPs have been commonly adopted in nonvolatile memories, RF antenna switch controllers and LCD drivers, where key design constraints are settling time, current drivability and silicon area [29], [35]–[42]. More recently, their field of application has been extended to energy-autonomous systems such as battery-less circuits, biomedical implants, IoT and BAN nodes. In these applications, CPs are widely exploited to boost the input voltage of the primary battery to a suitable level and/or to convey the electric energy extracted from surrounding environment towards a storage buffer [7], [25]–[27], [43]–[53].

Considering the kick-start CP, the main adopted design constraints are self-starting from ultra-low input voltage, low-power consumption and low-area occupation, which make their practical realization a challenging task.

In literature different papers have treated CPs able to work with near- and sub-100-mV input voltage [20], [27], [43], [53]. A common adopted strategy is to boost the control signal of the switches to get rid of the drawbacks due to the threshold voltage. As an example, in [20] the cold-start circuit is constituted by two complementary CPs to boost the gate signals of the MOSFETs exploited as switches. In [27] clock signals are boosted from $-V_{IN}$ to 2 V_{IN} to achieve the double effect of reducing the number of stages and the on-resistance of the switches. In [43] bootstrapped configuration was improved by re-using the output signal of the startup voltage multiplier to increase the amplitude of the non-overlapped signals applied to the auxiliary bootstrap capacitors. Similar strategy is applied in [53], where a phase generator is used to provide the boosted gate signals of the MOSFETs and to adapt their turn on sequence to facilitate the startup of the whole system (adaptive scheme).

Having this in mind and focusing on TEG-based applications, this work proposes a novel CP architecture to achieve startup function without any off-chip component for significant area and cost reduction. The proposed topology has been designed and simulated in a 28-nm Fully Depleted Silicon On Insulator (FD-SOI) technology. A minimum input voltage of 50mV is achieved preserving fast response and high output power level with respect to the traditional topologies. The remainder of this paper is organized as follows. Section II reports a brief review of charge pumps and an accurate analysis of the switch response in low-voltage operation. Section III describes the detailed circuit of the proposed solution. Section IV provides the simulation results and, finally, Section V presents the conclusions.

II. CHARGE PUMP IN SUBTHRESHOLD REGION

Among the different available topologies in literature, namely Fibonacci, series-parallel, exponential and Cockcroft–Walton, the Dickson CP represents the widest adopted topology to be fully integrated on IC, since it shows higher performance as compared to the others topologies [28], [54]. A simplified schematic of an N-stages Dickson CP is shown in Fig. 2, where each stage (red-dash box) is made up by a Charge Transfer Switch (CTS) and a pumping capacitor, C_P. In the schematic shown in Fig. 2 the top parasitic capacitance is assumed to be equal to a fraction of the pumping capacitor. Thus, introducing parameter β[1], the stray capacitance is equal to βC_P. Finally, the last CTS and C_{OUT} form the output stage. Note that the specific CTS circuit topology is a one of the main diversification factors among the various proposed Dickson CP architectures and, hence, it is at key design aspect to consider.

In the first monolithic integrated CP [54] the CTS was simply implemented with the diode-connected n-type MOSFET depicted in the blue-dash-dot box of Fig. 2, which works in saturation or in cut-off region. During steady-state operation, the output voltage of an N stage CP can achieve the value expressed by (1) where V_{IN}, V_{CK} and V_{DROP} are the input, clock and CTS drop voltage, respectively, f is the clock frequency and I_{OUT} is the load current.

$$V_{OUT} = \left(V_{IN} - V_{DROP}\right) + N\left(\frac{V_{CK}}{1+\beta} - V_{DROP}\right) - \frac{NI_{OUT}}{fC_P} \quad (1)$$

The amplitude of the clock signal, V_{CK}, can be arbitrarily set. As an example, clock boosting as well as some regulation schemes for CPs act on V_{CK} to adjust CP output voltage targeting a reference voltage [55]. However, since the clock signal is often generated starting from the input source,

[1] Parameter β represents the ratio between the stray capacitance and the pumping capacitance and is therefore lower than 1.

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it is conventionally assumed to be equal to the input voltage, V_{IN}, as also done afterward. Of course, as apparent in (1), although the simplicity and the ability to drive an adequate current to the load, this topology has an efficiency and a voltage gain strongly affected by V_{DROP} voltage[2].

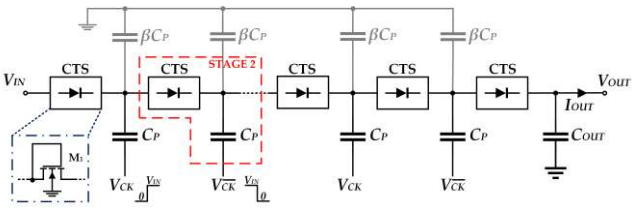

FIGURE 2. Dickson charge pump simplified scheme.

It is also worth noting that relationship (1) is only valid if the time needed to transfer the charge from one stage to the following one is small enough with respect to the clock half period. Under this condition, in which the charge is assumed to be entirely transferred, the CP works within the Slow Switching Limit (SSL) and the CP output resistance is equal to (N/fC_P). On the other hand, when the charge is partially transferred between the stages, the CP works in the so named Fast Switching Limit (FSL) and its output resistance is given by the sum of the resistance of each CTS, R_{CH}, (i.e., (N+1) R_{CH}) [56].

In general, in high performance CP topologies, the CTS is made up by one or two main transistors, acting as a switch, whose control terminals (i.e., gate and/or body nodes), are properly driven by an auxiliary circuits included in the same CTS block. These strategies are typically known as gate and body biasing techniques and can be singularly implemented, or together, in order to manage the electrical properties, such as threshold voltage and channel resistance, of the main CTS transistors [28], [57]–[59].

A. CTS IN SUBTHRESHOLD CONDITION

In the design context considered in this paper, where the CP works under ultra-low voltage conditions, the transistors of the CTS work in subthreshold region (i.e., with V_{GS} voltage lower than the transistor threshold voltage, V_{TH}). The transistor current-voltage relationship in this region is given by [60] and expressed in (2), where n is the sub-threshold slope, I_0 is a technology-dependent constant, $V_T = kT/q$ is the thermal voltage, W/L is the transistor aspect ratio, V_{DS} is the drain-to-source voltage, V_{BS} is bulk-to-source voltage and V_{TH} is the threshold voltage, whose value is given by (3), where V_{TH0} is the zero-bias threshold voltage (i.e., the value of V_{TH} for V_{DS} and V_{BS} equal to zero) and λ_{DS} and λ_{BS} are positive technology parameters which model the Drain Induced Barrier Lowering (DIBL) effect and the body effect, respectively.

$$I_{SUB} = I_0 \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}}\right) \tag{2}$$

$$V_{TH} = V_{TH0} - \lambda_{DS} V_{DS} - \lambda_{BS} V_{BS} \tag{3}$$

To evaluate the effectiveness of a transistor working as a switch, a commonly used metric is the ratio between the current flowing during the forward conduction, I_{FWD}, and the backward current when the switch is off, I_{BWD}, which, of course, it is desirable to be (much) greater than unity. Under subthreshold condition, combining (2) and (3) this ratio can be approximated as

$$\frac{I_{FWD}}{I_{BWD}} \approx \frac{1 - e^{-\frac{V_{DS,FWD}}{V_T}}}{1 - e^{-\frac{V_{DS,BWD}}{V_T}}} e^{\frac{\Delta V_{GS} + \lambda_{DS}\Delta V_{DS} + \lambda_{BS}\Delta V_{BS}}{nV_T}} \tag{4}$$

where parameters ΔV_{GS}, ΔV_{DS} and ΔV_{BS} are the difference between V_{GS}, V_{DS} and V_{BS} during on- and off-phase, respectively.

By inspection of (4), the ratio results independent from the zero-bias threshold current, I_0, and by the transistor aspect ratio, W/L. Moreover, gate and body biasing techniques, which increase the corresponding voltage difference, positively contribute to (4).

Regarding transistor length, a widely adopted strategy is to decrease its value to maximize I_{FWD}/I_{BWD}. Indeed, coefficient λ_{DS}, is inversely proportional to L and, consequently, a decrease of L leads to an increase of λ_{DS} and, in turn, of (4). Therefore, the minimum transistor length must be adopted to maximize I_{FWD}/I_{BWD}.

Considering a CTS with only one transistor along the input-output path, the voltage across its drain source nodes is equal to a voltage drop, V_{DROP} or $2V_{IN}$ when the switch is on and off, respectively (i.e., $V_{DS,FWD}$=V_{DROP} and $V_{DS,BWD}$ =$2V_{IN}$). Hence, during a complete cycle, ΔV_{DS} is negative and can heavily reduce the ratio I_{FWD}/I_{BWD} up to an unacceptable lower bound $(I_{FWD}/I_{BWD})_{\min}$=1. From (4), defining $V_{IN,\min}$ the minimum input voltage value at which I_{FWD}/I_{BWD} =1, applying the approximation reported in the Appendix, we get

$$\left(V_{IN,\min}\right)_{\text{singleMOS}} \approx \frac{\left(\Delta V_{GS} + \lambda_{BS}\Delta V_{BS}\right) - nV_T \ln\left(\frac{V_T}{V_{DROP}}\right)}{2\lambda_{DS}} \tag{5}$$

[2] V_{DROP} is a function of CTS topology, device parameters and also clock frequency. If the CTS is a diode-connected MOS operating in sub-threshold region, $V_{DROP} = V_T \ln\left(\frac{1}{4^{N+1}} \frac{(1+\alpha_T) f C_P V_T}{I_{SUB,0}}\right)$ [28], where it is apparent the dependence on the clock frequency.

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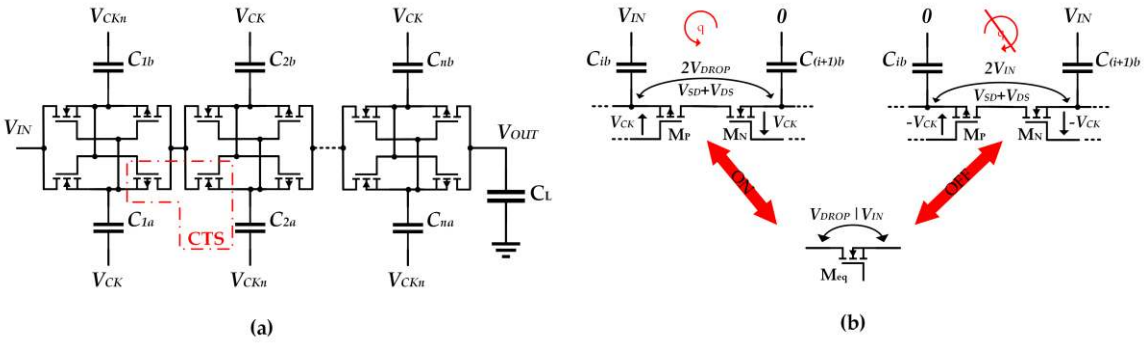

FIGURE 3. **Cross-coupled CP: (a) simplified scheme; (b) Voltage distribution in the ON and OFF state.**

It is worth noting that relationship (5) does not represent a limit under which the CTS and, hence the CP, does not work, but it provides a voltage limit under which CP performances (settling time, voltage and power conversion efficiency) suddenly decrease.

Among the various CTS proposed in literature, the more efficient one is represented by the dual-branch topology, also named cross-coupled or latched CP, shown in Fig. 3a [61], which is often exploited in energy harvesting applications [29]. This CP when used above threshold (i.e., with transistor in linear region during the on state and completely turned off in the other condition) allows to reduce the CP output ripple and enhance its charge transfer, thus improving the power efficiency.

Of course, in subthreshold region the latched CP entails limitations on the conduction level given by the series connection which includes both n-type and p-type MOS transistor. Indeed, according to Fig. 3b, modelling the CTS with only one transistor whose equivalent coefficients $\lambda_{DS,eq}$ and $\lambda_{BS,eq}$ are the parallel of the corresponding n-type and p-type MOS transistor coefficients (i.e., $\lambda_{DS,eq} = \lambda_{DS,n} // \lambda_{DS,p}$ and $\lambda_{BS,eq} = \lambda_{BS,n} // \lambda_{BS,p}$, respectively) and defining $V_{DS,eq} = V_{DROP}$, we get the minimum input supply voltage of the cross-coupled CP as

$$\left(V_{IN,\min}\right)_{cr-cpl} \approx \frac{\left(\Delta V_{GS} + \lambda_{BS,eq}\Delta V_{BS}\right) - nV_T \ln\left(\dfrac{V_T}{V_{DROP}}\right)}{\lambda_{DS,eq}} \qquad (6)$$

By comparing (6) and (5) for equal voltage parameters and assuming identical coefficients for the NMOS and PMOS transistors, we find that the numerator of (6) is slightly lower than that of (5), while the denominator of (6) is at least 4 times lower than that of (5); hence, we find that the value predicted by (6) is about four times greater than the value given by (5).

In conclusion, despite the advantages due to its dual branch nature, the latched CP is less useful in subthreshold region and, hence, unsuited in very low voltage application, where the traditional Dickson CP can still work.

III. PROPOSED HYBRID CROSS-COUPLED CP

To overcome the drawbacks of the cross-coupled CP working in subthreshold discussed above, due to series connection of n-type MOSFET and p-type MOSFET, in the following an improved and novel topology is presented. A counterintuitive idea is to use a hybrid structure in which resistors replace the weakest transistor (i.e. the transistor with higher values of λ_{DS} and λ_{BS}), in order to decrease the minimum start-up voltage while maintaining good performance. This idea is applied on only the odd CTS and combined with the adoption of also a doubled clock signal.

The simplified block scheme of the proposed CP is depicted in the left side of Fig. 4. The architecture is constituted by $N/2$ building blocks and a clock booster (Fig. 5) which generates two counterphase clock signals with amplitude equal to twice the input voltage, $2V_{IN}$ (named in the Fig. 5 V_{2CK} and V_{2CKn}). The transistor level schematic of a single building block, shown in the red-dash box at the right of Fig. 4, is based on the series of two half-stages of a cross-coupled topology, where, resistors R_A and R_B substitute of the first two weakest transistors. In Fig. 4b it is assumed that the PMOS transistor is the weakest one[3]. Hence, each building block provides a gain factor equal to four (a factor equal to three dues to the first part and one more due to the last part) and, hence, it is equivalent to a three-stage CP.

The operation principle can be described considering the down-side branch. When V_{2CK} is low, the transistor M_{1A} is turned on and capacitor C_{1A} is charged, while C_{2A} transfers its charge to the output (at the same time, C_{1B} transfers part of its charge to C_{2B} through R_B and M_{2B}). When the clock signal turns high, C_{1A} transfers part of its charge to C_{2A} through R_A and M_{2A} providing the output voltage of a single building block, equal to $V_{IN} + 3V_{CK}$ (meanwhile capacitor C_{1B} is charged on the complementary branch).

The backward current, I_{BWD}, determines a voltage drop on resistance R_A, thus the M_{2A} gate-source voltage becomes

[3] Note that if in the considered technology the n-type MOSFET is the weakest transistor, resistors R_A and R_B have to be used to substitute M_{1A} and M_{1B}.

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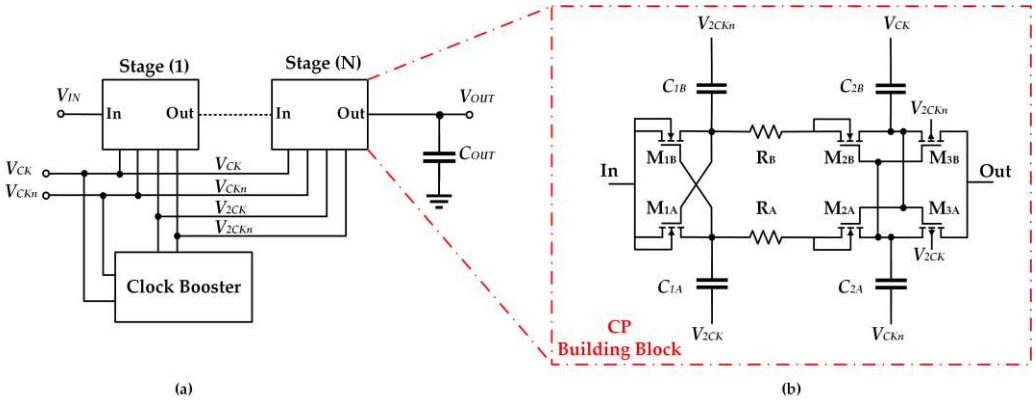

FIGURE 4. **Block scheme: (a) CP block diagram; (b) building block transistor level schematic.**

lower than zero and I_{BWD} is heavily reduced for its exponential dependence.

It is worth noting that resistance R_A and R_B in the CTS can be made enough small to have a negligible impact during the forward behavior, thus for that CTS the V_{DROP} is due to only the V_{DS} of one NMOS. On the other hand, thanks to a feedback effect, they have a key role during the other half-period since, despite their low value, they heavily reduce the backward current, I_{BWD}.

Indeed, considering again the down-side branch during that phase in which V_{2CK}=0 and V_{CKn}=V_{IN} and assuming the input voltage of the building block equal to jV_{IN}, being j an integer value, after the transient the M_{2A} gate and M_{1A} are both equal to jV_{IN}.

The all-NMOS topology in Fig. 5 has been adopted as clock booster. It is based on the well-known Nakagome's cell introduced in [62] whose output nodes are connected to two pseudo-inverters to recover the full voltage excursion of $2V_{IN}$ (signals diagram are reported in the rightmost part of Fig.6). When V_{CK} is low the capacitor with that terminal charges up to V_{IN}, M_{2b} is turned off and the output signal V_{2CK} through M_{3b} is electrically connected to the ground.

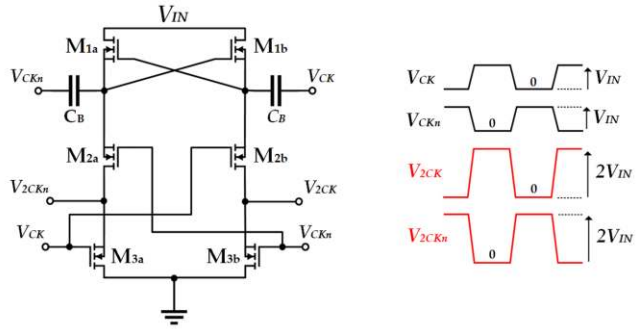

FIGURE 5. **All-NMOS clock booster and phase diagram.**

In the other half period, in which V_{CK} is high, M_{1b} and M_{3b} are switched off and through M_{2b} the output node is boosted to $2V_{IN}$ (i.e., V_{CK}+V_{IN}). Following the same procedure reported in the Appendix for the cross-coupled CP we find that the minimum supply voltage of the proposed CP is given by

$$\left(V_{IN,\min}\right)_{proposed} \approx \frac{\left(\Delta V_{GS} + \lambda_{BS,n}\Delta V_{BS}\right) - nV_T \ln\left(\frac{V_T}{V_{DROP}}\right)}{3\lambda_{DS,n}} \quad (7)$$

and it is lower not only than (6), but it also lower than (5). Thus, this topology is the most advantageous in very low voltage domain, i.e. when the transistors are forced to work in subthreshold region.

An intuitive explanation of the increased performance of the hybrid cross-coupled CP derives from the observation that when transistors work in deep-subthreshold, drain current depends exponentially by the "control" voltages (gate-source, drain-source and source-bulk) and the current levels are extremely low. Consequently, the on resistance is usually higher than hundreds of kilo-ohms. In this condition, a CTS constituted by two transistors in series, like that one exploited in the cross-coupled topology, not only shows a doubled resistive path along the current path, but also each transistor has an halved drain-source voltage, which exponentially decrease the current drivability of the MOSFET itself.

IV. SIMULATION RESULTS AND COMPARISON

To verify the effectiveness of the proposed hybrid cross-coupled CP and validate the actual advantage in term of low start-up voltage under sufficient output power transmission, a CP with 2 building blocks has been designed and simulated by using a 28-nm FD-SOI technology provided by STMicroelectronics.

As stated in Section I, the design has been targeted for a TEGs which generates a voltage in the range of tens of mV and delivers a power in the range of μW. However, it is worth noting that the cold-start subsystem has to provide only the initial energy to kick-start the primary converter, thus the power reduces to sub-μW range.

Parameters of the MOS used and available in the technology (flip-well low-threshold transistor) are

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summarized in Table I for the aspect ratio of unitary transistor $(W/L)_{un}$=0.3/0.03 µm/µm. Moreover, the following parameters have been considered for the CP design: V_{IN} = [40, 100] mV, f=1 MHz and C_{OUT}=180 pF. The aspect ratio of the low-threshold transistors have been set to $120(W/L)_{un}$ and $240(W/L)_{un}$. for the NMOS and PMOS, respectively.

An un-silicide P+ poly 30 kΩ resistor has been chosen to implement resistors R_A and R_B of the building block, while Metal-Insulator-Metal (MIM) capacitors have been used as pumping capacitors and their value has been set to 15 pF.

TABLE I. MOS TRANSISTOR PARAMETERS (W/L=0.3/0.03 µm/µm)

	I_0 (µA)	n	V_{TH0} (mV)	λ_{DS}	λ_{BS}
NMOS	1.07	1.44	386	0.11	0.09
PMOS	1.06	1.59	515	0.17	0.1

The clock signal is assumed to be generated by another block that can be implemented adopting ring oscillators, as done in [20], or *LC* tank oscillators, as done in [17]. Clock signals V_{CK} and V_{CKn} are assumed to be non-overlapping.

To emulate the drivers, ideal buffers have been implemented with switches having a resistance equal to 5 kΩ and 10 GΩ when the switch is close and open, respectively. Finally, a Thevenin voltage generator with an internal resistance equal to 1 kΩ emulates the thermoelectric generator.

Regarding the clock booster (Fig. 5), top- and bottom-side transistors, $(W/L)_{1/3a,b}$, have aspect ratios equal to $240(W/L)_{un}$, while the transistors in the middle of the Clock booster, $(W/L)_{2a,b}$, are equal to $600(W/L)_{un}$ in order to decrease the threshold voltage of the pseudo-inverter. Capacitances C_B of the clock booster have been set to 30 pF and implemented by POLY to NWELL capacitors to realize a compact design.

Finally, layout view is depicted in Fig. 6 and the total silicon area is equal to 0.0116 mm^2.

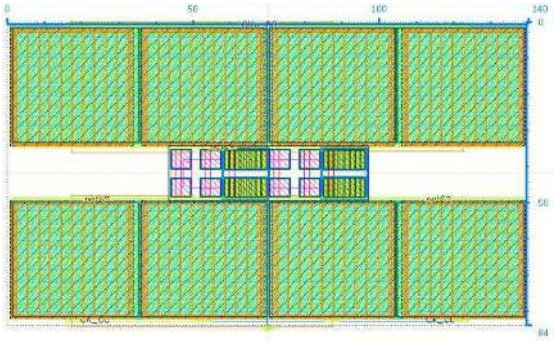

FIGURE 6. Layout of the Hybrid Cross-Coupled CP.

In order to carry out a comparison with the same maximum output voltage (equal to $7V_{IN}$), post-layout transient simulations were run for the proposed hybrid cross-coupled CP topology with two stages and the traditional CP topologies, namely the diode-based and the cross-coupled CPs, with six stages. Of course, the total pumping capacitance of the proposed topology, equal to 180 pF, has been uniformly distributed among the stages of the other two topologies, which also means about equal the same silicon area for all the three CPs.

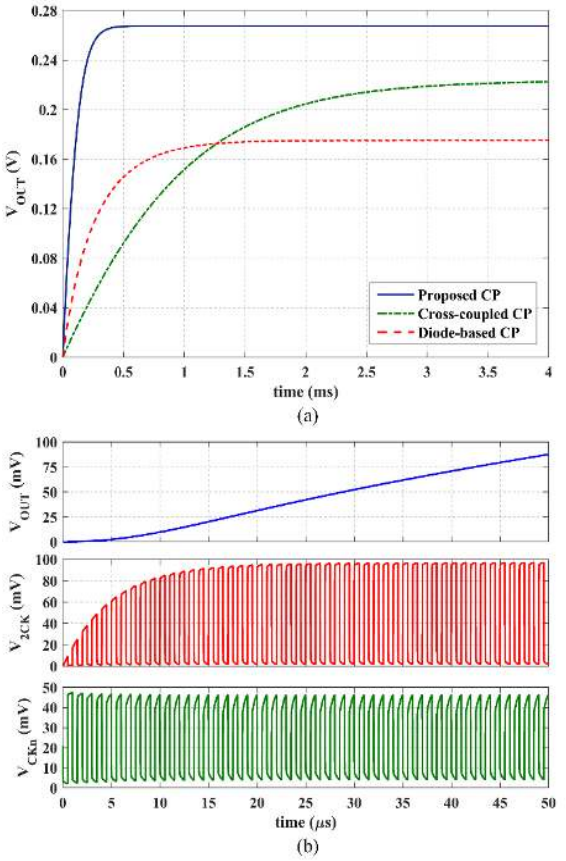

FIGURE 7. Open-circuit CPs transient behavior at V_{IN}=50 mV: (a) complete transient for all the topologies; (b) initial transient of the proposed topology.

Figure 7a shows the open-circuit time response of the three compared CPs under an input voltage equal to 50 mV. It is apparent that the proposed solution is about two times faster than the other two topologies and, moreover, it is the only one reaching an output voltage equal to 270 mV.

Fig. 7b reports the output voltage of the hybrid cross-coupled topology and the signals of the clock booster in Fig. 5 during the first 50 µs. The maximum value of V_{2CK} approaches its ideal value, equal to $2V_{DD}$, proving that clock booster shows a high voltage and power conversion efficiency. Moreover, from Fig. 7b it can be seen that the intrinsic time constant of the clock booster slightly affects the CP transient behavior.

In order to consider comparison metrics, let us consider the Power Conversion Efficiency (PCE)

$$\eta = \frac{P_{OUT}}{P_{TEG}} \tag{8}$$

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where P_{TEG} is the total power provided by the TEG (i.e., CP the input power) and P_{OUT} is the power transferred by the CP to the load, and the Voltage Conversion Efficiency (VCE)

$$VCE = \frac{V_{OUT,actual}}{V_{OUT,ideal}\Big|_{I_{OUT}=0}} \tag{9}$$

defined as the ratio between the actual output voltage at a given P_{OUT} and the ideal CP output voltage value at zero output current (in our design the ideal output voltage, $V_{OUT,ideal}$, is equal to $7V_{IN}$). In addition, we consider the settling time, T_S, as the time needed to reach the 63% of the maximum ideal output voltage.

Figures 8a and 8b compare the voltage and power conversion efficiencies versus the delivered CP output power for V_{IN} equal to 50 mV and 70 mV[4]. By inspection of Fig. 8 it is apparent that the hybrid cross-coupled CP topology shows the best performances in terms of *VCE* and of maximum output power that can be delivered for a given input voltage. Thus, the curves suggest that the hybrid cross-coupled CP could be used in applications which requires high power while preserving efficiency.

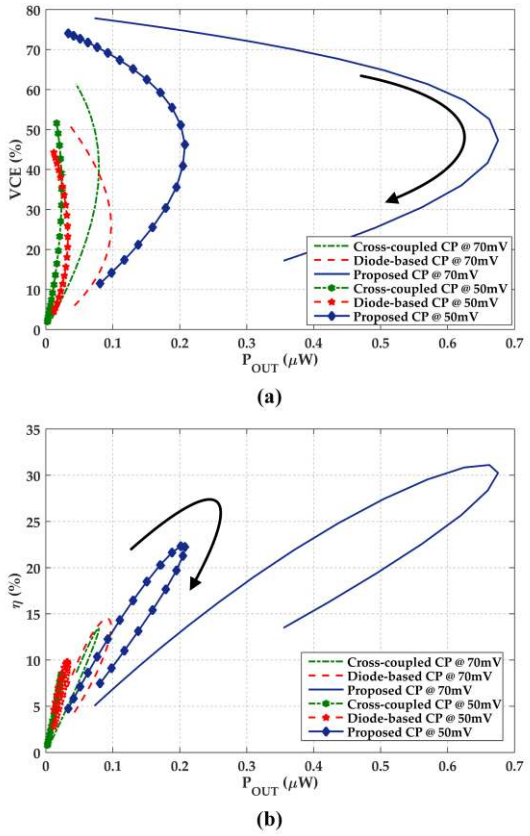

FIGURE 8. **Performance metrics versus output power when varying the load resistance: (a) voltage conversion efficiency; (b) power conversion efficiency.**

[4] Curves in Fig. 8 are obtained by sweeping the load resistance from higher to lower values than the CP output resistance (black arrow).

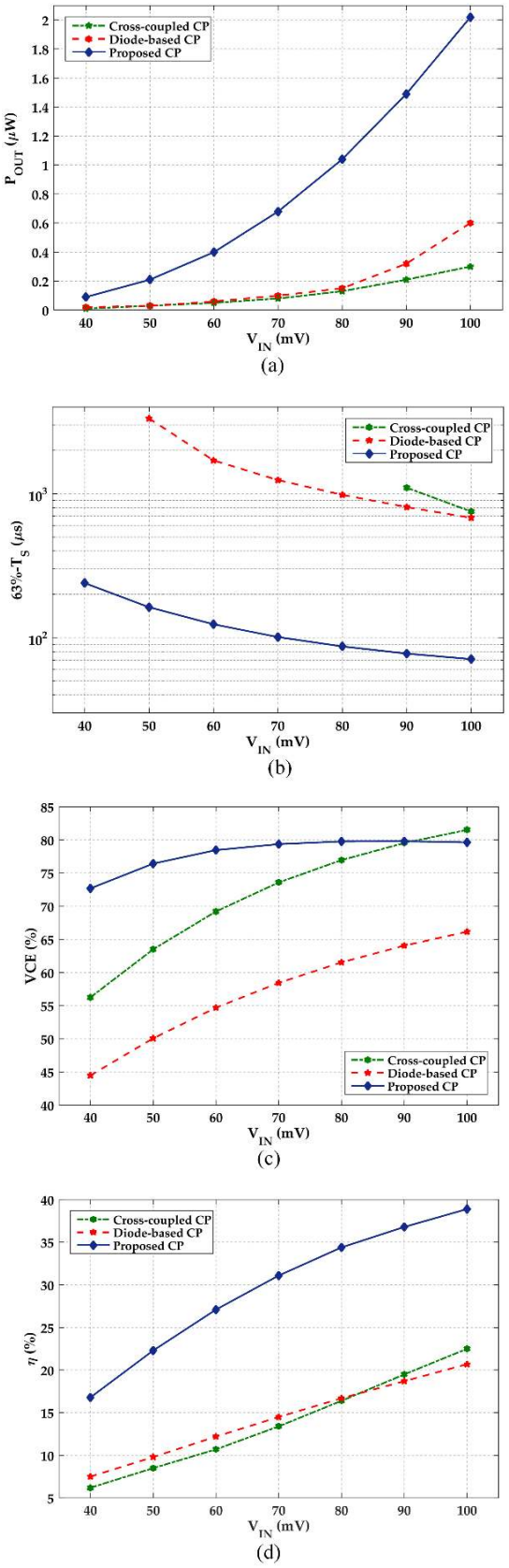

FIGURE 9. CP performances versus input voltage: (a) output power; (b) settling time; (c) VCE; (d) power conversion efficiency.

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Performances of the three CPs versus the input voltage, V_{IN}. are reported in Fig. 9, where the advantages of the proposed topology are evident. Indeed, from Fig. 9a it is apparent that for any value of the input voltage the hybrid cross-coupled CP delivers more power (two times on average) than the other topologies. Moreover, by inspection of Fig. 9b the CP in Fig. 4 exhibits a settling time about one order of magnitude lower than that of the traditional solutions in Fig. 2 and Fig. 3. Fig. 9c shows that the VCE of the proposed solution is slightly worse than that of the cross-coupled CP only for input voltage higher than 90 mV.

Finally, Fig. 9d shows that the Hybrid Cross-Coupled CP exhibits a power conversion efficiency ranging from about 16% to 39% in the considered input voltage range, while the other two conventional CPs shows values of η more than two times lower. As explained in the previous Section, all these advantages are basically due to the adoption of resistors which conduct in the same manner in the on and off state.

Table II reports corner analysis results at the minimum supply voltage (50 mV) and for different temperatures. Its inspection reveals that the input power is always lower than 1.75 µW while, in the typical case, it is equal to about 750 nW, falling in the range of the available output power from an extended class of TEGs.

Furthermore, the corner Fast-Slow (FS) at 0°C is the worst corner, being the maximum output power equal to 28.7 nW.

The robustness of the CP against process variations is further assessed by post-layout Monte Carlo simulations. As an example, Fig. 10 show Monte Carlo simulation results in the worst-case corner for *VCE* and η over 1000 iterations. Similar Gaussian distributions are obtained in all the other cases, therefore, for the sake of conciseness, we only report mean value and standard deviation in the result summary in Table III.

TABLE II. CORNER ANALYSIS RESULTS (V_{IN}=50 mV)

Parameter	*Corner*	*Temperature (°C)*		
		0	27	70
Settling time (µs) [5]	SS	327	146.6	--
	SF	411.6	165.1	--
	FS	562.6	231.3	--
	FF	469.4	186.7	--
Maximum input power (nW)	SS	524.5	946	1718
	SF	425.3	825.5	1666
	FS	544.5	1006	1699
	FF	454	874.5	1588
Maximum output power (nW)	SS	81.1	227.8	202.1
	SF	58.8	210.8	219.3
	FS	28.7	140.2	178.7
	FF	40.8	179.5	212.0
Peak VCE (%)	SS	84.48	75.93	54.78
	SF	86.19	78.91	58.09
	FS	82.55	72.95	52.78
	FF	85.19	77.18	57.33
η (%)	SS	15.5	24.1	11.8
	SF	13.8	25.5	13.2
	FS	5.3	13.9	10.5
	FF	9	20.5	13.4

[5] Settling time at 70°C is not reported since the 63-% nominal output voltage is not reached

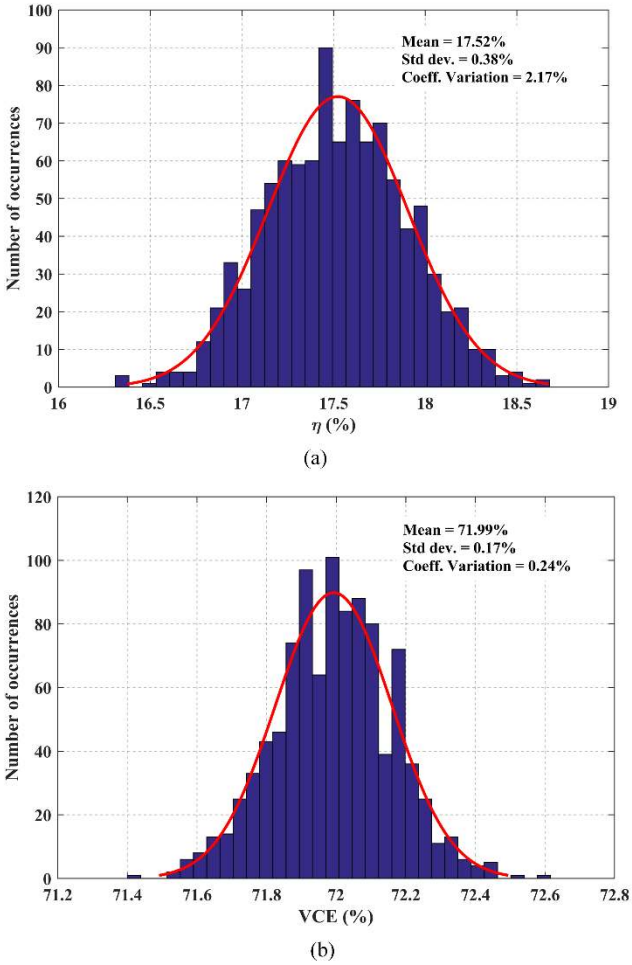

FIGURE 10. Monte Carlo results for the worst-case corner (FS at 0°C): (a) voltage conversion efficiency; (b) power conversion efficiency.

TABLE III. MONTE CARLO SIMULATION RESULTS (CORNER TT, 27°C)

	μ	σ	σ / μ (%)
Settling time (µs)	177.72	3.91	2.20
Maximum input power (nW)	753.04	7.6	1.01
Maximum output power (nW)	206.56	2.31	1.12
Peak VCE (%)	76.85	0.18	0.24
η (%)	27.43	0.33	1.18

From this Table it is apparent that the relative standard deviation is lower than 3% in all cases, showing that the topology is robust against process and mismatch variations.

Finally, additional information is gathered in Table IV, where performances of the proposed CP are compared with the state-of-the-art. From Table IV it is apparent that the topology, while maintaining a comparable value of *VCE*, has the lowest minimum input voltage and area occupation while maintaining a comparable value of *VCE* (Fig. 11a). By inspection of Fig. 11b, which reports η as function of the output power density of some of the cited works, the

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TABLE IV. COMPARISON WITH THE STATE OF THE ART

Ref.	Proposed [b]	[26]	[27]	[43]	[45]	[47]	[20]	[53]
Topology	Hybrid cross-coupled	Cross-coupled /composite	Cross-coupled	Bootstrap	Cross-coupled	Bootstrap	Cross-coupled	Adaptive
Technology (nm)	28	130	65	65	180	130	180	65
No. of stages	2	24	3	10	6	3	2x6	10
Auxiliary circuits	Clock booster 2x	Start-up circuit	Clock booster 3x	Clock booster 2x	Backward control circuit	--	Clock booster 2x	--
Application	TEG	TEG	TEG, solar cell	TEG, solar cell	TEG, solar cell	TEG, solar cell	TEG	TEG, solar cell
Minimum supply (mV)	50	70	150	100	320	270	57	120
Clock frequency (MHz)	1	0.040	15.2	10	0.45	0.8	0.025	1
Total pumping cap. (pF)	120	46.08	22.5	>1000	288	150	>1000	286
Load capacitance (pF)	180	10000 [a]	30	100	50.7	500	350	--
Settling time (μs)	127	$1.5{\cdot}10^{6}$	40	--	100	--	$1.35{\cdot}10^{5}$	--
Max output power (μW)	0.68	15	1.5	6.6	--	7	0.08	3
Peak η (%)	38.9	58	38.8	33	78	58	89	38.8
Peak VCE (%)	80	50	80	76	89	58	93	58
Area (mm^2)	0.0116	0.6	0.032	1.32	1.37	0.42	0.96	0.78

proposal is allocated in the middle zone, while the best results are outperformed by CP introduced in [34]. Finally, in comparison with [20] and [26], which can work in sub-100 mV, the proposed one generates a higher output power and shows a better VCE, respectively.

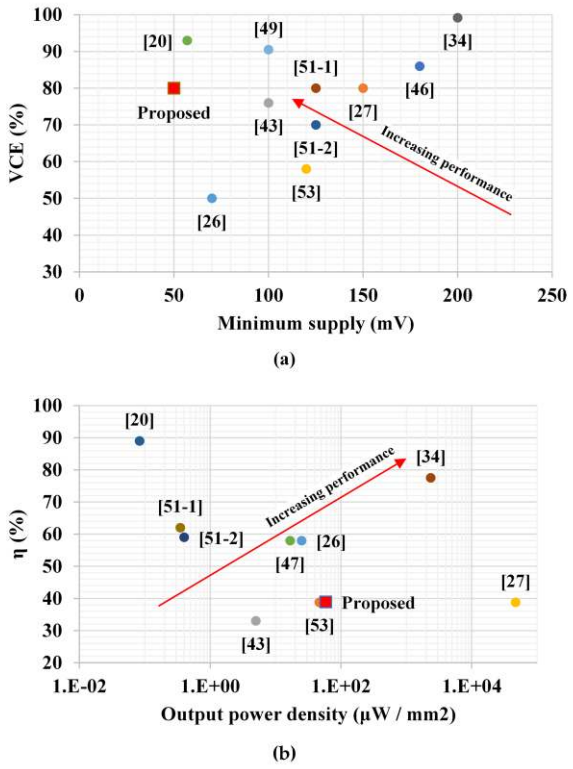

FIGURE 11. Comparison with the State-of-the-Art: (a) voltage conversion efficiency versus minimum supply voltage; (b) power conversion efficiency as a function of the output power density (b).

V. CONCLUSION

In this paper, an ultra-low input voltage boost DC–DC converter, named hybrid cross-coupled CP, and suited for TEG applications was presented. The proposed CP exploits resistors in the charge transfer switch to allow efficient operation in the subthreshold region, where transistors exhibit an on resistance in the order of hundreds of kilo-ohms. Since the resistors conduct in the same manner for the on and off state, the proposed topology reaches higher performance than conventional solutions for an input voltage ranging from 50 mV to 100 mV.

The overhead of the proposed topology may rely on the increased area occupation due to resistors. Moreover, conventional cross-coupled CP shows comparable *VCE* for input voltages higher than 100 mV.

Designed with a 28-nm FD-SOI technology, is able to provide an output power which ranges from 50 nW to 3.4 μW and achieves a voltage conversion efficiency higher than 76%. Moreover, the hybrid cross-coupled CP shows a settling time about 25X lower than the conventional dual-branch cross-coupled charge pump.

APPENDIX

Assuming I_{FWD} and I_{BWD} described by eq. (2), in which expression in (3) replaces the threshold voltage V_{TH}, we can calculate their ratio as

$$\frac{I_{FWD}}{I_{BWD}} = \frac{e^{\frac{V_{GS,FWD}+\lambda_{DS}V_{DS,FWD}+\lambda_{BS}V_{BS,FWD}}{nV_T}}}{e^{\frac{V_{GS,BWD}+\lambda_{DS}V_{DS,BWD}+\lambda_{BS}V_{BS,BWD}}{nV_T}}} \frac{1-e^{-\frac{V_{DS,FWD}}{V_T}}}{1-e^{-\frac{V_{DS,BWD}}{V_T}}} \qquad \text{(A1)}$$

(A1) can be further re-written assuming the voltages differences between values in forward and backward conditions and relationship (4) can be consequently obtained.

Assuming I_{FWD} equal to I_{BWD} and considering $V_{DS,FWD}$ and $V_{DS,BWD}$ lower and much greater than V_T, respectively, we can approximate (4) as

$$1 \approx e^{\frac{\Delta V_{GS}+\lambda_{DS}\Delta V_{DS}+\lambda_{BS}\Delta V_{BS}}{nV_T}} \frac{V_{DS,FWD}}{V_T} \qquad \text{(A2)}$$

Moreover, since $V_{DS,FWD}=V_{DROP}<<V_{DS,BWD}=2V_{IN,\min}$, from (A2) we get

$$nV_T \ln\left(\frac{V_T}{V_{DROP}}\right) \approx \Delta V_{GS} + \lambda_{BS}\Delta V_{BS} - 2\lambda_{DS}V_{IN,\min} \qquad \text{(A3)}$$

and relationship (5) can be consequently obtained.

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