A Surface-Potential-Based High-Voltage Compact LDMOS Transistor Model

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***Abstract*—In this paper, a surface potential-based compact model is described for high-voltage LDMOS transistors. This model combines the low-voltage MOS region with the high-voltage drift region of an LDMOS transistor. The model includes the effect of the gate extending over the drift region as well as its temperature behavior and geometry scaling. In contrast to subcircuit models, the model has no internal node, since the so-called internal drain voltage is explicitly expressed in terms of the external terminal voltages. By use of an explicit formulation of the surface potential, the dc model thus combines the benefits of short computation times and robustness with accuracy. A comparison with dc measurements shows that the dc model provides an accurate description in all regimes of operation, ranging from subthreshold to super-threshold. In addition, a nodal charge model is derived, to account for the time-dependent behavior of the device. Capacitances obtained from high-frequency measurements show a good agreement with those obtained from the nodal charge model.**

***Index Terms*—High-voltage MOS, integrated circuit design, LDMOS, modeling, silicon-on-insulator (SOI).**

I. Introduction

TODAY, high-voltage LDMOS devices are extensively used in all kinds of integrated power circuits, like switch-mode power supplies and power amplifiers. Optimal design of these power circuits requires high-voltage LDMOS models for circuit simulation, which describe the device characteristics accurately over a wide range of biases. In addition, LDMOS devices processed in thin-film silicon-on-insulator (SOI) provides a new and attractive technology for smart power integrated circuits in consumer and automotive applications [1]. Thus, with the (SOI-)LDMOS transistor being a frequently used component in power circuits, inclusion of the specific (SOI-)LDMOS transistor aspects, like the effect of the gate extending over the drift region and the temperature behavior, is essential.

A frequently followed approach in high-voltage modeling is to describe the LDMOS transistor by a subcircuit model (also called macromodel), which consists of a combination of circuit elements [2]–[5]. A similar approach is to define a compact model with an internal node inside [6]. In both approaches, the model consists of an additional (internal) node which is solved numerically by the circuit simulator. The disadvantage of this approach is that during circuit simulation these models may give rise to an increase of computation time, or may have difficulty to reach convergence at all. Furthermore, some of these models lack an accurate description of one or more specific device characteristics.

Another approach in LDMOS modeling is to solve the potential at the internal node inside the model by means of a numerical iteration procedure, like in [7]–[10]. As long as care is taken that the iteration procedure is always converging to the desired solution and the convergence error is sufficiently small, this approach is valuable and gives sufficiently smooth characteristics. The drawback of the models in [7]–[10], however, is that the subthreshold regime is not included.

Thus, the need for a compact LDMOS model without internal node, which takes into account the specific high-voltage characteristics, is clear. So far, some models [11]–[15] in which the potential at the internal node is expressed explicitly in terms of the external terminal voltages (and thus no internal node exists) have been developed. The model of [11], however, lacks a nodal charge description, while in [12] the voltage drop across the channel is taken from an empirical expression. So far, one compact model that takes into account most of the specific LDMOS aspects, has been developed [13], [14]. The use of this compact model, however, has been found to be limited due to the occurrence of nonconvergence in circuit simulation, caused by discontinuities in the model expressions and their derivatives. Hence, even more important for successful IC-design is a compact model that is robust by having all its expressions and derivatives continuous, allowing fast, converging circuit simulations.

In order to combine accuracy with robustness, we have developed a new compact LDMOS model [15], for which the model developed in [13] served as a starting point. Like in [6] and [13], the model is surface potential based, providing a precise current description, also in the so-called moderate inversion region. The model includes mobility reduction due to the vertical electrical field, velocity saturation in the channel region and drain-induced barrier lowering. In addition to [13], we have further incorporated static feedback. The model is aimed for long-drift-region devices, since velocity saturation in the drift region is not included.

II. Model Methodology

In Fig. 1, a cross section of the LDMOS transistor is given for which the compact model is developed. The p-well bulk (B) is diffused from the source-side under the gate (G), and thus forms a graded channel region. The internal drain Di represents the point where the graded channel (of length L) turns into the lightly doped n^{-}-drift region (of length L_D and thickness t_{Si}). With the gate extending over the drift region, an accumulation layer forms in the drift region underneath the gate oxide. Thus, above the threshold voltage of the channel region, electrons flow

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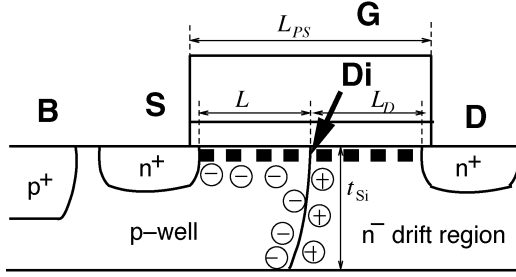

Fig. 1. Cross section of the LDMOS transistor, for which the compact model is derived.

through an inversion channel from the source terminal (S) toward the drain terminal (D) at the end of the drift region.

In our compact modeling approach, expressions for the current $I_{\rm ch}$ through the inversion channel as well as for the current $I_{\rm dr}$ through the drift region are derived, both in terms of the known external drain, gate, source, and bulk voltages $V_{\rm D}$, V_G, $V_{\rm S}$, and V_B, respectively, as well as of the unknown internal drain voltage $V_{\rm Di}$. In contrast to a subcircuit model, this internal drain voltage is expressed explicitly in terms of the external terminal voltages. The expression for this internal drain voltage is derived by equating $I_{\rm ch}$ to $I_{\rm dr}$. Next, the internal drain voltage is used to calculate (also in an explicit way) the surface potentials, in which the final drain-to-source current $I_{\rm DS}$ is formulated. In this way, $I_{\rm DS}$ is surface-potential based and it is explicitly expressed in terms of the external terminal voltages.

A. Channel Current

To obtain an accurate and continuous description of the channel current and its derivatives in all operation regimes, a charge-sheet MOSFET model approach based on surface-potential formulations is taken. In the channel region, the surface potential ψ_s satisfies the implicit equation obtained from Poisson's equation and Gauss' law [16]. In order to reduce computation time, the explicit yet accurate relation between the surface potential and the terminal voltages according to [17] is used. By denoting this explicit relation by Ψ, we thus write the surface potentials ψ_{s_0} at the source $x = 0$ and ψ_{s_L} at the internal drain $x = L$ according to

$$\begin{aligned}\psi_{s_0} &= \Psi[V_{\rm SB} + \phi_B, V_{\rm GB} - V_{\rm FB}; k_0]\\ \psi_{s_L} &= \Psi[V_{\rm DiB} + \phi_B, V_{\rm GB} - V_{\rm FB}; k_0]\end{aligned} \tag{1}$$

valid in all regimes ranging from accumulation to weak and strong inversion. Here, $V_{\rm FB}$ is the flatband voltage of the channel region, and $k = \sqrt{2q\epsilon_{\rm Si}N_A}/C_{\rm ox}$ is the body factor, with $C_{\rm ox} = \epsilon_{\rm ox}/t_{\rm ox}$ the gate oxide capacitance per unit area, $t_{\rm ox}$ the oxide thickness, q the electronic charge, $\epsilon_{\rm Si}$ the permittivity of silicon, $\epsilon_{\rm ox}$ that of oxide, and N_A the p-well doping concentration. The potential $\phi_B = 2\phi_F$ is taken as model parameter, where the Fermi-potential ϕ_F of the channel is given by $\phi_F = \phi_T \ln(N_A/n_i)$, with n_i the intrinsic carrier concentration of silicon and ϕ_T the thermal voltage.

Due to the p-diffusion from the source side under the gate, the doping concentration N_A, and thus the body factor k, decreases toward the end of the channel region. However, since the current is only significant once the source side is in strong inversion, we will further assume an effective body factor k_0 equal to the one at the source side.

The channel current is given by

$$I_{\rm ch} = \frac{W\mu_{\rm ch}}{L}\left(\int_{\psi_{s_0}}^{\psi_{s_L}} (-Q_{\rm inv})d\psi_s + \phi_T\left(Q_{{\rm inv}_L} - Q_{{\rm inv}_0}\right)\right) \tag{2}$$

where W is the device width, $\mu_{\rm ch}$ the electron mobility, and $Q_{\rm inv} = -C_{\rm ox}V_{\rm inv}$ is the strong inversion charge with

$$V_{\rm inv} = V_{\rm GB} - V_{\rm FB} - \psi_s - k_0\sqrt{\psi_s}. \tag{3}$$

Here, $Q_{{\rm inv}_0}$ and $Q_{{\rm inv}_L}$ represent the strong inversion charge per unit area at $x = 0$ and $x = L$, respectively. Next, we approximate the inversion charge by making a Taylor expansion of $V_{\rm inv}$ around $\psi_s = \psi_{s_0}$, i.e.,

$$V_{\rm inv} = V_{{\rm inv}_0} - \xi\left(\psi_s - \psi_{s_0}\right) \tag{4}$$

in which $V_{{\rm inv}_0}$ represents the inversion charge at the source, and $\xi = 1 + (1/2)k_0/\sqrt{V_1 + \psi_{s_0}}$. For simplicity, a fixed voltage $V_1 = 1$ V is used, and after substitution of (3) and (4) into (2) we arrive at

$$I_{\rm ch} = \frac{W\mu_{\rm ch}C_{\rm ox}}{L}\left(V_{{\rm inv}_0} - \frac{1}{2}\xi\Delta\psi_s + \xi\phi_T\right)\Delta\psi_s \tag{5}$$

where $\Delta\psi_s = \psi_{s_L} - \psi_{s_0}$ is the potential drop across the channel. In this way, $I_{\rm ch}$ is a second-order polynomial in ψ_{s_L}, which will provide us, later, the explicit solution of the internal drain potential $V_{\rm Di}$.

Velocity saturation in the channel is accounted for by taking the mobility $\mu_{\rm ch}$ equal to

$$\mu_{\rm ch} = \frac{\mu_{\rm eff}}{1 + \theta_3\Delta\psi_s} \tag{6}$$

with $\mu_{\rm eff}$ representing the effective electron mobility, and θ_3 a model parameter given by $\theta_3 = \mu_0/(Lv_{\rm sat})$ with μ_0 the zero-field electron mobility and $v_{\rm sat}$ the saturated drift velocity of electrons (cf. [18, p. 283]). The effective electron mobility is bias dependent according to

$$\mu_{\rm eff} = \frac{\mu_0}{F_{\rm mob}}, \quad F_{\rm mob} = 1 + a_\theta E_{\rm eff} \tag{7}$$

for constant a_θ, and $E_{\rm eff}$ representing the effective vertical electrical field in the channel region. This field, given by [18, p. 185], is taken equal to the one at the source, i.e., equal to

$$E_{{\rm eff}_0} = -\frac{Q_{{\rm inv}_0} + \eta Q_{{\rm dep}_0}}{\epsilon_{\rm Si}} \tag{8}$$

where $Q_{{\rm dep}_0}$ represents the depletion charge per unit area at the source side, and η is a constant, ideally equal to 1/2 for electrons and 1/3 for holes. For ease of parameter extraction, we next replace in the equation above $Q_{{\rm dep}_0}$ by $Q_{{\rm dep}_0} - Q_{{\rm dep}_0}|_{V_{\rm SB}=0}$, and obtain

$$F_{\rm mob} = 1 + \theta_1 V_{{\rm inv}_0} + \theta_2\left(\sqrt{\psi_{s_0}} - \sqrt{\psi_{s_0}|_{V_{\rm SB}=0}}\right) \tag{9}$$

where $\theta_1 = a_\theta C_{\rm ox}/\epsilon_{\rm Si}$ and $\theta_2 = a_\theta C_{\rm ox}\eta/\epsilon_{\rm Si}$ are model parameters. Notice that with the above choice of mobility model, both the current and the conductances are fully continuous, also in $V_{\rm DS} = 0$. In the model, $\beta = W\mu_0 C_{\rm ox}/L$ is taken as model parameter.

B. Drift Region Current

For devices with a drift region length L_D in the same order of magnitude as the inversion channel length L, the channel current saturates before the onset of depletion in the drift region

[13]. In the linear operating regime, the drift region current $I_{\rm dr}$, neglecting the diffusion current, is thus given by

$$I_{\rm dr} = \frac{W\mu_{\rm acc}}{L_D}\int_{V_{\rm Di}}^{V_{\rm D}} \left(-Q_{\rm acc}^{\rm dr}\right) dV_{\rm C} + \frac{W\mu_{\rm dr}}{L_D}\int_{V_{\rm Di}}^{V_{\rm D}} \left(-Q_b^{\rm dr}\right) dV_{\rm C} \qquad (10)$$

in which the first term is the current through the accumulation layer, and the second one the current through the bulk of the drift region. Here, $\mu_{\rm acc}$ is the electron mobility through the accumulation layer, while $\mu_{\rm dr}$ is that through the bulk. Furthermore, $Q_{\rm acc}^{\rm dr}$ represents the charge per unit area in the accumulation layer, and $Q_b^{\rm dr}$ the number of dopants per unit area in the bulk of the drift region. For given potential $V_{\rm C} \in [V_{\rm Di}, V_{\rm D}]$ along the lateral position of the drift region, the accumulation charge is given by

$$Q_{\rm acc}^{\rm dr} = -C_{\rm ox}V_{\rm acc} = -C_{\rm ox}\left(V_{\rm GC} - V_{\rm FB}^{\rm dr}\right) \qquad (11)$$

valid for $V_{\rm GC} > V_{\rm FB}^{\rm dr}$. The number of dopants per unit area is given by

$$Q_b^{\rm dr} = -qN_D t_{\rm Si_{eff}} \qquad (12)$$

where N_D is the doping level of the drift region, and $t_{\rm Si_{eff}}$ is its effective thickness. Due to depletion in the drift region caused by the pn-junction, the effective thickness is given by $t_{\rm Si_{eff}} = t_{\rm Si} - t_{\rm dep}$, where $t_{\rm dep}$ is the thickness of the depletion layer. In the LDMOS device, the extension of the depletion layer into the drift region is a two-dimensional effect. Since incorporation of the two-dimensional depletion effect is too complicated, we follow a pragmatic approach, and write for ease of parameter extraction the effective drift region thickness as

$$t_{\rm Si_{eff}} = t_{\rm Si}|_{V_{\rm SB}=0} f_{\rm lin} \qquad (13)$$

where $t_{\rm Si}|_{V_{\rm SB}=0}$ is the thickness at $V_{\rm SB} = 0$. The function $f_{\rm lin}$ accounts for $V_{\rm SB} > 0$ for the reduction of the drift region thickness due to the extension of the depletion layer into the drift region, according to

$$f_{\rm lin} = 1 - \lambda\frac{\sqrt{\phi_0 + V_{\rm SB}} - \sqrt{\phi_0}}{\sqrt{\phi_0}}. \qquad (14)$$

Here, λ is a model parameter. Subsequently, elaboration of (10) yields

$$I_{\rm dr} = \frac{f_{\rm lin}}{R_D}V_{\rm DDi} + \frac{W\mu_{\rm acc}C_{\rm ox}}{2L_D}\left(\left(V_{\rm acc_{Di}}\right)^2 - \left(V_{\rm acc_D}\right)^2\right) \quad (15)$$

where $V_{\rm acc_{Di}}$ and $V_{\rm acc_D}$ represent the accumulation charge at the internal drain Di and at the drain D, respectively. In the model the on-resistance R_D of the drift region, given by

$$R_D = \frac{L_D}{W\mu_{\rm dr}qN_D t_{\rm Si}|_{V_{\rm SB}=0}} \qquad (16)$$

is taken as a model parameter.

The electron mobility in the accumulation layer is reduced by the vertical electrical field, according to

$$\mu_{\rm acc} = \frac{\mu_{\rm acc0}}{F_{\rm mob,acc}}, \quad F_{\rm mob,acc} = 1 + a_{\theta,\rm acc}E_{\rm eff}^{\rm dr} \qquad (17)$$

where $a_{\theta,\rm acc}$ is a constant, and $E_{\rm eff}^{\rm dr} = -Q_{\rm acc}^{\rm dr}/\epsilon_{\rm Si}$ represents the effective vertical electrical field in the drift region. To arrive at a sufficiently simple expression for $I_{\rm dr}$, the effective vertical electrical field is taken equal to $E_{\rm eff}^{\rm dr} = -(1/2)(Q_{\rm acc}^{\rm dr}|_{V_{\rm C}=V_{\rm S}} + Q_{\rm acc}^{\rm dr}|_{V_{\rm C}=V_{\rm D}})/\epsilon_{\rm Si}$, and obtain

$$F_{\rm mob,acc} = 1 + \theta_{\rm 1acc}\left(\frac{1}{2}(V_{\rm GS} + V_{\rm GD}) - V_{\rm FB}^{\rm dr}\right) \qquad (18)$$

for given model parameter $\theta_{\rm 1acc} = a_{\theta,\rm acc}C_{\rm ox}/\epsilon_{\rm Si}$. In the model, also $\beta_{\rm acc} = W\mu_{\rm acc0}C_{\rm ox}/L_D$ is taken as model parameter. Thus, we arrive at a second-order polynomial of the drift region current $I_{\rm dr}$ in terms of $V_{\rm Di}$, valid in the linear operating regime, i.e., provided that $V_{\rm GD} - V_{\rm FB}^{\rm dr} > 0$.

C. Calculation of Internal Drain Potential

In the linear operating regime, the potential drop $\Delta\psi_s$ approximately equals $V_{\rm DiS}$. Thus, the internal drain potential is solved from

$$I_{\rm ch}|_{\Delta\psi_s = V_{\rm DiS}} = I_{\rm dr}. \qquad (19)$$

As the potential drop in the linear regime is relatively small, we neglect, while solving (19), the mobility reduction term due to the lateral electrical field (i.e., $\theta_3 = 0$) in $I_{\rm ch}$. In this way, we obtain a second order polynomial for the channel current in terms of the unknown potential drop $V_{\rm DiS}$, and the solution of (19) for $V_{\rm DiS}$ is explicitly expressed in terms of the terminal voltages.

The current is assumed to saturate in the *channel* region. Thus, in saturation we derive the potential drop $V_{\rm DiS} = V_{\rm DiS,sat}$ from solving

$$\left.\frac{\partial I_{\rm ch}}{\partial\Delta\psi_s}\right|_{\Delta\psi_s = V_{\rm DiS,sat}} = 0. \qquad (20)$$

Subsequently, we incorporate saturation by taking an effective potential drop $V_{\rm DiS,eff}$ according to [19], which takes the minimum of $V_{\rm DiS}$ and $V_{\rm DiS,sat}$ in a smooth manner. Finally, the surface potential ψ_{s_L} is calculated by using $V_{\rm DiB} = V_{\rm SB} + V_{\rm DiS,eff}$ in (1).

D. Additional Effects

In the final current calculation of $I_{\rm DS}$, second-order effects like channel length modulation, drain-induced barrier lowering, and static feedback are incorporated. Also, the effect on drain and bulk current of avalanche occurring in the MOSFET region is taken into account. Finally, the temperature dependence of the relevant model parameters is included.

III. DC Results

We have characterized a 12-V SOI-LDMOS transistor, with oxide thickness $t_{\rm ox} = 38$ nm, and with different mask widths $W_{\rm mask}$, gate mask lengths $L_{\rm PS}$, and ambient temperatures T. In addition, a thermal subcircuit is used in which the temperature rise due to self-heating is calculated [5]. In the following figures, symbols correspond to the measurement data, while the solid lines represent our compact model. In Fig. 2 we observe that the model describes the subthreshold current accurately and in a smooth manner also at the transition from the weak- to strong inversion regime. In Fig. 3, we observe that in the linear regime the model is also accurate at high gate voltages, where the effect of the gate extending over the drift region is significant. In Fig. 4, we observe that for $V_{\rm GS} = 6$, and 12 V, the output conductance

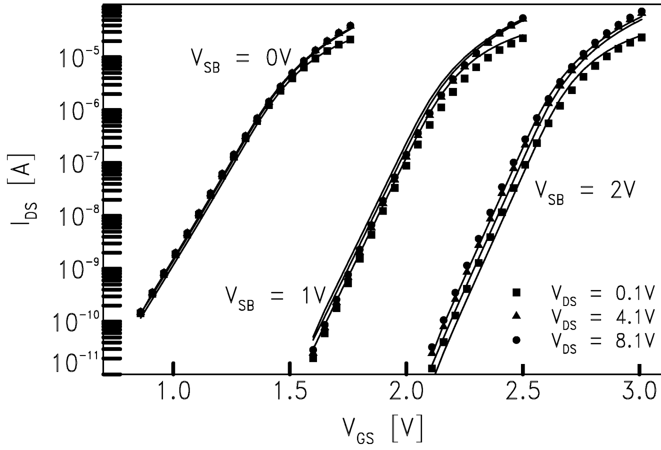

Fig. 2. Measured (symbols) and modeled (solid lines) drain current $I_{\rm DS}$ in the subthreshold operating regime, for $V_{\rm SB} = 0$, 1 and 2 V, for $W_{\rm mask} = 17$ μm, $L_{\rm PS} = 1.6$ μm, and $T = 25$ °C.

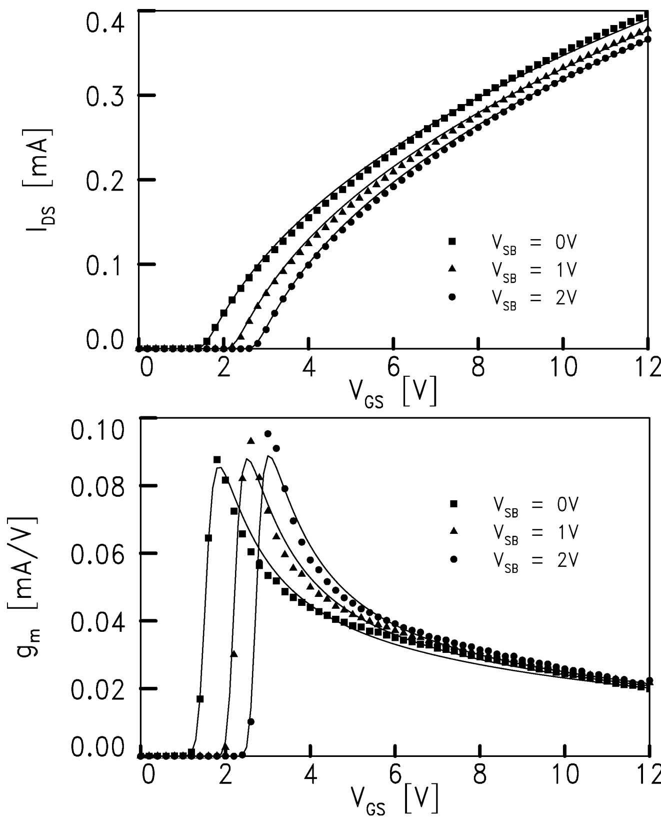

Fig. 3. Measured (symbols) and modeled (solid lines) drain current $I_{\rm DS}$ and transconductance $g_{\rm m} = \partial I_{\rm DS}/\partial V_{\rm GS}$ in the linear operating regime for $V_{\rm DS} = 0.1$ V, and for various bulk voltages $V_{\rm SB}$, for $W_{\rm mask} = 17$ μm, $L_{\rm PS} = 1.6$ μm, and $T = 25$ °C.

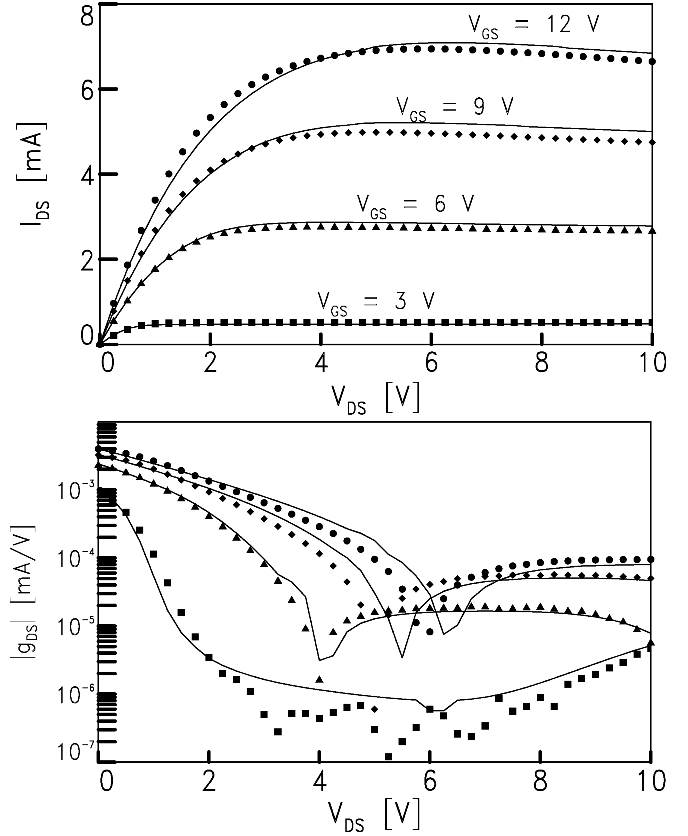

Fig. 4. Measured (symbols) and modeled (solid lines) drain current $I_{\rm DS}$ and output conductance $g_{\rm DS} = \partial I_{\rm DS}/\partial V_{\rm DS}$ for $V_{\rm GS} = 3$, 6, 9, and 12 V, and $V_{\rm SB} = 0$ V, for $W_{\rm mask} = 17$ μm, $L_{\rm PS} = 1.6$ μm and $T = 25$ °C.

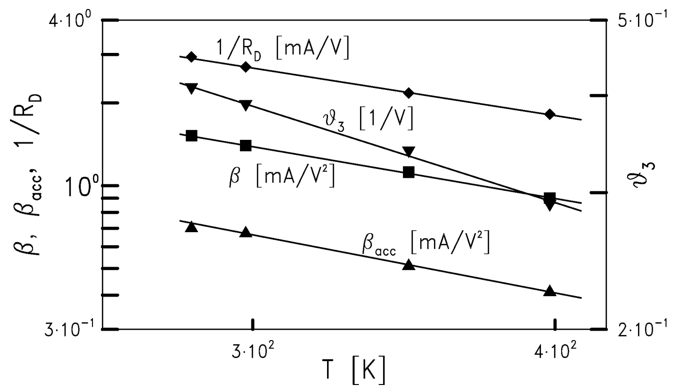

Fig. 5. Model parameter scaling of β, $\beta_{\rm acc}$, R_D, and θ_3 with ambient temperature T.

becomes negative, due to self-heating. We conclude that also the saturation regime is well described by our LDMOS model for both low and high gate voltages.

Next we demonstrate the physical scaling of the model with device width, drift region length and temperature. In Fig. 5 we observe that the model parameters indeed exhibit the temperature power-law behavior as expected from physics. In Fig. 6, we see that the gain parameters β and $\beta_{\rm acc}$ as well as the drift region conductance $1/R_D$ indeed scale with width. Finally, the dependence of the model on the device length is demonstrated by varying the gate mask length $L_{\rm PS}$. As the channel region length L is fixed due to the diffusion process, varying the gate mask length implies that we vary the length L_D of the drift region. In Fig. 7 we observe that the model predicts the electrical behavior accurately for the various lengths. Moreover, as we observe in Fig. 8, the resistance parameters $1/\beta_{\rm acc}$ and R_D of the drift region scale linearly with gate length $L_{\rm PS}$, i.e., with drift region length L_D, as expected. Thus, the model scales well with device width, length and temperature. Finally, we mention that the model has been successfully used to characterize different wafer-process technologies with the same accurate results.

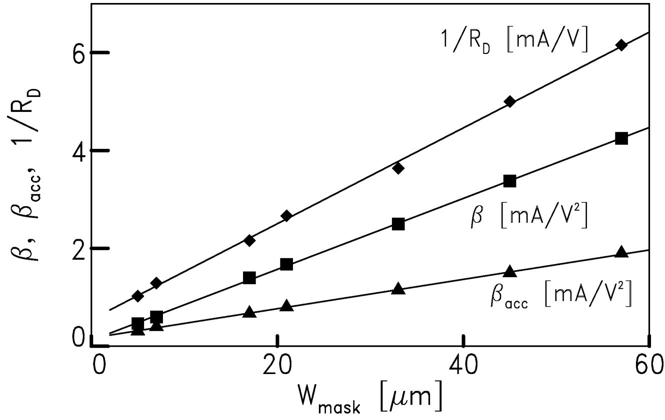

Fig. 6. Model parameter scaling of β, $\beta_{\rm acc}$, and R_D with device mask width $W_{\rm mask}$.

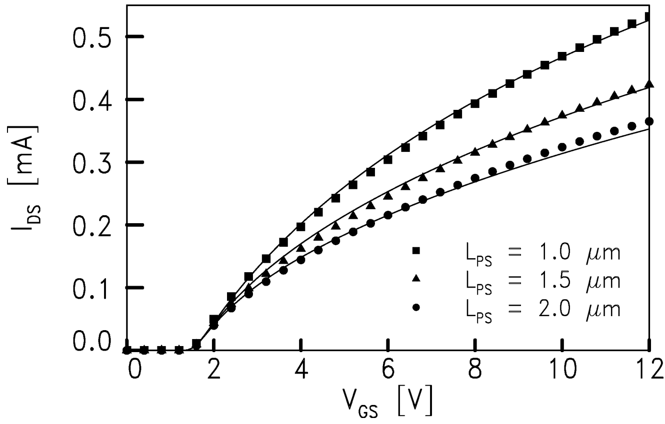

Fig. 7. Drain current $I_{\rm DS}$ in the linear operating regime at $V_{\rm DS} = 0.1$ V and $V_{\rm SB} = 0$ V, for $W_{\rm mask} = 17\ \mu$m, $T = 25\ ^\circ$C, and various gate lengths $L_{\rm PS}$.

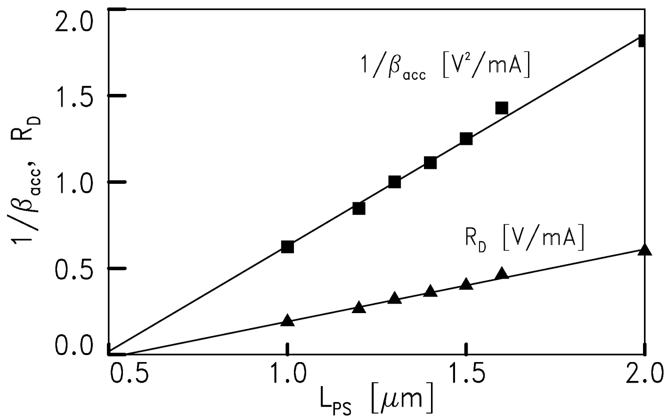

Fig. 8. Drift region model parameter scaling of $\beta_{\rm acc}$ and R_D with gate length $L_{\rm PS}$.

IV. Nodal Charge Model

In order to simulate the time-dependent behavior of the LDMOS transistor, we have developed a nodal charge model. In this charge model, the total gate charge $Q_{\rm G}$ is given by the sum of the gate charge of the channel region and that of the drift region [14], i.e., $Q_{\rm G} = Q_{\rm G}^{\rm ch} + Q_{\rm G}^{\rm dr}$ where the gate charge of the channel and that of the drift region are, respectively, given by [14]

$$Q_{\rm G}^{\rm ch} = -W\int_0^L (Q_{\rm acc} + Q_{\rm dep} + Q_{\rm inv})dx$$
$$Q_{\rm G}^{\rm dr} = -W\int_L^{L+L_D} \left(Q_{\rm acc}^{\rm dr} + Q_{\rm dep}^{\rm dr} + Q_{\rm inv}^{\rm dr}\right)dx. \quad (21)$$

Thus, the nodal gate charge consists of the opposite of the total charge underneath the thin gate oxide, being accumulation, depletion and inversion charge.

The total bulk charge $Q_{\rm B}$ of the transistor is given by the sum of the bulk charge due to the channel region and that of the drift region, i.e., $Q_{\rm B} = Q_{\rm B}^{\rm ch} + Q_{\rm B}^{\rm dr}$, where the bulk charge of the channel and that of the drift region are respectively given by

$$Q_{\rm B}^{\rm ch} = W\int_0^L (Q_{\rm acc} + Q_{\rm dep})dx$$
$$Q_{\rm B}^{\rm dr} = W\int_L^{L+L_D} Q_{\rm inv}^{\rm dr}dx. \quad (22)$$

Notice that for sufficiently negative gate voltages, holes enter the drift region from the p-well bulk, which gives rise to an inversion charge in the drift region.

Since the LDMOS transistor is asymmetric, two limits are identified for the distribution of the charge underneath the thin gate oxide, cf. [14]. The first limit is valid well-above threshold (i.e., for the gate voltage sufficiently large), and the drain charge is approximated by

$$Q_{\rm D} = F_L Q_{\rm D_{inv}}^{\rm ch} + Q_{\rm D_{acc}}^{\rm dr} + F_L Q_{\rm S_{acc}}^{\rm dr} + Q_{\rm D_{dep}}^{\rm dr} \quad (23)$$

as one would expect from the Ward–Dutton charge partitioning scheme [20] (valid in case of a uniform MOSFET). Here, $F_L = L/(L + L_D)$, and

$$Q_{\rm D_{inv}}^{\rm ch} = W\int_0^L \frac{x}{L}Q_{\rm inv}dx$$
$$Q_{\rm D_{acc}}^{\rm dr} = W\int_0^{L_D} \frac{\tilde{x}}{L_D}Q_{\rm acc}^{\rm dr}d\tilde{x}$$
$$Q_{\rm S_{acc}}^{\rm dr} = W\int_0^{L_D} \left(1 - \frac{\tilde{x}}{L_D}\right)Q_{\rm acc}^{\rm dr}d\tilde{x}$$
$$Q_{\rm D_{dep}}^{\rm dr} = W\int_0^{L_D} Q_{\rm dep}^{\rm dr}d\tilde{x}. \quad (24)$$

The second limit is valid below threshold (i.e., for the gate voltage sufficiently small), and the drain charge is approximated by

$$Q_{\rm D} = F_L Q_{\rm D_{inv}}^{\rm ch} + Q_{\rm D_{acc}}^{\rm dr} + Q_{\rm S_{acc}}^{\rm dr} + Q_{\rm D_{dep}}^{\rm dr} \quad (25)$$

which means that all accumulation charge of the drift region is attributed to the drain. In [14], the above charge partitioning is referred to as *modified* Ward–Dutton charge partitioning. Thus, the drain charge $Q_{\rm D}$ is expressed in terms of the nodal charges of both the channel and the drift region. In the model, the transition from the first limit (23) into the second limit (25) has been implemented in a smooth and continuous way.

The nodal charges of the channel region can be expressed in its surface potentials at $x = 0$ and $x = L$. To that end, a transformation from integration variable x to ψ_s, as described in [21], is performed, so that the integrals of (21) and (24) along the channel region can be written as

$$Q_{\rm G}^{\rm ch} = C_{\rm OX}\left(\overline{V}_{\rm ox} + \frac{A}{12\xi}\Delta V_{\rm inv}\right) \tag{26}$$

and

$$Q_{\rm D_{inv}}^{\rm ch} = -\frac{C_{\rm OX}}{2}\left(\overline{V}_{\rm inv} - \frac{\Delta V_{\rm inv}}{6}\left\{1 - \frac{A}{2} - \frac{A^2}{20}\right\}\right) \tag{27}$$

where the potential $\overline{V}_{\rm ox} = V_{\rm GB} - V_{\rm FB} - (1/2)(\psi_{s_0} + \psi_{s_L})$ represents the average voltage drop across the oxide, the fraction A is given by $A = \Delta V_{\rm inv}/(\overline{V}_{\rm inv} + \xi\phi_T)$, and

$$\overline{V}_{\rm inv} = \frac{1}{2}\left(V_{{\rm inv}_0} + V_{{\rm inv}_L}\right), \quad \Delta V_{\rm inv} = V_{{\rm inv}_0} - V_{{\rm inv}_L}. \tag{28}$$

In the model, $C_{\rm OX} = WLC_{\rm ox}$ is taken as parameter.

The nodal bulk charge $Q_{\rm B}^{\rm ch}$ is calculated via the nodal source charge $Q_{\rm S_{inv}}^{\rm ch}$. With the latter given by

$$\begin{aligned} Q_{\rm S_{inv}}^{\rm ch} &:= W\int_0^L \left(1 - \frac{x}{L}\right) Q_{\rm inv} dx \\ &= -\frac{C_{\rm OX}}{2}\left(\overline{V}_{\rm inv} + \frac{\Delta V_{\rm inv}}{6}\left\{1 + \frac{A}{2} - \frac{A^2}{20}\right\}\right) \end{aligned} \tag{29}$$

we take for the nodal bulk charge of the channel region

$$Q_{\rm B}^{\rm ch} = -\left(Q_{\rm G}^{\rm ch} + Q_{\rm D_{inv}}^{\rm ch} + Q_{\rm S_{inv}}^{\rm ch}\right) \tag{30}$$

which thus, consists of the depletion and accumulation charge of the channel region.

The nodal charges of the drift region can be expressed in terms of its surface potentials at $x = L$ and $x = L + L_D$. Analogously as has been done for the channel region, a transformation from integration variable $\tilde{x}$ to $V_{\rm C}$ is performed, so that the integrals of (21) and (24) for the drift region can be written as

$$\begin{aligned} Q_{\rm G}^{\rm dr} &= C_{\rm OX}^{\rm dr}\left(\overline{V}_{\rm ox}^{\rm dr} + \frac{A_{\rm acc}}{12}\Delta V_{\rm acc}\right) \\ Q_{\rm D_{acc}}^{\rm dr} &= -\frac{C_{\rm OX}^{\rm dr}}{2}\left(\overline{V}_{\rm acc} - \frac{\Delta V_{\rm acc}}{6}\left\{1 - \frac{A_{\rm acc}}{2} - \frac{A_{\rm acc}^2}{20}\right\}\right), \\ Q_{\rm S_{acc}}^{\rm dr} &= -\frac{C_{\rm OX}^{\rm dr}}{2}\left(\overline{V}_{\rm acc} + \frac{\Delta V_{\rm acc}}{6}\left\{1 + \frac{A_{\rm acc}}{2} - \frac{A_{\rm acc}^2}{20}\right\}\right) \end{aligned} \tag{31}$$

where

$$\overline{V}_{\rm acc} = \frac{1}{2}\left(V_{\rm acc_{Di}} + V_{\rm acc_D}\right) \quad \Delta V_{\rm acc} = V_{\rm acc_{Di}} - V_{\rm acc_D} \tag{32}$$

and the fraction $A_{\rm acc}$ is given by

$$A_{\rm acc} = \frac{\Delta V_{\rm acc}}{\overline{V}_{\rm acc} + \frac{f_{\rm lin}F_{\rm mob,acc}}{(\beta_{\rm acc}R_D)}} \tag{33}$$

while $C_{\rm OX}^{\rm dr} = WL_DC_{\rm ox}$ is taken as model parameter. The potential $\overline{V}_{\rm ox}^{\rm dr}$ represents the average voltage drop across the oxide in the drift region, and is given by

$$\overline{V}_{\rm ox}^{\rm dr} = \frac{1}{2}(V_{\rm GD} + V_{\rm GDi}) - V_{\rm FB}^{\rm dr} - \frac{1}{2}\left(\tilde{\psi}_{s_{\rm D}} + \tilde{\psi}_{s_{\rm Di}}\right) \tag{34}$$

where $\tilde{\psi}_s$ is the surface potential in the drift region with reference to bulk of the drift region. Thus, by use of the function Ψ, we write

$$\begin{aligned} \tilde{\psi}_{s_{\rm Di}} &= -\Psi\left[V_{\rm DiB} + \phi_B^{\rm dr}, -\left(V_{\rm GDi} - V_{\rm FB}^{\rm dr}\right); k_{\rm dr}\right] \\ \tilde{\psi}_{s_{\rm D}} &= -\Psi\left[V_{\rm DB} + \phi_B^{\rm dr}, -\left(V_{\rm GD} - V_{\rm FB}^{\rm dr}\right); k_{\rm dr}\right] \end{aligned} \tag{35}$$

where $\phi_B^{\rm dr} = -2\phi_F^{\rm dr}$, $\phi_F^{\rm dr} = -\phi_T\ln(N_D/n_i)$, and $k_{\rm dr}$ is the body factor of the drift region, i.e., $k_{\rm dr} = \sqrt{2q\epsilon_{\rm Si}N_D}/C_{\rm ox}$.

The depletion charge in the drift region is taken as

$$Q_{\rm dep}^{\rm dr} = k_{\rm dr}C_{\rm ox}\sqrt{-\tilde{\psi}_s} \tag{36}$$

and the inversion charge in the drift region as $Q_{\rm inv}^{\rm dr} = C_{\rm ox}V_{\rm inv}^{\rm dr}$, with

$$V_{\rm inv}^{\rm dr} = -\left(V_{\rm GC} - V_{\rm FB}^{\rm dr}\right) + \tilde{\psi}_s - k_{\rm dr}\sqrt{-\tilde{\psi}_s}. \tag{37}$$

Subsequently, the charges $Q_{\rm D_{dep}}^{\rm dr}$ and $Q_{\rm B}^{\rm dr}$ are approximated by their average values in the drift region. Thus, the nodal charges in the drift region are also given in surface potential formulations.

V. AC Results

In order to verify the charge model, measurements were performed on 14-V SOI-LDMOS devices with bulk and source tied together, by use of a S-parameter analyzer at a frequency f of 100 MHz. The oxide thickness $t_{\rm ox}$ is 60 nm, while the mask width $W_{\rm mask}$ varied from 10 to 100 μm. We performed an open correction, and included a gate resistance R_G in our model, of 340 Ω. Furthermore, to model the capacitance of the pn-junction between the p-well and n$^-$-drift region we used an additional capacitance model for this junction. The layouts we measured were common drain, which provide access to the Y-parameters $Y_{\rm GG}$, $Y_{\rm GD}$, $Y_{\rm DG}$ and $Y_{\rm DD}$. The capacitances of the device without gate resistance are determined from the Y-parameters including gate resistance, by means of

$$\begin{aligned} C_{\rm GG} &= \frac{{\rm Im}\{Y_{\rm GG}\}}{\omega} \\ C_{\rm GD} &= \frac{{\rm Im}\{Y_{\rm GD}\}}{\omega} \\ C_{\rm DG} &= \frac{{\rm Im}\{Y_{\rm DG}\}}{\omega} - R_G{\rm Re}\{Y_{\rm DG}\}\frac{{\rm Im}\{Y_{\rm GG}\}}{\omega} \\ C_{\rm DD} &= \frac{{\rm Im}\{Y_{\rm DD}\}}{\omega} - R_G{\rm Re}\{Y_{\rm DG}\}\frac{{\rm Im}\{Y_{\rm GD}\}}{\omega} \end{aligned} \tag{38}$$

where $\omega = 2\pi f$. In Figs. 9–15, the measured capacitance values are shown, compared to simulations. Notice that in Figs. 9–12 the capacitances are plotted versus gate voltage, while in Figs. 13–15 they are plotted versus drain voltage.

In Fig. 9 we observe that the capacitances $C_{\rm GG}$ and $C_{\rm GD}$ for $V_{\rm DS} = 0$ agree well with the modeled ones, over the total $V_{\rm GS}$ range. The transition from accumulation in the channel and inversion in the drift region for sufficiently negative gate voltage,

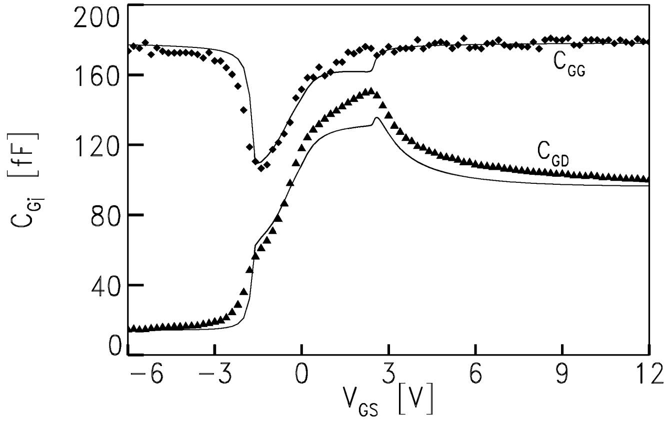

Fig. 9. Measured (symbols) and modeled (solid lines) capacitance value $C_{\rm GG}$ and $C_{\rm GD}$ versus $V_{\rm GS}$, for $V_{\rm DS} = 0$ V, for $W_{\rm mask} = 50\ \mu$m, and $L_{\rm PS} = 5\ \mu$m.

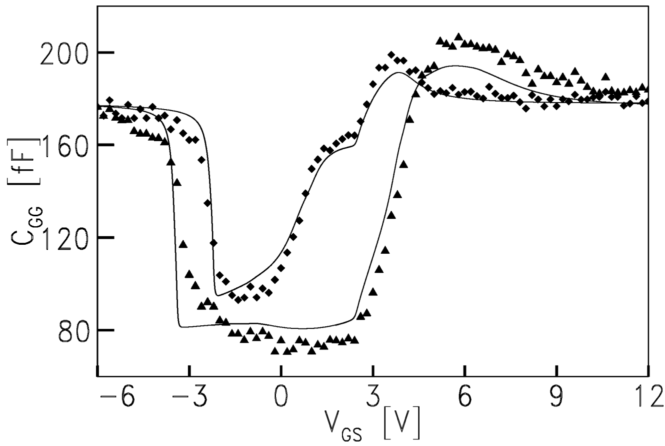

Fig. 10. Measured (symbols) and modeled (solid lines) capacitance value $C_{\rm GG}$ versus $V_{\rm GS}$, for $V_{\rm DS} = 1$ and 5 V, for $W_{\rm mask} = 50\ \mu$m, and $L_{\rm PS} = 5\ \mu$m.

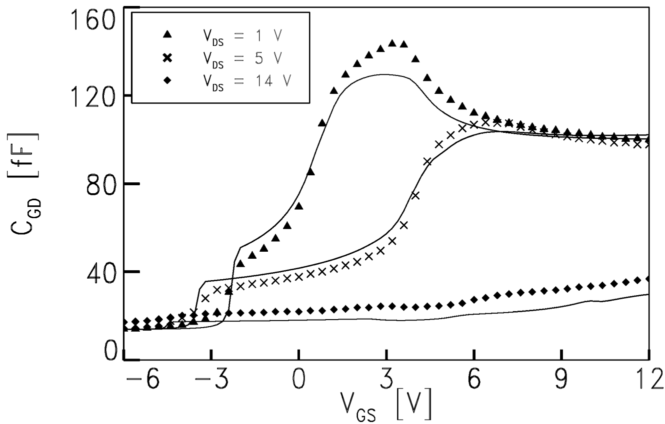

Fig. 11. Measured (symbols) and modeled (solid lines) capacitance value $C_{\rm GD}$ versus $V_{\rm GS}$, for $V_{\rm DS} = 1$, 5, and 14 V, for $W_{\rm mask} = 50\ \mu$m, and $L_{\rm PS} = 5\ \mu$m.

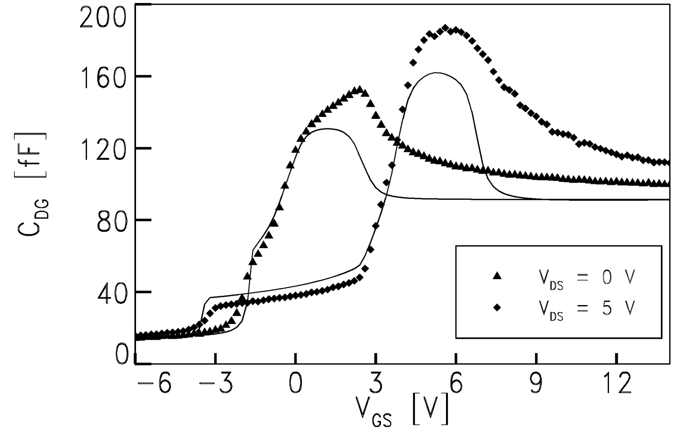

Fig. 12. Measured (symbols) and modeled (solid lines) capacitance value $C_{\rm DG}$ versus $V_{\rm GS}$, for $V_{\rm DS} = 0$ and 5 V, for $W_{\rm mask} = 50\ \mu$m, and $L_{\rm PS} = 5\ \mu$m.

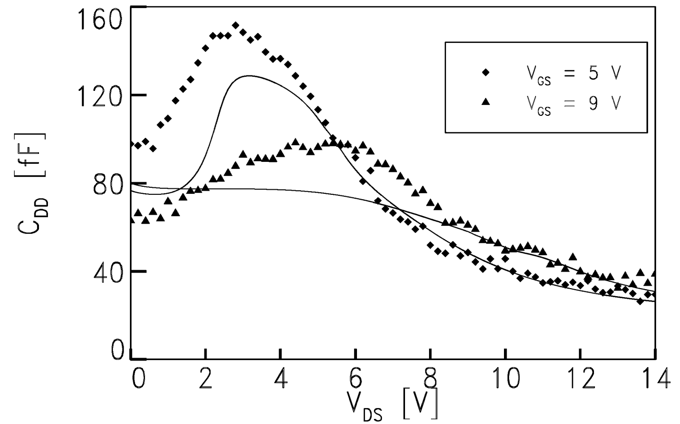

Fig. 13. Measured (symbols) and modeled (solid lines) capacitance value $C_{\rm DD}$ versus $V_{\rm DS}$, for $V_{\rm GS} = 5$ and 9 V, for $W_{\rm mask} = 50\ \mu$m, and $L_{\rm PS} = 5\ \mu$m.

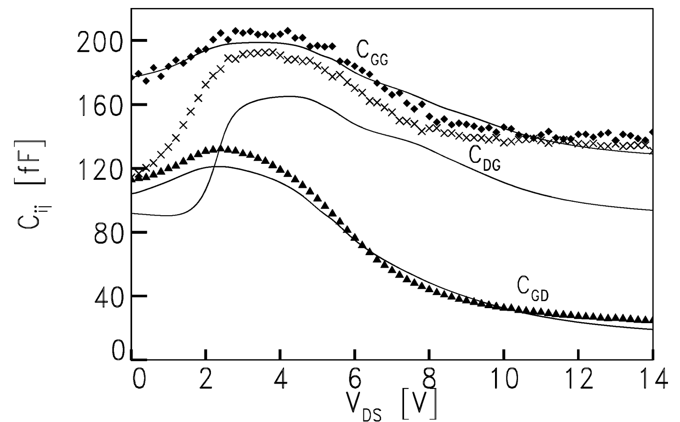

Fig. 14. Measured (symbols) and modeled (solid lines) capacitance values $C_{\rm GG}$, $C_{\rm GD}$ and $C_{\rm DG}$ versus $V_{\rm DS}$, for $V_{\rm GS} = 5$ V, for $W_{\rm mask} = 50\ \mu$m, and $L_{\rm PS} = 5\ \mu$m.

into strong inversion in the channel and accumulation in the drift region for sufficiently positive gate voltage, is accurately modeled. In Figs. 10 and 11 we observe that also when dc current is flowing for $V_{\rm DS} > 0$, these capacitances are very well described by the model. Notice that the internal drain solution $V_{\rm DiS}$ automatically accounts for the decrease of $C_{\rm GD}$ above the threshold voltage (which is about 3 V). In general, from the results of Figs. 9–11 we conclude that the nodal gate charge $Q_{\rm G}$ adequately models the small signal current through the gate.

In Figs. 12 and 13, the capacitances representing the small signal current through the drain terminal are plotted. Notice that

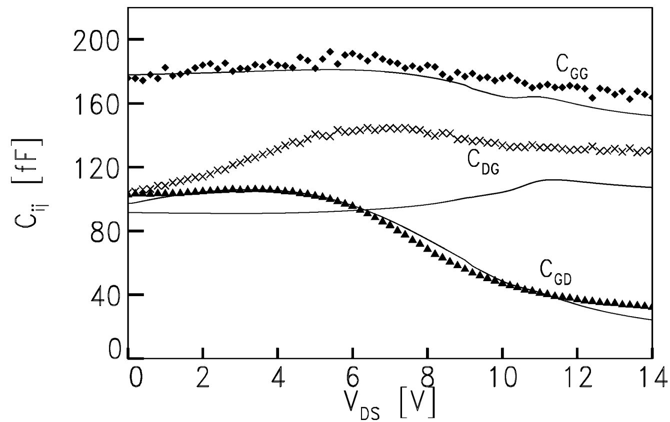

Fig. 15. Measured (symbols) and modeled (solid lines) capacitance values $C_{\rm GG}$, $C_{\rm GD}$ and $C_{\rm DG}$ versus $V_{\rm DS}$, for $V_{\rm GS} = 9$ V, for $W_{\rm mask} = 50$ μm, and $L_{\rm PS} = 5$ μm.

the results also depend on the gate resistance and the capacitance values $C_{\rm GG}$ and $C_{\rm GD}$; see (38). In Fig. 12 we observe that the capacitance value $C_{\rm DG}$ is reasonably well described. As a result of the modified Ward–Dutton charge partitioning, below threshold $C_{\rm DG}$ decreases like in the measurements, although the decrease is somewhat too fast. Finally, in Figs. 14 and 15 an overview of $C_{\rm GG}$, $C_{\rm GD}$ and $C_{\rm DG}$ versus drain voltage is given for $V_{\rm GS} = 5$ and 9 V, respectively. We observe that $C_{\rm GG}$ and $C_{\rm GD}$ are very well described, whereas $C_{\rm DG}$ is somewhat underestimated.

VI. Conclusion and Discussion

A surface potential-based compact LDMOS transistor model, without internal node, has been presented. The so-called internal drain voltage is explicitly expressed inside the model in terms of the external terminal voltages. By subsequent use of an explicit relation between surface potentials and terminal voltages, an accurate dc-current description has been obtained, valid in all operating regimes ranging from subthreshold to strong inversion, in both the linear and saturation regime. In addition to the dc model, a nodal charge model has been developed. Due to the asymmetry of an LDMOS device, a modification to the Ward–Dutton charge partitioning scheme has been taken. A comparison between capacitances obtained from high-frequency measurements shows a good agreement with those obtained from the nodal charge model. Finally, by having all expressions and their derivatives continuous at all bias conditions, it should be noted that our compact model shows an improved convergence behavior during circuit simulations. Also the use of this compact model in a subcircuit model to describe higher voltage LDMOS devices has been proven to be successful. Finally, we mentioned that the source code and documentation of the model are available in the public domain [22].

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