A Survey of Techniques for Formal Verification of Combinational Circuits

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With the increase in the complexity of present day systems, proving the correctness of a design has become a major concern. Simulation based methodologies are generally inadequate to validate the correctness of a design with a reasonable confidence. More and more designers are moving towards formal methods to guarantee the correctness of their designs. In this paper we survey some state-of-the-art techniques used to perform automatic verification of combinational circuits.

We classify the current approaches for combinational verification into two categories: functional and structural. The functional methods consist of representing a circuit as a canonical decision diagram. Two circuits are equivalent if and only if their decision diagrams are equal. The structural methods consist of identifying related nodes in the circuit and using them to simplify the problem of verification. We briefly describe some of the methods in both the categories and discuss their merits and drawbacks.

1 Introduction

Successful design of a complex digital system requires verifying the correctness of the implementation with respect to its intended functionality. Traditionally, the task of design validation is carried out by means of simulation. In a simulation based approach, the designer needs to create a complete set of test vectors which represents all possible inputs to the system. The outputs for each of these test vectors are analyzed to guarantee the correctness of the design. This process is highly CPU-time intensive; in almost all practical situations it is infeasible to exhaustively simulate a design to guarantee its correctness.

Due to the limitations of a simulation based approach, various formal verification strategies are becoming increasingly popular. By using these techniques, it is possible to guarantee the correctness of a design under all possible input combinations.

The process of designing a complex system usually starts with an abstract model of the system. This model is subjected to extensive simulation after which it becomes the "golden specification" of the design. From this abstract model, a detailed implementation is derived in a hierarchical manner. First the abstract model is translated into a synthesizable behavioral RTL model representing the block structure behavior of the design. This behavioral RTL model is then translated into a structural model which is a logic level description of the system. From the structural RTL model a transistor netlist and subsequently the physical layout of the design is derived.

In a successful design methodology it is essential to catch bugs early in the design cycle. For this, the functionality of the design is verified at every level of hierarchy against the original ("golden") specification. This kind of formal verification in which different implementations of the same design are compared to check their equivalence is known as implementation verification. Implementation verification typically proceeds in two phases. In the first phase, a Boolean network representing the original design is extracted from the RTL description or the transistor level netlist [40, 14, 15, 38, 63]. In the second phase, the correctness of this Boolean network is verified using some formal methods.

In this paper we will focus only on the second phase. We will describe some recent advances made in the area of verifying the equivalence of two Boolean networks. More specifically, we will focus only on the verification of combinational circuits i.e., circuits in which the outputs depend only on the current inputs (as opposed to sequential circuits in which the outputs depend not only on the present inputs but also on the past sequence of inputs). Some sequential verification problems can also be reduced to a combinational verification problem (e.g. when the corresponding latches in the two designs can be identified). Although techniques exist for verifying general sequential circuits, currently it is not practical to verify large industrial designs using them.

The combinational verification problem can be stated as follows: Given two Boolean netlists, check if the corresponding outputs of the two circuits are equal for all possible inputs. This problem is NP-hard and hence a general solution which can handle arbitrary Boolean functions is not likely to exist. However, since the functions that are implemented in practice are not random Boolean functions, various techniques have been developed which can successfully verify large designs.

Research in combinational equivalence checking has seen significant and rapid improvements since introduction of OBDDs [13]. Thus, details of numerous equivalence checking techniques [19, 27, 29, 45, 55, 59, 64, 65, 66, 68], developed before an extensive investigation of OBDDs based procedures began in late 1980s, have not been covered in this survey. The work in equivalence checking, especially as done in the last decade, can be classified into two main categories:

- The first approach consists of transforming the output functions of the two networks into a unique (i.e. canonical) representation. Two circuits are equivalent if and only if the canonical representations of the corresponding outputs are the same. The most popular canonical representations are based on Binary Decision Diagrams (BDDs). We will discuss methods based on BDDs in Section 2. In the worst case these methods can require exponential space (in the number of inputs). We will discuss some techniques for dealing with this "memory explosion" problem in BDD representations.
- The second approach consists of identifying equivalent points and implications between the two circuits. Using this information the process of equivalence checking can be simplified. Since a typical design proceeds by a series of local changes, in most cases there are a large number of implications between the two circuits to be verified. These implication based techniques have been very successful in verifying large circuits and form the basis of most combinational verification systems. We will discuss some of these techniques in section 3.

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2 Methods Based on Decision Diagrams

In this approach, the output functions of the two networks are represented as canonical BDDs. The two circuits are equivalent if and only if the BDDs of their corresponding outputs are equal (i.e. isomorphic).

A BDD over a set of $X_n = \{x_1, \ldots x_n\}$ of Boolean variables is a directed acyclic graph with one source and at most two sinks labeled by 0 and 1. Each non-sink (internal) node is labeled by a variable in X_n and has two outgoing edges - corresponding to where the variable evaluates to a 0 or to a 1. For a given assignment to the variables, the function value is evaluated by tracing a path from the root to the terminal. For a given input $m = (m_1, \ldots, m_n)$, the evaluation starts at the root and at an internal node with label x_i the outgoing edge with label m_i is chosen (see Figure 1).

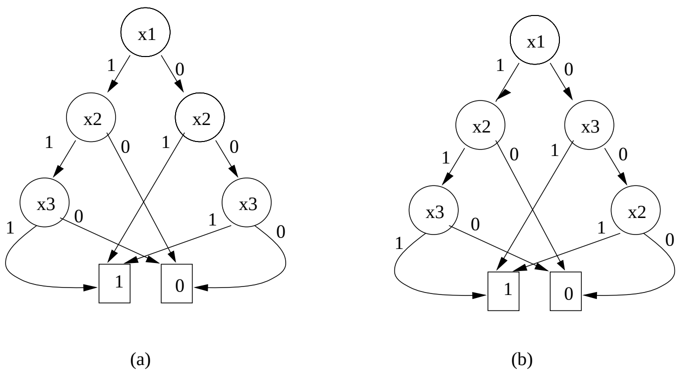

Figure 1: (a) ROBDD and (b) Free BDD

Though BDDs have been researched for about four decades [46, 1], they found widespread use only after Bryant [13] showed that such graphs, under two restrictions, are canonical and can be easily manipulated. The first restriction is that a total ordering of the variables is enforced in the graph. That is, if we consider variables to be ordered as $x_1 < x_2 < \ldots < x_n$, then every path from the root to a sink encounters the variables in that order. The second restriction is that the graph is reduced. A graph can be reduced by the repeated application of the following two rules until they are no longer applicable. These rules are:

- Merging Rule: Two isomorphic subgraphs should be merged.
- Deletion Rule: A vertex whose two branches point to the same vertex should be deleted.

The resulting BDD is called a Reduced Ordered BDD (an ROBDD). The important symbolic manipulation procedures introduced by Bryant were *apply* and *compose*; these techniques operate on two identically ordered ROBDDs. *Apply* allows two ROBDDs to be combined under some Boolean operation, and *compose* allows the substitution of an ROBDD variable with a function.

Since ROBDDs are canonical, they can be used directly for checking the equivalence of two Boolean circuits. Two circuits are equivalent if and only if the ROBDDs representing the corresponding outputs of the two circuits are equal. ROBDDs are typically constructed using some variant of Bryant's *apply* procedure [13]; the ROBDD for a gate g is synthesized by the symbolic manipulation of the ROBDDs of its inputs, based on the functionality of g. The gates of the circuit are processed in a depth-first manner until the ROBDDs of the desired output gate(s) are constructed. For details on ROBDDs, and the implementation of a typical ROBDD package, please refer to [10, 13, 16].

Although ROBDDs are canonical and hence can directly be used for combinational verification, their construction is often a time and memory intensive process. The size of an ROBDD representing a Boolean function can be exponential in the number of primary inputs in the worst case. This problem is commonly referred to as the "memory explosion" problem. In the following sections we will discuss various methods which deal with the memory explosion problem during ROBDD construction.

2.1 Variable Ordering

The size of an ROBDD is strongly dependent on the ordering of its variables. Much of the prior research in ROBDDs has focused on finding good variable orders to reduce the size of an ROBDD representing a Boolean function. Given a combinational netlist, [47, 24] discuss some heuristics for ordering the primary input variables which lead to a compact ROBDD representation of the outputs. These techniques for the first time successfully demonstrated that ROBDDs could be used for verifying large circuits. Another significant advance in variable ordering was made with the introduction of dynamic variable reordering [60]. In this procedure a periodic reordering of variables is attempted to reduce the memory requirement. Given a graph G, a variable v is successively moved to each position in the ordering list and the resulting graph size is examined. The variable is finally assigned the position which results in the smallest graph size. This process is known as *sifting* and is repeated for each variable in the graph. Sifting n variables, in a graph of size G, requires $O(n \cdot |G|)$ effort. A less expensive procedure may also be used where variables are reordered in a window of say, 3 consecutive variables. This window is then moved forward to include the next variable in the graph, and the process is repeated till all n variables have been considered. Improvements to sifting based reordering techniques were suggested by [57] where the number of sift operations were reduced by grouping, and thereby sifting together, the symmetric variable pairs. Further improvements were suggested in [56] where the concept of extended symmetry was introduced to group a larger block of variables.

Though computationally somewhat expensive, dynamic reordering techniques are widely used as they allow the variable ordering to adapt to the changing functions that are being represented. Although good variable ordering methods have considerably increased the class of functions which can be efficiently verified using ROBDDs, there are still many functions for which any ROBDD is exponential in the number of inputs (e.g. integer multiplier). Further, the problem of finding optimum variable orders is an intractable problem and there are many instances where although a good orderings might exist, the heuristics are unable to find them.

2.2 Breadth First Manipulation

In [54, 3], it was shown that by manipulating ROBDDs in a breadth-first fashion much larger ROBDDs can be processed than is possible by the conventional *apply* procedure [13] which operates as a depth first algorithm. This gain in memory is achieved by keeping only a few levels of ROBDDs in the main memory at any given time and storing the rest in the secondary memory which is typically much larger. Breadth first algorithms allow an orderly memory access. This results in fewer page faults and consequently a significant improvement in performance, especially for large circuits. Recently a complete package was implemented [61] using the breadth-first manipulation idea which gives an order of magnitude performance gain over the conventional ROBDD packages.

The main drawback of this approach is that as only a few levels are kept in the main memory at a time, it is difficult to dynamically reorder the ROBDD during an operation.

2.3 Node Decompositions

ROBDDs employ a decomposition known as the "Shannon Decomposition" in which a function f is decomposed in terms of a variable x as follows:

$$f = \overline{x} f_{\overline{x}} + x f_x \qquad (1)$$

Here f_x represents the positive cofactor of f with respect to x and is obtaining by replacing variable x by the value 1. Similarly, $f_{\overline{x}}$ represents the negative cofactor with respect to x and is obtained by replacing x by 0.

Canonical but fundamentally different data structures such as ordered Functional Decision Diagrams (OFDDs) [39] and Ordered Kronecker Functional Decisions Diagrams (OKFDDs) [22] have also been proposed to extend the set of functions that can be efficiently symbolically manipulated. In OFDDs the function is decomposed using the "Reed-Muller" ("Davio") expansion. In this decomposition, the function f is represented as either:

$$f = f_{\overline{x}} \oplus (x(f_x \oplus f_{\overline{x}}));\ \ or\ \ f = f_x \oplus (\overline{x}(f_x \oplus f_{\overline{x}})) \qquad (2)$$

OFDDs are canonical like ROBDDs and hence can be used in verification. There are some functions for which ROBDDs are exponential but OFDDs are polynomial. Thus OFDDs extend the class of functions which can be verified in polynomial memory resources, but conversely there are functions for which OFDDs are exponentially larger than ROBDDs. OKFDDs try to benefit from both decompositions; each variable has an associated decomposition which can be either Reed-Muller or Shannon. Variables are ordered and every occurrence of a given variable must use the same decomposition. Although in theory OKFDDs can be exponentially more compact than both OFDDs and ROBDDs, in practice they seem to have provided only a modest improvement over ROBDDs (approx. 35%).

2.4 Non-Canonical BDDs

Non-canonical BDD representations such as XBDDs [37], gBDDs [4], IBDDs [32] have been explored to obviate OBDD memory explosion, often leading to more efficient verification. For example, in IBDDs any variable can appear multiple times on any path from the root to the terminal; an order is imposed on the multiplicity of the occurrence. In other words, an IBDD can be considered as "layered" BDD such that within each layer the appearances of variables obey a linear order as in ROBDDs. It was shown in [32] that some functions intractable for ROBDDs such as *hidden-weighted-bit* function, Booth-encoded as well as integer multiplier, etc. can be verified in polynomial time using IBDDs. However, due to lack of detailed experimental results and/or publicly available function manipulation packages, we feel that further research is warranted to gauge the true potential of these novel non-canonical data structures.

Another strategy to reduce the BDD sizes in function representation is to relax the total ordering requirement of ROBDDs. One such relaxation is to allow variables to occur in any order but at most once along any path from the root to the terminal. Such BDDs are called Free BDDs (Figure 1(b)). In general free BDDs are not canonical and their manipulation is an intractable problem [23]. However, in [26] it was shown that restricted forms of free BDDs known as typed-Free BDDs are canonical and can be easily manipulated. In typed-Free BDDs, for any given variable assignment, the resulting paths in all graphs contain variables in the same order. The variable ordering for different assignments might be different. Unfortunately, the practical problems in choosing a good *type* can greatly reduce the flexibility gained from relaxing the variable ordering constraints. Some heuristics for generating typed Free BDDs were presented in [8, 7]. Typed-free BDDs extend the class of functions which can be represented in polynomial space but there are still some practical functions for which Free BDDs are exponential (e.g. integer multiplier).

2.5 Partitioned ROBDDs

All the BDD methods discussed so far represent a function over the entire Boolean space as a single graph (rooted at a unique source). It was shown in [33, 31, 53] that exponentially more compact representations can be obtained by partitioning the Boolean space and representing the functionality over each partition as a separate graph. This compactness in representation is achieved without sacrificing the desirable properties of the underlying graph which is used to represent each partition. In [33, 31] this notion of partitioning was used to discuss a function representation scheme called partitioned-ROBDD, which was then extensively developed, theoretically as well as experimentally, in [53]. In partitioned-ROBDD every partition of the Boolean space is represented as an ROBDD. Different partitions can have different ordering. It was shown that partitioned-ROBDDs provide a compact, canonical and efficiently manipulable representation for Boolean functions. The notion of partitioning is general and can be applied to any BDD representation.

It was shown in [33, 31, 53] that the class of functions representable in polynomial space by monolithic ROBDDs is strictly contained in the class of functions that have a polynomially sized partitioned-ROBDD representation. Similarly, it was shown in [53] that the class of functions with polynomially sized Free BDDs is strictly contained in the class of functions with polynomially sized partitioned-Free BDDs. Note, partitioned-ROBDDs can be exponentially smaller than even free BDDs. Further, for combinational verification only one partition needs to be present in the memory at a given time. This further reduces the total memory requirement of verification. Using this representation, some industrial circuits could be verified for the first time [53]. One can try to construct only a limited number of partitions and abort the computation after some preset time limit. Thus, even though only part of the Boolean space could be analyzed, at least some partial information about the function can be obtained. Also, when a design is erroneous, there is a high likelihood that the erroneous minterms are distributed in more than one partition and can be detected by processing only a few partitions. Experience with erroneous circuits suggests that in almost all cases the errors can be detected by constructing only one or two partitions [33].

Partitioned-ROBDDs allow a control on the space/time resources and functional-coverage as well as on the success of verification experiments. Using such data structures the success of a verification experiment may possibly be ensured by changing the parameters of decomposition and the number of partitions that need to be created. Since this data structure is still a subject of intensive research, its full impact can be judged only with time.

2.6 Com bining Bottom-up and T op-down approaches of ROBDD construction

In this section we discuss a mixed bottom-up/top-down approach for ROBDD construction which attempts to minimize the intermediate peak memory requirement during ROBDD construction - a critical issue in practical use of OBDDs. Though the following discussion is with respect to ROBDDs, it should be equally applicable to other BDD methods as well.

Traditionally, ROBDDs for a given netlist are built in a bottom-up manner. To construct the ROBDD for a given node, ROBDDs of all the nodes that are present in the transitive fan-in of that node are constructed in terms of the primary inputs before the ROBDD of the target node is constructed. In this method, the peak intermediate memory requirement can often far exceed the final (canonical) representation size of the given function. This places a limit on the complexity of circuits that can be verified using ROBDDs, and also usually dictates the time required for ROBDD construction. In [52, 36], techniques to reduce the intermediate peak memory requirement by a suitable combination of bottom-up and top-down approaches were presented. Using these techniques, ROBDDs for many circuit outputs can be constructed for which the conventional method fails. The reduction in peak memory is often accompanied by a significant speed up in the ROBDD construction process as well.

Let us look at an example where the memory requirement for a bottom-up scheme is exponential while the decomposition/composition approach requires only polynomial resources. Consider the function shown in Figure 2. Here f and g are two internal nodes. Assume that the ROBDD of g is exponential in terms of the primary inputs (PIs) for any variable ordering. Further assume that all the other internal nodes of the function require only polynomial memory resources. If we try to build the ROBDD of the primary output y in a bottom-up fashion, we will need to build the ROBDD of g in terms of the PIs. But since the ROBDD of g is exponential for any given variable ordering, the peak memory required in the bottom up scheme will be exponential. The functionality of y can be expressed in terms of f and g by the equation $y = f \vee (f \wedge g)$. This simplifies to $y = f$. Therefore, to construct the ROBDD of y we do not need to construct the ROBDD of g. We can introduce a new variable representing g and build the ROBDD of y in terms of this variable. Since g is eventually not present in y, we need not ever construct the ROBDD of g. This can let us get an exponential reduction in the peak memory requirement and extend the class of circuits that can be efficiently processed using ROBDDs.

The previous example shows that in a typical ROBDD construction procedure there is frequent functional simplification due to Boolean Absorption: $x \vee (x \wedge y) = x$ and Boolean Cancelation: $x \wedge \overline{x} \wedge y = 0$. This means that the final output function can often be simpler (i.e. has a smaller ROBDD) than the intermediate functions that are used to implement it. The bottom-up methods may fail when any node in the transitive fan-in of the target node requires an exponentially large graph.

The procedures of [36] and [52] try to avoid building ROBDDs of the intermediate functions having a large ROBDD representation by introducing suitable decomposition points. The ROBDD of the output is then built in terms of these decomposition points and PIs. The functionality of the decomposition points is expressed as ROBDDs in terms of previously introduced decomposition points and PIs. Finally, the decomposition points are composed back to obtain a canonical ROBDD of the output function.

Two issues need to be addressed here:

- Finding a good decomposition set
- Determining a good order of composition of the decomposition variables to get the monolithic representation so that the intermediate memory explosion during the composition phase is low.

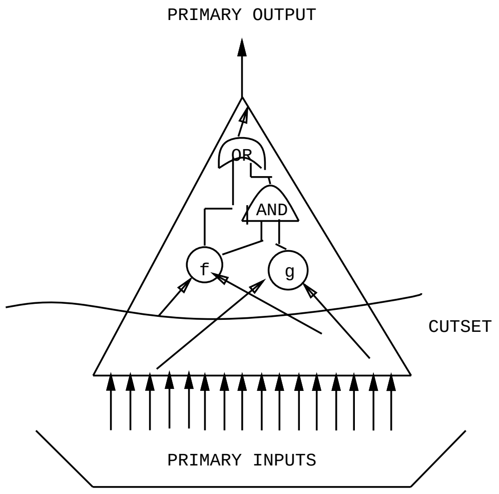

Figure 2: *Example where decomposition can avoid exponential blowup*

Heuristics for introducing good structural and functional decomposition points were described in [36] and for finding good order of composition were discussed in [52]. A reduction in memory is achieved since the intermediate points of large ROBDD sizes are avoided and also because dynamic variable reordering has to focus only on the target function and hence is more effective. Such an approach is fully compatible with other approaches of reducing memory (like variable ordering) and can be seamlessly integrated within any ROBDD package. Therefore, there seems to be no apparent trade-off in using it.

2.7 Probabilistic Verification

Another important way of verifying two circuits is to probabilistically check their equivalence [9, 34]. In probabilistic verification, every minterm of a function f is converted into an integer value under some random integer assignment ρ to the input variables. All the integer values are then arithmetically added to get the hash code $H_\rho(f)$ for f. One can assert, with a low probability of error, that $f \equiv g$ *iff* $H_\rho(f) = H_\rho(g)$. The arithmetic evaluations are carried in an integer field, that is, all arithmetic operations are done modulo some prime p. If f, g are functions of n-variables, and ϵ denotes the upper bound on the error probability, then if $p \gg n$, a reasonable assumption, $\epsilon \approx n/p$. Otherwise $\epsilon \approx 1 - e^{-n/p}$. The probability of erroneously deciding that functions are equivalent decreases *exponentially* with the number of runs: after k runs, the error probability is ϵ^k.

[9] suggested probabilistic verification of Boolean functions through hashing their free BDD representation to an integer value under some random integer assignment ρ to the input variables. Alternately, it was shown in [34] that we can also transform arbitrary representation of Boolean functions by first interpreting the given function as an integer-valued arithmetic expression. This arithmetic expression can then be evaluated on integer assignments to its input variables. By using the properties of such integer-valued arithmetic transformations, many analysis techniques were developed to probabilistically verify Boolean as well as other discrete functions with a negligible probability of error. For example, by decomposing a circuit into regions which have mutually disjoint

variable support set, and using such arithmetic transforms it was shown that an n-bit ALU requiring $\Theta(n^2)$ time using ROBDDs requires only linear resources with the probabilistic method [34].

In [34] some other methods for exploiting Boolean function properties for efficient hashing were also discussed. For example, it was shown that if the space of each function is partitioned into mutually disjoint subspaces then the hash code of the function corresponding to each partition can be calculated independently; the hash code of the function is the sum of the hash codes of individual partitions. This implies that to check if $H_\rho(f) = H_\rho(g)$, we can partition and hash both f and g independently. We do not need to keep the partitions of both f, and g, in the memory at the same time. Further, it is not necessary that both f and g have been partitioned identically. The effectiveness of this technique was shown on special classes of functions like Hidden-Weighted-Bit (HWB) function in [34]. The techniques presented in [53] are directly applicable to probabilistic verification as well and provide automatic ways to generate such partitions.

Another technique called *collapse-with-compose* [34] allows efficient hashing of functions when orthogonal partitions cannot be easily found. This algorithm generates the hash code of the function directly from a decomposed representation without having to build the monolithic ROBDD of the output. For many difficult circuits in ISCAS-85 benchmark circuits, it was shown in [34] that this method can significantly outperform the monolithic ROBDD methods.

Since one is deriving the integer representation of a function rather than its Boolean representation, one can often obtain the hash code by exploiting the algebraic properties of a higher level representation, circumventing its conversion to a Boolean representation. This was illustrated in [34] where hash code for an n-input HWB function was computed from its abstract specification in $\Theta(n^3)$ time using only $\Theta(n)$ space. Similarly, the hash code for integer multiplier could be obtained 5 times more efficiently from the arithmetic specification of the multiplication function than from its circuit description using only a minimal of space.

2.8 Verification of Arithmetic Circuits

So far we have discussed methods to compare two logic circuits at the bit-level. For many arithmetic circuits this may not be a desirable thing. First, the BDD data structure that is used for bit level verification may grow exponentially with the size of the circuit (for example, integer multiplication). Secondly, even if we can guarantee that the two netlists are equivalent that doesn't necessarily imply that the circuit is implementing the correct specification. To overcome these limitations of bit-level verification, a different approach for verifying arithmetic circuits was proposed in [44, 17]. Here a logic circuit represented as a vector of Boolean functions $\vec{f}$ is compared against the specification which is represented as a word level function F. The basic idea of this methodology is illustrated in Figure 3 [17]. Here the primary inputs are grouped into two sets, $\vec{x^1}$ and $\vec{x^2}$. For each set $\vec{x^i}$, we are given an encoding function ENC_i describing a word-level interpretation of the signals, e.g., unsigned binary, two's complement, BCD etc. The logic network is described as a set of Boolean functions given by $\vec{f}\,(\vec{x^1}, \vec{x^2})$ and an encoding, ENC_o for the outputs. The specification is given as a word-level function $F(X_1, X_2)$. The problem consists of verifying the following equation:

$$ENC_o(\vec{f}\,(\vec{x^1}, \vec{x^2})) = F(ENC_1(\vec{x^1}), ENC_2(\vec{x^2})) \quad (3)$$

For the word-level verification problem we need a data structure which can efficiently represent both bit-level and word-level

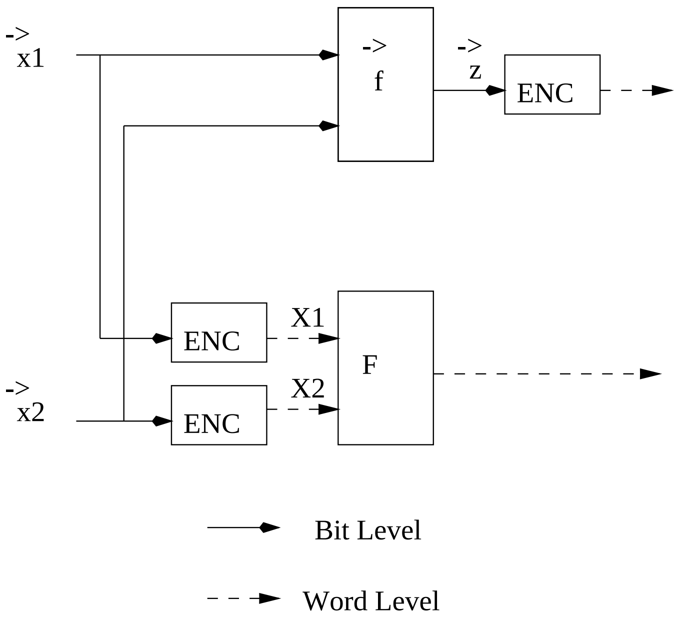

Figure 3: Word-Level Verification

functions. Many data structures have been proposed for this purpose, e.g., MTBDDs [21], ADDs [5], EVBDD [44], *BMD [17], Hybrid Decision Diagrams (HDDs) [20]. Out of these, the *BMD and the HDD data structures are of particular interest as they can represent integer multiplication efficiently. However, the verification strategy presented in [17] can not take advantage of this fact. This is because in the verification methodology, a bit level representation of the multiplier has to be created first which is then translated into the word-level representation. To circumvent this problem, [17] proposes a hierarchical verification strategy. This strategy requires a well-defined structure for the multiplier which has to be known *a priory*. This manual intervention somewhat reduces the appeal of both *BMDs and HDDs. In [28] a heuristic to efficiently construct *BMDs is presented which works well for integer multipliers but unfortunately not for other circuits like dividers and exponentiation.

[25] proposes a verification method which uses the recurrence equations of various arithmetic circuits such as multipliers, square functions, cube functions etc. to verify them. For example, a multiplier satisfies the recurrence equation, $f(x+1, y) = f(x, y)+y$ where $f(x, y) = xy$. Thus, to prove $f(x, y)$ represents a multiplier, we need to prove $f(x + 1, y) = f(x, y) + y$, where x, y are input vectors for given circuit. Each side of the equation is represented as a separate circuit, and both circuits are efficiently compared by techniques such as such as [48, 35] which exploit the fact that the given circuits have very similar internal structures. As only a multiplier obeys the above recurrence relation, we can verify that the given circuit is indeed a multiplier without needing to represent the specification.

2.9 Boolean Expression Diagrams

Boolean expression diagrams [2] are a generalization of BDDs, and can be thought of as BDDs extended with Boolean *operator* vertices. The variable vertices are defined in BEDs identically to how they are defined for BDDs, and the Boolean operator vertices have the standard definition. Due to the use of the Boolean operator vertices, there is straightforward linear size transformation from a combinational circuit, with a 2-input *and-or-not* decomposition, to its corresponding BED. To manipulate such diagrams they use observations similar to ones used in the MORE [30] approach. MORE is based on the observation that the BDD for $f \vee g$ can be constructed by introducing a new variable x, and creating a function $(x \wedge f) \vee (\overline{x} \vee g)$ where x is then implicitly existentially quantified out. To quantify out x we move towards the terminal vertices using the sifting procedures similar to ones used in [60]. BEDs can be seen as extending this idea to allow arbitrary operators and allowing these operators to remain in the graph. Equivalence of f, g can be checked by sifting variables/operators through a graph of $f \oplus g$ till it can be determined to reduce to 0. Such techniques can be efficient if a good order in which variables should be sifted can be easily determined. However given the fact BEDs are quite sensitive to the order in which the variables/operators should be sifted, more research needs to be done to determine an appropriate sifting order.

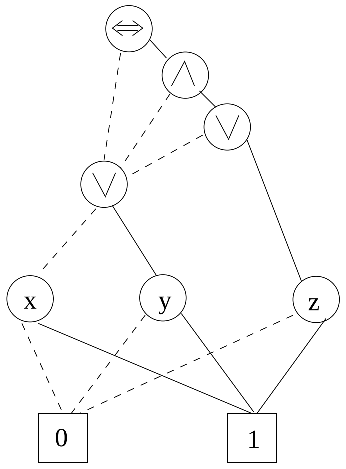

Figure 4: A BED for $(x \vee y \vee z) \wedge (x \vee y) \iff (x \vee y)$

3 Combinational Verification Using Internal Correspondences

Typically during synthesis at the gate level, the designer makes local modifications to the logic network for adjusting timing, area, delay and other characteristics. Since the changes that are made to the networks are localized in nature, most of the original network remains structurally unchanged. Various techniques have been developed which exploit the internal correspondences in the two circuits to speed up the process of verification. We will first explain the terminology used in the rest of this section and then describe some of the methods that make use of the internal correspondences in combinational verification.

3.1 Terminology

We assume that the reader is familiar with the basic definitions of Boolean networks, fanins, fanouts, transitive fanins (TFIs) and transitive fanouts (TFOs) [12].

Definition 1 *Given a Boolean network $\eta = (V, E)$, a* **cutset** *in the TFI of a node $v \in V$ is defined as a set $S = \{v_1, v_2, \ldots, v_k\}$ of nodes in the TFI of v such that any path from the primary inputs to v must pass through a node $v_i \in S$. The size of the cutset is k. (Where unambiguous, we will use the terms nodes and gates interchangeably.)*

Definition 2 *A gate G is said to be* **unjustified** *under the present set of value assignments (preassigned values) to some of its fanin and fanout signals (preassigned signals) if among the assignments possible on the remaining signals there are (a) multiple assignments which are consistent with the preassigned signals, and (b) at least one assignment which can produce value at some signal that is inconsistent with its preassigned values.*

Examples of unjustified gates are shown in Figure 5. For instance, in the AND gate, suppose the output has already been assigned a Boolean value of 0. Now, if an assignment $\{a = 1, b = 1, c = 1\}$ is made, there is a conflict at this gate. Similarly, there exist multiple assignments that can be made at its inputs such as $\{a = 0, b = X, c = X\}$ for which the output value 0 can be produced. Thus, this is an example of an unjustified gate. Similarly, the reader can observe that for the output $c = 0$, the XOR gate in Figure 5 represents an unjustified gate.

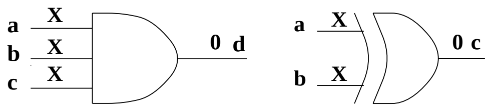

Figure 5: *Example of Unjustified Gates*

Definition 3 *Given an initial assignment of Boolean values to a subset of nodes in a Boolean network η, the process of determining the Boolean values at other nodes in η using the connectivity information of the nodes and the truth tables of the Boolean functions at the nodes is called* **direct implication***. Boolean values at nodes that cannot be derived by direct implication but can be derived using the law of contrapositum [67] involve* **indirect implication***. The process of deriving indirect implications is called* **learning***.*

Figure 6 shows examples of a direct implication and an indirect implication. In the circuit on the left, if we set signal $a = 1$ then by a simple simulation (looking only at circuit connections, and the functionality of each circuit node) we can conclude that the signal f is forced to be a 0. Hence, $a = 1 \rightarrow f = 0$ is called a *direct* implication. Similarly for the circuit on the right, by law of contrapositum we can deduce that $f = 1 \rightarrow a = 0$. However, the reader can check that such a deduction could not have been arrived at by a naive simulation process such as the one used to derive the direct implication; thus, $f = 1 \rightarrow a = 0$ is an *indirect* implication.

3.2 Learning Techniques: Techniques for Detecting Indirect Implications

There are several verification methods that extract and use internal correspondences between two given networks using learning based methods. Learning involves the extraction of indirect implications between nodes in a circuit. Recursive Learning (RL) [43], and Functional Learning (FL) [50, 35] are two of the more popular learning techniques. The concepts of FL and RL are illustrated below by means of an example.

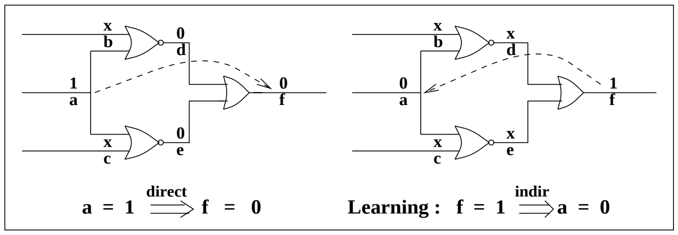

Figure 6: *Indirect Implication*

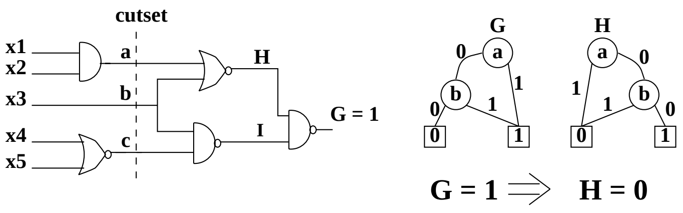

Figure 7: *Example of Functional Learning*

Consider the circuit shown in Figure 7. Suppose that a Boolean 1 is injected at gate G. We wish to learn what $G = 1$ implies at gate H. Let us choose a cutset $\lambda = \{a, b, c\}$ of internal gates in the circuit. In FL, we build the ROBDDs for gates G and H based on λ. The ROBDDs for G and H are shown in the Figure 7. From these two BDDs we can infer that $G = 1 \Rightarrow H = 0$. Also, note that this relation between G and H cannot be derived by using direct implication. This is because after a Boolean 1 is injected at G, it becomes *unjustified*. Therefore, direct implication based simulation due to $G = 1$ cannot result in Boolean values being implied at any other gate in the circuit. However, $G = 1 \Rightarrow \underline{H} = 0$ can be derived by carrying out the Boolean operation: $G \wedge \overline{H}$ and examining the resulting ROBDD for equivalence with G. The time complexity of functional learning is controlled by the size of BDDs and is impractical when the BDDs grow quite large.

In RL we note that $G\!=\!1$ can be satisfied by either $H\!=\!0$, $I\!=\!X$ or $H = X$, $I\!=\!0$. However, $I\!=\!0$ implies that $b\!=\!1$ which in turn implies that $H\!=\!0$. Therefore, $G = 1$ implies $H = 0$. Here, given a value assignment in the circuit, the deduction process recursively analyzes the effect of each justification vector, and intersects the common "effect" of every justification vector that can satisfy the given circuit condition. The result of this intersection process is the implication of the original value assignment in the circuit. The time complexity of recursive learning is exponential in the number of recursion levels, and in practice is limited to two or three levels of recursions. Both recursive learning as well as functional learning are called a *complete* method for learning in digital circuits, i.e. given sufficient time, they can determine all *constant-value relationships* in the circuit, i.e., all cases where a constant Boolean value $v \in \{0, 1\}$ at a given gate implies another constant Boolean value at another gate. However, since FL is based upon BDD based manipulations, it can, relatively more conveniently, detect more complex relationships between a set of functions with another set of functions: for example, a gate $f = 0$ may simply imply that disjunction of a set of functions must be 1. Or, under $f = 0$, some gates must assume identical value.

3.3 Techniques for Exploiting Internal Equivalences

There are several verification methods that exploit internal correspondences between two given networks. Berman *et al.* [6] proposed a technique to use internal equivalences in order to establish the functional equivalence of two networks. A min-cut based algorithm for decomposing networks was proposed to break down the entire verification problem into smaller sub-problems. A set of potentially equivalent gate pairs are identified in the two networks; later the equivalence of the paired gates is decided using exhaustive simulation. Now, using a cut of equivalent gates, it is attempted to verify if the given circuits are also equivalent. However, this method was plagued with the problem of *false-negatives*. A false negative refers to a situation where although the two functions which are being compared are equivalent, the verification algorithm incorrectly classifies them as different. Figure 8 shows an example of false-negative. F and G are equivalent outputs (both being equal to b) and node $d1$ is functionally equivalent to node $d2$. However, if a verification of F and G is attempted in terms of the cutsets shown by dotted lines in Figure 8, F will turn out to be inequivalent to G. Although they note that the false negatives can be resolved if the given cut can be composed in terms of primary input variables using OBDDs, they do not give relevant details of corresponding procedures, or any empirical results outlining the efficiency of such a technique.

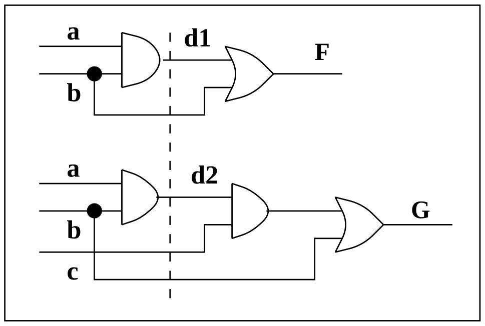

Figure 8: *False Negative*

Cerny and Mauras [18] introduced the notion of *cross-controllability* and *cross-observability* among the internal nodes on the appropriate cutsets in the two given networks to check for equivalence. By *cross-controllability* at a cutset λ they refer to the combination of Boolean values that can be produced at λ; by *cross-observability* at λ they refer to the combination of Boolean values which if produced at λ will imply that given primary output pairs will assume identical Boolean values. The circuits are now equivalent if it can be proved that *cross-controllability* $\subseteq$ *cross-observability* for any cutset λ. However, no systematic algorithm for choosing an "appropriate" cutset was presented and we do not know of any wide scale utilization of this technique.

Brand [11] proposed an ATPG based technique to determine equivalences between the internal nodes in two given circuits. This method can find nodes which are equivalent under the observability don't care (ODC) set. Given two circuits C_1 and C_2, and two potentially equivalent nodes $n_1 \in C_1$ and $n_2 \in C_2$, a new XOR gate Y, is introduced in C_1 such that n_1 and n_2 are the two fanins of Y.[1] Fig. 9 shows an example of such a *miter* circuit. The dotted lines show the original circuit connections. A new XOR gate is

[1]In verification algorithms, potential equivalent nodes between

introduced and the outputs of the XOR gate feeds the nodes that were originally fed by node n_1. Next, an ATPG tool is used to test the fault s-a-0 at Y as shown in the figure. If the fault is proved to be redundant then n_2 can replace n_1 in circuit C_1. However, this method of finding equivalent nodes can become inefficient if the faults that are tested to determine internal equivalences are intractable or if not too many internal equivalences exist in the two designs.

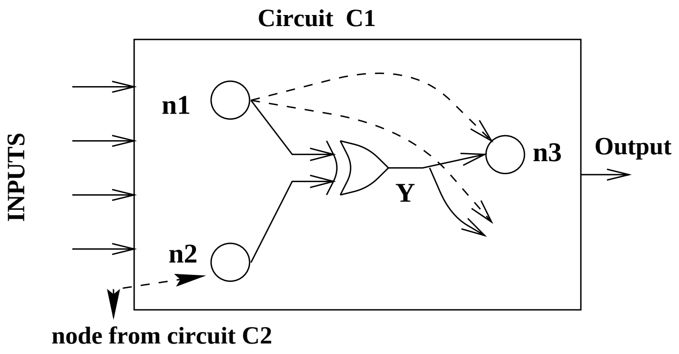

Figure 9: *Testing node equivalences by creating a miter*

3.4 Learning Based Verification Techniques

Recently, several learning based techniques for combinational verification have been proposed. In [42], a combinational verification tool, HANNIBAL, based on recursive learning was presented. HANNIBAL operates in two distinct phases. In the first phase, learning is carried out at all the nodes in the two networks for a user specified number of learning levels; often, this phase itself can verify several primary outputs of the two networks. In the second phase, using the learning information derived in the first phase, an ATPG tool is invoked for verifying the remaining primary outputs. In [49] another verification tool, VERIFUL, was presented which is based on functional learning. This tool also has two phases like HANNIBAL. Here learning is carried out at each gate g using ROBDDs. These ROBDDs are built using a cutset that is at a structural distance[2] d away from g. Here d can vary from 1 to a predetermined maximum distance d_{max}. The amount of learning obtained in a network can be increased by increasing d_{max}. However, the sizes of the ROBDDs that are built usually increase with the increase in d. This results in an increase in the time and space resources required. Two other learning based verification algorithms were presented in [35, 58]. Both of these methods consist of an initial learning phase followed by an ROBDD based equivalence-checking phase. Methods to reduce the ROBDD sizes using the learning information were presented. In [58] the ROBDDs were pruned with an ATPG tool that uses the learning information derived in the first phase. In [35] *invariants*[3] based on learnings are used to simplify the ROBDDs. This technique also successively composes BDDs in terms of cutsets of internal equivalent gates till the functional equivalence is resolved.

two circuits are typically decided by simulating the given circuits on some k simulation vectors. Two nodes are now called potentially equivalent if they have an equivalent output on each of the k vectors. The value of k can be decided dynamically or a priori.

[2]The structural level in functional learning of [49] is a close analogue of the level of learning in recursive learning.

[3]If $a \Rightarrow b$, where a and b are two nodes, then $\overline{a}+b$ is an invariant.

The learning based techniques have several limitations. First, they are unable to derive *all* internal equivalences in limited computational resources. All the known learning techniques discover equivalences between internal gates in circuits using two indirect implications: to find if $f \equiv g$ they individually determine if $f \Rightarrow g$, and then if $g \Rightarrow f$. However, finding indirect implications, whether through ROBDD operations [49] or techniques such as recursive learning [43], can be relatively expensive. Another problem is that there is no simple method to determine, a priori, the number of levels of learning that will be required on a given pair of circuits. Hence, a complete automation of learning based verification tools may be difficult.

Recently another efficient technique that analyzes internal similarities between circuits using ROBDDs was proposed in [48]. Beginning from gates closest to primary inputs, function $(g \oplus h)$ is calculated for all potentially equivalent gate pairs (g, h) using ROBDDs. The equivalent gates between two circuits are merged as shown in Figure 9. The ROBDDs are built using internal variables which are usually introduced at gates that have already been shown to be equivalent. The set of internal variables (gates) is chosen such that we minimize gates that have a path to another gate in the same set. This technique gives up to an order of magnitude speed-up over [58] on many benchmark circuits.

3.5 BDD Hash Based Techniques

Using such techniques many internal equivalent gates can be identified rather easily without always explicitly carrying out an XOR between pair of potentially equivalent candidates [41, 51]. While constructing OBDDs for a given circuit, the OBDD construction is suspended at some well defined intervals, and the OBDDs of the set of the gates already processed is examined; if any two gates possess an identical OBDD then a common variable is introduced at both the gates. The equivalent gates can be merged to produce a simpler network. After examining all gates whose OBDD was already processed, the OBDD construction for the rest of the circuit is again resumed. To identify such equivalent gates, the primary inputs of given circuits form the first cutset for building BDDs for the gates in the network and the gates are processed in a breadth first order. The gates are hashed into a hash table, **BDD-hash**, using the pointer to their BDDs as the keys. The hashing mechanism is shown in Figure 10. The dotted lines show *cutset*1 and *cutset*2 respectively. The *cutset*1 consists of the primary inputs to the network. BDDs for the gates $n3$, $n4$ and $n5$ are built in terms of *cutset*1. The gates $n4$ and $n5$ hash to the same collision chain in **BDD-hash** because they have identical BDDs in terms of *cutset*1. Heuristics based on the size of the shared BDD data structure and the number of structural levels of circuitry for which BDDs are built using any cutset are used to limit the size of BDDs at any time. They are also used to introduce new cutsets based on already discovered equivalent gates. If false negative is required to be resolved between any two potentially equivalent candidate gates g, h, then we can compose the $g \oplus h$ OBDD in terms of the cutset of gates where for each member on this cutset we have already found a functionally equivalent gate.

4 Conclusion

Due to the memory explosion problem, BDDs alone appear unsuitable for verifying large designs. However, they form a crucial representation vehicle for the internal correspondence based verification techniques. A practical combinational verification tool must consolidate diverse techniques for extracting internal correspondences. Such a technique must use the state of the art BDDs, ATPG, as well as implication based techniques. For example, it has been observed that a verification technique based on exploiting

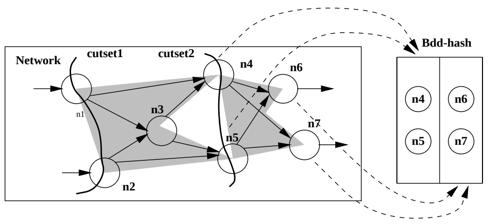

Figure 10: *Hashing of gates with equivalent internal BDDs*

internal equivalences can fail on circuits that have relatively few equivalent nodes. Therefore, such a technique needs to be combined with a learning algorithm to make use of the indirect implication relations that exist between the nodes of the two circuits. To verify inequivalent circuits or internal nodes, use of ATPG techniques appears essential. Finally, in cases where both internal equivalence and learning techniques prove inadequate, verification techniques should be augmented by functional partitioning, possibly using representations such as partitioned-ROBDDs.

5 Ac knowledgemen t

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