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Review

A Survey on Capacitor Voltage Control in Neutral-Point-Clamped Multilevel Converters

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Abstract: Neutral-point-clamped multilevel converters are currently a suitable solution for a wide range of applications. It is well known that the capacitor voltage balance is a major issue for this topology. In this paper, a brief summary of the basic topologies, modulations, and features of neutral-point-clamped multilevel converters is presented, prior to a detailed description and analysis of the capacitor voltage balance behavior. Then, the most relevant methods to manage the capacitor voltage balance are presented and discussed, including operation in the overmodulation region, at low frequency-modulation indexes, with different numbers of AC phases, and with different numbers of levels. Both open- and closed-loop methods are discussed. Some methods based on adding external circuitry are also presented and analyzed. Although the focus of the paper is mainly DC–AC conversion, the techniques for capacitor voltage balance in DC–DC conversion are discussed as well. Finally, the paper concludes with some application examples benefiting from the presented techniques.

Keywords: multilevel converter; neutral-point-clamped multilevel converter; capacitor voltage balancing

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1. Introduction

The neutral-point-clamped (NPC) multilevel converter [1–6] is nowadays a mature technology that has become established as a standard topology for a number of applications, at a wide voltage and power range [7–10], in recent decades.

The advantages and drawbacks of voltage-source multilevel converters in comparison with conventional two-level converters have been extensively detailed in the literature [8,10–15]. The main advantages are: lower device voltage rating, reduced harmonic distortion, reduced common mode voltage, enhanced power losses distribution in the converter, and higher efficiency. These advantages are obtained at the cost of increasing the number of semiconductors and passive components, and also requiring higher modulation and control complexity.

There are three basic multilevel topologies [9,12–14,16–18]: NPC, flying capacitor, and cascaded H-bridge. Starting from the original version of these basic topologies, a number of different multilevel topologies have been developed, such as the modular multilevel converter [19], the stacked multicell converter [20], the multilevel active-clamped converter [21], and reduced switch count converters [22].

In comparison to other multilevel topologies, the NPC family needs only one common DC voltage source for all converter legs and presents the advantage of being implemented

with a full semiconductor layout, as the required capacitors are placed outside the converter legs; that is, no passive components, usually bulky in comparison with the semiconductors, are inside the converter legs. This feature enables the possibility of compacting the converter implementation, reducing volume, and increasing the power density. However, the main drawback of the NPC topology [3] is the requirement to keep the capacitor voltages balanced [4,16]. This survey provides a review of the solutions proposed in the literature to overcome this specific drawback.

The area of application of multilevel converters and, among them, the NPC converters, has expanded over the years. In earlier years, around the 1990s, multilevel converters were intended for high-voltage and high-power applications [13,23], with power semiconductor technology available at that time. Since then, technical evolution has provided enhanced power semiconductor technologies, faster digital processors to implement modulation and control, and thousands of technical papers providing a deeper knowledge about the multilevel converter operation. This development has made multilevel converters suitable not only for high voltage and high power but also for low–medium voltage and power applications [24–29]. For high-voltage and high-power applications, the lower device voltage rating is the most valuable feature of multilevel converters. Instead, in low–medium voltage and power applications, the focus is put on taking advantage of its inherent enhanced voltage and current quality, higher efficiency and better power loss distribution.

Therefore, as a result of the current state of the technology, the NPC is at present one of the most implemented multilevel topologies, mainly in DC–AC converters. The conventional operation of a NPC converter requires that the DC capacitor voltages be equal (balanced) to $V_{Dc}/(n-1)$ at any time and in any operation conditions [3,4,30], where V_{DC} is the total DC-link voltage and n is the number of levels. If this requirement is not verified, on one hand, some power semiconductor devices withstand a higher off-state voltage that could lead to overvoltage failure, and on the other hand, unbalanced voltages could also generate output voltage distortion. In the most typical case, the operation of the NPC converter is not allowed if the DC capacitor voltages are unbalanced. Therefore, some actions should be included in the switching strategy and/or control of the NPC converter to achieve the required DC capacitor voltage balance.

The NPC converter capacitor voltage balance depends on several factors [30,31], such as the amplitude modulation index, the frequency modulation index and the load power factor. Moreover, a higher number of levels, which can enhance the converter voltage and current quality, will increase the difficulty to balance the capacitor voltages. Even more, some applications can benefit from operating with a capacitor voltage imbalance that must be controlled [32,33]. That is, the capacitor voltage balance issue is complex and not straightforward.

As most of the applications of the NPC multilevel converters are for DC–AC conversion, the present survey is focused mainly on this type of power conversion. However, as NPC multilevel converters are also suitable for DC–DC conversion, the capacitor voltage balance for DC–DC conversion is also addressed in a specific section.

This survey reviews and summarizes the modulations, control strategies, and circuits proposed by many researchers to deal with the NPC multilevel converter capacitor voltage balance, which seems not to be covered previously in the literature. The paper is organized as follows. In Section 2, the fundamentals of NPC multilevel converters are described. The NPC capacitor voltage balance is analyzed in Section 3. Open- and closed-loop balancing methods are reported in Sections 4 and 5, respectively. Section 6 shows some hardware-based balancing methods. Balancing techniques for the NPC DC–DC conversion case are described in Section 7. Section 8 presents some cases where the NPC converter operates under a controlled unbalanced condition, which some applications can take advantage of. Finally, conclusions are provided in Section 9.

2. Fundamentals of NPC Multilevel Converters

The fundamentals of NPC multilevel converters are briefly described in this section, including the functional diagram and operating principles, the main topologies, a basic summary of the modulations, and other basic control methods without a modulator.

2.1. Functional Diagram and Operating Principle

The operation of the NPC multilevel converter is extensively reported in the literature [2,4,12–14,16]. Figure 1 depicts a basic functional diagram for one leg of a NPC multilevel converter. The DC-link is split by $(n-1)$ series connected capacitors, thus the total DC-link voltage (V_{DC}) is the sum of all the capacitor voltages $V_{ci.}$

$$V_{DC} = \sum_{i=1}^{n-1} v_{ci}. \quad (1)$$

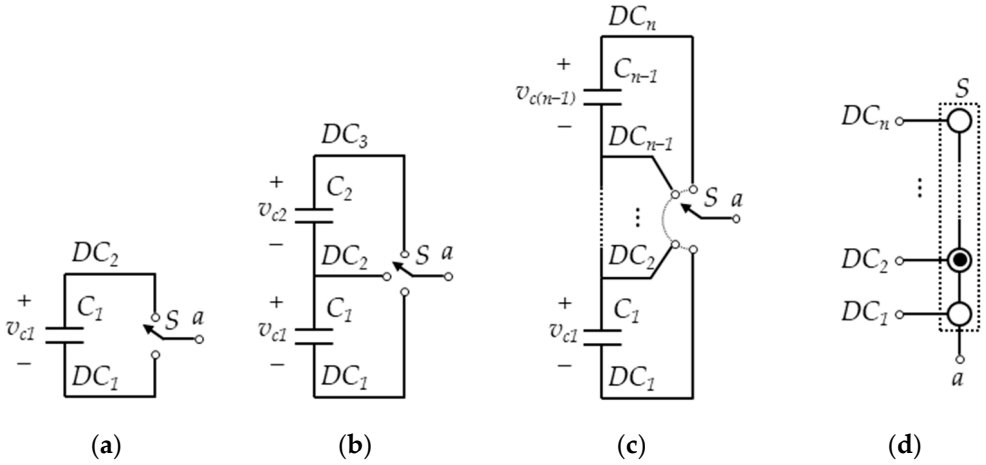


Figure 1. Functional schematic for one leg of a NPC converter. (**a**) Symbol 1, two levels. (**b**) Symbol 1, three levels. (**c**) Symbol 1, n levels. (**d**) Symbol 2, n levels, where the output a is connected to the neutral point DC_2.

When the capacitor voltages are balanced, each capacitor voltage is $V_{ci} = V_{Dc}/(n-1)$. The output of the leg can be connected to any of the outer DC-link points and to any of the intermediate points created by the series connection of the capacitors, usually known as neutral points, by means of a proper power semiconductor arrangement and control, represented in Figure 1 as an ideal commutator. Therefore, depending on the position of the commutator, the output voltage can present n different values (levels). For instance, for the 3-level leg shown in Figure 1b, the output voltage can take $n = 3$ different voltage levels with reference to DC_1 (0, $V_{c1} = V_{DC}/2$, $V_{c1} + V_{c2} = V_{DC}$). Figure 1c,d shows equivalent symbols for the n-level NPC converter leg.

The NPC multilevel converters present a set of advantages [4,14,26]:

1. The passive energy storage components such as capacitors and inductors are placed outside the power semiconductor array, enabling compact converter implementations with higher power density.
2. Since the power devices only have to block $V_{DC}/(n-1)$ voltage, typically, it enables higher converter DC-link voltage and power ratings.
3. Reduction of switching losses [15,34]: (i) since switching transitions take place at lower blocking voltage $V_{DC}/(n-1)$; and (ii) lower voltage-rated devices have lower switching losses, typically.
4. Reduction of the output AC voltage harmonic distortion, hence the output filter size is smaller (if required); lower converter AC-side common-mode voltage [35,36]; and lower electromagnetic noise [15].

5. Enhanced fault-tolerance capacity, because of the increased redundancy, since the failure of one device does not inevitably lead to a full leg shutdown [37,38].
6. Better loss sharing among converter devices, improving the temperature performance of the converter and, subsequently, enhancing its reliability [39].
7. Since multiple voltage levels are available at the DC-link, it enables the implementation of a specific control for each DC-link voltage level, which may allow a more efficient control of the power flow between systems [32,33].

However, NPC multilevel converters show two main drawbacks:

1. The number of power semiconductor devices increases significantly with the number of levels.
2. Typically, the DC-link capacitor voltages must be kept balanced at all time [16]. Unbalanced DC-link capacitor voltages cause some power devices to block more than one voltage level $V_{DC}/(n-1)$, which is unacceptable in most cases as it can lead to a device overvoltage failure. Moreover, it typically generates low-frequency output voltage distortion [40,41].

Some applications of NPC multilevel converters are motor drives [23,42,43], photovoltaic power generation [32,44–46], wind power generation [47–49], static synchronous compensation [10,50], and DC–DC conversion [29,51].

2.2. Topologies

The four main NPC topologies are depicted in Figure 2, taking the 4-level case as an example, although the extension to the n-level case is straightforward [4]. Other NPC topologies can be obtained by modifying or combining these basic topologies [52].

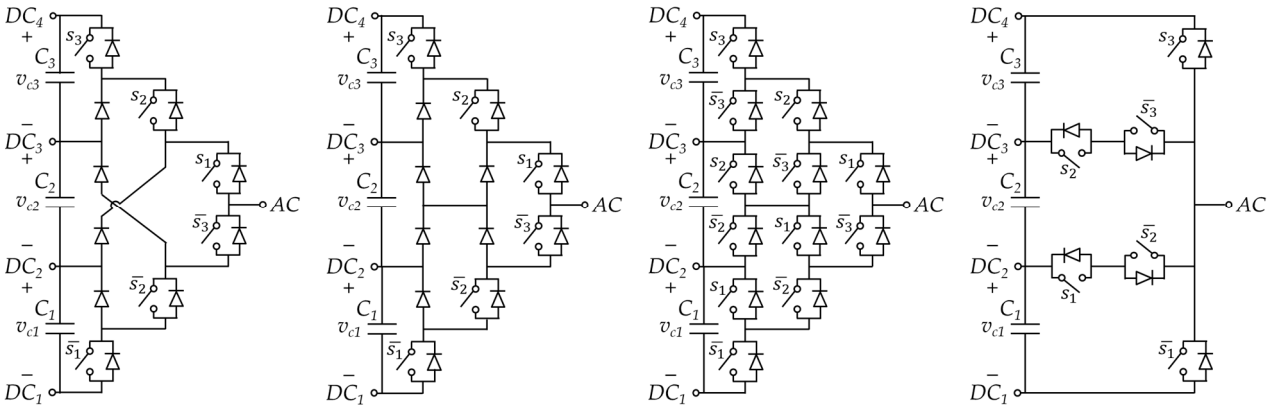


Figure 2. Main leg topologies of NPC converters, for four levels: (**a**) diode-clamped; (**b**) modified diode-clamped; (**c**) active-clamped; (**d**) reduced active-clamped.

Note that, at present, the commercial versions of NPC converters are limited to the 3-level case [10]. However, this survey addresses the generic n-level case, as it is expected that NPC converters with higher number of levels will be commercially applied in the near future.

Figure 2a shows the diode-clamped topology, which refers to the pioneer NPC topology [1,5], which is the most popular topology. It is well known that, for $n > 3$, some of the clamping diodes in this topology are required to block more than one voltage level $V_{DC}/(n-1)$, making necessary a series connection of diodes per position [16], which may hinder the implementation of this topology [13].

To overcome the abovementioned drawback, the diode-clamped topology is modified by adding supplementary clamping diodes and inner connections [6], as shown in Figure 2b. There is no need for series connection of clamping diodes in this modified diode-clamped

topology, since all the semiconductors block one voltage level [4]. However, the topology does not guarantee inherently this blocking voltage for all components, and some additional circuitry may be required [6].

In the diode-clamped topology, the loss distribution among the converter power devices is unequal, causing unsymmetrical temperature distribution of the semiconductor junction [53]. This shortcoming can be alleviated by using the active NPC (ANPC) topology [21,39,53,54] depicted in Figure 2c. Starting from the modified diode-clamped topology [6], Figure 2b, transistors are placed in parallel with the clamping diodes, resulting in the ANPC topology shown in Figure 2c. In this topology, the additional transistors enable redundant current paths that enhance the power loss distribution. Moreover, the ANPC topology guarantees the same blocking voltage value $V_{DC}/(n-1)$ for all devices [4,21].

There is an obvious interest in reducing the large number of semiconductors required by multilevel topologies. The reduced active-clamped topology [2,55] shown in Figure 2d is a popular topology with a reduced number of semiconductors, at the expense of increasing the blocking voltage value of some devices beyond one voltage level [4]. This topology is also known as T-type [27,56] or π-type [57,58] topology for the 3-level and 4-level cases, respectively.

It is worth highlighting that, whatever the topology used to implement the NPC multilevel converter legs, the operation of the leg can be reduced to the functional schemes depicted in Figure 1c,d.

2.3. Modulations

The most conventional control method for power electronics converters consists of a controller (a proportional-integral controller, in many cases) which generates the reference voltage input to a modulator. In this subsection, a basic summary of the modulations for NPC multilevel converters [4,9,10] is presented. Modulations for DC–AC conversion are mostly considered, although a brief overview of DC–DC conversion is also given at the end of this subsection.

Figure 3 shows a simple classification for multilevel modulations. Modulations that synthetize a given reference AC voltage can be broadly divided into two different subgroups, for low and high switching frequency.

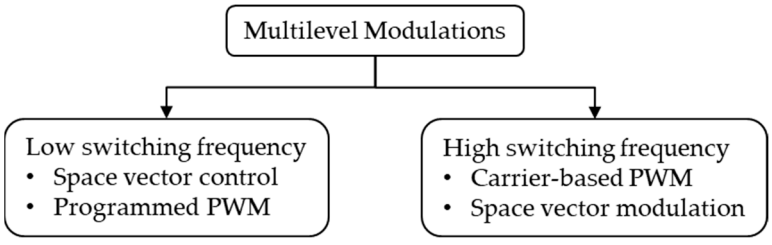
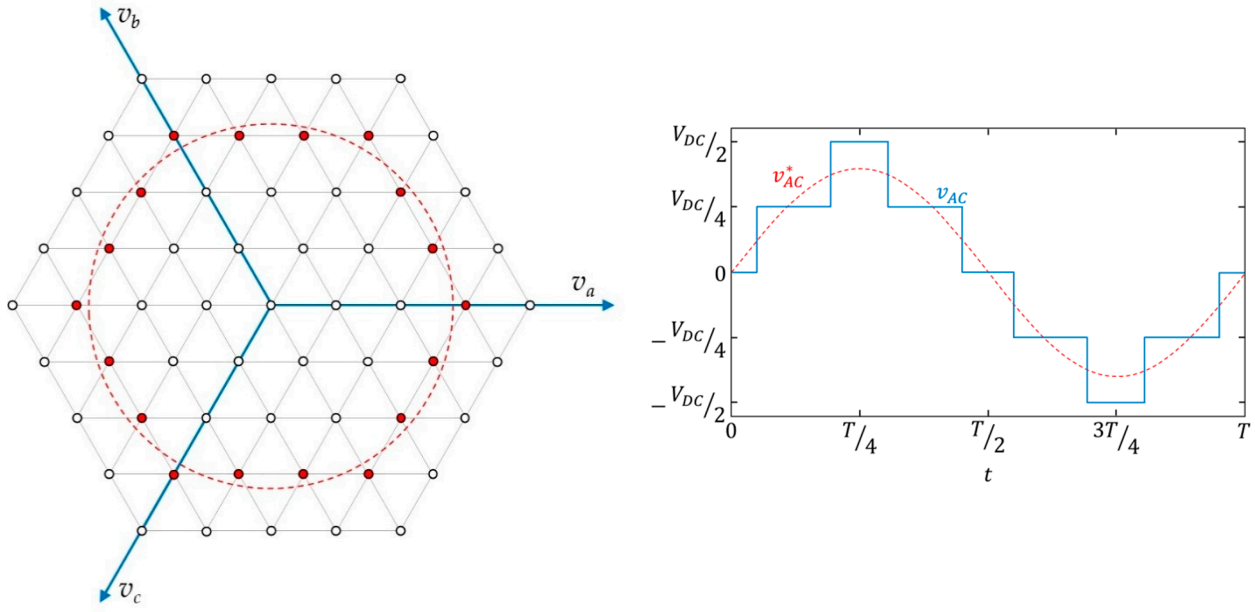


Figure 3. Basic classification of modulations for multilevel converters.

2.3.1. Space Vector Control

At every point in time, the space vector closest to the reference vector is selected and applied in the converter [59]. Figure 4a shows the space vector diagram for a 5-level three-phase converter, where the steady-state circular reference vector trajectory is depicted in dashed red. The different space vectors selected for this specific reference vector trajectory are highlighted in red. The output voltage generated with this modulation is not able to follow the fundamental reference voltage, presenting steady-state error and low-order harmonics. It is mainly intended for converters with a very high number of levels.



(**a**) (**b**)

Figure 4. Five-level three-phase converter: (**a**) space vector control; (**b**) nearest-level control in one converter leg (modulation index m = 0.8).

This strategy can also be implemented on a per leg basis through selecting the leg AC terminal voltage closest to the reference voltage, as shown in Figure 4b. In this case, the strategy receives the name of nearest-level control [16].

2.3.2. Programmed Pulse Width Modulation (PWM)

The leg AC terminal voltage waveform is approximated by means of a PWM waveform with quarter-wave symmetry, specified by means of k independent switching angles [2]. Figure 5 presents an example of a 3-level converter, with k = 3, where α_1, α_2 and α_3 are the switching angles. One of the switching angles is used to obtain the desired fundamental component voltage amplitude. The remaining switching angles can be used for other purposes, typically to eliminate (k – 1) output voltage harmonics, which is known as selective harmonic elimination (SHE) [60].

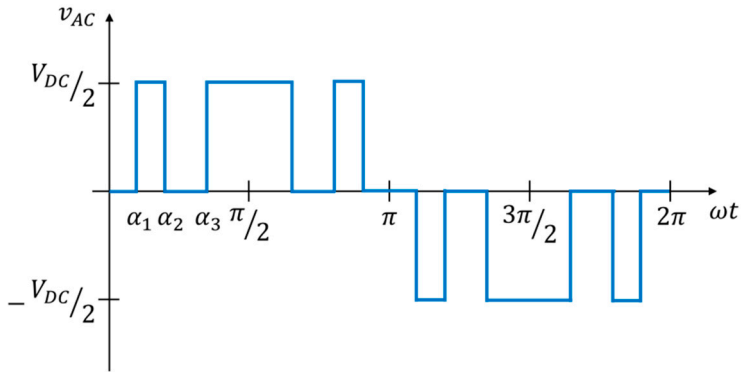


Figure 5. Three-level leg AC voltage pattern with quarter-wave symmetry with three independent switching angles.

This strategy requires the offline calculation of the solution to the nonlinear system of equations to find the switching angles, and its real-time application with a look-up table. As k increases, the harmonic content of the output voltage waveform improves, but

the calculation of the angles becomes more complex, leading even to a lack of solution. Moreover, this modulation strategy leads to closed-loop controls with reduced dynamic performance [61].

2.3.3. Carrier-Based PWM

This strategy is the natural extension of the carrier-based bipolar PWM [61] to multilevel converters [5,9,10,62]. In its simplest form, the n-level case requires one sinusoidal modulating waveform and $(n-1)$ carriers per leg, where each carrier is placed between two voltage levels. Hence, this modulation is also known as level-shifted PWM. The level-shifted carriers can present a different phase shift [63], although the best output voltage harmonic content is obtained with no phase shift. As an example, Figure 6 shows this modulation for a 3-level converter, where one sinusoidal modulating waveform and two level-shifted carriers per leg are used. The modulating signals of all legs are phase-shifted, $2\pi/p$ where p is the number of legs. At every point in time, the leg position is given by the number of carriers below the modulating signal, and the switch control signals $S_1, \ldots, S_n$ are obtained by comparison of the modulating signal with each of the carriers.

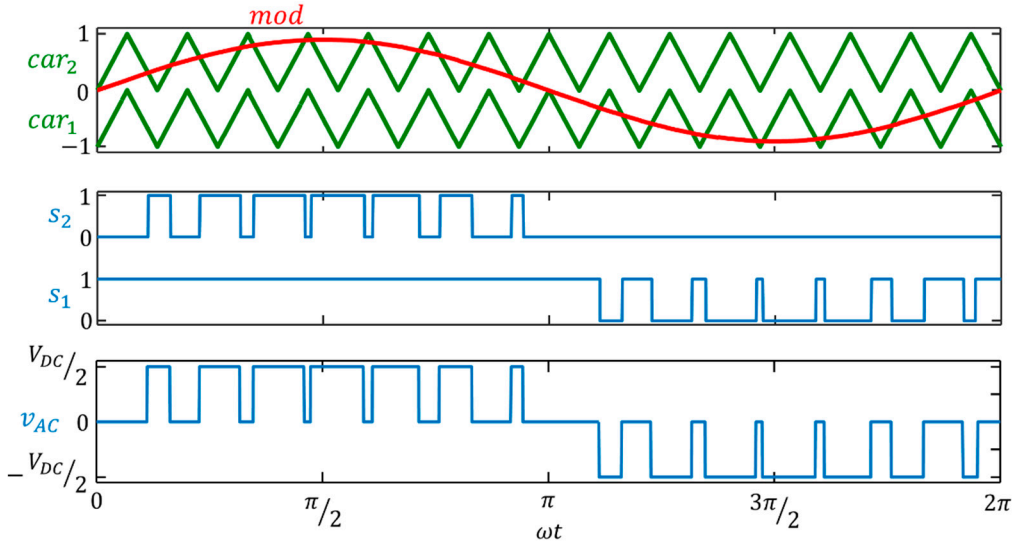


Figure 6. Basic carrier-based PWM strategy in a 3-level converter: per leg modulating and carrier signals, switch control signals, and the resulting leg output AC voltage (modulation index $m = 0.9$).

This modulation has been commonly used in the industry, since it gathers simplicity and good performance [24].

2.3.4. Space Vector Modulation (SVM)

Power electronics converters have a finite number of possible switching states that provide a finite number of discrete output voltages, where each one can be represented by means of its corresponding voltage space vector. By means of a linear combination of the converter space vectors, the SVM strategy generates an average output voltage vector equal to the reference output voltage vector over one switching period [64].

The number of space vectors increases significantly with the number of levels [65,66], together with the number of redundant switching states (different switching states with the same space vector). Therefore, multilevel converters have available many options, with several degrees of freedom, to select the space vectors used for the linear combination that generates the output voltage vector. Hence, space vectors are usually selected to pursue some additional operation goals. For instance, the number of switching transitions can be minimized by selecting the minimum possible number of space vectors [4]. The output voltage harmonic distortion can also be minimized by selecting the space vectors closest to the reference, a strategy known as the nearest three vectors (NTV−SVM) [66,67]. Figure 7

depicts an example of the NTV−SVM, where the nearest three vectors (V_1, V_2, and V_3) to the reference voltage V^* are selected.

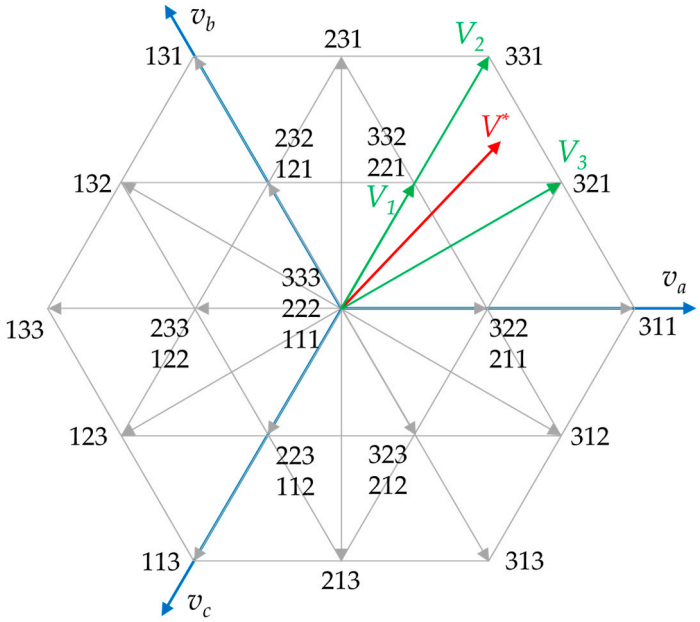


Figure 7. Nearest three vectors selection (NTV−SVM) in a three-phase DC–AC converter.

Another possible space vector selection is the so-called virtual vector SVM (VV−SVM) [68]. In this strategy, the output voltage vector is generated by a linear combination of virtual space vectors, which are defined by the user as a linear combination of certain converter switching states. Among other advantages, this modulation is particularly useful to balance the capacitor voltages [69,70].

A three-dimensional SVM (3D−SVM) [71,72] is applied mainly in unbalanced three-phase systems.

It is worth highlighting that SVM strategies have a carrier-based PWM equivalent [73–78], with a suitable common-mode component added to the modulating signals, or even the introduction of multiple modulating signals per phase. The only difference between both modulations is found in the procedure to determine the gating signals of the converter switches: in SVM, the converter is considered as a whole; in carrier-based PWM, each phase is considered separately [61].

The SVM technique offers flexibility and capacitor voltage balancing, although the computation burden grows as the number of levels increases. However, new calculation algorithms with reduced computation burden allow us to overcome this drawback [7].

2.3.5. Modulations for DC–DC Conversion

At present, there are few applications of NPC multilevel converters to DC–DC conversion. However, some modulations are found in the literature for NPC multilevel DC–DC converters, without galvanic isolation [79], and with galvanic isolation [80,81].

2.4. Control Methods without a Modulator

Unlike conventional control techniques for power electronics converters (controller + modulator), some control methods do not require a modulator. These control methods directly determine the corresponding switching state of the converter, without a modulator, to pursue the system control goals. In this subsection, these kinds of control methods are briefly described.

Hysteresis control is the strategy used in direct torque control (DTC) [82] and direct power control (DPC) [83]. When the controlled system variable goes outside the hysteresis

band limits, the converter switching state changes to redirect the variable back inside the hysteresis band.

In predictive control and, more specifically, in finite-control-set model predictive control, the error of the controlled variables and eventually other performance indicators are included in a cost function by means of the mathematical model of the system. In every switching period, the cost function is evaluated for all the switching states of the converter, and the switching state that minimizes the cost function is selected and applied in the following switching period [47,48,84].

A relevant drawback of both strategies is their variable switching frequency and spread harmonic spectrum, although it can be mitigated by introducing some strategy modifications [85,86].

3. Analysis of the Capacitor Voltage Balance

As shown in Figure 1, the DC-link of the $n-$level NPC converter is split by $(n-1)$ series-connected capacitors, typically with the same capacitance ($C_1 = C_2 = \cdots = C_{n-1}$). Proper converter operation requires the capacitor voltages to be balanced; i.e., all the capacitor voltages should be $v_{Ci} = V_{DC}/(n-1)$at all times.

Since the converter legs are often connected to the inner DC-link points (neutral points), the ordinary operation of the converter causes the circulation of current through the DC-link neutral points, which modifies the capacitor voltage balance. Figure 8a shows the 3-level case, where the relationship between the neutral-point current i_{DC2} and the derivative of the capacitor voltage imbalance $v_{imb} = v_{C2} - v_{C1}$ is deduced as

$$i_{DC2} = i_{c2} - i_{c1} = C_2 \cdot \frac{dv_{c2}}{dt} - C_1 \cdot \frac{dv_{c1}}{dt} = C \cdot \frac{d(v_{c2} - v_{c1})}{dt} = C \cdot \frac{dv_{imb}}{dt}. \quad (2)$$

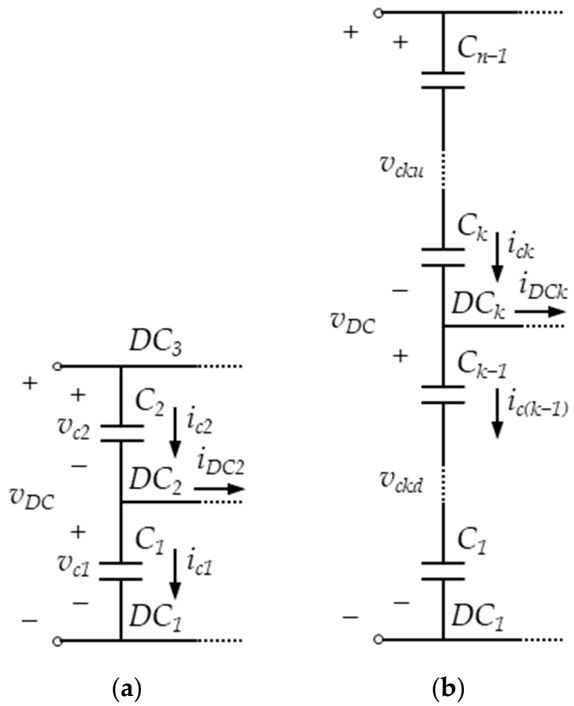


Figure 8. Relationship between the neutral-point current and the DC-link capacitor balance: (**a**) 3-level case; (**b**) n-level case.

Figure 8b shows the extension to the general n-level case, where only the influence of the current through the neutral point k is considered. The neutral-point current i_{DCk} is proportional to the derivative of the imbalance voltage v_{imbk} between the average voltage

of the $(n-k)$ top DC-link capacitors $v_{cku}/(n-k)$, and the average voltage of the bottom $(k-1)$ capacitors $v_{ckd}/(k-1)$, according to

$$i_{DCk} = i_{ck} - i_{c(k-1)} = \frac{C}{n-k} \cdot \frac{dv_{cku}}{dt} - \frac{C}{k-1} \cdot \frac{dv_{ckd}}{dt} = C \cdot \frac{d\left(\frac{v_{cku}}{n-k} - \frac{v_{ckd}}{k-1}\right)}{dt} = C \cdot \frac{dv_{imbk}}{dt}. \quad (3)$$

Starting from a capacitor voltage balance condition, it is deduced from (3) that the DC-link capacitor voltage balance is kept when all the DC-link neutral-point currents are zero; that is, when no charge is provided or extracted through the neutral points [87].

For a n-level converter, the DC-link capacitor voltage balance condition is obtained by applying (3) with $i_{DCk} = 0$ to all the $(n-2)$ DC-link neutral points [87].

Since the converter legs are often connected to the DC-link neutral points, the ordinary operation of the converter does not allow obtaining zero instantaneous currents through the DC-link neutral points at all times, leading unavoidably to capacitor voltage imbalance. Nevertheless, considering a given period of time and by means of a proper method, it is feasible to get zero average neutral-point currents. In this case, a zero net charge flows through the neutral points, and therefore the average capacitor voltage balance is kept. Note that, within the considered period, the instantaneous neutral-point currents cause capacitor voltage ripple, the amplitude of which depends on the neutral-point current value, the capacitor value, and the length of the period considered for averaging. That is, average capacitor voltage balance can be achieved, but some transient imbalance is present (capacitor voltage ripple). With the same capacitor value, the higher the neutral-point currents and the longer the period, the higher the capacitor voltage ripple and transient imbalance amplitude.

The DC-link capacitor voltage balance depends on the neutral-point current's behavior which, in turn, depends strongly on the modulation strategy of the converter. Hence, although a generalized analysis is feasible, a modulation strategy is required to achieve proper detail and quantification. Therefore, in the literature, the analysis of the capacitor voltage balance in NPC multilevel converters is mostly related to a specific modulation as, for instance, 3-level PWM [88], n-level PWM [89], 3-level SVM [40], 3-level VV−SVM [69], 4-level VV−SVM [90], 3-level SHE [91], n-level SHE [92].

To illustrate the charge/discharge of the DC-link capacitors, a simple analysis of the neutral-point current (i_{DC3}) in a 4-level NPC leg is shown in Figure 9a, operating with a simple space vector control strategy and assuming a sinusoidal output current. In the case of the unity power factor, as depicted in Figure 9b, the output current is in phase with the output voltage and the neutral-point current i_{DC3} presents only positive values. Hence, in this case, the average value of i_{DC3} is always positive, leading to a DC-link capacitor voltage imbalance. Figure 9c shows the case with an output current lagging 90° from the output voltage. In this case, the neutral-point current i_{DC3} has the same positive and negative waveform, and zero average value, therefore the balance is kept. With this modulation strategy, only active currents have influence on imbalance [93].

In a multiphase system, the analysis can be performed in the space vector diagram. The neutral-point current is shown for each switching state for the 3-level three-phase NPC in the diagram depicted in Figure 10. From Figure 10 and (2), it is simple to deduce the trend of the DC-link voltage balance for each switching state. Zero and large vectors do not have influence on the balance. Small vectors can be generated by two redundant switching states having the same but opposite influence on the balance. Medium vectors have influence on the voltage balance but they do not have any redundant switching state. This simple analysis can be directly extended from 3- to n-level.

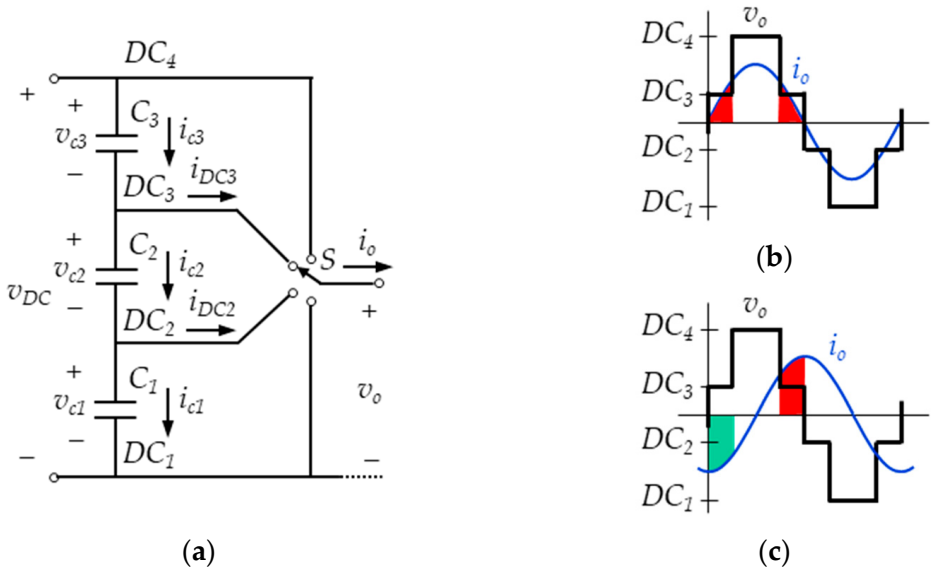


Figure 9. Current through the neutral point DC_3 (i_{DC3}). In red, the current flows out of the neutral point DC_3 (positive i_{DC3}); in green, the current flows into the neutral point DC_3 (negative i_{DC3}): (**a**) functional model of a 4-level NPC leg; (**b**) case with pure active output current (power factor = 1); (**c**) case with pure reactive output current (power factor = 0).

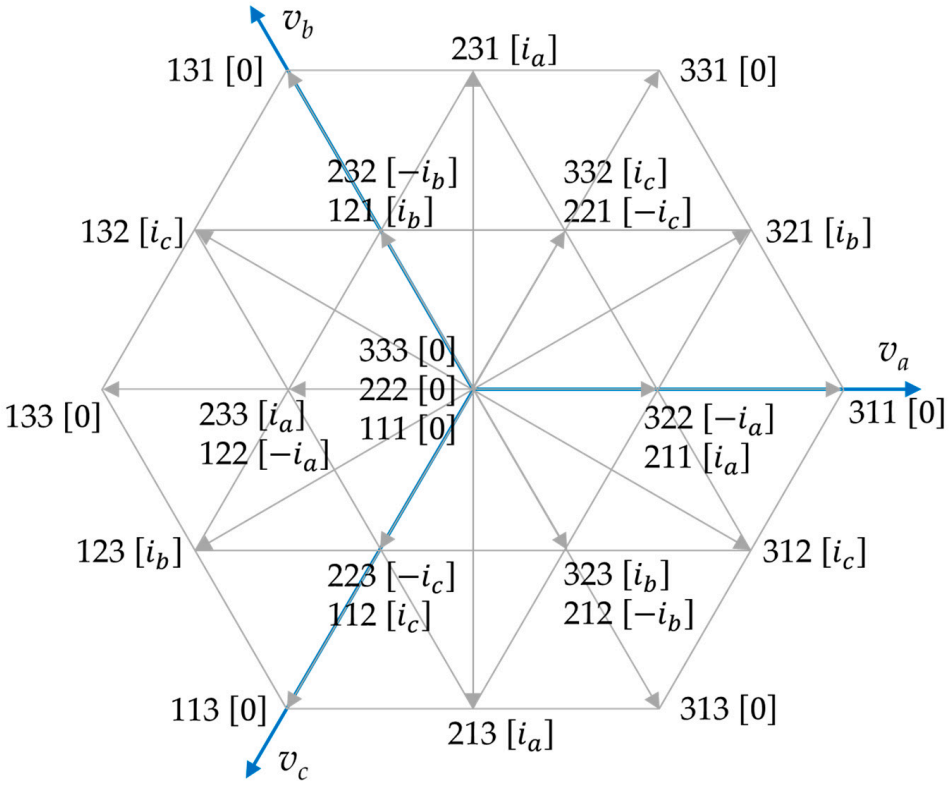


Figure 10. Space vector diagram with neutral-point current information for a 3-level three-phase NPC DC–AC converter.

As detailed above, the DC-link capacitor voltage balance is achieved when the average currents through all the neutral points are zero. It is worth highlighting the significance of the setting of the averaging period length to calculate the average neutral-point currents. It can be set from a switching period to a line period, or even longer. A shorter averaging period causes smaller charge flowing through the neutral points, yielding smaller voltage

ripple, and allowing the use of smaller DC-link capacitors. When a longer averaging period is used, bigger DC-link capacitors are required to avoid a large voltage ripple amplitude, but the method to maintain the balance can be simpler. Note that higher voltage ripple amplitude could lead to an excessive blocking voltage in the switching devices [31] and significant output AC voltage distortion [94,95].

The implementation of a balancing method is essential to control the average neutral-point currents and consequently to guarantee the capacitor voltage balance, at all times. Note that the balancing method should be used to keep the balance, starting from a balanced condition, and must also have the capacity to take the system to a balanced condition, starting from an unbalanced condition. If no balancing method is considered in the converter control, the DC-link capacitor voltage balance can be kept only in a very reduced number of cases and operating conditions [96–98], since the converter itself has a limited capability to maintain the balance. Even in these most favorable cases, the average neutral-point currents may take non-zero values if the switching pattern presents some imbalance, or during transient operation, which may lead to DC-link capacitor voltage imbalance [88,99].

A classification of the solutions for DC-link capacitor voltage balancing is shown in Figure 11. Software solutions consist of properly adapting modulations and/or control methods to guarantee the balance, which can be implemented on an open-loop or closed-loop basis. Hardware solutions consist of adding additional circuitry. These solutions are described in the following sections.

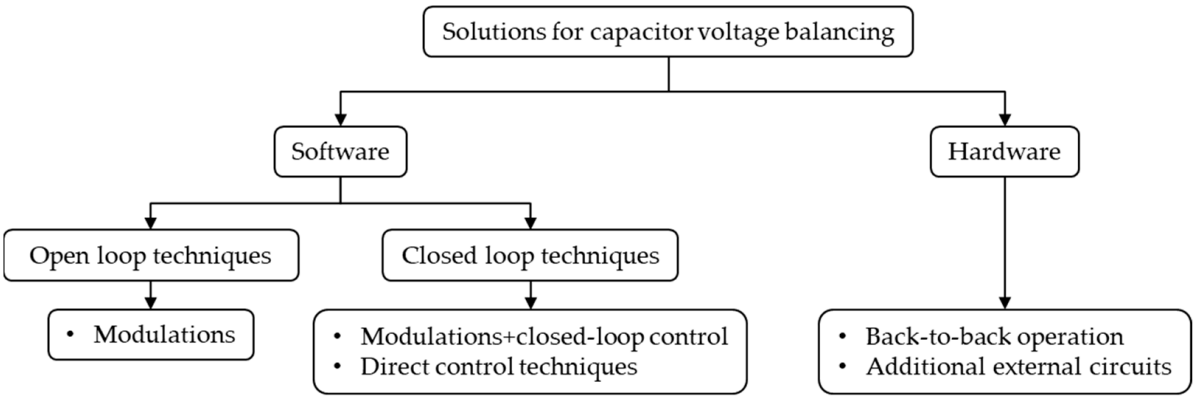


Figure 11. Classification of the solutions for DC-link capacitor voltage balancing.

4. Open-Loop Techniques

There are a set of methods that pursue the DC-link capacitor voltage balance which can be classified as open-loop techniques. Typically, these techniques analyze the unbalance problem considering the specific modulation strategy used in each case, and then propose certain arrangements over the modulation strategy to keep the balance. Good balance behavior can be reached in some cases. However, the lack of feedback inherently limits the ability to compensate for the imbalance.

The selection of the NPC converter voltage vectors is usually done to provide the best output voltage quality, the smallest number of commutations (to minimize switching losses), and to keep the balance, where the use of the redundant switching states is essential. To reduce switching losses, early modulation strategies for NPC converters employed a set of rules to restrict the selection of the switching states, such as for instance allowing only commutations between two adjacent voltage levels (carrier-based PWM) or by using the nearest three vectors (NTV−SVM).

As observed in Figure 10, and extensively in the *n*-level cases, when using conventional SVM techniques, as the modulation index increases, larger voltage vectors are required to generate the output voltage. This creates a lack of redundant switching states, making

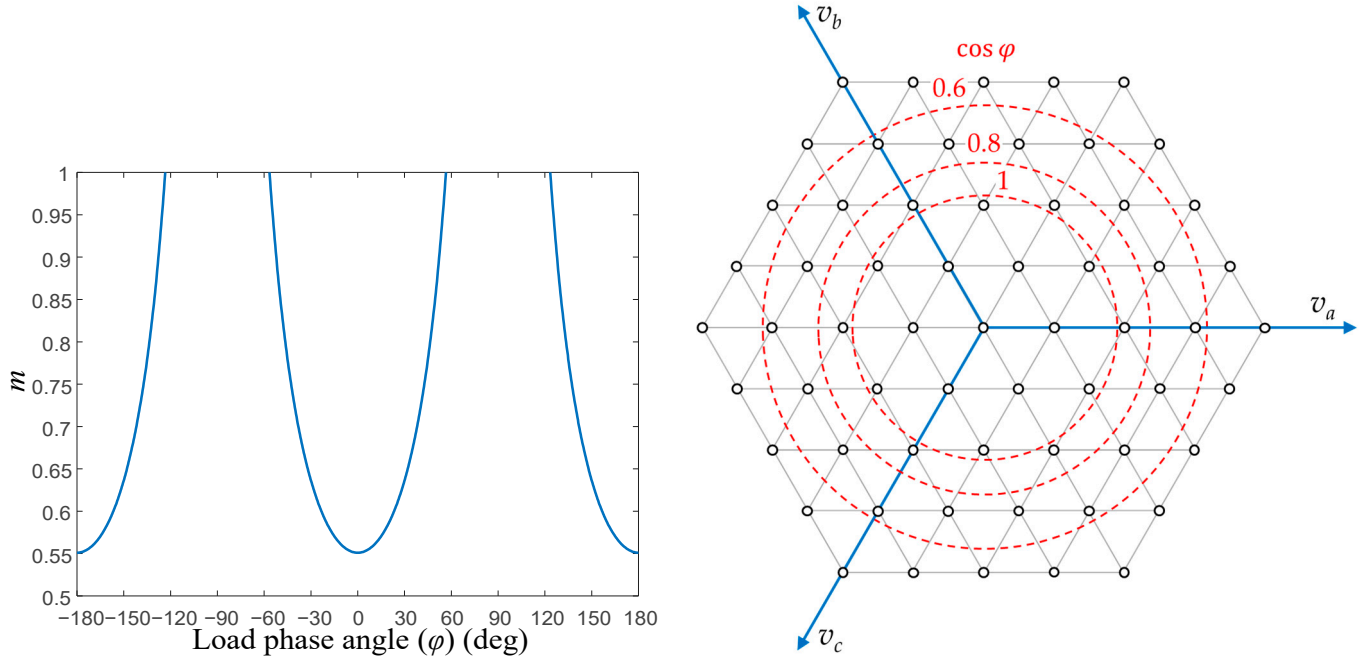
unattainable the balance within the switching period [100–102]. This difficulty varies depending on the load conditions (load power factor and harmonic content).

In the case of a 3-level three-phase NPC AC–DC converter, balanced operation within a switching period cannot be achieved for fairly high modulation index values and low load power factors. A low-frequency ripple (1/3 of the line frequency) appears in the neutral points [40]. That is, balance is not possible within the switching period, but can be achieved within a longer period at the expense of having higher voltage imbalance ripple amplitude [103]. This ripple causes, on one hand, higher blocking voltage in the semiconductor devices and, on the other hand, as the ripple propagates from the DC side to the AC converter side, output voltage distortion [40,104].

In the case of a n-level three-phase NPC DC–AC converter, with $n \geq 4$, to keep balanced operation within a switching period, it must be verified that [101]

$$m < \frac{0.551}{|\cos \varphi|}. \tag{4}$$

where φ is the load phase angle and m is the modulation index, defined as the peak value of the fundamental line-to-line voltage divided by the total DC-link voltage. For a modulation index higher than (4), some of the capacitor voltages collapse, which results in a critical system failure. This boundary for balanced operation is depicted in Figure 12a. In Figure 12b, this boundary is shown over a space vector diagram of a 5-level three-phase converter.



(**a**) (**b**)

Figure 12. Boundary for balanced DC-link capacitor voltage operation within a switching period: (**a**) maximum modulation index depending on the load phase angle; (**b**) maximum modulation index depending on the load phase angle, over a space vector diagram of a 5-level three-phase converter.

In a modulation, there is usually freedom to adjust the zero-sequence voltage. As the neutral-point currents are related to the zero-sequence voltage [105], this degree of freedom is used as an open-loop balancing technique [31,40,88,105], although the balance is not achieved for the full operation range.

The VV−SVM switching strategy synthesizes the output voltage from a set of virtual voltage vectors defined as a linear combination of the vectors corresponding to certain

switching states. All the virtual voltage vectors are defined to have an associated switching average neutral-point current equal to zero, as detailed in Figure 13. Thus, whatever set of voltage vectors is used to generate the output voltage, no imbalance is introduced. The VV−SVM strategy is capable of controlling the DC-link capacitor voltage balance for any load, modulation index and number of levels, provided that the addition of the output three-phase currents equals zero, as detailed for 3-level [69,70], 4-level [90], *n*-level [106], *n*-level two-leg [107], with optimized spectral performance [108] and with implementation as a carrier-based PWM for *n*-level *n*-leg NPC [109]. The extension to the overmodulation region is found in [110,111]. Because of the virtual voltage vector definition, the VV−SVM presents a higher number of commutations (about 4/3, for $n = 3$) per switching period than the conventional NTV−SVM. However, VV−SVM may present a similar device junction temperature stress compared to a conventional NTV−SVM, thanks to its better switch utilization [112].

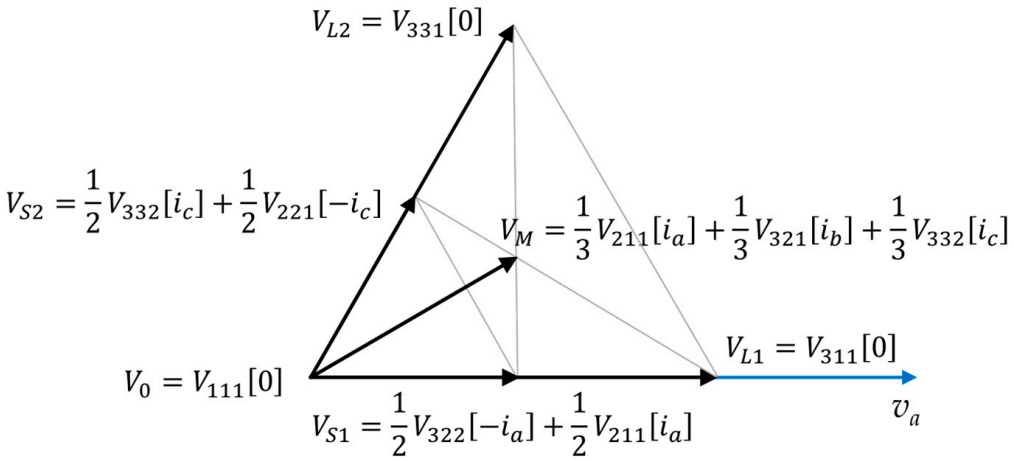


Figure 13. Virtual space vectors defined for the first sextant of the space vector diagram shown in Figure 10 [69].

Other alternative PWM strategies have been also defined to achieve capacitor voltage balance under a number of levels $n \geq 4$, such as carrier-overlapped PWM [89,113,114]. The balancing is guaranteed on average over the line cycle for all modulation index values and with lower commutations than with the VV-SVM.

Hybrid modulations [41,115] take advantage of the benefits of each modulation. For instance, for $m < 0.5$ NTV−SVM can be used to reduce commutations, and for $m > 0.5$ VV−SVM can be used to assure the balance, at the expense of increasing commutations.

Finally, note that, under certain operating conditions, balance can be kept by means of the natural balancing mechanisms of the NPC converter. This "do-nothing" control is known as natural balancing [96,97] or self-balancing [92,98]. However, the requirements to keep the balance by natural balancing are very restrictive. For NPC converters, natural balancing seems to be reported in the literature only for the 3-level [92,97,98], and the extension to a higher number of levels is apparently not feasible. It is also strongly sensitive to many operating factors, such as the modulation strategy, the transient operation, the load power factor, and the load current harmonic content, among others. Therefore, although the technique has been demonstrated suitable for the 3-level NPC in some cases with restricted operating conditions and small disturbances [96,98], under more demanding operating conditions, its limited aptitude can lead to a steady-state imbalance or an excessive neutral-point voltage ripple.

5. Closed-Loop Techniques

Balance can be theoretically guaranteed by means of the open-loop methods described above. However, in practical implementations, there are some drawbacks, such as asymmetries in semiconductors, passive components and switching signals, or harmonic contents,

among others, which degrade the efficacy of the open-loop methods. Therefore, closed-loop balancing techniques are essential to compensate for these deviations and to guarantee the balance in all operating conditions. Closed-loop techniques are usually based on the feedback of the DC-link capacitor voltages, although some methods consider other variables, such as the output currents.

The control of the zero-sequence voltage component is likely the most extended control-loop technique to keep the balance. Modulations generate the desired AC output voltage and have inherently a certain freedom to set a zero-sequence voltage. This zero-sequence voltage is translated into a variable voltage between the AC load neutral point to ground but, as the AC loads have an isolated load neutral point in most cases, there is no path for the zero-sequence currents to flow and, hence, zero-sequence currents are zero.

Once the balance is guaranteed, these methods usually pursue other additional control objectives: reduction of the neutral-point voltage oscillation to reduce the semiconductor voltage stress and to improve the quality of the AC output voltage; reduction of the common-mode voltage; and reduction of the number of commutations per period.

Early methods proposed in the literature show significant limitations. For instance, in [99], an offset is added to the modulation waveform in a carrier-based PWM, by means of a closed-loop control system, where voltage imbalance and the output load currents are fed back. However, it presents significant drawbacks: load currents are required to be fed back; limited operating range; and it is only possible to control the DC-link midpoint of converters with an odd number of levels. In [116], for a n-level NPC, the capacitor voltages and the load currents and angle are fed back to inject a zero-sequence voltage over a carrier-based PWM. Since the output phases are allowed to commutate only between adjacent DC levels, the balance cannot be kept for all the operating range with this method.

A set of methods have been presented for the 3-level NPC, based on the proper selection of the redundant vectors and feedback of the imbalance, which guarantee the balance in all the operating range for the line period. Balance cannot be achieved for the switching period, and a low-frequency voltage imbalance ripple is present, which propagates to the output through the modulation and produces an output voltage distortion [40,94,117–119]. In order to reduce this distortion, the DC-link voltage imbalance is fed forward to modify the amplitude of the triangular carrier waveforms [94] or the length of the voltage vectors in the space vector diagram [117].

In [120,121], the load currents are considered, concurrently with the voltage unbalance, in the balance control loop, using a carrier-based PWM, where a zero-sequence voltage is also injected.

Other methods propose the regulation of the dwell times of the switching states to balance the NPC, for 3-level [122] and for 4-level [123] or, at least, to reduce the output voltage distortion [95].

The closed-loop methods described above do not achieve the balance within the switching period, because of the limited benefits of the used modulations. To reach it, it is required to use a wider set of voltage vectors to generate the reference vector, at the cost of having a higher number of commutations per switching period; that is, the use of modulations based on virtual vectors is suitable to achieve the control goals.

In [102], a closed loop to balance the DC-link is proposed for a 3-level NPC, using an optimized VV–SVM modulation [108]. It is worth highlighting that, with this modulation, under ideal operating conditions, balance can be assured within the switching period for all the operating range in an open-loop operation. Since non-idealities can limit the effectiveness and the response speed of the method, a zero-sequence voltage is introduced by the closed-loop control by adding an offset to the leg duty ratios in the modulation. Figure 14 shows the performance of this closed-loop control. Starting from a DC-link capacitor voltage unbalanced condition, the balance is recovered within 100 ms, as shown in Figure 14a. Figure 14b shows the control effort variable p_2 to inject/extract current from the DC-link neutral point, to achieve the balance condition. This control effort variable

modifies the duty ratios given by the modulator, see Figure 14c, resulting in perturbed or modified duty ratios, as shown in Figure 14d, which are effectively applied to the converter.

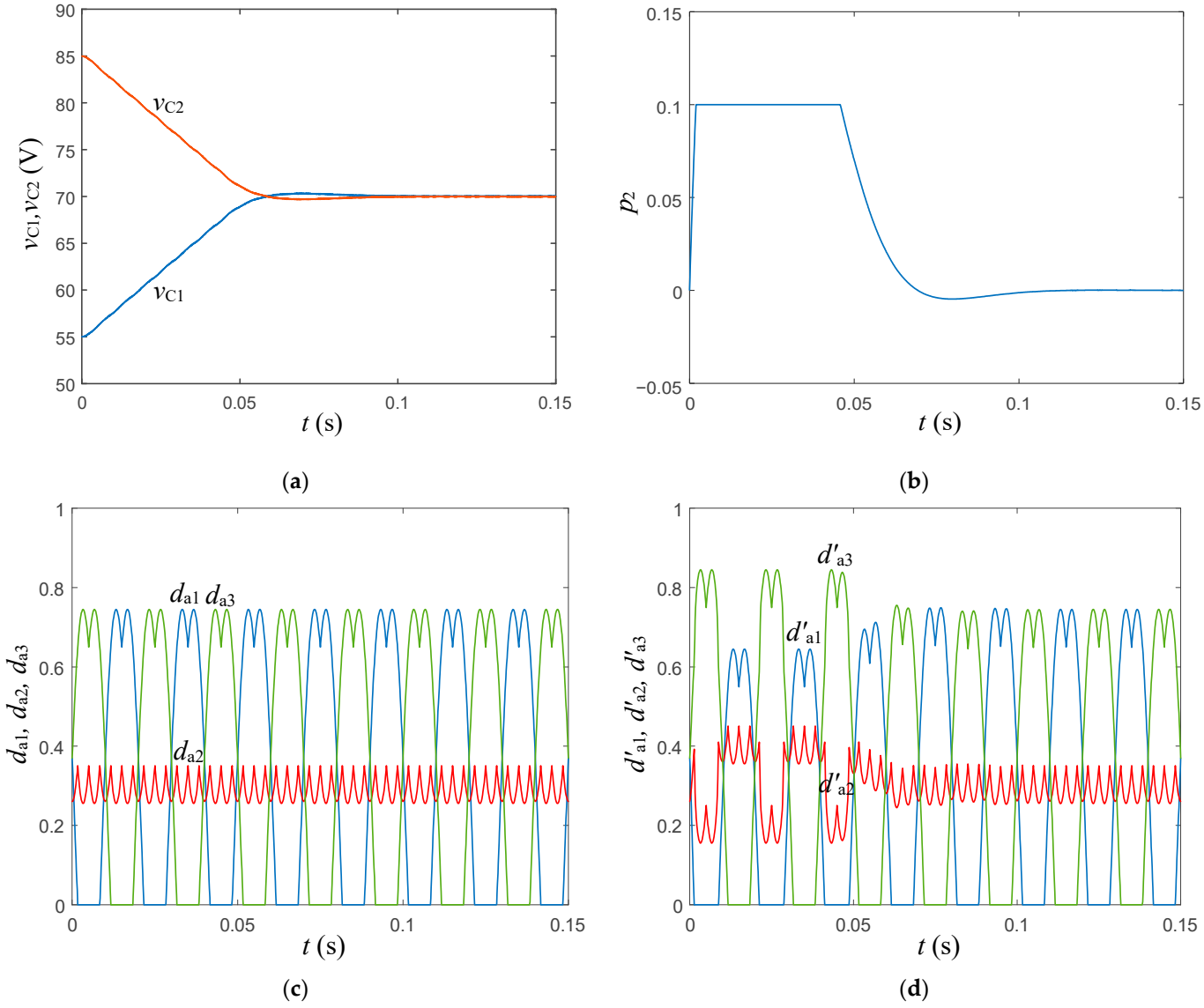
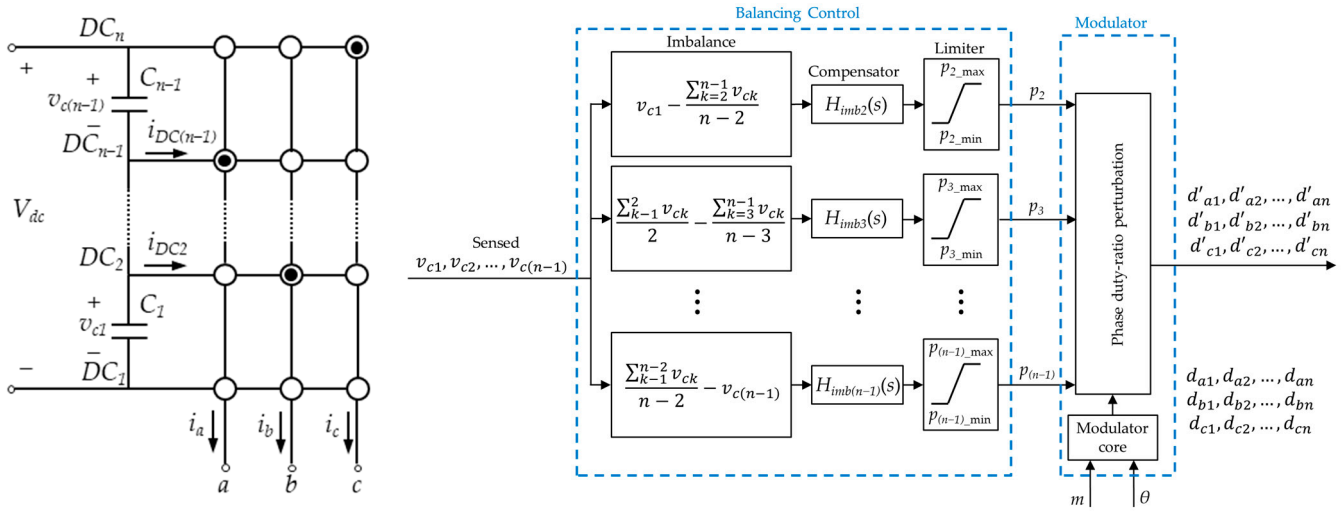


Figure 14. DC-link capacitor voltage balance recovery transient for the 3-level NPC [102]: (**a**) DC-link voltages v_{c1} and v_{c2}; (**b**) control effort variable p_2 to recover the voltage balance; (**c**) original phase-a duty ratios; (**d**) perturbed phase-a duty ratios.

For the n-level NPC [124] shown in Figure 15a, this controller is also suitable. The control structure is shown in Figure 15b. The $(n-1)$ DC-link capacitor voltages are sensed and used to calculate the $(n-2)$ unbalance values corresponding to each inner DC-link neutral point. The imbalance values are then processed by a compensator and a limiter. Variables p_j indicate the control effort required to extract/inject current from/into each DC-link neutral point to recover the voltage balance. This information is sent to the modulator together with the modulation index and line cycle angle to generate the phase duty ratios of connection to the different DC-link levels.



(**a**) (**b**)

Figure 15. *N*-level three-phase converter: (**a**) functional schematic; (**b**) balancing control structure [124].

Several variations of this closed-loop method can be found in the literature. For the 3-level NPC, in [125], the VV–SVM calculation is modified considering the voltage imbalance, similar to in [120]. Other works take advantage of the degrees of freedom given by the VV–SVM to control other variables, in addition to the imbalance, such as for instance the reduction of the common mode voltage [126,127], reduction of the switching losses [128], or to tailor the solution for a specific application (aircraft electric starter generator) [129,130].

The same control loop method is proposed with a carrier-based PWM modulation for a 3-level NPC [131]. The extension for a *n*-level *n*-leg NPC is found in [132], with an enhanced decoupled DC-link capacitor voltage control [133]. An interesting implementation of this strategy on a FPGA for a 4-level NPC is described in [134]. Other carrier-based PWM methods are found in [57,135], where the closed loop is based on mathematical expressions to determine the duty ratios, not requiring PI or PID controllers, and in [56], which uses a hybrid of zero-sequence voltage injection and virtual zero-level modulation.

In the overmodulation region, the balance in every switching cycle can also be guaranteed [110,111,136], basically conceived as a particularized extension of modulations for the linear region.

At low frequency-modulation indices, SHE modulation strategy is commonly used. The balance is achieved by using the redundant states method for a 3-level NPC [91] and for a 5-level NPC [137]. However, this approach presents limitations in the maximum applicable modulation index and the regulation capability of the DC-link capacitor voltages. In [138], the balance control is performed by introducing small variations of the switching angles defined by the SHE modulation method for a 3-level ANPC, although extension to a higher number of levels is not apparently developed. A comprehensive and powerful modulation strategy is proposed in [139], suitable for *n*-level *n*-leg NPC, guaranteeing the balance for any modulation index and load power factor. Similar to the SHE method, this approach obtains the converter switching angles to generate the desired output voltage but keeping the balance in open-loop operation, and it is generated with a carrier-based modulation, including a closed-loop control [132,133].

Hysteresis control techniques are also used for closed-loop balance control. The proper redundant switching state is selected by means of an hysteresis controller [82,140], or in combination with zero-sequence injection [141].

Model predictive control (MPC) is a subset of predictive control strategies that generate predictions from a model of the system, for all the possible converter switching states. A quality function is evaluated based on those predictions, and the switching state that mini-

mizes the quality function is actually applied to the converter in the next switching period. There are in the literature a significant number of works with predictive control for the NPC: 3-level [84,142,143]; 3-level back-to-back [144]; 4-level [47,48,145]; *n*-level [36,50,87]; *n*-level back-to-back [146]; or dual T-type 5-level NPC [147]. In general, with predictive control, the balance can be achieved for the entire operating range. The drawbacks of the predictive control in comparison to modulations are well known: a spread harmonic spectrum, and higher computation burden with increasing number of levels.

Finally, there exist other different control methods, as for instance, the quasi two-state mode for the *n*-level NPC [148] or second-order harmonic voltage injection [149].

6. Hardware Methods

DC-link capacitor voltages can also be balanced by means of hardware methods. Some extra hardware is added to the NPC converter, specifically to guarantee the balance. This solution usually provides a robust balance, uncoupled from the NPC converter operation, but reduces the overall efficiency and introduces significantly higher cost and complexity.

Back-to-back operation may be considered a hardware balancing method. Converter operation can be arranged so that each converter counteracts the effect of the other converter on the balance [30,93]. However, a closed-loop method, usually a zero-sequence voltage injection, is required to guarantee the balance [150,151].

The simplest way to assure the balance is by means of separate DC sources [23], which typically requires a dedicated transformer [152], as shown in Figure 16a.

In the specific case of 3 levels, the balance can be achieved by controlling the zero-sequence current if the DC-link neutral point is connected to the neutral point of the AC side system [153]. This method causes the circulation of a zero-sequence current on the AC side, which may not be acceptable due to magnetic component saturation or heating, among other issues.

The most common solution consists of external circuitry added to the DC-link, working as a DC–DC converter. In three-phase converters, in most cases, this external circuit presents a structure based on the conventional multilevel leg topologies, with properly modified connections, and eventually with added inductors and/or capacitors. Different types of this external circuit are applied: an external circuit based on a NPC-type leg is applied to a 4-level NPC [154]; an external circuit based on a flying-capacitor type leg is applied to a 3-level converter [155] and to a *n*-level converter [156]; and an external circuit based on an ANPC-type leg is applied to a 5-level converter [157], shown in Figure 16b.

Some other variations of configurations for the external balancing circuit are found in the literature. An external circuit with a structure based on the NPC-type leg, with additional inductors, is presented for 4- and 5-level in [5], for 3-level in [103], for 4-level in [158], shown in Figure 16c, and for a 5-level motor drive [42,43,159]. An external circuit based on resonant switched capacitors is presented for *n*-levels in [160].

The balance is also addressed with a two-stage structure. In [161], from a single DC supply, a DC–DC boost converter with three output terminals is used to set and balance the DC-link capacitor voltages of a 3-level single-phase NPC converter. A DC–DC converter is proposed in [45] to balance the 3-level DC-link from unbalanced photovoltaic panels, as shown in Figure 16d.

Balancing can also be achieved by means of external circuitry connected to the AC side of the converter. This kind of solution takes advantage of the natural balancing properties of the NPC converter, by connecting a proper external L−C [96] or R−L−C [97,162] branch to the AC side, acting as a bandpass filter. In general, its application seems to be restricted to a specific operating range. Therefore, hardware methods are preferred to be connected on the DC side.

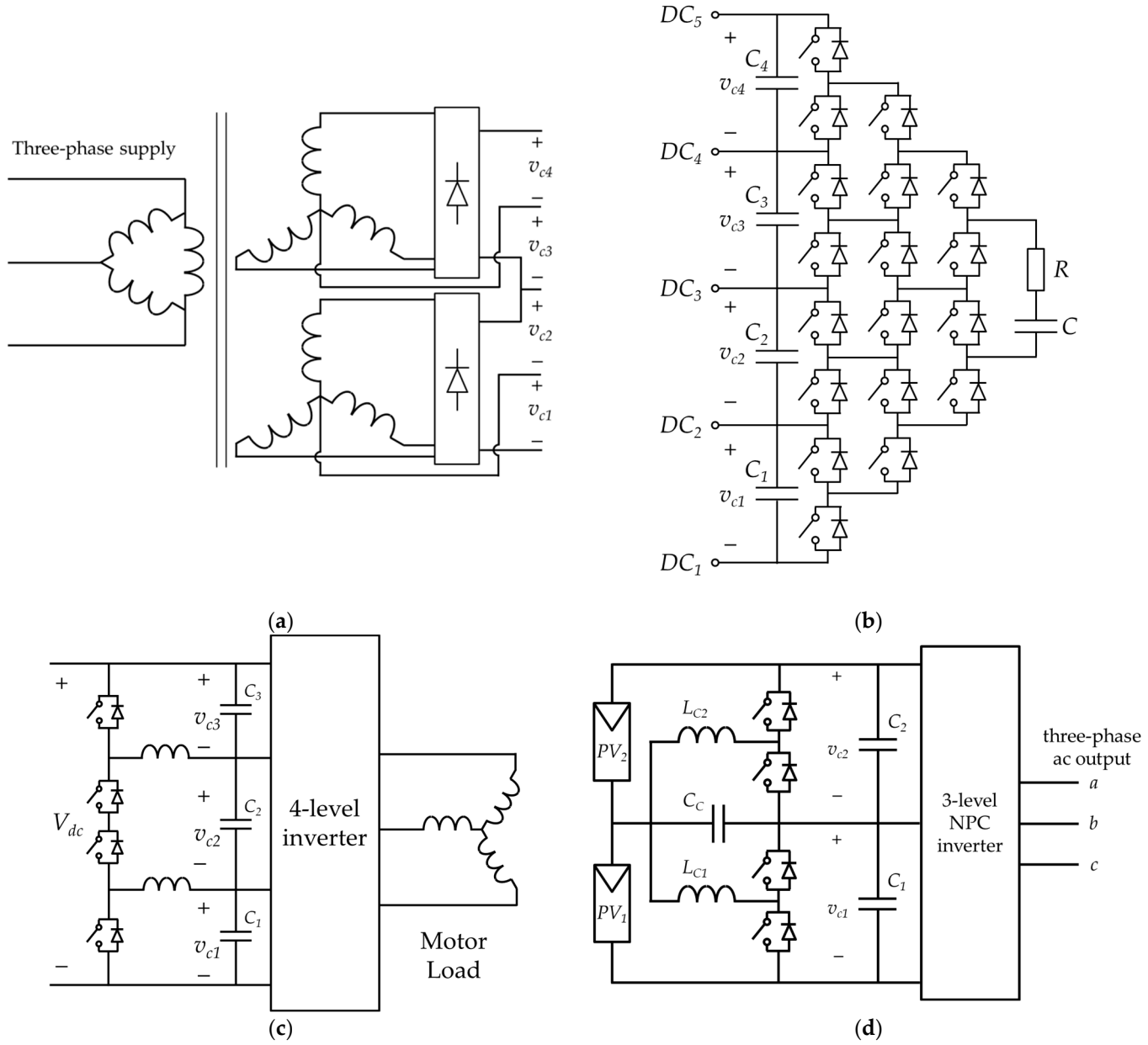


Figure 16. Circuits for balancing with hardware methods: (**a**) Separated DC sources in a 5-level NPC [152]; (**b**) external circuit added to a 5-level NPC as auxiliary voltage balancing circuit [157]; (**c**) 4-level two-quadrant DC–DC converter [158]; (**d**) two-stage configuration. DC–DC converter to balance the DC-link voltages from the unbalanced voltages of the photovoltaic panels [45].

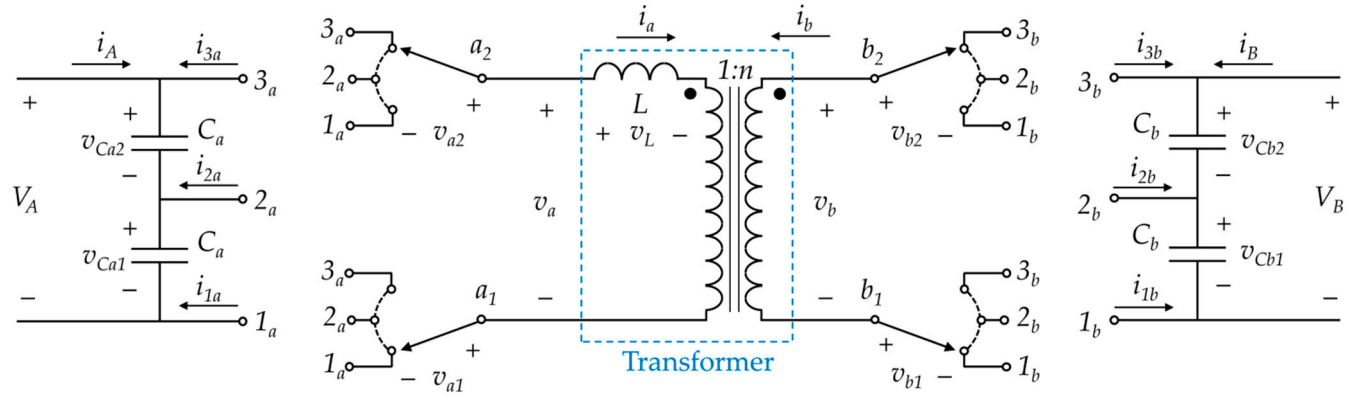
7. Balance in DC–DC Conversion

Although multilevel NPC converters are applied in most cases in DC–AC conversion, there are a small number of applications in DC–DC conversion. Obviously, since the modulations for DC–DC conversion are different from those in DC–AC conversion, the DC-link capacitor voltage balance issue must be addressed in a different manner.

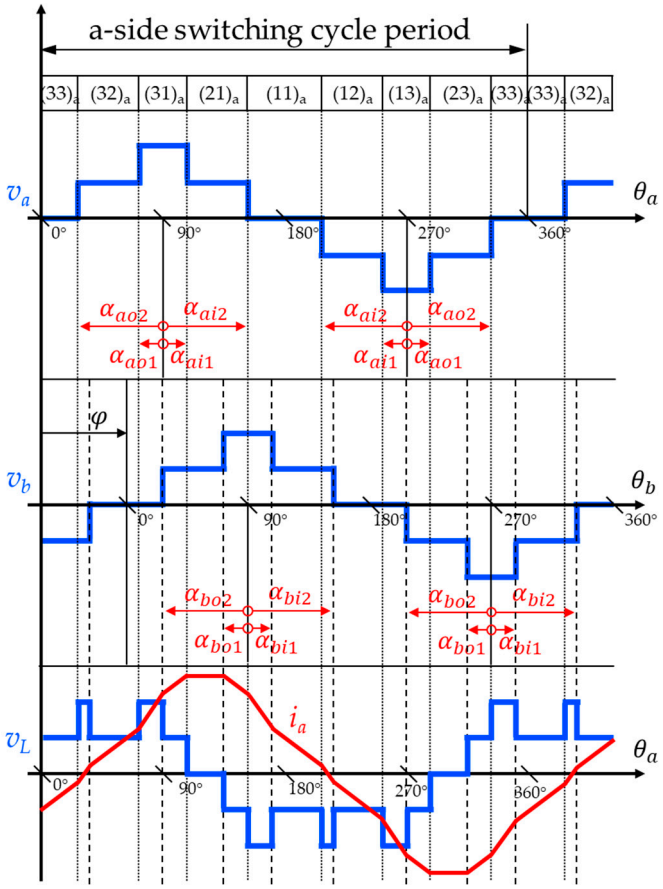
A bidirectional multilevel DC–DC converter implemented with a back-to-back *n*-level ANPC structure [21] is presented in [79]. The modulation is similar to that of the quasi two-state mode [148], which assures the balance in every switching cycle. However, to guarantee the voltage balance under non-ideal operations, duty ratios are slightly modified by the closed-loop balance control method in [124].

In recent years, interest in the dual active bridge (DAB) converter has grown. The DAB converter features galvanic isolation and bidirectional power transfer capability; thus

it is a suitable DC–DC conversion topology for solid state transformers or battery chargers. Moreover, the increasing power levels of these applications can be managed by a multilevel DAB. An illustrative example is found in [163], where a single-phase 3-level NPC DAB is presented. The topology and the switching strategy are shown in Figure 17a,b, respectively. The power flow is regulated by means of the phase shift φ between v_a and v_b, and the full bridges on each side of the converter have four degrees of freedom.



(**a**)



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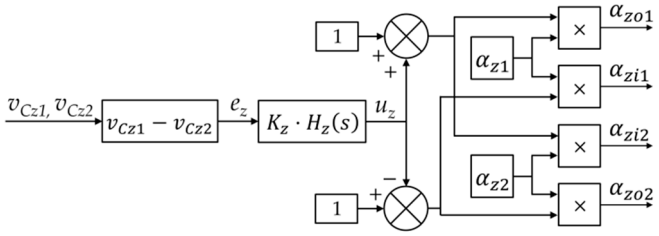

(**c**)

Figure 17. Three-level DAB DC–DC converter [163]: (**a**) Topology with phase legs a_1, a_2, b_1, and b_2 depicted as single-pole triple-throw switches; (**b**) voltage waveforms v_a, v_b, and v_L, and current waveform i_a for the proposed modulation. The switching states for a-side are shown on top of the figure. All waveforms are plotted assuming $V_A = V_B/n$. (**c**) Control scheme for the capacitor voltage balancing.

Two out of the four degrees of freedom affect the capacitor voltage balancing and are reserved for the capacitor voltage balancing control. The remaining two degrees of freedom can be used to optimize the converter performance. Figure 17c shows the proposed control scheme for the capacitor voltage balancing [163]. This control scheme modifies the quarter-wave symmetry switching angles (α_{Z1}, α_{Z2}), obtained considering balanced DC-link voltages, from the imbalance error variable and a compensator. That is, imbalance is corrected by slightly modifying the position of the switching angles to inject or draw current from the DC-link neutral point. This imbalance correction method is applied to single-phase DAB with 3-level [164,165], 4-level [166], n-level [81,167], and three-phase 3-level DAB [168]. A different balancing method is found in [169,170] for a single-phase 3-level DAB, where different switching sequences are applied in each switching period to inject or draw current from the DC-link neutral point, depending on the sign of the DC-link voltage imbalance.

8. Converter Operation beyond Balance

NPC multilevel converters were originally intended for high-voltage and power applications. In this context, DC-link voltage imbalance is not acceptable, since some semiconductor devices have to block an excessive voltage which can lead to a semiconductor failure. However, over the years, the field of application of the NPC multilevel converters has progressively expanded to medium- and low-voltage and power applications, mainly to take advantage of the better waveform quality. Therefore, while working with smaller voltages, the semiconductor devices can bear the different blocking voltages caused by the DC-link voltage imbalance, and the converter is able to operate with this voltage unbalanced condition.

Since unbalanced DC-link capacitor voltages can lead to output voltage distortion, modulations must consider the imbalance to provide undistorted output voltage, as, for instance, for 3-level NPC, carrier-based PWM [171], SVM [172], and VV–SVM [173], among others.

In photovoltaic power systems, the use of multilevel NPC converters, as shown in Figure 18 [32], allows the independent control of the voltage of each photovoltaic array v_{PVi}, such that each photovoltaic array operates at its specific maximum power point. In comparison to a conventional 2-level inverter, this approach is able to maximize the power obtained from the photovoltaic arrays. Although the DC-link capacitor voltages are different to extract the maximum power from each photovoltaic array, with a proper modulation [106], the system in Figure 18 delivers symmetrical and balanced three-phase output currents without low-frequency distortion. A similar implementation is found in [174] and also for a photovoltaic and battery hybrid system [175].

In conventional 2-level inverters with batteries, since the battery modules are series connected, when one of the battery modules is fully discharged, all the series-connected battery modules must stop working to avoid damaging this module. The application of multilevel NPC converters to battery management is shown in Figure 19 [33]. This converter structure allows individual control of the charging/discharging of each battery module. Since the battery modules are not identical, the charges of different battery modules will eventually be different from each other. Therefore, with this individual control, the current of each battery module is controlled to equalize the state of charge of the battery modules. For instance, considering a discharge, all the battery modules are discharged but keeping the same state of charge at all times. Hence, all the battery modules will reach the fully discharged condition at the same time. In comparison to a conventional 2-level system, the system operation can be significantly extended [33].

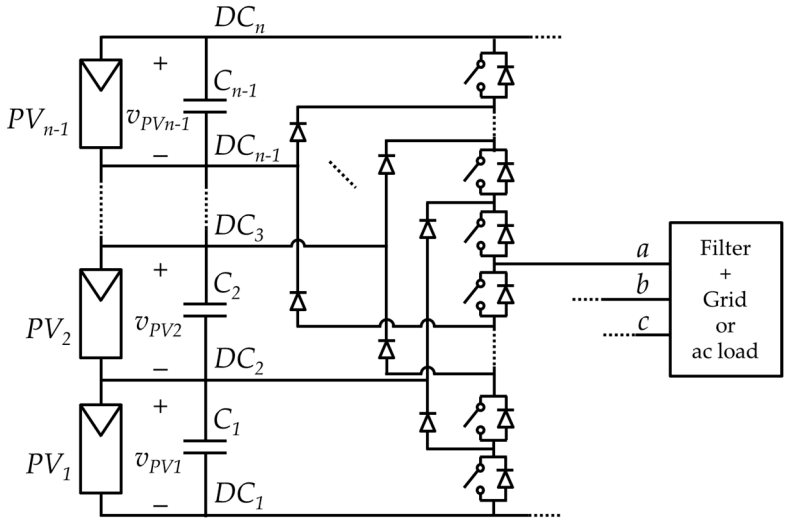

Figure 18. Connection of $(n-1)$ series-connected photovoltaic arrays to the grid (or AC load) through a n-level three-phase NPC inverter.

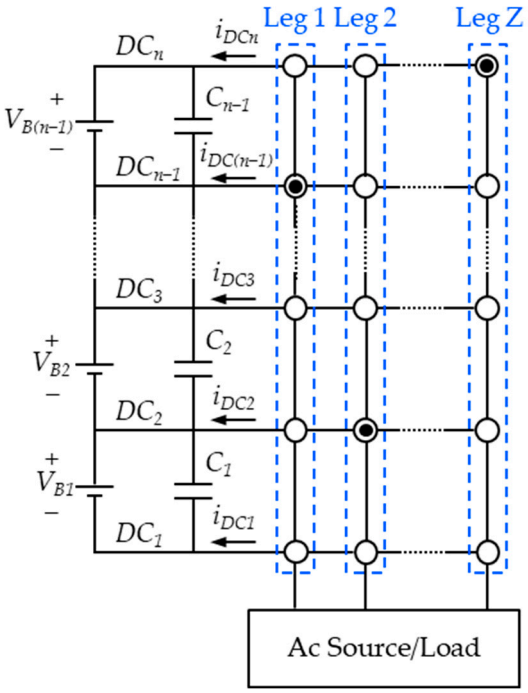

Figure 19. Functional schematic of an n-level Z-leg NPC DC–AC converter fed by $(n-1)$ batteries on the DC side and connected to a generic Z-phase source or load on the AC side. Each leg is represented as a single-pole n-throw switch. The switch position is indicated by a solid circle.

Finally, DC-link voltage unbalanced operation is also found for a single-phase 4-level NPC inverter [161] and for an asymmetrical DC-link voltage formed by a supercapacitor and a battery [176].

9. Conclusions

This paper presents a review of the state of the art of the control methods of the capacitor voltages in NPC multilevel converters. A summary of these methods is found in Table 1.

Table 1. Summary of methods.

Open-Loop Methods				
• No variable is fed back. • Typically not enough to keep balance because of non-idealities or perturbations.				
Conventional PWM/SVM	*VV-SVM*	*Carrier-overlapped PWM*	*Hybrid modulations*	*Self-balancing*
+ Lower number of commutations per switching cycle than other alternatives. − Balance in every switching cycle not possible for high values of m; the limit depends on the load power factor. − For more than three levels, in the region where balancing is not possible, capacitor voltages collapse.	+ Balance in every switching cycle under all operating conditions. + Lower required capacitance than with alternative modulations. − Higher number of commutations per switching cycle than other alternatives.	+ Balance in every line cycle. + Lower number of commutations than VV–SVM. − Higher required capacitance than VV–SVM. − Higher number of commutations than conventional PWM/SVM.	• The applied modulation is selected depending on m. + Takes advantage of the benefits of each modulation in each operating region. − Increased complexity compared to other alternatives.	• It is a "do-nothing" method. − Balance only for the 3-level case with restricted operating conditions and small disturbances.
Closed-Loop Methods				
• DC-link capacitor voltages are fed back (currents are also fed back in a few cases).				
Modification of modulating signals	*Selection of redundant vectors*		*Modification of switching angles*	*Predictive Control*
• Applicable to carrier-based PWM strategies with one or more modulating signals per phase. The modification typically represents the introduction of a zero-sequence voltage. + Simple. − Effectiveness limited by the inherent limitations of the employed PWM strategy.	• In SVM strategies, the proper redundant vector is selected or the share of redundant vectors is modified to correct the imbalance. This implies the introduction of a zero-sequence voltage. + Computationally intensive. − Effectiveness limited by the inherent limitations of the employed SVM strategy.		• In programmed PWM strategies, the switching angles are modified to correct the imbalance. + Simple. − Introduction of low-frequency distortion in the synthesized AC voltage while modifying the switching angles.	+ Balance in all operating regions. − Typically, introduces variable switching frequency and spread harmonic spectrum. − Significant computation burden for high number of levels.
Hardware Methods				
• Extra hardware added to the NPC converter to guarantee a balanced operation. + Provides robust balance, uncoupled from the NPC converter operation. − Reduces the overall efficiency and introduces significantly higher cost and complexity.				
Separate DC sources	*Auxiliary balancing circuit*		*Back-to-back*	
• Use of independent $n-1$ DC voltage sources, typically generated through a power converter.	• Additional dedicated circuit connected at the DC side or AC side to aid in the redistribution of the DC-link capacitor bank energy.		• Two DC–AC converters connected back-to-back where each converter counteracts the effect of the other converter on the balance.	
DC-DC Conversion				
• DC–DC conversion can be implemented with NPC multilevel converters.				
Back-to-back structure			*Dual-active Bridge*	
+ Bidirectional power flow. + Full balance control. − Limited range of voltage conversion ratios. − No galvanic isolation.			+ Bidirectional power flow. + Full balance control. + Galvanic isolation. − Higher hardware complexity than in the back-to-back structure.	
Operation beyond balance				
• Operation of NPC multilevel converters under DC-link capacitor voltage unbalance is feasible. • This feature can be used to improve the system performance in some applications.				
Photovoltaic power systems			*Battery powered systems*	
+ Independent control of the voltage of each photovoltaic array. + Maximum power extracted from each photovoltaic array, despite different panel conditions and irradiation levels. + Increased total power extraction.			+ Independent control of each battery module current. + Balancing of the state of charge of each battery module, despite different state-of-health and loading. + Extended battery range.	

A brief description of the converter operation, topologies, and modulations has been presented, prior to the analysis of the capacitor voltage balance issue. The DC-link capacitor voltages are regulated by controlling the DC-link neutral-point currents. This control can be achieved basically by means of a proper selection of the switching states of the converter.

Among the many open-loop modulations to keep the balance, the virtual-vector space-vector modulation is a robust option, since it allows keeping the balance within every switching period, for all operating conditions, although at the cost of a higher number of commutations. However, converter non-idealities can introduce deviations in the open-loop modulation performance and can lead to imbalance. Therefore, the use of a closed-loop balancing method becomes essential in most cases.

The injection of zero-sequence voltage to the open-loop modulation, based on the feedback of the DC-link voltages, is the most usual closed-loop control method. With this strategy, the DC-link neutral-point currents are regulated to adjust the DC-link voltages, both to keep the balance or to set the DC-link capacitor voltages to the desired reference value.

Balance can also be achieved with hardware methods, by means of an external circuitry added to the converter to keep the balance. However, it is preferred to avoid these hardware methods since they introduce higher complexity and cost.

Balance in DC–DC conversion has also been considered, in particular, the multilevel NPC-DAB converter.

Some applications, such as photovoltaic generation, can benefit from working with different DC-link capacitor voltages. This can be implemented with the multilevel NPC converters. In this case, the goal is not to keep the balance but to control each DC-link capacitor voltage to the desired reference value through the proper control of the DC-link neutral-point currents.

Similarly, in battery powered systems, a multilevel NPC converter can enable the independent control of the current of each battery module in a DC-link formed by a series connection of battery modules, with the ultimate goal to achieve an equal state-of-charge of all battery modules. This control is possible, again, through the proper control of the neutral-point currents.

Finally, it is worth highlighting that there are many available options to solve the problem of the balance or regulation of the DC-link capacitor voltages in multilevel NPC converters. At present, since the balance can be assured, the challenge lies more in improving the converter operation by reducing harmonic distortion or increasing efficiency, among others.

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Abbreviations

ANPC	Active neutral-point-clamped converter
DAB	Dual active nridge
DPC	Direct power control
DTC	Direct torque control
FPGA	Field programmable gate array
MPC	Model predictive control
NPC	Neutral-point-clamped converter
NTV-SVM	Nearest-three-vectors SVM
PI	Proportional-integral controller
PID	Proportional-integral-derivative controller
PWM	Pulse width modulation
SHE	Selective harmonic elimination
SVM	Space vector modulation
VV-SVM	Virtual-vector SVM
3D-SVM	Three-dimensional SVM

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