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# A Survey on Reduced Switch Count Multilevel Inverters

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**ABSTRACT** An efficient and cost-effective power converter is a pre-requisite for the modern power applications. With the evolvement of matured medium power self-commutated switching devices, multilevel inverters (MLIs) are emerged as a promising solution for high-power medium-voltage applications. Though, MLIs are performing a promising role in industrial applications, their high device count, size, cost and control complexities have restricted their market penetration. To address the disadvantages of MLIs, researchers are continuously contributing to new generation topologies under the name of reduced switch count (RSC) MLIs. From the past decade, numerous RSC-MLIs topologies have been reported for various applications. Therefore, this paper presents a comprehensive review and classification of RSC-MLI topologies, in terms of their structure, features, limitations, suitability and selection for specific applications.

**INDEX TERMS** Power converters, multilevel inverters, reduced switch count.

## I. INTRODUCTION

The idea of reducing the switch count in inverters was originated in 1996 by proposing a low power bidirectional dc-link inverters with a total of eight switches for motor drive application [1]. However, the continuous evolution of high-performance semiconductor devices has motivated the creation of various research trends in inverters, such as multilevel inverters (MLIs) [2]–[7]. The MLIs use the concept of aggregating multiple small voltage levels to synthesize a stepped output voltage waveform, which turns out to be an attractive solution for high-power, medium-voltage applications [8]. Lower total harmonic distortion (THD), reduced stress on switches, reduced $dv/dt$, lower $di/dt$ and reduced electromagnetic interference (EMI) are the prime advantages of MLIs [2]–[4]. Thus, MLIs are proven to be a matured technology for various commercial and customized products for a wide power range of applications such as high-voltage direct-current (HVDC) transmission, flexible ac transmission systems (FACTS), adjustable speed drives (ASD), active front-end converters (AFC), custom power devices (CPD), battery energy storage systems (BESS), electric vehicles (EV) and renewable energy generation (REG) [4]–[6], [9]–[17]. Among the topologies of MLIs, diode clamped (DCMLI) [4], [6], [16]–[19], flying capacitor (FCMLI) [5], [20]–[24] and cascade H-bridge (CHB) [4], [11], [14], [15], [21], [25], [26] are most popular and termed as classical MLIs. Even though, these topologies have gathered a great attention both from academia and industry, their practical implementation is heavily influenced by the application, control complexity and cost.

The main drawback of the DCMLI is its unequal loss distribution which further leads to uneven distribution of junction temperature and impart the limitations on maximum power rating, output current, and switching frequency of the inverter [4], [19]. This unequal loss distribution can be substantially improved by replacing the clamping diodes with active switches and thus, this inverter configuration is known as active neutral point clamped (ANPC) [19]. However, the advantages with ANPC comes at the expense of more complex circuit and the need to control the additional switching devices. The requirement of large number of capacitors and their pre-charge circuit limits the use of FCMLI in traction drives only [5]. On the other hand, modular structure and

fault tolerant ability of CHB turns out to be a sounding solution for applications such as FACTS, HVDC, CPD, EV and REG. Cascaded family of inverters are also characterized by cascade connection of modular chopper cells to form each cluster/phase-leg/arm. Cascaded MLI with H-bridge cells is known as cascaded H-bridge (CHB) MLI. Whereas, cascaded MLI composed with bi-directional chopper cells are known as modular multilevel inverters (MMI). However, the common concepts hidden among the family members allow to use the common term modular multilevel cascade inverter (MMCI) as a family name [15], [27]. Although, these topologies are scalable and suitable for high power applications but the requirement of isolated dc sources has limited their usage to active power transfer applications such as FACTS and HVDC [11].

The switch count of these MLIs increases with the number of levels. An increase in switch count involves additional drivers, band-circuits, isolation circuits and their associated heat sinks and protection requirements [28]–[31]. Moreover, increased switch count further increases computational burden on the controller. Thus, the size, cost and complexity of classical MLIs increase at higher levels, making the overall inverter expensive and imposing limitations on practical implementation and market penetration [29]. The reliability and losses in the conventional MLIs can be improved by incorporating a Z-source network, popularly known as Z-source inverters (ZSI) [32], [33]. These ZSIs operate in single buck-boost mode with fewer number of components and no dead time requirement [34], however, the size of Z-source network, possible EMI and limited modularity restricted their penetration in high-power applications.

Hence, researchers continued to explore and evolve newer topologies by making more or less changes to the classical MLIs. Thus emerged, asymmetrical CHB configuration to increase the number of levels with significant reduction in switch count [11] and other modified configurations to improve the performance of classical MLIs [19], [35]–[42]. However, control complexity, unequal device blocking voltages and limited switching redundancies of these configurations limited the fault tolerant ability, utilization of dc-sources, and even power distribution [29]. On the other hand, the increased component count of power semiconductor devices and capacitor/dc sources of classical MLI topologies has triggered the researchers to come up with newer topologies with reduced size and cost. Thus, MLI with reduced device count originated and this domain of MLIs has been called reduced switch count (RSC) MLIs [43]. From the past decade, various enthusiasts carried out extreme research on RSC-MLIs and developed numerous topologies with significant reduction in component count, total blocking voltage, cost and ease of control.

In recent years, several review papers on RSC-MLIs have been reported. In [44], RSC-MLIs are divided into unipolar and bipolar topologies and further classified into series, parallel and mixed connection of submodules. In this classification, only five different submodules are considered. In [45], recently developed RSC-MLIs for renewable energy integration and drives application are discussed. However, the topologies are summarized based on three categories, i.e., symmetrical, asymmetrical, and modified. In [46], another classification of RSC-MLIs topologies is presented based on number of phases, presence of transformer, number of dc sources, and voltage ratio of dc sources. On the other hand, in the proposed paper the categorization is carried out by considering either the motivating factors behind the development of the topology or its key contributing features. Based on this, the topologies are classified as generalized, stacked, unit based, switched capacitor, transformer based, and three-phase topologies. In this context, the qualitative and quantitative features of topologies of RSC-MLI have been discussed in this paper. Also, a comparison has been made among all the reported topologies in-terms of their structural and operational features such as device count, device ratings, device blocking voltages, power distribution, redundant switching states, utilization of input dc-sources, modularity, fault tolerant ability and generalization to higher levels. This facilitates selection of a well-informed topology for any given application.

The structure of this paper is as follows. Section-II presents a detailed report on RSC-MLIs, starting from the various factors considered for developing an RSC-MLI and classification of RSC-MLIs topologies. Section-III presents detailed features of each reported RSC-MLI topology. Further, a comparison of reported topologies is given in Section-IV. Finally, future trends and conclusions of the paper are given in Section-V and VI.

## II. RSC-MLI: BACKGROUND

The objective of RSC-MLIs is to overcome the limitations of classical MLIs in terms of their size and complexity. However, the changes in their topological arrangement affect their structural and operational features such as device blocking voltages, switching redundancies, device ratings, utilization of dc-sources, charge balancing of dc-link capacitors, power distribution, modularity, generalization to higher levels, switching operation and fault tolerant ability.

### A. MOTIVATIONAL FACTORS

Researchers often consider one or more features mentioned below as a motivation factor behind developing a new RSC-MLI topology. The main features are listed as follows.

- **Device count:** To develop the topology with appreciable reduction in device (switches/diodes/capacitors/dc-sources) count.
- **Device blocking voltages/ratings:** To develop the topology, involving identical device ratings and producing minimum device blocking voltages. For a topology, the total sum of the voltage blocking capability requirement for all its power switches is referred to as total standing voltage (TSV) or total voltage blocking capability of inverter [43].
- **Modularity:** Topologies with modular structure can easily be extended to higher levels.

- **Fault tolerant ability:** Fault tolerant ability enables the inverter to withstand abnormal working conditions such as faults on switching devices or dc sources, ensuring reliability with balanced operation.
- **Even power distribution:** Ability of the inverter to obtain required phase-voltage levels by distributing uniform power across all basic units/H-bridges. This feature contributes to charge balance among dc link voltages.
- **Requirement and Utilization of dc-sources:** Equal utilization of dc sources to contribute to natural balancing of dc-link voltages in closed loop applications. Reduction in the requirements of dc sources increased the role of capacitors and thus emerged self-balancing and voltage boosting topologies.
- **Application area:** As the features of RSC-MLI vary with topological arrangement, there exists no specific topology, which can be absolutely advantageous in any sort of application. Hence, a critical analysis is carried out among the newly developed topologies in finding out its best application in the areas such as FACTS, HVDC, CPD, BESS, ASD, IPQC, EV and consumer electronics.

### *B. CLASSIFICATION*

The interconnection of the switching devices, dc link voltages, diodes and other auxiliary components in a topology, can be arranged in any of the physical pattern such as ladder, staircase, column, U-shaped, cascade structure and even sometimes may not have any specific layout. Thus, considering the topological and operational features, developed RSC-MLIs can be classified as follows.

- ***Modular topologies*:** Topologies which can be extended to higher levels without affecting the device ratings are called modular configuration. Presence of modularity increases the ease in extending the topology to higher levels.
- ***Unit based configurations*:** Topology that can be scalable for any level in phase-voltage termed as generalized configuration. On the other hand, if the topology is designed for obtaining a fixed number of output voltage levels, then it is known as Unit based configuration.
- ***Half-bridge (chopper) cell-based topologies*:** To preserve modularity, most of the RSC-MLI's incorporate a half-bridge cell as a basic building block. Chopper units producing a two-level voltage i.e., $E$ or 0, are further connected in series, parallel, cascade as per the desired output voltage of RSC-MLI.
- ***Topologies with H-bridge/HSC structure*:** To avail the benefits of classical H-bridge, multiple topologies are reported by integrating H-bridge with multiple modular/non-modular units. On the other hand, to permit the topology produce output for multiple switching combinations, few topologies involve hexagon switched cell (HSC) structure.
- ***Topologies with bi-directional switching devices*:** Several RSC-MLI topologies have been reported with bi-directional switching devices to clamp the midpoint of dc sources. A discrete semiconductor devices are incorporated to construct a switch with bi-directional voltage blocking and current conducting capability or a reverse blocking insulated gate bipolar transistor (RBIGBT) is used [47].
- ***Symmetrical/Asymmetrical topologies:*** Most often MLIs incorporate symmetrical sources (in terms of magnitude) in the input (dc-link), and can be called as symmetrical topologies. However to increase the number of levels without increasing the device count, asymmetrical topologies are preferred [11]. These topologies incorporate unequal ratio of sources in the input (dc-link), and attempts to produce output voltage for their possible additive and subtractive combinations. The dc-voltage ratios of sources can either be in geometric progression (GP) or arithmetic progression (AP), but to obtain effective reduction in device count, GP with common ratio of two (binary) or three (trinary) is preferred. Operation with trinary voltage ratios is feasible if the topology has the ability to facilitate output for all the additive and subtractive combinations of input dc voltages. The reduced device count of these configurations decreases the inverter size but increase the device blocking voltages/ratings, limits switching redundancies, restricts fault tolerant ability, limits capacitor voltage balancing and produces non-uniform power distribution among basic units.
- ***Topologies with even power distribution***: Even power distribution is a feature of control aspect. This phenomenon is also referred as charge balance control or equal utilization of dc-sources. To achieve this, the topological switching operation is carried out in a way, that the average current consumed from each of the sources is equal, which makes the average powers equal. In other way, for a given topology, even power distribution or even load sharing is possible only, if all the input sources contribute equally towards the output voltage.
- ***Topologies with equal blocking voltages*:** Reduction in switch count of RSC-MLIs has modified their topological arrangement, which in turn modified the interconnection of switching devices and input dc-sources (or capacitors). This impacted the voltage rating/stress of the switching devices, such that they may encounter unequal blocking voltages. Thus, considering the device blocking voltages, RSC-MLI can be classified into topologies with even and uneven blocking voltages.
- ***Topologies with fault tolerant ability***: Reliability of an inverter is ensured by its fault tolerant ability. Reduced device count of RSC-MLI's drastically restricted the switching redundancies, which provides an alternate path for the faulty switch and play a vital role in inverter reconfiguration. Thus, prominence of RSC-MLIs for industrial and domestic applications demands the topologies with fault tolerant ability.

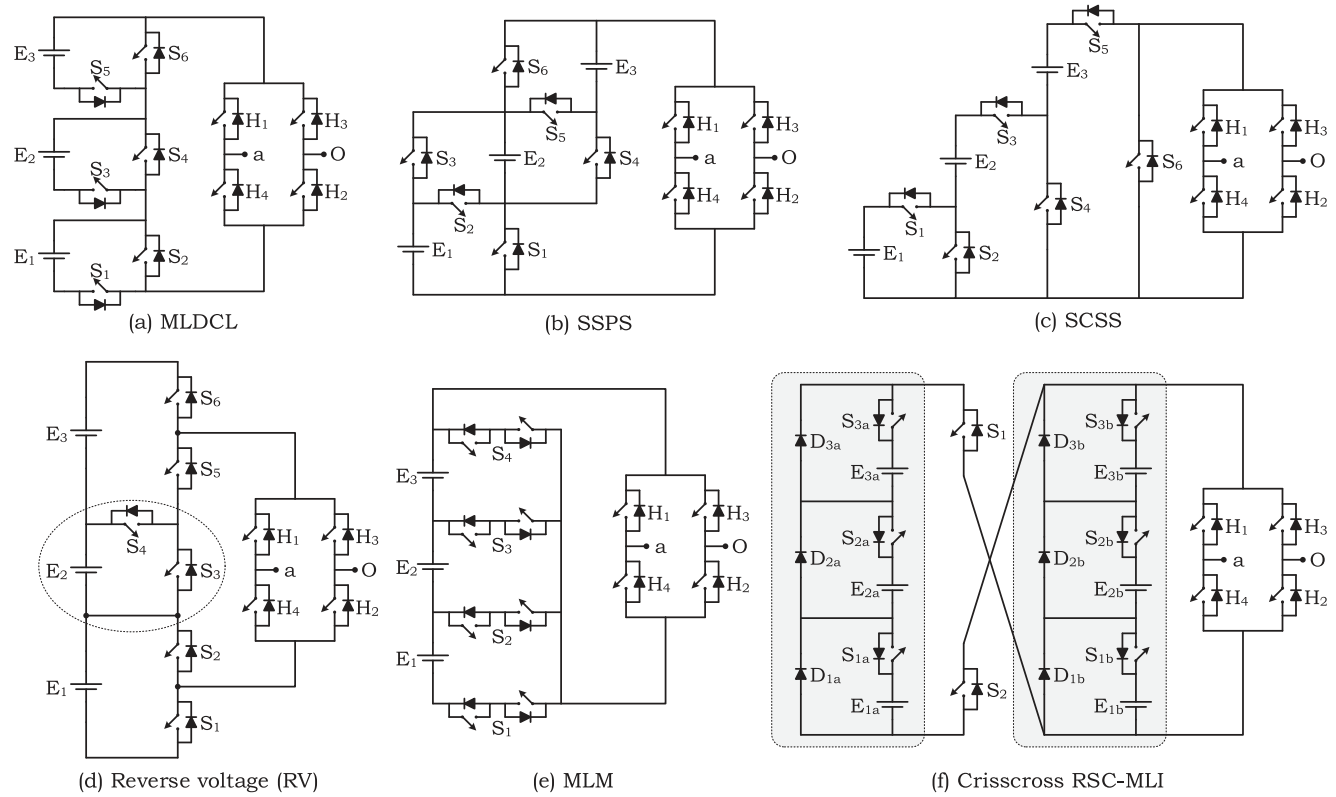



**FIGURE 1.** Topologies with separate level and polarity generators.

### C. CATEGORIES

Considering the above classification, the reported RSC-MLI topologies can be categorized as shown in Table 1. It is to be noted that, this categorization is carried out by considering either the motivating factors behind the development of the topology or its key contributing features.

## III. RSC-MLI TOPOLOGIES AND FEATURES

The physical structure, operational features, merits, limitations and suitable applications of these topologies shown in Table 1 are explained in this section.

### A. GENERALIZED RSC-MLI TOPOLOGIES

Considering the similarities in physical structure and type of the switching devices incorporated, the topologies listed under generalized RSC-MLI can further be classified as follows

#### 1) TOPOLOGIES WITH SEPARATE LEVEL AND POLARITY GENERATOR

Most of the RSC-MLI possess the topological arrangements that produce odd number of phase-voltage levels with separate polarity and level generators. Among these, the popular configurations are multilevel dc-link (MLDCL) [48], [49], switched series parallel sources (SSPS) [50], [51], reverse voltage (RV) [52], [53], series connected switched sources (SCSS) [54], [55], multilevel module (MLM) [56] and crisscross (CC) [57]. Per-phase structures of these configurations with three dc sources are shown in Fig. 1. The level generator in these structures consists of series connection of several basic units. Each basic unit consists of a half-bridge or chopper-cell with an isolated dc source. In case of MLM, the level generator consists of bidirectional switches. For MLDCL and SSPS topologies, the switches in the level generator operates with uniform voltage stress and equal device blocking voltages. In case of RV, SCSS and MLM the voltage stress increases with addition of new basic unit. However, in all these topologies, the blocking voltage of each device in polarity generator is equal to the total dc link voltage. All these topologies support both symmetrical and asymmetrical configurations except SCSS and MLM. However, their inability to synthesize output voltage for subtractive combination of dc-sources limits their asymmetric ability for trinary voltage ratios. The modular and redundant structure of MLDCL allows to tolerate multiple open-circuit (OC) faults on certain devices in level generator [141]. In [142], a modified MLDCL configuration is reported for grid integrated PV system by replacing by-pass switches in the level generator of MLDCL with diodes. Though, this modification reduced the device requirement, however, the main disadvantage for this solution is that it cannot inject reactive power into the grid.

In SSPS, the level generator cannot produce zero voltage and it is obtained from polarity generator. To obtain any positive or negative voltage level in SSPS shown in Fig. 1(b), only two devices in level generator are in conduction. With

**TABLE 1. Categorization of RSC-MLI Topologies**

- **Generalized RSC-MLIs:**
  - With separate level and polarity generators
    - Multilevel dc-link (MLDCL) [48, 49]
    - Switched series parallel sources (SSPS) [50, 51]
    - Reverse voltage (RV) [52, 53]
    - Series connected switched sources (SCSS) [54, 55]
    - Multilevel module (MLM) [56]
    - Crisscross switched (CCS) RSC-MLI [57]
    - A trinary asymmetric topology [58]
  - T-Type topologies
    - T-type [59-63] and Cascaded T-type [64]
    - Half-leg T-type RSC-MLI [59, 65, 66]
  - Topologies with Hexagon switched cell (HSC) structure
    - Hybrid T-type topologies [67-69]
      - Topology – I (bi-directional switch on one side of HSC) [67, 68]
      - Topology – II (bi-directional switch on both side of HSC) [67, 68]
      - Topology – III (bi-directional switches inside HSC) [69]
    - Extended HSC structures [70-72]
  - Topologies with ladder-based structures
    - Cascaded bi-polar switched cells (CBSC) [73]
    - Switched dc-sources (SDS) [74-76]
    - Packed U-cell (PUC) [43, 77]
- **Stacked topologies:**
  - Stacked configuration with level doubling network (LDN) [78-81]
    - CHB with LDN [78-80] and T-type with LDN [81]
  - Non-LDN based topologies [82-93]
    - Hybrid ANPC [82, 87-90]
    - HFC [91, 92]
    - T-type with cross connected modules (CCM) [93]
- **Unit-based MLIs:**
  - Basic unit topology [94]
  - Symmetrical unit-based topologies
    - Five-level topology [95]
    - Nine-level topology [96]
  - Asymmetrical unit-based topologies
    - Envelope (E-type) type [97]
    - Square T-type (ST-type) [98]
  - Compact module multilevel inverter [99]
  - HSC unit [100]
  - Extended HSC units
    - Topology–1 [28]
    - Topology–II [101]
    - Topology–III [71, 102]
  - Asymmetrical T-type topologies [103, 104]
    - Topology–1 [103]
    - Topology–1I [104]
- **Switched capacitor (SC) RSC-MLIs:**
  - Series/parallel based SC unit topologies
    - Topology-1: Basic SC unit [105]
    - Topology-1I: Modified SC unit [106]
  - FBC (full bridge cell) with inherent SC unit
    - Seven-level SC tripler topology [107, 108]
    - 13-level SC tripler plus doubler topology [109]
  - Switched capacitor cell (SCC) with half-bridge cells (HBC)[110, 111]
  - SC doubler topologies [112, 113]
  - Modified HSC based switched capacitor topology [114]
  - Modified T-type switched capacitor topologies
    - Topology–I (five-level T-type with one dc source) [115]
    - Topology–II (dual T-type) [116]
    - Topology–III (Seven-level boost topology) [117]
    - Topology–IV (Nine-level cross-connected boost topology) [118]
  - Single-stage switched-capacitor module ($S^3CM$) [119]
  - Seven-level SC module [120]
  - Nine-level quadruple boost inverter [121]
  - Hybrid SC: stacked configuration [122, 123]
  - Floating capacitor-based SC topologies [124-126]
    - Topology-1: Split capacitor or floating capacitor topology [124]
    - Topology-2: Switched capacitor-based boost topology [125]
    - Topology-3: Switched capacitor-based hybrid topology [126]
  - Multi-layered/stage topologies [127, 128]
    - Topology–1 [127]
    - Topology–II [128]
- **Transformer based RSC-MLIs:**
  - Transformer-based reduced components (TBRC) topologies [129-131]
  - Two-Phase five-level converter with Scott transformer [132, 133]
  - $H_4$-$H_6$ topology [134]
- **Three-phase topologies:**
  - Two-level inverter based topologies [135, 136]
  - Multilevel inverter-based topologies [137-140]

series/parallel operation, SSPS is operated in self-balancing mode, where one stiff dc link voltage is sufficient to charge all the dc link capacitors such that the output voltage is boosted, and number of levels are increased. This feature of SSPS is well suited for battery charging and energy storage applications [51]. Further, the series/parallel operation increases the utilization of dc sources, which is advantageous in grid-connected PV systems [143]. A further reduction in switch count and switching losses are possible with an addition of an H-bridge to SSPS RSC-MLI [50]. To minimize the switching losses, the additional H-bridge can be operated at carrier frequency and level generator at fundamental frequency. Motivated by series/parallel switching of SSPS, various asymmetrical stair-case topologies are reported in recent times to reduce dc sources [144]–[146]. Adapting minor modification in SSPS, a three-stair thirteen-level asymmetrical boost topology with voltage gain of two is reported in [144]. Similarly in [145], a nine-level self-balancing boost topology with a voltage gain of two is reported for high-frequency power distribution system application. A scalable asymmetric stair-case configuration involving both bi-directional and uni-directional switches is reported in [146]. Structurally, all these configurations resemble conventional SSPS, however offers more switching redundancies and increased voltage levels.

RV topology is also modular structure and can be extended to higher levels by duplicating the encircled middle stage of level generator shown in Fig. 1(d). In addition to the above configurations, a crisscross RSC-MLI configuration is reported in recent times, which also involves an H-bridge for polarity generation, and a crisscross two-string structure as level generator [57]. Each string structure consists of multiple half-bridge units connected in series, further both the strings are connected in crisscross pattern with a pair of unidirectional switches as shown in Fig. 1(f). Each half-bridge unit consists of a dc-source, a uni-directional switch and power diode, and can produce a voltage either $E$ or 0. This configuration is fault tolerant with possible even power distribution among dc sources and can operate with both symmetrical and asymmetrical voltage ratios. With $n$ number of symmetrical voltage sources per string, (i.e., $2n$ sources overall), CCS requires $(2n + 6)$ switches and obtains $(4n + 1)$ levels. For symmetrical configuration, rating of devices in semi-half bridge cells is equal to the magnitude of dc-source. However, the device blocking voltage of crisscross switches are higher (sum of the total dc-link of both strings). This topology can be extended either by increasing the submodules in each string or series connection of several crisscross two-string structures. A reduced switch count version of this topology is also proposed in [57] by replacing one of the string structure with a dc source.

The level generators of topologies shown in Fig. 1 can generate levels with additive combinations of dc sources only. However, the topology presented in [58] and shown in Fig. 2, can generate the output voltage waveform with additive and subtractive operation of input dc sources. Therefore, this

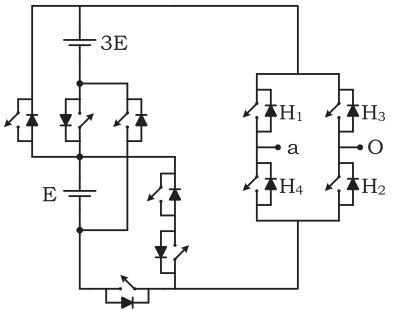



**FIGURE 2.** A trinary asymmetric separate level and polarity generator-based topology.

topology supports asymmetry with trinary voltage ratios in dc sources.

### 2) TOPOLOGIES WITH T-TYPE STRUCTURE

The topological structure where bi-directional switch interconnects multiple nodes of dc-link with phase-leg of full/half bridge on load side is called as T-type structure. These structures involve both uni and bi-directional switches. The popular configurations of the T-type topology with full bridge, cascaded and half-bridge structure are shown in Fig. 3 [59]–[63], [64], [147]. Among the three, T-type with full bridge structure is popular due to its simplified structure with appreciable reduction in switch count. However, each of them has their own merits and limitations and are explained in this section.

*i) T-type RSC-MLI:* This H-bridge based topology is proposed in 2006 [59]–[63]. The uni-directional switches are arranged to form an H-bridge and the mid-point of one phase-leg of H-bridge is connected to the dc link voltages through bi-directional switches. The switching devices in a phase-leg of an H-bridge to which the bi-directional switches are connected are operated at carrier frequency and the devices in the other phase-leg operate at modulating signal frequency. The per phase structure of T-type with three dc voltage sources is shown in Fig. 3(a). At any instant, only two devices are in conduction, which helps in reducing the conduction losses. This topology produces unequal device blocking voltages and the absence of redundancies limited this configuration to symmetrical only. This topology can be extended either by increasing the number of dc sources with bi-directional switches or by cascading several T-type modules [64]. The latter one creates switching redundancies and facilities to operate with asymmetrical voltage ratios. However, dc link voltages in an individual T-type module should be identical. Fig. 3(b) shows the cascaded T-type MLI with two five-level T-type modules.

*ii) Half-leg T-type RSC-MLI:* In half-bridge based T-type topology, the dc link is common to all the phases and each phase-leg is connected to the dc link through bi-directional switches [66], [147]. The structure of this topology for three-level is shown in Fig. 3(c). This can produce even and odd levels in phase-voltage and can be extended to higher levels by increasing the dc sources with bi-directional switches. In Fig. 3(c), two devices per leg are in conduction at any time and voltage rating of bi-directional switches is lower than the devices in phase-leg. Therefore, this configuration produces lower conduction losses and less total blocking voltage as compared to DCMLI and ANPC [19].

This topology is reported for various PV and grid connected applications [65]. Fault tolerant strategies and reconfiguration of this inverter for open-circuit switch faults is reported in [66]. This topology doesn't possess switching redundancies however, the charge balance among the dc link voltages can be obtained by equalizing the rate of charge over a fundamental cycle [59] or by involving sophisticated modulation techniques such as SVM.

### 3) TOPOLOGIES WITH HSC STRUCTURES

These topologies involve uni-directional switches to form a hexagon switch cell (HSC) structure and uses bi-directional switches to connect HSC to the dc link. This HSC structure permits the topology to operate with switching redundancies. However, depending on the arrangement of bi-directional switches and dc-link, there are various HSC based configurations reported.

*i) Topology – I (bi-directional switch on one side of HSC):* This configuration is hybrid connection of T-type with HSC and, thus can be called as hybrid T-type or improved T-type RSC-MLIs. The topological structure of this RSC-MLI with two stiff dc sources $E_S$ and $E_R$ on either side of HSC as shown in Fig. 4(a) [67], [68]. This topology can be extended by increasing the bi-directional switches or by cascading several modules. From Fig. 4(a), it is observed that, short circuiting uni-directional switches $H_5$ and $H_2$ and, open circuiting voltage source $E_R$, makes this topology identical to five-level T-type MLI. Thus, the addition of uni-directional switches modifies the H-bridge to HSC and, facilitates the topology to operate for asymmetrical configurations. Further, for $E_S = E_R$, the configuration operates as symmetrical and is asymmetrical if $E_S \neq E_R$. Symmetrical configuration of this topology with $n$ dc link capacitors can produce $(4n + 1)$ levels in phase-voltage. To operate the inverter for other voltage levels, asymmetrical configuration with appropriate voltage ratios should be selected. For instance, considering $E_S = E_R = 2E$ in Fig. 4(a), then capacitor voltages, $E_{C1} = E_{C2} = E_S/2 = E$ and the inverter operates for nine-level. If $E_S = 2E_R = 2E$, produces seven-level in phase-voltage with magnitude varying from $\pm 3E$. Further, switching operation of this topology with $E_S = \frac{2}{3}E_R = 2E$, produces eleven-levels.

*ii) Topology – II (bi-directional switch on both side of HSC):* This configuration is similar to Topology-I presented above, but interconnects both sides of HSC and dc links through bi-directional switches as shown in Fig. 4(b) [67], [68]. This topology resembles back-to-back connection of two half-leg T-type modules through a pair of uni-directional devices. This increases asymmetrical ability of the inverter and enables to obtain voltage levels with significant reduction in switch count. However, the remaining features and operation of this topology remains to be similar as Topology – I [67], [68], [148], [149].

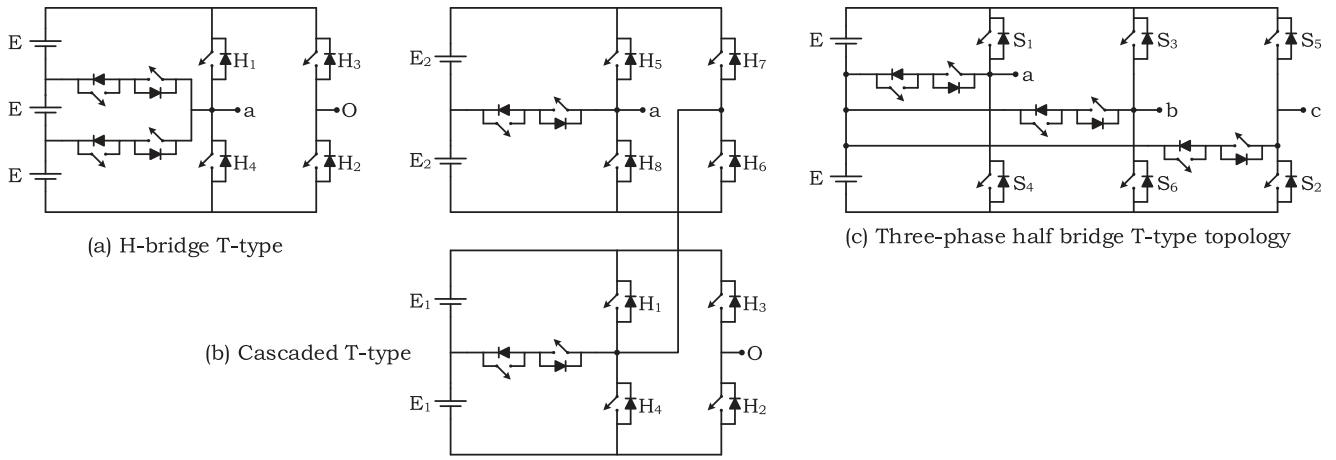



**FIGURE 3.** **Topologies with T-type structures.**

*iii) Topology – III (bi-directional switches inside HSC):* The topology shown in Fig. 4(c) is an extension of topology–II shown in Fig. 4(b) by connecting two cross-connected switches inside HSC [69]. Similar to Fig. 4(b), this configuration also produce a maximum output voltage of ($E_s$ + $E_R$). However, involvement of cross-connected switches increase the switching states and permit the configuration to produce output up to 25 switching combinations [69]. With symmetrical dc sources, most of these switching states have redundancies and produce nine-level output voltage, varying from +2$E$ to –2$E$ in steps of $E$/2. However, by selecting $E_S$ = $E$ and $E_R$ = 5$E$, this configuration can produce 25-level output voltage, varying from +6$E$ to –6$E$, with step-size of $E$/2. The TSV of this topology is 5($E_S$ + $E_R$) + 2 max($E_S$, $E_R$). This configuration is extended to higher levels either by cascading or by connecting additional dc-link capacitors with bi-directional switches in T-connection.

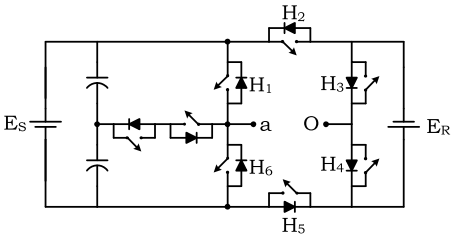
*iv) Extended HSC structures [70]–[72]:* The physical arrangement of these extended HSC structures are shown in Fig. 4(d) and (e), where the topology is valid for both symmetrical and asymmetrical configurations. In Fig. 4(d), for symmetrical configuration with $n$ dc sources involves $n$ bi-directional switches and six uni-directional switches to obtain (2$n$ + 1) levels in phase-voltage [70]. However, to work with asymmetrical configuration, the magnitude of the voltage sources multiplies through a factor of two and the maximum output voltage and the number of levels becomes equal to (2$n$ − 1)$E$ and (4$n$ − 1), respectively. By replacing the exterior bi-directional switches on either side of Fig. 4(d) with uni-directional switches, a modified configuration is reported in [72] and shown in Fig. 4(e). In addition to these, few other configurations are also reported, where the HSC is extended to higher levels by involving a nested structure as reported in [71].

### 4) *TOPOLOGIES WITH LADDER-BASED STRUCTURES*

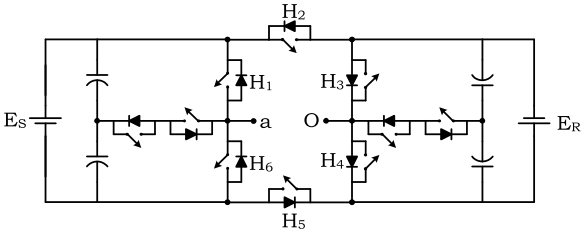
Few configurations possess ladder based physical arrangement with bi or uni-directional switches connected on either side of the dc-link. The popular configurations under this category are cascaded bi-polar switched cells (CBSC) [73], switched dc-sources (SDS) [74]–[76] and packed U-cell (PUC) [43], [77]. These configurations with three sources in dc-link are shown in Fig. 5. PUC and SDS uses uni-directional switches in their structure and CBSC is framed with bi-directional switches. The topological configuration of PUC is similar to SDS, however it includes few modifications in the arrangement of switches and dc voltage ratios [43], [77]. SDS is also known as cross-connected sources (CCS) RSC-MLI. In common, all of these configurations operate with limited redundancies with restricted fault tolerant ability and utilization of dc sources. The fault tolerant ability of SDS can be improved by connecting an additional cross switch between the dc-sources in every two U-cells [150]. This cross-connected switch facilitates fault tolerant ability by by-passing any faulty unit or dc source or a switch.

Unlike, SDS and PUC, CBSC involves a greater number of switches. However, the gate drivers are equal to the number of bi-directional switches. In addition, CBSC produces lower conduction losses as, at any instant, only two devices are in conduction. CBSC is extended to higher levels either by cascading or by connecting a pair of bi-directional switches with an additional voltage source.

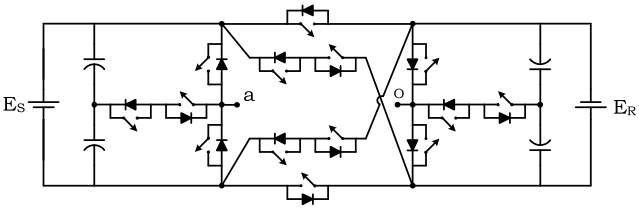
CBSC and SDS operates with unequal device blocking voltages, and valid for both symmetrical and asymmetrical configurations. However their in-ability to realize the output voltage for subtractive combination of dc-link voltage ratios has restricted their asymmetrical ability [73]. Unlike SDS and CBSC, PUC have uniform device blocking voltages. PUC operates for both additive and subtractive combinations of dc sources, however with symmetrical dc sources, the switching combinations of PUC cannot produce more than three-levels in phase-voltage. This is due to the consecutive addition and subtraction of dc voltages in switching path. Therefore, this topology is advantageous with asymmetrical dc sources. Further, on operating PUC with asymmetrical dc voltages, levels can be increased, however the magnitude of



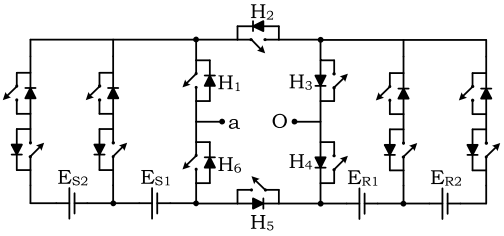

(a) Hybrid T-type MLI with bi-directional switch on one side of HSC.



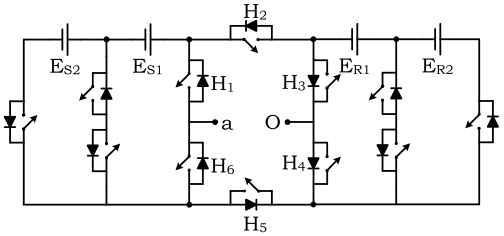

(b) Hybrid T-type MLI with bi-directional switch on both side of HSC.




(c) Hybrid T-type MLI with cross connected bi-directional switches inside HSC.




(d) Extended HSC topology reported in [70].




(e) Extended HSC topology reported in [72].

**FIGURE 4.** Hybrid T-type topologies and extended HSC structures.

the output voltage will always be less than the total dc input voltage.

A 49-level PUC is reported in [151], [152] by cascading two asymmetrical seven-level PUC units demonstrates the asymmetric ability of PUC. A ZPUC converter is reported in [153] to operate PUC with a single dc-link for both single-phase and three-phase systems. To achieve this, ZPUC involves an additional FC module in conventional PUC, however the operation and number of levels vary with the available redundancies. The unipolar voltage produced by each leg of ZPUC facilitates its scope in modular multilevel converters (MMC).

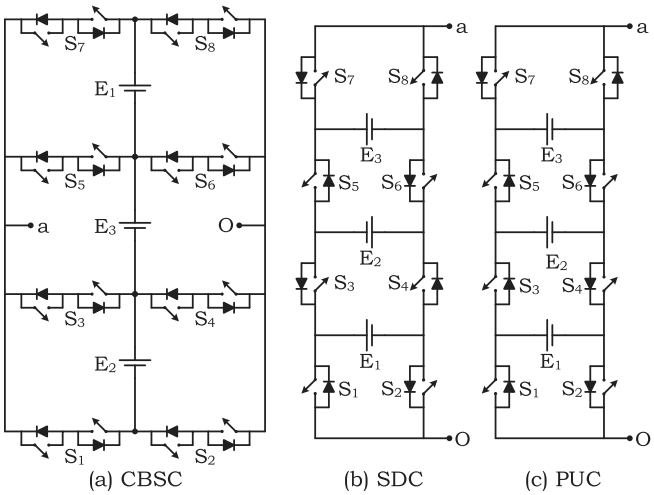



**FIGURE 5.** Topologies with ladder-based structures.

### B. STACKED TOPOLOGIES

These configurations are developed by interconnecting two or more inverter topologies. Similar concept was implemented in past to develop hybrid topologies from classical MLIs to reduce their switch count and address voltage balancing issues. If a stacked configuration is developed with two inverter configurations, one among them is termed as primary inverter (one with stiff dc source or larger dc bus voltage) and the other one is called as secondary inverter. In recent times, this concept of stacking is reported to develop asymmetrical configurations with effective voltage balancing capability. Such reported configurations are listed under this category [78]–[81].

#### 1) STACKED CONFIGURATION WITH LEVEL DOUBLING NETWORK (LDN)

LDN is a level doubling network used to effectively double the output voltage levels of a given topology by reducing their switch count and voltage balancing issues. LDN consists of a floating capacitor and complimentary pair of switching devices, and, is connected in cascade to the configuration whose levels need to be increased [79], [80].

Assuming $V_{LDN}$ is the dc-link voltage of LDN, then its corresponding output switches between $V_{LDN}$ and zero. If $V_{LDN}$ is exactly half of the dc bus voltage of the cascaded topology ($V_{HB}$), then the output voltage of the cascade combination ($V_o$) have fundamental component and odd harmonics only. The power delivered/absorbed by LDN in one half cycle will be compensated in the next half cycle. For suppose $V_{LDN} < V_{HB}/2$, then $V_o$ will have negative dc component which introduces negative dc component in the output current that will charge the LDN capacitor. Similarly, If $V_{LDN} > V_{HB}/2$, then $V_o$ will have positive dc component which introduces positive dc component in the output current that will discharge the LDN capacitor. This repetitive charging and discharging will take place until $V_{LDN} = V_{HB}/2$. Thus, LDN has self-balancing

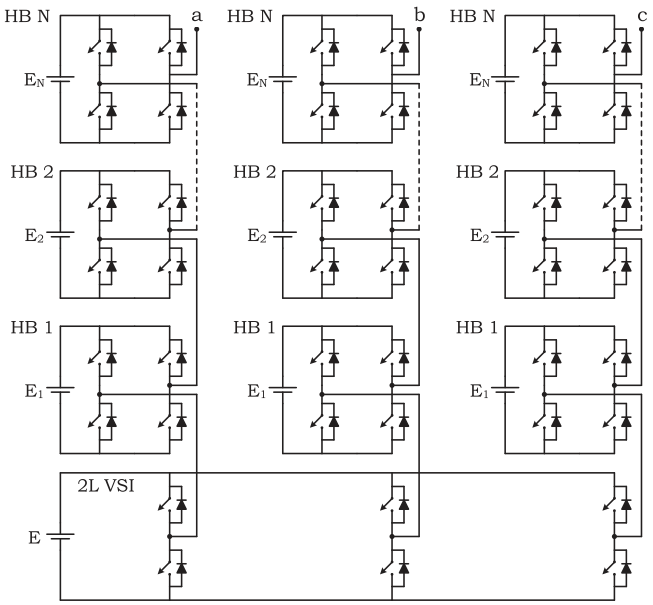



**FIGURE 6.** Stacking of two-level inverter with CHB [80].

capability in addition to doubling the number of levels of any MLI topology. However, the structure and control principle of LDN has limited the capacitor to have discharging operation in positive half-cycle and charging in negative half-cycle. This demands a higher value of capacitance to suppress the ripple-voltage in low-frequency drives. In case, if multiple LDNs are involved to a configuration whose dc-link voltage is $V_{HB}$, then only one among ($LDN_1$) them will directly charge to $V_{HB}/2$ from the $V_{HB}$, and $LDN_2$ will charge to $V_{LDN\,1}/2$ (i.e., $V_{HB}/2^2$) from $LDN_1$. This will continue until LDN charges to least voltage i.e., $V_{HB}/2^n$. This may result in loss of self-balancing ability for all LDNs except the one with lowest voltage. Under this condition, each LDN (except one with least voltage) requires a closed-loop voltage control or needs to be charged from an auxiliary dc source. In literature, this concept of LDN is well reported for both classical MLIs and RSC-MLI configurations.

LDN for symmetrical seven-level CHB MLI configuration to achieve an equivalent 13-level asymmetric topology is reported in [78], [80] and shown in Fig. 6. In this topology, the LDN has a three-leg structure with dc-link arrangement and is common to LDN of all phases. This configuration is similar to the hybrid configuration of seven-level CHB with two-level inverter [78], [80]. LDN maintains uniform loading among operating modules of the cascaded units, which significantly improves the power quality, reduces the switching frequency, as well as cost and size of the power filter. In [81], the concept of LDN incorporating stiff dc-sources both in LDN and *c*ascaded inverter, is extended to half-leg T-type RSC-MLI, thereby increasing its levels from four to seven. Similarly, with $n$ sources in dc-link this topology produces $(n + 1)$ uni-polar levels in pole-voltage. Further, the LDN converts this $(n + 1)$ level uni-polar voltage to $(2n + 1)$ level bi-polar voltage with magnitude varying from $+nE$ to $-nE$.

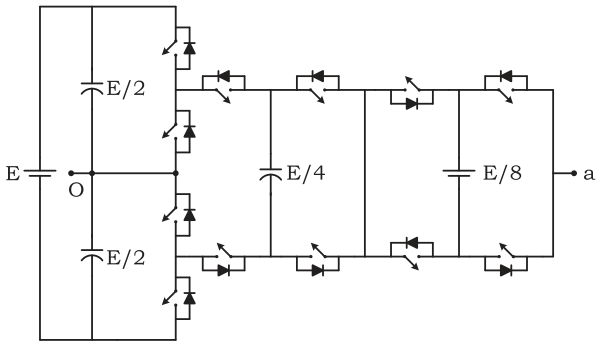



**FIGURE 7.** A hybrid 11-level configuration by stacking 5-level ANPC (primary) and FC module (secondary).

### 2) STACKED CONFIGURATION WITHOUT LDN

Stacked configuration of MLIs developed without involving LDN are listed under this category. In literature, hybrid MLI configurations are reported by stacking two or more inverter topologies by including more/less topological modifications. One such popular example is a nine-level RSC-MLI developed by stacking two five-level topologies, where each five-level inverter is framed by stacking a three-level FCMLI and a capacitor fed H-bridge inverter [86]. Motivated by [86], a 49-level asymmetrical RSC configuration is developed by stacking a 17-level asymmetrical configuration with various selector switches to produce a 49-level pole-voltage with step size of $E/96$ [87]. The 17-level asymmetrical configuration is framed by stacking a three-level FCMLI (primary inverter) with three H-bridge units (secondary inverter). The selector switches are operated at fundamental frequency. This arrangement of dc-link followed by selector switches remains in common to all phases, and a separate 17-level inverter is placed in each phase [87].

An alternative approach to arrange this 49-level configuration is also reported in [87], where the configuration is framed by stacking a nine-level FC unit (Primary inverter) with two H-bridge modules (secondary inverter). However dc-link of this arrangement involves six dc sources of each $E/12$, and multiple selector switches to interconnect the dc-link and the stacked inverter structure [87]. Motivated from concept of stacking, various other configurations are reported in literature. However only few of them possess simplified modular structure and turned to be attractive RSC-MLI configurations. Such popular stacked configurations are explained here under [84]–[93].

*i) Toplogy-1 (Hybrid ANPC configuration):* A hybrid 11-level RSC-MLI configuration developed by stacking 5-level ANPC (primary) and FC module (secondary) is reported in [82], [83] and shown in Fig. 7. In this configuration, ANPC module operates at fundamental frequency and FC module operates at carrier frequency. ANPC is a hybrid multilevel

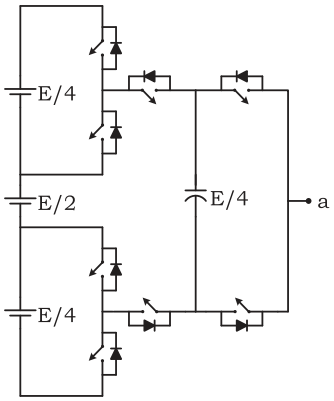



**FIGURE 8.** Five-level hybrid flying-capacitor (5L-HFC) inverter.

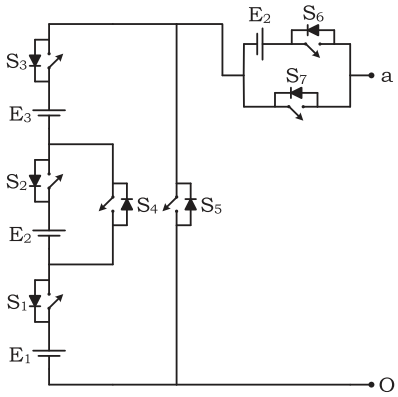



**FIGURE 9.** Basic unit RSC-MLI topology.

converter developed from NPC and FC converters. Thus, ANPC possesses robustness of NPC and flexibility of FC. Hence, advantages of both NPC and FC are incorporated into ANPC converter which enables it to be employed in many industrial applications. Most often ANPC is extended to higher levels by increasing FC units.

Compared with 5L-NPC and 5L-FC topologies, the cost and control complexity of the 5L-ANPC topology is reduced, since it requires only one FC per phase without any clamping diodes. Furthermore, the dc-link capacitor voltages can be self-balanced if passive front-end rectifiers are used. Due to these advantages 5L-ANPC inverters, has been used in industrial applications. Motivated by [82], a nine-level RSC-MLI developed by stacking a 5L-ANPC and a half-bridge are reported in [89], [90], where the half-bridge operates at line frequency to balance the dc-link voltages, irrespective to the modulation scheme.

*ii) Topology-2 (HFC configuration):* Motivated from ANPC [82], Fig. 8 shows a five-level HFC (hybrid flying capacitor) reported by stacking a three-level FC unit and two two-level converter units in [91], [92]. As compared to 5L-ANPC, the dc-link of this topology is divided into three series connected capacitors with middle-point connections. The top and bottom capacitor voltages are equal and, also half of the middle capacitor voltage. Therefore, the voltage rating of switching devices connected to the dc bus is decreased by a half as compared with 5L-ANPC.

Further, the loss distribution in 5L-HFC is improved as compared with 5L-ANPC. However, by splitting the dc-link into three series-connected capacitors, the 5L-HFC inverter suffers from voltage unbalance among the capacitors. This problem can be solved by using a chopper circuit comprising of active switches, inductors and a diode [92]. However, in back-to-back configuration systems, the voltage unbalance problem can be solved by modifying the modulation technique [92]. A similar topology for four-levels is presented in [52].

*iii)* Topology-3 *(T-type and cross-connected modules):* To address the high device count of classical MLIs, high device rating and voltage balancing issues of complicated topological structure of SC topologies, a modular RSC-MLI configuration is reported by stacking T-type and cross-connected module (CCM) [93]. The number of levels can be increased by connecting several cross modules. Features of this configuration are modularity, ability to extend to higher levels without increasing the ratings of circuit components and boosting the input voltage without requiring bulky inductors and transformers.

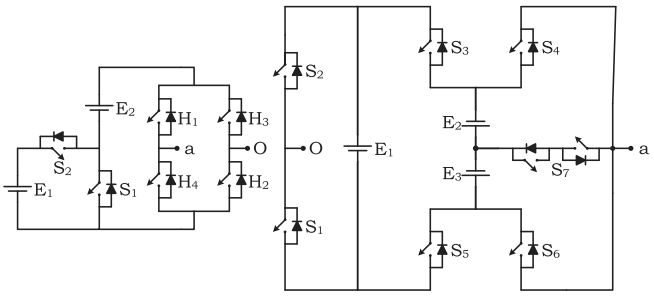
### C. UNIT-BASED RSC-MLIS

To simplify the topological size, cost and complexity, few authors reported sustainable topologies with extreme reduction in switch count, with respect to the classical MLIs. However, these topologies can produce only a finite number of levels in output voltage and doesn't have the feasibility to operate for a generalized level. In the other way, each building/basic unit of these configurations acts as an RSC-MLI with a fixed topological configuration and output voltage levels. Reviewing the topologies reported, the following are the unit-based configurations.

#### 1) BASIC UNIT RSC-MLI

This H-bridge based topology reported in 2015 [94], involves separate polarity and level generators. The topological arrangement of the basic unit RSC-MLI to obtain five-level unipolar voltage is shown in Fig. 9. The basic unit shown in Fig. 9 has two parts i.e., three-cell structure and single-cell structure. Three cell structure involves three voltage sources connected through five uni-directional switches and single cell structure consists of one voltage source and two uni-directional switches. The purpose of highlighted single-cell structure is to facilitate the voltage levels (missing levels in phase-voltage) that are not produced by three-cell structure. With symmetrical voltage ratios, level generator produces five-level unipolar voltage.

Processing the output of level generator through a polarity generator, produces nine-level phase-voltage. This topology possesses limited switching redundancies and produces unequal device blocking voltages. To extend this RSC-MLI to




(a) Five-level symmetrical unit. (b) Nine-level symmetrical unit

**FIGURE 10.** **Symmetrical unit-based RSC-MLIs topologies.**

higher levels, several basic units are connected in cascade [94]. However, to increase the voltage levels with appreciable reduction in switch count, several units of level generator (duplicating only three-cell structure) are connected in series followed by a common polarity generator [94].

### 2) SYMMETRICAL UNIT-BASED TOPOLOGIES

In [95], [96], two unit-based configurations, which operate with decent reduction in device count for a definite number of output voltage levels has been reported. These configurations are explained here under.

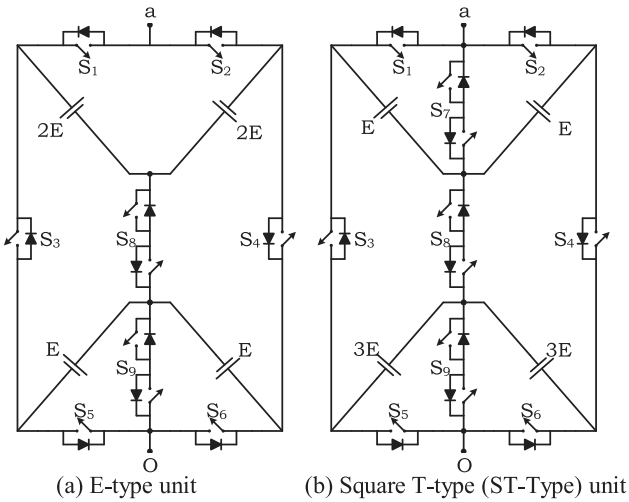
*i) Five-level configuration:* Each unit shown in Fig. 10(a) is a symmetrical five-level inverter and reported for nine-level by cascading two units [95]. Switching pulses are exchanged among the cascaded units for every cycle. This results in uniform performance of the units.

*ii) Nine-level configuration:* This nine-level symmetrical configuration shown in Fig. 10(b) seems to be similar to topology–I of hybrid T-type configuration, where the dc-link capacitors are limited to two with equal voltages [96]. However, this configuration appears to be a rearrangement of nine-level symmetrical configuration of hybrid T-type topology–I. This configuration is extended to higher levels by cascading several units.

### 3) ASYMMETRICAL UNIT-BASED TOPOLOGIES

Two asymmetrical configurations namely, E-type in [97] and, ST-type in [98] shown in Fig. 11 has been reported.

E-type module shown in Fig. 11(a) is a 13-level inverter with four dc sources of 1: 2 voltage ratio, two bi-directional and six uni-directional switches arranged in an envelope structure. Square T-type (ST-type) shown in Fig. 11(b) was inspired from E-type, where each basic unit acts as a seventeen-level inverter by itself [98]. The basic unit of ST-Type involves four dc voltages with 1: 3 voltage ratio, six uni-directional and three bidirectional switches. As similar to E-type, this topology is extended to higher levels by cascade/series connection. Both these topologies have unequal device blocking voltages and limited switching redundancies. In [154], a K-type topology is reported for 13-levels, which is similar to E-type except replacing dc sources, $E_2$ and $E_4$ in Fig. 11(a) with capacitors




(a) E-type unit (b) Square T-type (ST-Type) unit

**FIGURE 11.** **Asymmetrical unit-based RSC-MLIs.**

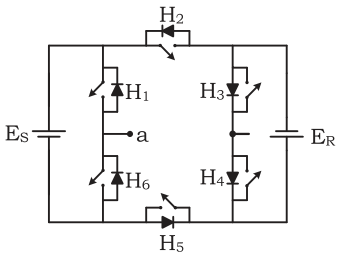



**FIGURE 12.** **Hexagonal switched cell (HSC) topology.**

and series connected switches with anti-parallel diodes. A control method is given in [154] to charge these capacitors.

### 4) *COMPACT MODULE CONFIGURATIONS*

The basic topology of seven-level module with three dc sources and ten switches [99]. This seven-level module can be extended to form a 13-level compact module with additional six switches [99]. It is worth noting that most of the RSC-MLIs based on T-type and HSC modules do not take dead-time into consideration. As the freewheeling current path during dead-time is considered, an undesirable voltage spikes might be possible. But in this topology, a proper freewheeling path is provided to enable smooth flow of inductive current. Therefore, the output voltage during dead-time is dependent on the direction of freewheeling current and a smooth voltage level transition is assured [99].

### 5) HSC CONFIGURATION

In [100], authors reported the basic unit of this configuration as a novel H-bridge, however in recent times it was popular as hexagonal switched cell (HSC). Each of the HSC unit acts a five-level inverter for 1: 1 dc-link voltage ratios and seven-level inverter for 1: 2 dc-link voltage ratios as shown in Fig. 12. This structure is modular, fault tolerant and extendable to higher levels by cascading, without changing the device ratings in each module. Furthermore, this topology

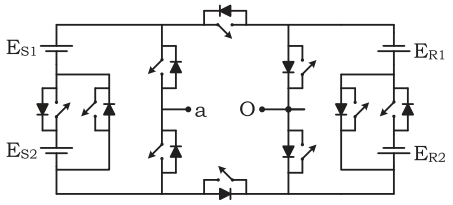



**FIGURE 13.** A nine-level extended HSC unit with four dc sources.

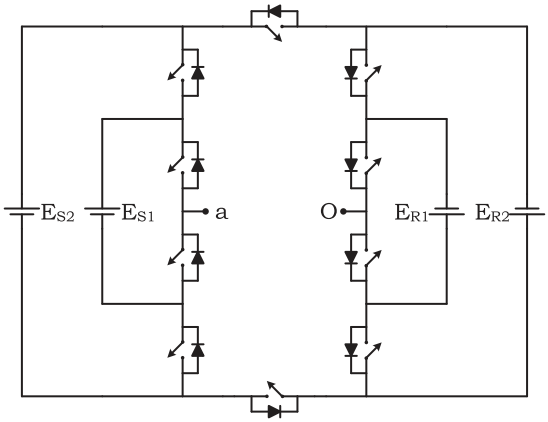



**FIGURE 14.** Extended HSC unit with four dc sources.

supports equal utilization of dc-link voltages in symmetrical configuration. Also, this configuration acted as a motivation to develop the non H-bridge based topologies to avoid separate polarity and level generator structures, such as hybrid T-type and extended HSC based configurations.

### 6) EXTENDED HSC UNITS

These topologies are derived by adding one or two additional dc sources for the HSC unit.

*i) Topology 1:* In [28], a nine-level basic unit is reported with four dc sources as shown in Fig. 13. This topology supports asymmetry and extended by cascading several units. With trinary voltage ratio, i.e., $E_{S1} = E_{S2} = E$ and $E_{R1} = E_{R2} = 3E$, this topology produces 17-levels.

*ii) Topology II:* In [101], an extended HSC unit is reported with four dc sources as shown in Fig. 14. By selecting, $E_{S1} = E$, $E_{S2} = 5E$, $E_{R1} = 2E$ and $E_{R2} = 10E$, Fig. 14 produces 31-level output voltage waveform. However, with the above asymmetric dc voltage ratio, this topology doesn't have any switching redundancy.

*iii) Topology III:* A basic unit with three dc sources and eight unidirectional switches is reported in [71], [102] and shown in Fig. 15. This basic unit supports both symmetrical and asymmetrical dc voltage ratios. This configuration operates in buck mode, where the maximum output voltage of this unit is limited to the sum of the two highest rating dc sources. Selecting $E_1 = E$, $E_2 = 2E$ and $E_3 = 5E$, each basic unit produces 15-level output voltage varying from $+7E$ to $-7E$. However, operating with symmetrical voltage ratios, it produces five-level output voltage varying from $+2E$ to $-2E$.

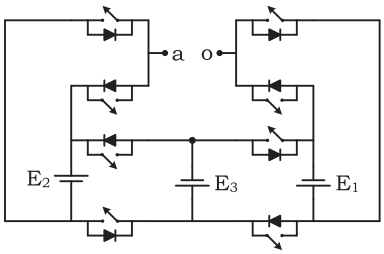



**FIGURE 15.** A basic unit derived HSC with three dc sources.

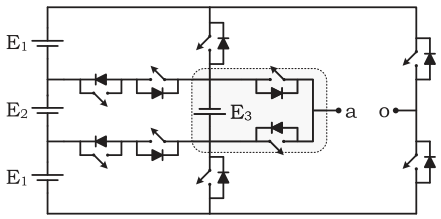



**FIGURE 16.** An extended H-bridge T-type topology [103].

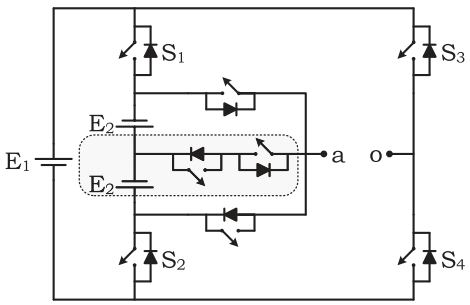


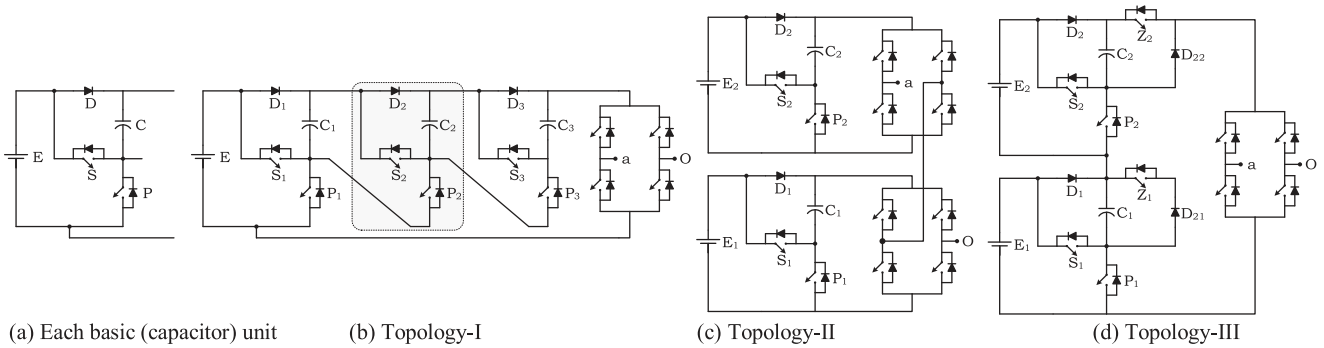

**FIGURE 17.** An extended H-bridge T-type topology [104].

### 7) ASYMMETRICAL T-TYPE TOPOLOGIES

These basic unit topologies are derived from T-type H-bridge topology.

*i) Topology 1:* This topology is derived from H-bridge based T-type topology to promote asymmetrical operation of dc sources [103]. The basic unit of this topology is shown in Fig. 16, produces nine-levels in symmetrical configuration and 13-levels with asymmetrical configuration ($E_1 = 2E$ and $E_2 = E_3 = E$). This topology can be extended to higher levels either by cascading multiple units or duplicating the highlighted portion in Fig. 16 and connect them in parallel as given in [103].

*ii) Topology II:* In [104], a T-type based basic unit is reported and shown in Fig. 17. By selecting, $E_1 = E$ and $E_2 = 2E$, this basic unit produces 11-level output voltage waveform. Switches, $S_1$ and $S_2$ are operated at fundamental frequency and both have to bear the maximum voltage stress. This topology can be extended to higher levels either by cascading multiple units or duplicating the highlighted portion in Fig. 17 and connect them one above the other as given in [104].




(a) Each basic (capacitor) unit (b) Topology-I (c) Topology-II (d) Topology-III

**FIGURE 18.** SC unit RSC-MLIs reported in [105].

### *D. SWITCHED CAPACITOR (SC) TOPOLOGIES*

To address the issue of voltage unbalance among the dc link capacitors and to reduce the requirement of input dc sources, switched capacitor topologies are reported. These topologies possess modular structure with switched capacitor units connected in organized patterns such as series, parallel or cascade. Majority of SC topologies are derived by cascading a front-side SC module with an end-side H-bridge or incorporating an SC module with in H-bridge [155]. These topologies produce the desired voltage levels and ensure the charge balance of dc link capacitors by switching them in series/parallel with dc source. In most of the topologies, the capacitor voltages are self- balanced as they are directly charged by the dc source. Unless a complicated charge balance scheme is required. By using optimized PWM scheme, the ripple in capacitor voltage can be reduced [155]. In these topologies the voltage gain (or voltage boosting factor) is calculated by dividing the generated peak ac output voltage with sum of the voltages of stiff dc sources present in the topology. The reported RSC-MLIs falling under this category are listed below.

#### 1) SERIES/PARALLEL BASED SC UNIT TOPOLOGIES

Each SC unit of these configuration operates in boost mode and produces a unipolar voltage, which is further converted to bi-polar with a polarity generator. Further, multiple SC units are integrated with a common dc source and switched in series parallel configuration promoting self-balancing and voltage boosting ability.

*i) Topology-1: Basic SC unit topology:* In [105], a novel switched capacitor (SC) unit with a power diode ($D$), a complimentary switch pair ($P$ and $S$) and one capacitor ($C$) has been reported and shown in Fig. 18(a). This SC unit is energized with a stiff dc source ($E$). When $P$ is ON, $C$ charges to $E$ through $D$ and produces an output voltage of $E$. Likewise, when $S$ is ON, $D$ becomes reverse biased and $C$ starts discharging to load, producing an output voltage of $2E$, there by the proposed SC unit operates in boost mode with voltage gain of two. However, this SC unit does not produce zero and negative levels, hence, a polarity generator is required. To extend this topology, the author suggested three possible configurations with series/parallel connection of SC units with a common or separate polarity generator for each unit.

*Configuration–I:* Fig. 18(b) shows the series connection of $n$ *SC* units with a common polarity generator. In each SC unit, the capacitor charges to $E$, when its corresponding switch $P$ is ON, there by connecting the capacitor in parallel to the dc source. Further the capacitor voltage is added to the output of former unit (or source voltage), when its respective $S$ switch is ON, thus producing a maximum output voltage of $(n + 1)E$ with a single stiff dc source. This configuration has equal device blocking voltages, operates in boost mode with self-balancing of dc link capacitors. However, at higher levels, a voltage drop across the capacitors is significant and may adversely affect its performance. In addition, this configuration does not have the feasibility to by-pass any of the SC unit under faulty condition.

*Configuration–II:* Incorporating a polarity generator in each SC unit, another possible way to extend the topology with cascade connection is shown in Fig. 18(c). Each module in Fig. 18(c) acts as a five-level inverter. Involvement of a stiff dc-source for each unit, reduces the capacitor voltage drop issues at higher levels and, further involvement of polarity generator for each unit supports asymmetry and improves fault tolerant ability, but increases device count with respect to Fig. 18(b).

*Configuration–III:* With an aim to minimize the capacitor voltage drop and device count, a modified SC unit with a stiff dc source for each unit and common polarity generator for all the units is reported as shown in Fig. 18(d). This modified SC unit involves an additional uni directional switch $Z_j$ and a power diode $D_{2j}$, and produces three voltage levels i.e., $E$, $2E$ and zero in its output. In any unit, with $P$ ON and $Z_j$ OFF, $D_{2j}$ turns forward biased which by-passes the SC unit and produces zero-level in its corresponding output. With $Z_j$ ON, $D_{2j}$ is reverse biased and, operating the complimentary switches $P$ and $S$, capacitor is connected either in parallel or series with the source, producing an output voltage of $E$ and $2E$ respectively. The purpose of $D_{2j}$ is to prevent current flowing backward when the unit is bypassed. Replacing $D_{2j}$ with controlled unidirectional switch, this configuration works well for inductive loads.

*ii) Topology-1I: Modified SC unit:* In [106], a SC unit shown in Fig. 19 has been reported, which appears to be inspired from Fig. 18(a) SC unit.

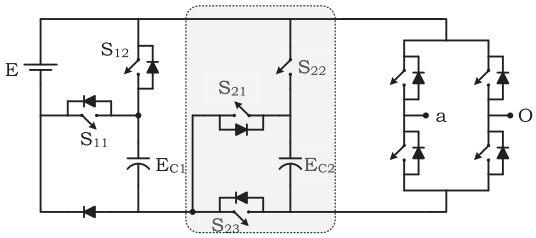



**FIGURE 19.** Modified switched capacitor unit topology [106].

In this, each unit consists of two modules, i.e., first one is the main module (non-repeating) with one stiff dc source, one capacitor, a complementary switching pair and one diode. The structure and operation of main module is similar to Fig. 18(a). Followed by main module, a secondary module (repeating module) which consists of three uni-directional switches and one capacitor. With one main module and one secondary module, Fig. 19 produces nine-levels. The overall voltage gain is four and TSV of Fig. 19 is 22$E$. By operating $S_{12}$ in main module, $C_1$ is charged to $E$ through the dc source. Further operating $S_{11}$ (in main module), $S_{22}$ and $S_{23}$ (in the secondary module), the $C_2$ is charged to 2$E$, from the dc source and $C_1$. This produces four-level uni-polar voltage which is further converted to nine-level with a polarity generator. This SC unit operates in boost mode and is extended to higher levels by duplicating the secondary module. This configuration has significant reduction in switch count but suffers from high device count and unequal device blocking voltages.

### 2) FBC (FULL BRIDGE CELL) WITH INHERENT SC UNIT

These topologies are developed by adding a triple boosting switched capacitor unit to the H-bridge. Topologies reported under this are explained below.

*i) Seven-level SC tripler topology:* In [107], [108], a self-balanced seven-level switched capacitor topology is reported and shown in Fig. 20(a). A triple boosting switched capacitor unit is incorporated by adding two capacitors and two diodes to the H-bridge. When switches $S_1$ and $S_4$ are turned ON while $S_2$ and $S_3$ are OFF, both capacitors $C_1$ and $C_2$ are charged by the voltage source, resulting in capacitors voltages equal to $E$. Therefore, this boosting unit produces unipolar voltage levels with maximum voltage of 3$E$. Further, a polarity generator is used to synthesize seven-level output waveform. The capacitors are self-balanced and TSV of this topology is 18$E$. This topology is suitable for PV integration [108]. This topology can be extended to higher levels by cascading several units.

*ii) 13-level SC tripler plus doubler topology:* This topology is similar to the Fig. 20(a), but a SC doubler unit is incorporated in polarity generator to produce 13-level output voltage. The circuit configuration is shown in Fig. 20(b) [109]. The capacitors $C_3$ and $C_4$ in SC doubler unit are charged to 3$E$ when the tripler unit output is 3$E$. All components employed in this SC doubler unit withstand the same voltage stress of 3$E$ and all the devices in tripler unit are rated for $E$. The TSV of this topology is 36$E$.

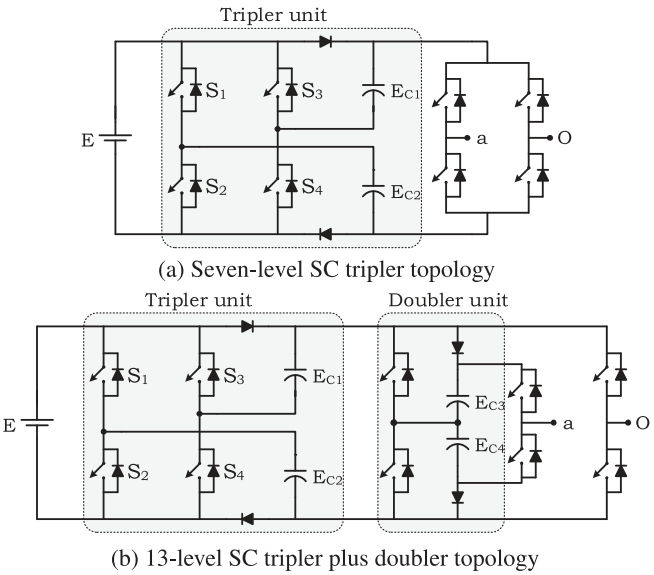



**FIGURE 20.** H-bridge based SC topologies.

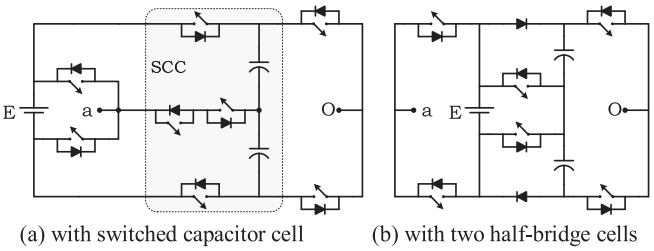



**FIGURE 21.** Five-level SC units.

### 3) SWITCHED CAPACITOR CELL (SCC) WITH HALF-BRIDGE CELLS (HBC)

To address the voltage balancing issues and device voltage stress of the switched capacitor topologies, a five-level SC unit shown in Fig. 21, which incorporates a switched capacitor cell (SCC) and two half-bridge cell (HBC) [110], [111] has been reported.

In Fig. 21(a), each capacitor charges to $E$ and, HBC balances the capacitor voltages and transforms the voltage produced by SCC to the load terminals [110]. This produces five-level output voltage varying from $\pm 2E$. A similar configuration shown in Fig. 21(b) is reported by the same authors by re-arranging the SCC and HBC structures [111]. Both these configurations have voltage boosting and balancing ability, support asymmetry, scalable to higher levels (by cascading), but suffer with unequal device blocking voltages. However, their device voltage stress is low and, do not increase with the number of levels.

### 4) SC DOUBLER TOPOLOGIES

To address the voltage unbalance issues of series connected sources, common ground issues with multiple sources and control algorithm issues in parallel operation of inverters, a seven-level SC configuration with multiple input voltage

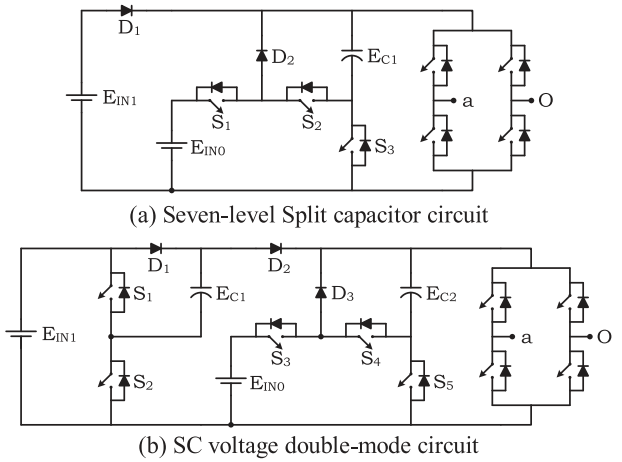



**FIGURE 22.** SC doubler and HBC topologies.

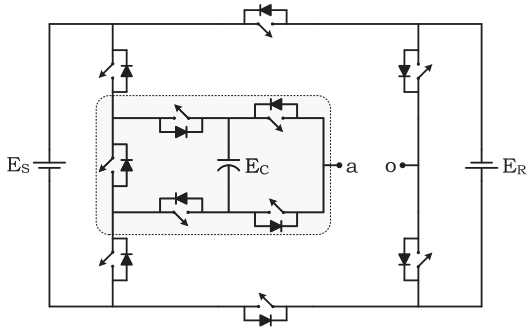



**FIGURE 23.** Modified HSC based switched capacitor topology.

sources sharing a common ground has been reported [112], [113]. This configuration is well suited for microgrids and electric vehicle networks, where asymmetric input sources are available with emphasis on high-frequency ac (HFAC) power distribution. Fig. 22(a) shows seven-level SC module with a separate polarity and level generator, where level generator incorporates two asymmetrical dc-sources, three unidirectional switching devices, one capacitor and two power diodes. Initially, capacitor $C_1$ is charged to the input voltage $E_{IN1}$ through $D_1$ by turning-on $S_3$. Assuming $E_{IN0} > E_{IN}$, the possible output voltage levels are $\pm E_{1N1}$, $\pm E_{1N0}$, $\pm (E_{1N1} + E_{1N0})$. This SC configuration requires stiff dc-sources, operates with unequal device blocking voltages and preferred for renewable and PV applications.

To increase the number of output levels, additional voltage sources, capacitors, and switches have to be connected [112]. Extending this SC configuration of Fig. 22(a), author reported SC doubler, SC half-circuit and hybrid configuration with SC doubler and SC half-circuit [113]. For topology shown in Fig. 22(b), the output voltage levels can be increased by employing a SC doubler circuit and further cascading it with a voltage source [113].

## 5. MODIFIED HSC BASED SWITCHED CAPACITOR TOPOLOGY

The switched capacitor topology shown in Fig. 23 is derived from HSC unit and reported in [114]. The switched capacitor can be connected in parallel to the dc source ($E_S$) and get charged to its voltage and further switched in series with the source to produce the desired voltage level. For $E_S = E_R$, produces seven-level with the maximum output voltage of $3E$. If $2E_S = E_R$, produces 11-level with total standing voltage of this topology is $22E$. This topology can be extended to higher levels either by cascading multiple units or duplicating the highlighted portion in Fig. 23 and connect them in parallel as given in [114].

## 6) MODIFIED T-TYPE SWITCHED CAPACITOR TOPOLOGIES

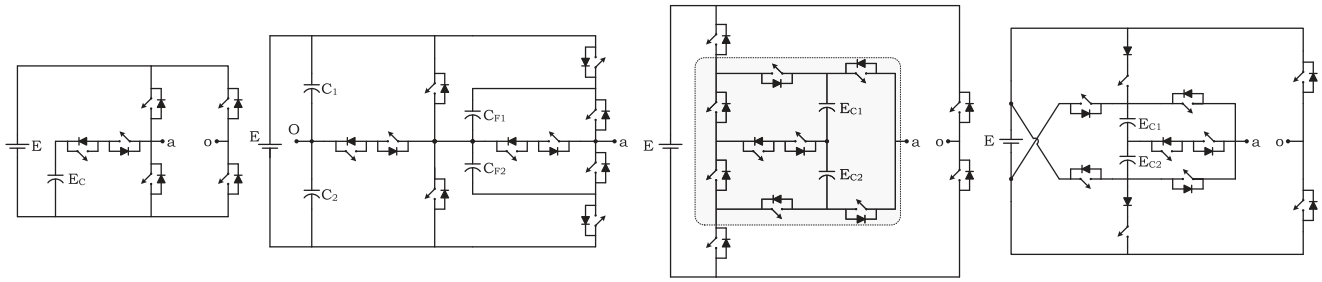
These topologies are derived from T-type by incorporating switched capacitor units. The topologies discussed under this category are operated in boost mode with single dc source.

*i) Topology–I (five-level T-type with one dc source):* In [115], a SC topology shown in Fig. 24(a), is proposed by changing the position of a dc source and further replacing with a capacitor in five-level H-bridge T-type unit shown in Fig. 3(b). By using a suitable control method [115], the capacitor can be charged to half of the dc source voltage and maintained in balanced state irrespective of the modulation index or load characteristics. This topology produces five-level output voltage with a voltage gain of one and can be extended to higher levels by cascading several units.

*ii) Topology–II (dual T-type):* In [116], a seven-level dual T-type topology is reported. This topology is shown in Fig. 24(b) and it is formed by series connection of two half-leg three-level T-type configurations through a pair of uni-directional switches. The capacitors, $C_1$ and $C_2$ are charged to $E/2$ and floating capacitors, $C_{F1}$ and $C_{F2}$ are charged to $E$. The floating capacitors operate symmetrically in every half-cycle, which results in self-balancing of their voltages. The TSV of this topology is $11E$. The voltage gain of this topology is 1.5 and the voltage levels in the output are ranging from $+1.5E$ to $-1.5E$. The ten switches in this topology form five complementary switch pairs and each switch pair operates symmetrically and experience the same voltage and current stress, thus renders equal power losses.

*iii) Topology–III (Seven-level boost topology):* In [117], a switched capacitor RSC-MLI with a voltage gain of three is reported. This topology is shown in Fig. 24(c) and it consists of one bidirectional switch and ten unidirectional switches. Two switched capacitors $C_1$ and $C_2$ are connected parallel to the dc source ($E$) and get charged to a voltage level equal to the dc source and further switched in series with the source to produce the desired voltage level. Therefore, this topology produces seven-levels in output voltage, ranging from $+3E$ to $-3E$. The inherent switching operation of this topology facilitates the self-balance of capacitor voltages. The TSV of this topology is $16E$.

*iv) Topology–IV (Nine-level cross-connected boost topology):* In [118], a nine level self-balancing boost configuration with a voltage gain of two is reported. The circuit configuration is shown in Fig. 24(d). Each capacitor is charged to $E/2$ and the output voltage varies from $+2E$ to $-2E$. Capacitor voltages are




(a) Five-level T-type with one dc source (b) Dual T-type topology (c) Seven-level boost topology (d) Nine-level cross-connected boost topology

**FIGURE 24.** Modified T-type switched capacitor topologies.

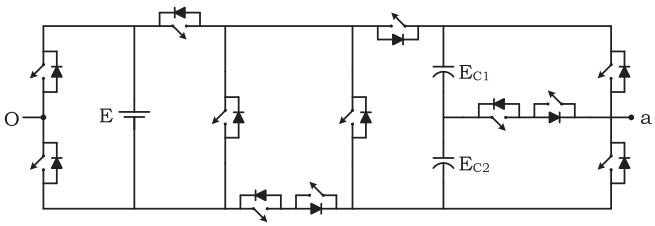



**FIGURE 25.** Single-stage switched-capacitor unit ($S^3$CM) topology.

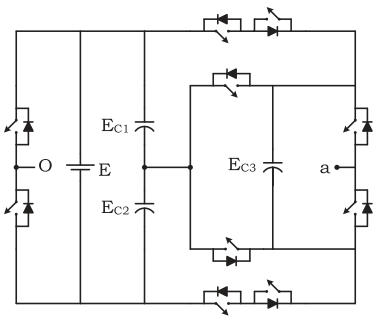



**FIGURE 26.** Seven-level boost topology.

self-balanced and independent of the load power factor and modulation index. The maximum blocking voltage of cross-connected switches is $2E$ and remaining switches is $E$. The TSV of this topology is $11E$.

### 7) SINGLE-STAGE SWITCHED-CAPACITOR UNIT ($S^3$CM)

As shown in Fig. 25, a single-stage switched-capacitor module ($S^3$CM) topology, which ensures that the peak inverse voltage across all the switches is within the dc source voltage has been reported [119]. This is a unit based switched capacitor RSC-MLI, where each $S^3$CM unit is a nine-level boost inverter. Each $S^3$CM unit have one stiff dc-source and two capacitors which are charged equally to half of the source voltage, and further the dc source voltage and dc-link capacitors together contribute to boost the output voltage to double of the source voltage. The voltage gain of this topology two and the total standing voltage is $11E$.

Motivated by the objective of $S^3$CM, reduce device count and increase number of levels, various compact single-stage configurations are reported [156]–[159]. In [156], [157], a nine-level boost topology with voltage gain two is reported. This configuration is similar to Fig. 25, but the device count reduced by one, which leads to reduction in TSV to $10E$. In [158], a seven-level $S^3$CM topology is reported with a voltage gain of 1.5 and TSV of $9E$. A ladder extension of $S^3$CM topology by combining hybrid T-type topologies is reported in [159].

### 8) SEVEN-LEVEL SC MODULE

Though most of the reported SC topologies possess self-balancing structures, they do suffer with increased device count and high voltage stress due the presence of H-bridge. In view of this, SC boost configurations without involving H-bridge are explained here under. The seven-level SC module shown in Fig. 26 involves three capacitors $C_1$, $C_2$ and $C_3$, among which authors termed $C_1$ and $C_2$ as dc-link capacitors and, $C_3$ as switched capacitor [120]. Both $C_1$ and $C_2$ charge and discharge periodically but not simultaneously, where they charge from dc source to half of its value ($E/2$) and discharge to load. $C_3$ is charged through the dc source to full magnitude ($E$). With appropriate switching operation, this SC configuration produces seven-level output voltage with levels $\pm 3E/2$, $\pm E$, $\pm E/2$ and zero. The switching redundancies of this configuration helps to effective control of dc-link capacitors and supports the inverter voltage boosting ability. Cascaded configuration of this SC module supports both symmetrical and asymmetrical voltage ratios. However, its complex topological structure increases the difficulty to realize it for three-phase applications.

### 9) NINE-LEVEL QUADRUPLE BOOST INVERTER

The SC configuration shown in Fig. 27 involve a stiff dc source ($E$), three capacitors and a half-leg structure operating at fundamental frequency at load end [121]. However, the structural arrangement and switching operation of Fig. 27 are modified such that it produces a nine-level quadruple boost output voltage. $C_1$ is charged through the dc-source to full of its magnitude and, further $C_2$ (also $C_3$) is charged from $C_1$ and source. However, both $C_2$ and $C_3$ will neither simultaneously

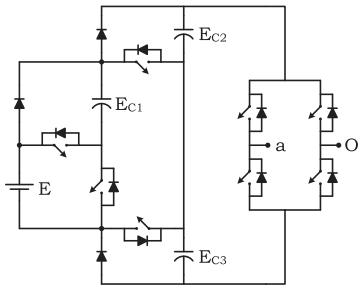



**FIGURE 27.** Nine-level quadruple boost converter.

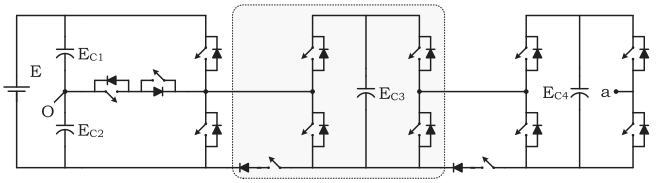



**FIGURE 28.** Hybrid seven-level SC with stacked configuration.

charge/discharge nor together contribute to the load voltage. This limits maximum load voltage to $4E$, which is obtained when the $C_2/C_3$ is switched in series with $C_1$ and dc source. Thus $C_1$, $C_2$, and $C_3$ are charged several times in a cycle, such that their voltages maintain at $E$, $2E$, and $2E$ respectively without any auxiliary balance circuit or complicated control strategy. For positive voltage levels $C_1$ pair up with $C_2$, and for negative voltage levels $C_1$ pair up with $C_3$.

### 10) HYBRID SC: STACKED CONFIGURATION

A hybrid configuration was developed by adopting SC techniques in stacked topologies [122]. [122] incorporated the concept of shared dc-link to develop a boost inverter to further reduce the dc-source requirement as shown in Fig. 28. This configuration is a stacked structure of three-level T-type inverter with H-bridge, through few auxiliary switches. Absence of auxiliary switches, charges dc-link capacitor of three-level T-type to half the magnitude. This limits the maximum possible output voltage to $3E/4$, though the applied source voltage is $E$. Therefore, to operate in boost mode, few auxiliary switches are incorporated, such that they ensure that total dc-link voltage of both T-type and H-bridge is equal to the dc-source voltage, thus boosting output voltage to $3E/2$. This configuration is extended to higher levels by duplicating highlighted part in Fig. 28. A configuration similar to [122], is reported in [123].

### 11) FLOATING CAPACITOR-BASED SC TOPOLOGIES

To minimize the requirement of dc sources and to boost up natural charge balance ability, three SC configurations i.e., floating capacitor based (FCB) configuration [124], switched capacitor (SC) based configuration [125] and a hybrid configuration with FCB and SC units [126] have been reported.

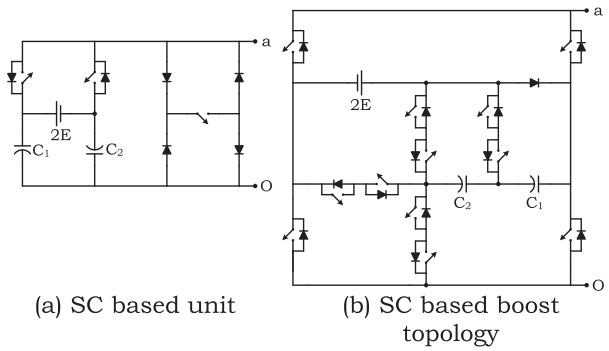



**FIGURE 29.** Split capacitor based topologies.

*i) Topology-1: Split capacitor or floating capacitor topology:* The structural arrangement of this floating capacitor based FCB unit is shown in Fig. 29(b), where the arrangement of the capacitors is such that it forms a spilt capacitor structure across the dc source and charges each capacitor to half the magnitude of the dc source voltage [124]. Thus, this FCB unit operates as a three-level inverter, producing $+E/2$, 0 and $-E/2$ levels in its output voltage. However, it is to be noted that, dc voltage source is responsible only for charging the capacitors but doesn't contribute for load current directly.

Further this configuration is extended to higher levels by cascading. Cascading $n$ identical units, this RSC-MLI produces $(2n + 1)$ levels in phase-voltage. However, replacing the diode bridge and uni-directional switch, with a bi-directional switch, reduces the device count to $2n$ uni-directional switches, $n$ bi-directional switches and $2n$ capacitors to produce levels from $+(n/2)E$ to $-(n/2)E$. Further, this configuration is valid for asymmetrical configuration (for binary and trinary dc voltage ratios) as well.

*ii) Topology-2: Switched capacitor-based boost topology:* The SC unit is shown in Fig. 29(b), which consists of one stiff dc source ($2E$), two capacitors, and several active and passive semiconductor devices has been reported in [125]. Switching operation of this SC unit is carried such that both the capacitors are periodically charged and discharged to half the magnitude of source voltage, without needing any voltage sensors or complex modulation methods. Thus, each capacitor charges to $E$ and produces nine-levels in output voltage varying from $\pm 4E$. This configuration can be extended to higher levels by cascading and suffers with unequal device blocking voltages.

*iii) Topology-3: Switched capacitor-based hybrid topology:* This hybrid structure is developed by stacking FCB and SC unit [126]. In this, the structure of SC unit shown in Fig. 29(a) is modified, such that $C_1$ charges from source and $C_2$ charges from $C_1$ and source. Operating this modified SC unit with a stiff voltage of $2E$, $C_1$ charges to $2E$ and, $C_2$ charges to $4E$. Thus, SC acts as a nine-level inverter producing $\pm 2E$, $\pm 4E$, $\pm 6E$, $\pm 8E$ and zero voltage levels in its output. Further, operating FCB with stiff source of $2E$, produces three-levels in its output voltage with $\pm E$ and zero levels. Therefore, operating SC unit at fundamental frequency and FCB at switching

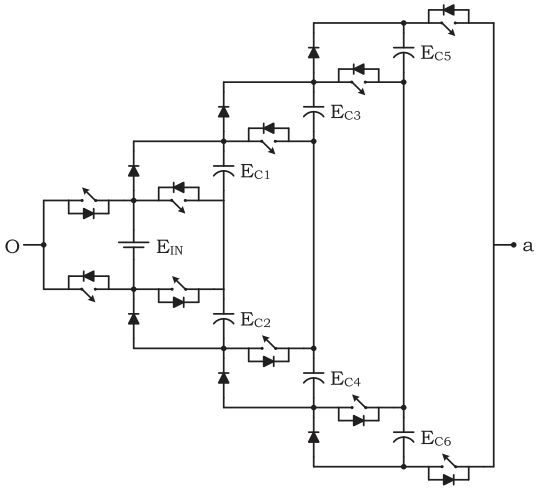



**FIGURE 30.** Multi-layered topology [127].

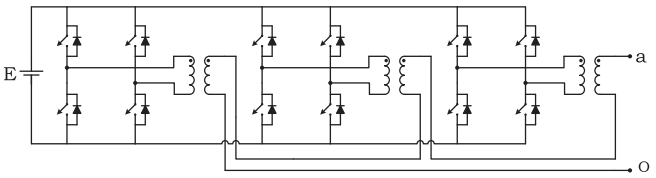



**FIGURE 31.** Transformer based reduced components (TBRC) topology.

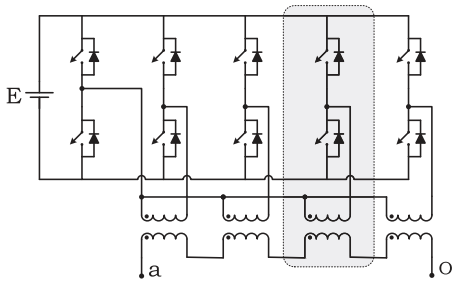



**FIGURE 32.** Single-source transformer based shared leg topology.

frequency, this hybrid configuration acts as a nineteen-level inverter with output varying between $\pm 9E$.

### 12) MULTI-LAYERED TOPOLOGIES

These multi-layered topologies are self-balanced and possess voltage boosting ability with multiple layers. The output of first layer is forwarded as input to the second layer and this continues for the next layers. There are various multi layered configurations reported, among them, topologies without separate polarity generator are remarkable as they reduce the device stress. Among the pool of such topologies, two well-known configurations reported in the recent times are discussed below.

*i) Topology-1:* The configuration shown in Fig. 30 is reported for nine-level, however, it has the ability to operate for any generalized (odd) level [127]. The key feature of this topology is its voltage boosting ability by operating the switches at device ratings less than the dc-source magnitude.

*ii) Topology-II:* In PV and micro-grid applications, a low-voltage dc source is used. From this source, a high amount of current is drawn in the case of boosting ac output voltage. The hybrid SC topology with multiple dc sources is the solution for the drawbacks of single dc source SC topologies [128].

This hybrid SC is a combination of asymmetrical dc sources and capacitors that leads to reduce the number of dc sources and their cost. In this topology, capacitor voltages are balanced at multiples of dc sources through different paths that are provided by power semiconductor devices [128]. This step-up inverter has the capability of bipolar voltage generation without using H-bridge. This hybrid topology eases capacitors voltage balancing and decreases the number of capacitors in higher power applications.

## *E. TRANSFORMER BASED TOPOLOGIES*

In literature, single-phase five-level inverters using coupled inductors are presented in [160], [161]. However, these configurations produce restricted number of levels. Therefore, to further increase the number of levels with appreciable reduction in device count, few inverter configurations incorporating transformer at load end are reported. These configurations are developed such that the presence of the transformer increases the levels in output voltage. Presence of transformer made them fault tolerant, reliable, eliminated voltage balancing issues, reduced filter and dc-source requirements. However, the presence of transformer increases the inverter size, weight, cost, losses and complexity. The following are listed under this category.

### 1) SINGLE-PHASE TRANSFORMER BASED REDUCED COMPONENTS (TBRC) RSC-MLI

To minimize the isolated dc-source requirements and eliminate voltage balancing issues in CHB, a topology by connecting multiple H-bridges with a common dc-supply at its input side and isolation transformers at the output side has been reported in [129] and shown in Fig. 31. All the H-bridges share a common dc-supply, with a single dc-source appended. Further the transformer secondary windings is cascaded and thus contribute to the output similar to the classical CHB. Similar configurations involving the concept of sharing leg is reported in [130] and shown in Fig. 32. A similar transformer based configuration by cascading half-bridges is reported in [131]. A similar concept with two dc sources is reported in [162].

### 2) TWO-PHASE FIVE-LEVEL CONVERTER WITH SCOTT TRANSFORMER

In literature, these are two-phase topologies producing two-phase output voltage which is further converted to three-phase via Scott connected transformer as shown in Fig. 33. These are popular in medium power rectifiers, where unity power factor (UPF) control is not necessary. However, these topologies can

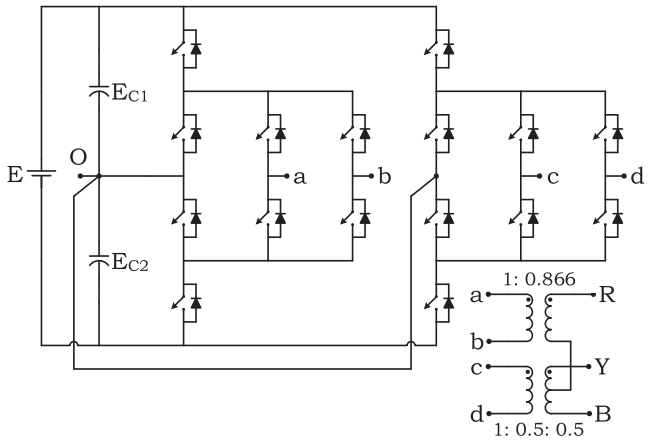



**FIGURE 33.** Transformer based two-phase topology.

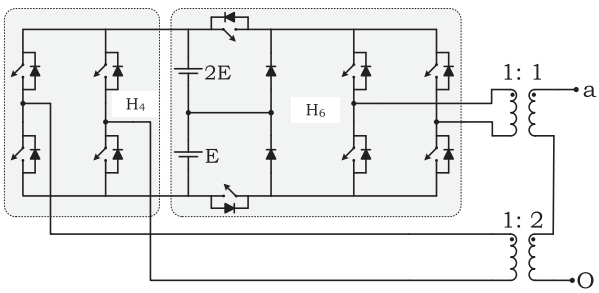



**FIGURE 34.** Transformer based $H_4$-$H_6$ topology.

also be incorporated in medium power grid tied systems for flexible control of active and reactive powers. In recent times, a five-level two-phase configuration for three-phase isolated grid-tied systems is reported in [132], [133]. This topology has two stages i.e., a five-level inverter to produce two-phase output and a Scott-T connected transformer to magnetically transform the output to three-phase. The key features of these two-phase topologies are presence of single dc-source in common to both the two-phases, large reduction in switch count, dc-link capacitor voltages have an inherent ability to self-balance and the voltage stress across the power devices equal to half of the dc-link voltage.

#### 3) $H_4$-$H_6$ TOPOLOGY

To reduce the number of levels with effective reduction in device count, a hybrid asymmetrical 19-level topology is reported in [134]. The configuration shown in Fig. 34 has two types of bridges: a conventional H-bridge inverter ($H_4$) and a single-phase six switch inverter ($H_6$). The corresponding output terminals of $H_4$ and $H_6$ bridges are connected to primary of two single-phase transformers in the ratio of 1: 2 and 1: 1 respectively. Next, secondary terminals of two transformers are connected in series to attain the maximum number of levels. Two dc-sources with $E$ and $2E$ voltages are connected in common to both $H_4$ and $H_6$ inverter. $H_4$ inverter produces three-level output voltage ($+6E$, 0, –6E after the transformer) and $H_6$ inverter operates as seven-level inverter with levels ($+3E$ to $-3E$). Finally, this hybrid configuration produces 19-levels in output voltage with magnitudes varying from $+9E$ to $-9E$. The key feature of this configuration is equal device blocking voltages. However, this configuration is complex to extend for higher levels.

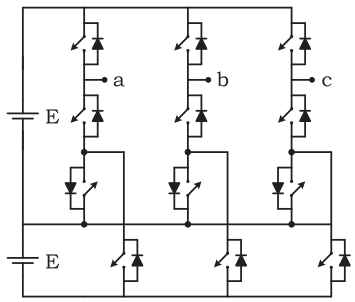



**FIGURE 35.** A three-phase three-level inverter by cascading two three-phase two-level inverters.

### *F. THREE-PHASE TOPOLOGIES*

The attractive feature of conventional two-level inverter is a common dc source to all the phases. Considering this, several RSC-MLIs are developed by modifying or extending the three-phase inverter structure with additional switches or chopper units. In literature, three-phase topologies are reported by hybridizing the conventional two-level inverter or multilevel inverter [135]–[140], [163], [164].

#### 1) TWO-LEVEL INVERTER BASED TOPOLOGIES

In [135], a three-phase three-level inverter is reported by cascading two three-phase two-level inverters as shown in Fig. 35. The main advantage of this topology is absence of fast-recovery diodes, requirement of two isolated power supplies when compared to same level CHB and retrofitting of two existing two-level inverters. On the flip side, the bottom three switches in this topology are rated such that they block the entire dc-link voltage. This topology is adopted for open-end winding induction motor by connecting a three-level inverter at one end and a two-level inverter at the other [164].

In [136], a modular symmetrical configuration by involving a two-level inverter with upper switches of each leg connected to common dc-link through series connected chopper units has been reported and shown in Fig. 36. Topological configuration of this MLI shown in Fig. 36 produce five-level line-voltage. Duplicating the chopper units, extends the configuration for higher level. With $n$ chopper units, this topology involves $3(2n + 2)$ switches to produce $(n + 2)$ levels in pole-voltage and $(2n + 3)$ levels in line-voltage. This configuration facilitates uniform utilization of dc sources but produces unequal device blocking voltages.

#### 2) MULTILEVEL INVERTER BASED TOPOLOGIES

In [137], [138], three-phase topologies that are derived by modifying three-level NPC have been reported. The authors

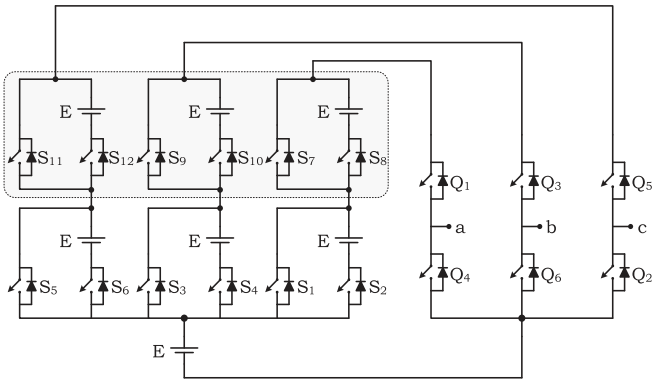



**FIGURE 36.** Three-phase two-level inverter based RSC-MLI topology.

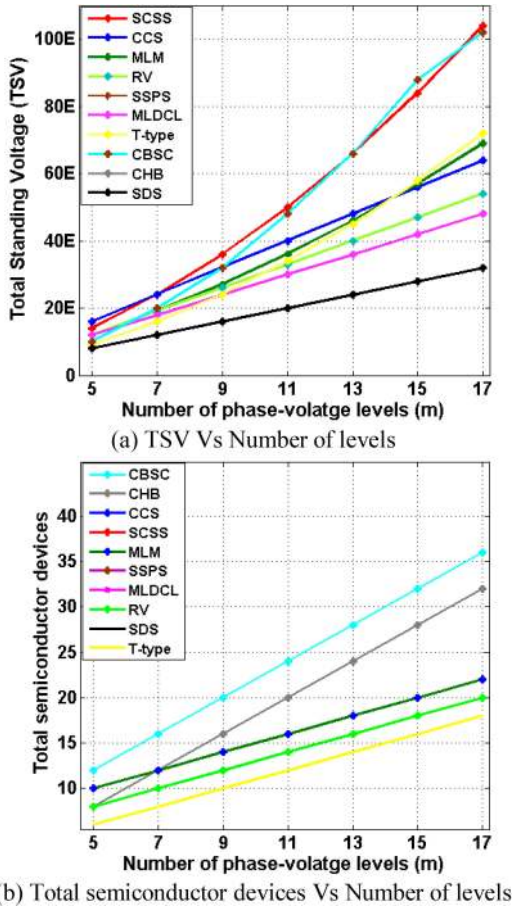



**FIGURE 37.** Comparison of TSV and total semiconductor count in generalized topologies.

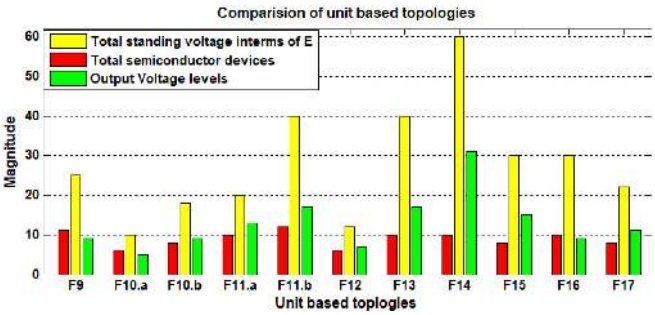



**FIGURE 38.** Comparison of TSV, total semiconductor count and number of voltage levels in unit based topologies.

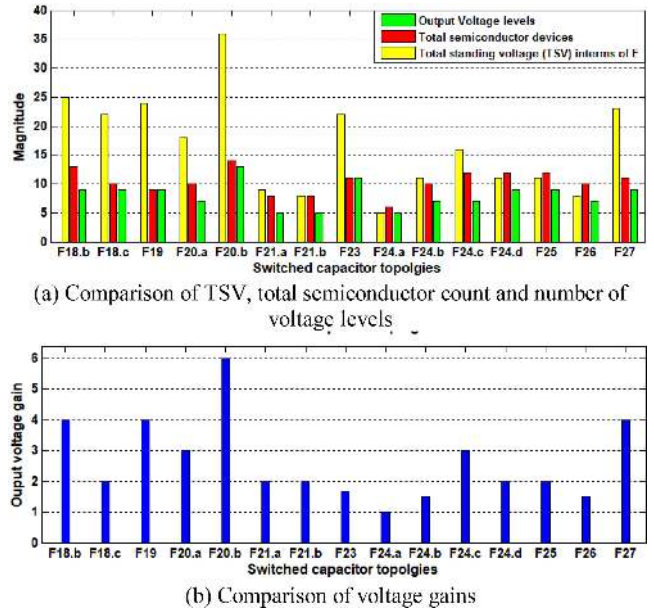



**FIGURE 39.** Comparison of TSV, total semiconductor count, number of voltage levels and voltage gain in switched capacitor topologies.

proposed four possible configurations with two different leg structures. The mid-point of each leg is connected to an auxiliary structure. This structure is formed with chopper cells. However, the position and arrangement of chopper cells is different in these topologies. These RSC-MLIs possess a generalized topological arrangement and can be operated with symmetrical and asymmetrical dc voltages. These configurations are reported for five-levels in pole-voltage. All these RSC-MLIs doesn't have switching redundancies, produces unequal blocking voltages and may result in non-uniform utilization of dc sources.

In [139], a hybrid three-phase five-level inverter is developed for PV application by integrating three-level T-type RSC-MLI and three-level DCMLI configurations with single-phase transformer. The primary windings of transformers are connected across the three-level T-type inverter and three-level DCMLI configuration and secondary windings being connected across three-phase load terminals. In [140], a novel three-phase five-level configuration is proposed by cascading half and full H-bridge inverters with isolation transformer, where half bridges acts as level generator and full bridge serves as polarity generator.

**TABLE 2.** **Comparison of Device Count and Salient Features of Generalized RSC-MLIs Topologies**

| GENERALIZED RSC-MLIs | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Topology name** | **With *n* dc sources (Identical)** | | | | **Symmetrical/ Asymmetrical/ Both** | **Blocking voltages (Equal/Unequal)** | | • **Features** ✓ **Merits** × **Limitations** |
| | **Levels in phase-voltage (*m*)** | **Device count/phase: Uni-directional (*U*), bi-directional (*B*) switches and capacitors (*C*)** | | | | **Level generator** | **Polarity generator** | |
| | | ***U*** | ***B*** | ***C*** | | | | |
| MLDCL [48, 49] | $2n+1$ | $2n+4$ | --- | --- | Both | Equal | Equal | ✓ Scalable, Modular, Redundant.<br>✓ Fault tolerant, dc-link voltage balancing.<br>✓ Same device rating for any level.<br>× Can't support trinary voltage ratios. |
| SSPS [50, 51] | $2n+1$ | $2n+4$ | --- | --- | Both | Equal | Equal | ✓ Series/parallel operation.<br>✓ Self-balancing topology.<br>✓ Voltage boosting ability.<br>× Can't support trinary voltage ratios. |
| RV [52, 53] | $2n+1$ | $2n+4$ | --- | --- | Both | Unequal | Equal | × Limited redundancies. Device ratings increases with dc-link voltage.<br>× Asymmetrical but doesn't support binary/trinary voltage ratios. |
| SCSS [54, 55, 165] | $2n+1$ | $2n+4$ | --- | --- | Symmetrical | Unequal | Equal | • Level generator: Stair-case structure.<br>× Scalable but no redundancies.<br>× Asymmetry is not possible. |
| MLM [56] | $2n+1$ | 4 | $n+1$ | --- | Symmetrical | Unequal | Equal | × Scalable but no redundancies.<br>× Asymmetry not possible.<br>× Device ratings increase with dc voltage. |
| Crisscross switched cells [57] | $2n+1$ | $(n+6)$ switches $(n+6)$ diodes | --- | --- | Both | Unequal | | ✓ Modular, scalable, and fault tolerant.<br>✓ Supports asymmetry and cascading.<br>× Blocking voltage of cross-connected switches is higher than total dc-ink voltage |
| T-type MLI [59-63] | $2n+1$ | 4 | $n-1$ | --- | Symmetrical | Unequal | | × No redundancies.<br>× Voltage rating of operating devices increases with dc-link voltage.<br>✓ Scalable structure with appreciable reduction in switch count.<br>✓ Two on-state conducting devices. |
| Cascaded T-type | Cascading '$n$' $l$-level T-type units | | | | Both | Unequal | | • All the merits & features of T-type are valid to each cascaded T-type unit.<br>✓ Facilitates switching redundancies even power distribution of dc-link.<br>× Source voltages of each T-type must be identical. |
| | $(l-1)+1$ | $4n$ | $n\frac{l-1}{2}$ | $n\frac{l-1}{2}$ | | | | |
| Three-leg T-type MLI [59, 65, 66] | $\frac{n-1}{2}+1$ ($n$ should be even) | 2 | $(n-1)$ | --- | Symmetrical | Unequal | | ✓ Common dc-link to all phases<br>✓ Alternate to NPC, ANPC and NPP. Lower conduction losses and high efficiency.<br>× Only Symmetrical. |
| HSC Based topologies [67-69] | Hybrid T-type Topology-I [67, 68] $m$-levels | 6 | $\frac{m-5}{4}$ | $\frac{m-1}{4}$ | Both | Unequal | | • Two stiff dc sources are sufficient.<br>• Symmetrical topology produce '$m$' level, if $(m-1)/4$ is integer i.e., $m = 9, 13, 17$.<br>• For non-integer values of $(m-1)/4$, asymmetrical should be opted.<br>× Doesn't support trinary voltage ratio. |
| | Hybrid T-type Topology-II [67, 68] $m$-levels | 6 | $\frac{m-5}{2}$ | $\frac{m-1}{2}$ | Both | Unequal | | • Includes all features of Topology-I, but operates with additional switching redundancies.<br>• DC-link capacitors can be replaced by stiff dc sources.<br>✓ Scalable structure: can be extended with or without cascading.<br>× Limited redundancies. |
| | Hybrid T-type Topology-III [69] $m$-levels | 6 | $\frac{m-1}{2}$ | $\frac{m-1}{2}$ | Both | Unequal | | ✓ Cross-connected switches increases switching redundancies and asymmetrical voltage ability. |
| Extended HSC based topologies [70, 72] | Topology-I $2n+1$ [70] | 6 | $n$ | --- | Both | Unequal | | ✓ Fault tolerant. appreciable redundancies.<br>✓ Supports binary voltage ratios.<br>× Few devices in HSC experience blocking voltage higher than total dc-ink voltage. |
| | Topology-II $2n+1$ [72] | $2n+2$ ($n$-even) | --- | --- | Both | Unequal | | ✓ Adequate redundancies, support asymmetry.<br>× Produce high device stress. |
| CBSC [73] | $2n+1$ | --- | $2n+2$ | --- | Both | Unequal | | ✓ Scalable structure, no polarity generator. Always two switches devices in conduction.<br>✓ Extended with or without cascading.<br>✓ Number of gate drives are equal to number of bi-directional switches. |
| PUC [43, 77] | For $n > 2$, $m = 5$ and for $n \leq 2$, $m = 2n+1$ | $2n+2$ | --- | --- | Both | Equal | | × Cannot produce more than three-level in phase-voltage with symmetrical sources.<br>× Switching path of any voltage level involves consecutive addition and subtraction of dc sources.<br>× Asymmetrical and always operates in buck mode. |
| SDS [74-76] | $2n+1$ | $2n+2$ | --- | --- | Both | Unequal | | ✓ Overcomes the demerits of PUC.<br>✓ Scalable, appreciable device reduction.<br>× Not valid for binary and trinary ratios. |

**TABLE 3. Comparison of Device Count and Salient Features of Stacked RSC-MLIs Topologies**

| Stacked topologies | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Topology name | Stacked configurations | Levels in phase-voltage ($m$), Switches: Uni ($U$) & bi ($B$) directional; diodes ($D$), capacitors ($C$); and dc-sources ($n$), levels in line-voltage ($M$) | | | | | | | Symmetrical/ asymmetrical /both | Blocking voltages equal/ unequal | Features<br>• Features<br>✓ Merits<br>× Limitations |
| | | $m$ | $n$ | $M$ | $U$ | $B$ | $D$ | $C$ | | | |
| LDN based topologies [78-81] | CHB+ LDN [78-80] | $4n+1$ | $3n$ | $8n+1$ | $12n+6$ | | | 3 | Asymmetrical | Uneven | • Operates CHB at fundamental & LDN at carrier frequency.<br>✓ LDN doubles the phase-voltage levels.<br>✓ DC-link voltage of each LDN is half of the dc-voltage of each CHB. |
| | TTC+LDN [81] | $2n+1$ | $n+3$ | $4n+1$ | 12 | $3n+3$ | -- | -- | Asymmetrical | Unequal | • Dc-link voltage of each LDN is equal to total dc voltage of TTC. |
| Non-LDN based topologies [82-93] | FC + CHB + Selector switches [86, 87] | 49 | 3 | | 8 + (3*16) | -- | -- | 4 | Symmetrical | Unequal | ✓ One FC is stacked with three HB to produce seventeen-level inverter.<br>• In FC, each capacitor is charged to half of its prior capacitor voltage. |
| | ANPC+FC [82, 83] | 11 | 1 | 23 | 12 | -- | -- | 4 | Symmetrical | Unequal | ✓ Advantages of both NPC and FC.<br>✓ Extended to higher levels by increasing FC units.<br>✓ Reduced cost and control complexity.<br>✓ For passive front-end rectifiers balances dc-link voltages naturally. |
| | HFC [91, 92] | 5 | 3 | 9 | 8 | --- | --- | 1 | Asymmetrical | Unequal | ✓ Reduced device ratings compared to 5L-ANPC. |
| | T-type + CCM [93] | $2n+1$ | 1 | $4n+1$ | $4n-1$ | $n/2$ | $n-2$ | $n$ | Symmetrical | Unequal | • T-type & CCM stacked; Extended to higher levels by increasing CCM.<br>• Boost topology: With a source voltage of $E$, involves $n$-capacitors, $(n-2)/2$ CCM modules to produce an o/p of $\pm nE$ with $2n+1$ level.<br>• Each CCM has two capacitors, two series diodes, four unidirectional switches and one bi-directional switch.<br>• TSV: $7n-2$. |

## IV. COMPREHENSIVE COMPARISON OF RSC-MLIS

This section presents a comparison on the features, merits and limitations of various RSC-MLIs. In Fig. 37, a comparative charts are given for selected generalized topologies. These charts are drawn to compare TSV and total number of semiconductor devices with respect to the number of levels. The total number semiconductor devices (total switch count) is the sum of power diodes, unidirectional and bidirectional switches. The bidirectional switches are treated as two unidirectional switches. For a better comparison, in Fig. 37 CHB is also included and assumed that the considered topologies are symmetrical. From Fig. 37(a), it can be concluded that TSV of SSPS and MLDCL are equal. Similarly, TSV of CHB and SDS are equal and lowest among the others. On the other hand, the total switch count of SDS and T-type topology are same and lowest among other. The total switch count of SSPS, MLDCL, RV and SCSS are equal and a little higher than SDS and T-type. CHB is having low TSV but the total switch count is high. In conclusion, SDS possesses low TSV and require least number of switches devices.

In Fig. 38, comparison charts for selected unit based topologies are presented in terms of TSV, total number of semiconductor devices and number of voltage levels. The X-axis indicates the figure numbers.

In Fig. 39(a), comparison charts for selected switched capacitor based topologies are presented in terms of TSV, total number of semiconductor devices and number of voltage levels. The X-axis indicates the figure numbers. The voltage gains comparison for the selected switched capacitor toplogies is shown in Fig. 39(b). The 13-level SC tripler plus doubler topology shown in Fig. 20(b) has highest voltage gain but its TSV is high. The topologies shown in Fig. 24(d) and Fig. 25 have better value for proposition.

Further, a comprehensive comparison on the features, merits and limitations of various categories of RSC-MLIs is presented in Table 2 to Table 7. The parameters considered for comparative study are: topological arrangement, physical structure, switching nature of level and polarity generators, requirement of dc supply, involvement of uni-directional or bi-directional switches, device count, device blocking voltages, utilization of dc sources, load power distribution, dc link voltage balancing, possibility to operate with asymmetrical dc sources, voltage boosting ability, switching redundancies, generalization of the topology to higher levels and fault tolerance ability.

From these comparisons, the following observations can be drawn:

**TABLE 4.** Comparison of Device Count and Salient Features of Unit-Based RSC-MLIs Topologies

| Unit-based MLIs | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Topology name | | Levels from each unit | With '*n*' identical units | | | | | | Symmetric/ asymmetrical /both | Blocking voltages equal/ unequal | Features |
| | | | uni (*U*) & bi (*B*) directional switches, diodes (*D*), capacitors (*C*), phase-voltage levels (*m*) and dc-sources (*N*) | | | | | | | | • Features<br>✓ Merits<br>× Limitations |
| | | | *m* | *N* | *U* | *B* | *D* | *C* | | | |
| [94] | Basic unit MLI [94] | 9-level | $6n+3$ | $3n+1$ | $5n+6$ | $n$ | --- | --- | Both | Unequal | • Involves Polarity generator.<br>✓ Cannot support trinary voltage ratios. |
| Symmetrical unit-based topologies | [95] | 9-level | $8n+1$ | $3n$ | $6n$ | $n$ | --- | --- | Symmetrical | Unequal | ✓ Similar to [67, 68], but with modified physical arrangement. |
| | [96] | 5-level | $4n+1$ | $2n$ | $6n$ | --- | --- | --- | Symmetrical | Level generator Equal | • Each unit has polarity generator.<br>✓ Modular, redundant structure.<br>✓ Equal utilization of dc-sources. |
| Asymmetrical unit based topologies [97, 98] | E-type topology [97] | 13-level | $12n+3$ | $4n$ | $6n$ | $2n$ | --- | --- | Asymmetrical | Unequal | ✓ Purely asymmetrical. No redundancies.<br>× Appreciable device reduction.<br>× DC-link voltage balancing is difficult.<br>✓ Cascading creates switching redundancies. |
| | ST-type topology [98] | 17-level | $16n+1$ | $4n$ | $6n$ | $3n$ | --- | --- | Asymmetrical | Unequal | • All features of E-type are applicable.<br>✓ Reduction in switch count compared to E-type. |
| Compact module topologies [99] | 7-level compact module | 7-level | 7 | 3 | 4 | 3 | --- | --- | Symmetrical | Equal | ✓ Smooth freewheeling transition for inductive current during dead-time.<br>✓ 7LCM possess lower conduction losses.<br>✓ Fault-intolerant.<br>× Limited redundancies.<br>× Maximum blocking voltage of almost of all the devices in 7LCM is $3E$. |
| | 13-level compact module | 13-level | 13 | 6 | 6 | 4 | --- | --- | Symmetrical | Unequal | |
| Basic HSC unit | HSC [100, 166] | 5-level | $4n+1$ | $2n$ | $6n$ | --- | --- | --- | Both | Unequal | ✓ No separate polarity generator.<br>✓ Simplified topological structure. |
| Extended HSC | Topology –I [28] | 9-level | $8n+1$ | $4n$ | $10n$ | --- | --- | --- | Both | Unequal | ✓ To enhance the asymmetric ability of conventional HSC.<br>✓ Cross-connected switch increases the switching combinations.<br>• Produces 9-level for symmetrical voltage ratios and 17-level for trinary voltage ratios. |
| | Topology –II [101] | 31-level Module | $30n+1$ | $4n$ | $10n$ | --- | --- | --- | Both | Unequal | • Output varies from $\pm (E_{S2}+E_{R2})$.<br>× Maximum possible voltage is only $E_{S2}+E_{R2}$. Operates in buck mode.<br>× $E_{S1}$ and $E_{S2}$ cannot be switched in additive combinations. Similarly, $E_{R1}$ and $E_{R2}$.<br>× $E_{S1}$ and $E_{R1}$ cannot be switched in substractive combination. Similarly, $E_{S2}$ and $E_{R2}$. |
| | Topology –III [102] | 15-level Module | $14n+1$ | $3n$ | $8n$ | --- | --- | --- | Both | Unequal | × Operates in buck mode.<br>× Peak output voltage restricted to the total magnitude of two dc sources holding highest voltages.<br>• Extended to higher levels by cascading. |
| Asymmetrical T-type topologies | Topology –I [103] | 13-level module | $12n+1$ | $4n$ | $6n$ | $2n$ | --- | --- | Both | Unequal | ✓ Developed to promote asymmetric ability of T-type.<br>• Originated by adding a half-bridge chopper unit between T-connection and load terminal of seven-level T-type module.<br>• Scaled for higher levels by cascading or by increasing chopper modules. |
| | Topology –II [104] | 11-level | $10n+1$ | $3n$ | $6n$ | $n$ | --- | --- | Both | Unequal | • Switches, $S_1$ and $S_2$ are operated at fundamental frequency but both have to bear the maximum voltage stress.<br>• Extended to higher levels either by cascading multiple units or duplicating bi-directional switch unit. |

- For modular topologies, the extension of topology to higher levels with the addition of new devices, does not affect the blocking voltage and rating of the existing devices.
- In H-bridge and HSC based topologies, the voltage rating of the devices in H-bridge and HSC are higher or equal to the total dc link voltage. In topologies such as MLDCL, SSPS, T-type, RV, SCSS, hybrid T-type, MLM,

**TABLE 5. Comparison of Device Count and Salient Features of Switched Capacitor RSC-MLIs Topologies**

| Switched capacitor RSC-MLIs | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Topology** | **Name** | **H-bridge /HSC based/ other** | **With *n* SC units (Identical)** | | | | | **Symmetrical/ Asymmetrical/ Both** | **Blocking voltages (Equal/ Unequal)** | • **Features** ✓ **Merits** × **Limitations** |
| | | | **Levels in phase-voltage (*m*)** | **Device count/phase: dc-sources (S), Uni-directional (*U*), bi-directional (*B*) switches, diodes (*D*), capacitors (*C*)** | | | | | | |
| | | | | **S** | ***U*** | ***B*** | ***D*** | ***C*** | | |
| Series parallel SC topologies: Basic SC unit [105] | Configuration–I | H-bridge based | $2n+3$ | 1 | $2n+4$ | --- | $2n$ | $n$ | Symmetrical | Equal | ✓ Self-balancing of dc-link voltage.<br>✓ $n$ capacitors charged by one source of $E$.<br>✓ Boost operation: o/p voltage is $(n+1)E$.<br>• Multiple redundancies.<br>× high voltage drop in series connected capacitors.<br>× Least fault tolerant capability. Not possible to by-pass any faulty unit. |
| | Configuration–II | H-bridge based | $4n+1$ | $n$ | $6n$ | --- | $n$ | $n$ | Both | Equal | • Each unit has a polarity generator and acts as a five-level inverter.<br>• Level generator don't facilitate zero-level.<br>• '$n$' units produces output voltage of $2nE$<br>✓ Supports binary and trinary voltage ratios.<br>✓ Reduces capacitor voltage drop.<br>✓ Multiple redundancies. Self-balancing of dc-link voltages.<br>× Increased switch count at higher levels. |
| | Configuration–III | H-bridge based | levels $4n+1$ | $n$ | $3n+4$ | --- | $2n$ | $n$ | Both | Unequal | ✓ Each unit has a stiff dc source & capacitor. Common polarity generator for all units.<br>✓ Operate in boost mode.<br>✓ $n$ units in series produces an o/p voltage magnitude of $2nE$.<br>✓ Multiple redundancies.<br>✓ Self-balancing of dc-link voltages.<br>× Complicated topological arrangement. |
| Series parallel SC topologies: Modified SC unit [106] | Series connection of SC units | H-bridge based | $2(2n+1)+1$ | 1 | $3n+6$ | --- | 1 | $n+1$ | Both | Uneven | • Involves polarity generator.<br>• To increase levels, second part of the basic 4-level SC unit is duplicated, such that polarity generator remains common for all units. However, this cannot by-pass faults.<br>• Voltage across the capacitors is not identical, i.e., first capacitor charges to the value of dc source and, second one charges to double of it, i.e., sum of first capacitor & dc-source.<br>• With $n$ units, produces o/p of $\pm(2n+1)E$. |
| | Cascade connection of SC units | H-bridge based | $8n+1$ | $n$ | $9n$ | --- | $n$ | $2n$ | Both | Uneven | ✓ Extended to higher levels by cascading.<br>✓ In cascaded SC topology, 9-level SC module is duplicated and cascaded.<br>✓ Fault tolerant, fault by-passes effectively.<br>✓ With $n$ units output varies from $\pm 4nE$.<br>✓ Self-balancing boost topology with separate polarity for each unit.<br>✓ Supports asymmetry. |

basic unit RSC-MLI, cascaded MLI with H-bridge and hybrid MLI using switched capacitor units, the switches in the polarity generator are rated for the total dc-link voltage.

- The topologies with separate polarity generator and level generator, possess symmetric switching operation for both positive and negative voltage levels. Most often, level generator of RSC-MLIs always produce the output voltage for additive combination of dc sources and does not facilitate switching states for subtractive combinations. This limits the asymmetry of the topology with trinary voltage ratios.
- Reduction in switch count, reduces the switching redundancies, creates unequal voltage stress and blocking voltages on the switches and limits the capability to balance the dc link voltages thus, leads to the unequal utilization of dc sources.
- Switching redundancies play a key role in reconfiguration of the inverter in faulty condition. Thus, limited or absence of switching redundancies in RSC-MLI topologies have restricted fault tolerant ability.
- Level generator of few RSC-MLIs does not produce zero voltage and is produced from polarity generator. In case of open circuit (OC) faults, these configurations may not

**TABLE 5. Continued.**

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| FBC (full bridge cell) unit with inherent SC | Seven level SC Tripler [107, 108] | SC tripler topology | $6n+1$ | $n$ | $8n$ | -- | $2n$ | $2n$ | Both | Unequal | • Each SC unit involves 4 uni-directional switches (arranged as an H-bridge), two diodes, polarity generator and opertes with volatge gain factor of 3 and TSV=16$E$.<br>• Capactiors are self-balancing and each charged to source voltage $E$.<br>• cascading $n$-units produces (6n+1) level with mangitude +3nE to –3n$E$. |
| | Thirteen-level SC tripler + doubler [109] | SC tripler + doubler | $12n+1$ | $n$ | $10n$ | -- | $4n$ | $4n$ | Both | Unequal | • Each SC is 13-level boost unit which is integration of tripler and doubler.<br>• Voltage gain of each unit is 6, TSV of 36E, with output varying from +6$E$ to –6$E$.<br>• Involves four capacitors: $C_1$ and $C_2$ form an SC tripler unit and, $C_3$-$C_4$ form doubler $C_1$=$C_2$= $E$; $C_3$=$C_4$= 3$E$.<br>• Volatge gain 6 and TSV of 36$E$. |
| Switched capacitor cell (SCC) with half-bridge cell (HBC) [110, 111] | Topology –I [110] | Half bridge Based | 5 | 1 | 6 | 1 | --- | 2 | --- | Unequal | • DC source will not contribute to load voltage directly.<br>• SCC, is surrounded by HBC on either side, to produce five-level output voltage of magnitude ±2$E$, from input of $E$.<br>• Total standing voltage of Topology - I and II are 9$E$ and 8$E$ is respectively. |
| | Topology –II [111] | Half bridge Based | 5 | 1 | 6 | | 2 | 2 | --- | Unequal | |
| Modified HSC based SC topology [114]. | [114] | HSC based | $10n+1$<br>(for 2: 1) voltage ratios | $2n$ | $11n$ | --- | --- | $n$ | Both | Unequal | • Outer strctural frame of the configuration is similar to HSC, where $C$ charges to $E_1$.<br>• PIV is $E_1$+$E_2$.<br>• TSV= 9 $E_1$+ 4 $E_2$.<br>• $V$o, max = 2$E_1$ + $E_2$, with 11-switching combinations.<br>• For $E_1$=$E_2$, produces for 7 level with, the maximum output voltage $V$o, max = 3$E$.<br>• If $E_1$ = 2$E$ & $E_2$ = $E$, TSV is 22$E$ and $V$o is 11-level, with gain factor of 5/3. |
| Modified T-type switched capacitor topologies | Topology –I [115] | H-bridge based | $4n+1$ | $n$ | $4n$ | $n$ | -- | $n$ | Both | Unequal | • Each unit produces five-level o/p with magnitude +$E$ to –$E$, at a step of $E$/2.<br>• Cannot operate in boost mode and effective control algorithm is required to charge capacitor to $E$/2.<br>• Each unit: PIV= $E$, and TSV=5$E$.<br>✓ Extended to higher levels by cascading<br>✓ Supports binary and trinary voltage ratios. |
| | Topology –II [116] | Half-bridge based | 7 | 1 | 6 | 2 | - | 4 | Single source | Unequal | • Seven-level boost inverter with voltage gain 1.5 and TSV of 11$E$.<br>✓ capacitors charge symmetrically for each half-cycle, which results in self-balancing. |
| | Topology –III [117] | H-bridge based | $6n+1$ | $n$ | 10 | 1 | - | $2n$ | Both | Unequal | ✓ Each unit two capcitors which are charged symmetrically to source voltage $E$.<br>✓ Self-balancing and volatge boosting.<br>• Seven level triple boost inverter with gain factor of 3 and TSV = 16$E$.<br>• Scaled to higher levels by cascading<br>× PIV greater than source voltage $E$. |
| | Topology –IV [118] | H-bridge based | $8n+1$ | $n$ | $8n$ | $n$ | $2n$ | $2n$ | Both | Unequal | ✓ Self-balancing volatge boosting ability with ouput voltage gain 2.<br>• PIV of cross-connected switches is 2$E$. However, PIV of remaining is within $E$.<br>• TSV= 11$E$.<br>• Claims maximum efficiency as 98.25%.<br>• Scalable to higher levels by cascading. |
| [119] | Single-Stage SC unit (S3CM) | Non H-bridge Based | 9 | 1 | 8 | 2 | | 2 | | unequal | ✓ Motivated by high PIV of SC topologies.<br>✓ Ensures PIV of all switches, is less than the dc source voltage.<br>✓ Boost operation: o/p ±2$E$, from $E$<br>✓ DC source & capacitors contribute to output.<br>✓ Nine-level output with $dv/dt$ =$E$/2. |
| Seven-level SC module [120] | Seven level SC | Non H-bridge | 7 | 1 | 6 | 2 | --- | 3 | Asymm etrical | Unequal | ✓ o/p voltage: ±3$E$/2, from dc-source $E$.<br>• Self-balanced of dc-link voltages. |
| [121] | Nine-level Quadruple | H-bridge Based | 9 | 1 | 8 | - | 3 | 3 | --- | unequal | ✓ Each unit is nine-level self-balancing boost converter. Non-scalable. |

**TABLE 5. Continued.**

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Boost inverter | | | | | | | | | | ✓ Produces ±4$E$ from a dc-source of $E$<br>✓ No H-bridge: Reduces device stress.<br>• Sustains inductive loading. |
| Floating capacitor-based SC topology [124-126] | Topology –1 FCB based topology [124] | non H-bridge based Each unit is a three-level inverter | 2$n$+1 | $n$ | 2$n$ | $n$ | | 2$n$ | symmetrical | Equal | ✓ Voltage balancing through split capacitor<br>✓ Extended to higher levels by cascading.<br>✓ asymmetry is possible for any voltage ratios (cascaded configuration).<br>✓ Equal load power distribution among dc-link capacitors.<br>✓ Output: ± ($n$/2)$E$ with i/p voltage '$E$'. |
| | Topology –2 SC based boost converter [125] | (non H-bridge) Each unit is a nine-level inverter | 8$n$+1 | $n$ | 4$n$ | 4$n$ | $n$ | 2$n$ | Both | Unequal | ✓ One stiff dc source required for each unit.<br>✓ Switched capacitors are periodically charged to half of source voltage.<br>✓ Cascading two units & operating with asymmetrical ratios produce 49-level o/p.<br>✓ Complex circuit configuration |
| | Topology –3 Hybrid topology (FCB and SC) [126] | (non H-bridge) Each unit is a nineteen-level inverter | 18$n$+1 | 2$n$ | 6$n$ | 5$n$ | $n$ | 4$n$ | Asymmetrical | Unequal | • One three-level FCB and nine-level SC units are stacked to form a hybrid SC unit, which acts a nine-teen level inverter.<br>• FC and SC are operated with 1: 2 voltage ratios and, operated at switching and fundamental frequency respectively.<br>✓ Self-balancing boost topology.<br>✓ Output varies from ±9$nE$ for '$n$' units. |

**TABLE 6. Comparison of Device Count and Salient Features of Transformer-Based RSC-MLIs Topologies**

| Transformer based RSC-MLI | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Topology name** | **Purpose of transformer** | **Levels in phase-voltage (m) Switches: Uni ($U$) & bi ($B$) directional; diodes ($D$), capacitors ($C$); and dc-sources ($n$), levels in line-voltage ($M$)** | | | | | | | **Symmetrical/ asymmetrical /both** | **Blocking voltages equal/ unequal** | **Features**<br>• **Features**<br>✓ **Merits**<br>× **Limitations** |
| | | ***m*** | ***n*** | ***M*** | ***U*** | ***B*** | ***D*** | ***C*** | | | |
| [132, 133] | To convert two-phase to three-phase | 5 | 1 | 9 | 16 | --- | --- | 2 | Symmetrical | Unequal | × Difficult to extend for higher levels.<br>× Require Scott connected transformer. |
| H4-H6 topology [134] | For boosting the output voltage. | 18 | 2 | --- | 10 | --- | 2 | --- | Symmetrical | Unequal | × Involves two transformers of different rating.<br>× Primaries of the transformers are connected to $H_4$ and $H_6$ converters respectively.<br>✓ Secondary's connected in series through load such that output voltage is obtained for their additive and subtractive combinations. |

**TABLE 7. Comparison of Device Count and Salient Features of Three-Phase Based RSC-MLIs Topologies**

| Three-phase topologies | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Topology name** | **Type** | **levels in pole-voltage** | **With '$n$' extending units (identical) Switches uni ($U$) & bi (B) directional; diodes ($D$), capacitors ($C$); and dc-sources ($N$), levels in line-voltage ($M$)** | | | | | | **Symmetrical/ asymmetrical /both** | **Blocking voltages equal/ unequal** | **Features**<br>• **Features**<br>✓ **Merits**<br>× **Limitations** |
| | | | ***M*** | ***N*** | ***U*** | ***B*** | ***D*** | ***C*** | | | |
| [136] | 3-leg based | $n$+1 | 2$n$+1 | 3$n$+1 | 6$n$+7 | --- | --- | --- | Symmetrical | Unequal | • Modular and redundant structure.<br>× Cannot support trinary voltage ratios.<br>× Complex switching logic. |
| [137, 138] | 3-leg based | $n$+2 | 2$n$+5 | $n$+1 | 2$n$+6 | 3 | --- | --- | Both | Unequal | ✓ Modular and redundant structure.<br>× Doesn't support trinary voltage ratio.<br>× Complex switching logic. |

permit to by-pass faulty operating unit and limits the fault tolerant ability of the topology.

- Requirement of dc supply: Few RSC-MLI possesses the topological structure where a common dc link will be connected to all the phases such as three-phase RSC-MLIs. Also, few other topologies require non-isolated dc voltages.
- In switched capacitor RSC-MLI, the dc sources can be replaced by capacitors and a single dc supply can be connected in parallel to them. This reduces the requirement of dc sources, however it cannot be preferred for high-voltage applications, as it causes voltage unbalance.
- Few other topologies such as SSPS, possess boost circuit configuration, where the topology charges multiple

capacitors through one stiff dc source such that voltage across each capacitor is equal to the dc source voltage.

## V. FUTURE TRENDS

Although, many RSC-MLI topologies are reported in open-loop with *RL* load, a few RSC-MLI configurations are reported for specific applications such as PV [167]–[169], adjustable speed drives [170]–[173], power quality [174], FACTS [175], solid-state transformers [176], energy storage [177], [178], electric vehicles [179], wireless power transfer [180] and power factor correction [181], [182]. While, the RSC-MLI topologies are widely popular in academia from the past decade, they are yet to be penetrated in commercial applications. Investigating the reasons behind it reveals that reduction in switch count in most of the configurations, in turn, reduced the switching redundancies and modularity, which further effected the utilization of dc-link, fault-tolerance and reliability. Nevertheless, there are a few configurations such as MLDCL, T-type, half-leg T-type and LDN steadily gaining their prominence and are expected to take share in future industrial applications.

## VI. CONCLUSION

In this paper an extensive review of recently reported reduced switch count multilevel inverters (RSC-MLIs) has been presented to provide a clear perspective and a technological update for researchers, engineers and manufacturers. A broad classification of RSC-MLIs into six categories with further sub classifications of various topologies are presented to provide easy selection of an appropriate converter for a particular application. The RSC-MLIs have evolved from a theoretical concept to real applications due to several remarkable features such as possibility of connecting directly to medium voltage, reduction in dc sources and semiconductor devices and their associated gate driver circuits, increased efficiency, less cost and small size. On the other side, the requirement of assorted switching devices with different ratings, reduced switching redundancies, limited fault tolerant ability, limited modularity, unequal dc voltage sharing and complex modulation schemes are yet to be addressed to increase the penetration of these converters into power market.

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