A Switched-Capacitor Charge-Balancing Analog-to-Digital Converter and Its Application to Capacitance Measurement

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Abstract—An analog-to-digital converter is developed based on the charge-balancing principle. It consists of a switched-capacitor integrator, comparator, and digital logic circuit. Driven by the two phase clock, the integrator accumulates consecutively the incremental signal charge while extracting the quantized reference charge from the accumulated signal charge each time its output becomes positive, to keep their charge balance. The ratio between the accumulated and extracted frequencies for a given period of time then provides the digital representation of an input analog signal.

A conversion accuracy higher than 14 bits can be expected from its integrated realization because the offset voltage and the finite open-loop gain of an op-amp and the parasitic capacitance have no effect upon the conversion process. It also features a small device-count integrable onto a very small chip area. Some applications are also presented to demonstrate its validity.

I. Introduction

The dual-slope and charge-balancing or incremental converters are two typical serial analog-to-digital (A/D) converters [1]. Both have the same analog circuitry consisting of an integrator and a comparator, but their principles of operation are quite different; the former is based on pulsewidth modulation, while the latter is based on delta–sigma modulation [2]. The latter is very attractive to digital data transmission because its high conversion rate permits oversampling and decimating techniques for enhancing accuracy [3]–[6].

In the instrumentation and measurement field, on the contrary, the dual-slope converter is more popular and is widely used for a digital meter [7], [8]. This is because the control logic to extract the quantized charge packet from a conventional active-*RC* integrator complicates the realization of the charge-balancing converter.

A switched capacitor manipulates the charge packet. Therefore, by replacing a conventional active-*RC* integrator with a switched capacitor one will facilitate the control logic. Based on this idea, a new charge-balancing A/D converter has been developed. Such an A/D converter has also been reported independently by Robert *et al.* [9], [10]. Compared with their incremental converter, the present converter features the simpler and gain-insensitive configuration.

Following this introductory section, Section II describes the circuit configuration and the principles of operation. The conversion accuracy when the A/D converter is fabricated in an IC form using advanced CMOS technology is estimated in Section III. Application to capacitance measurement and signal processing of intelligent capacitive transducers are presented in Section IV to demonstrate its capabilities. The paper concludes with Section V.

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II. Circuit Description

A. Unipolar Conversion

Fig. 1 shows the circuit diagram of the charge-balancing A/D converter. It consists of three main blocks; the switched-capacitor integrator comprising the op-amp A_1, two capacitors C_1 and C_2, and analog switches, the comparator comprising the op-amp A_2 and a D flip-flop (FF), and the control logic circuit comprising gates and counters. V_a is an input analog voltage, assumed positive for the time being, to be converted into an n-bit binary number with reference to the voltage V_r. ϕ and $\bar{\phi}$ are complementarily nonoverlapping two-phase clocks.

The reset pulse ϕ_R, which is generated every 2^n cycles of the two phase clock by ANDing the carry output (CO) of the modulo-2^n counter with the ϕ clock, discharges C_2. CO also clears the up-counter, thereby initiating the A/D conversion. The capacitor C_1 is then charged to V_a through M_1, M_4, and C_3, because the inverting input terminal of op-amp A_1 is virtually grounded. Closing M_3 and M_6 when Q is low, the incremental signal charge C_1V_a thus stored in C_1 is transferred onto C_2 in the next $\bar{\phi}$ phase. The capacitor C_3 samples the resultant output voltage and holds it during the next ϕ phase. This process of accumulating the incremental signal charge continues, as depicted in Fig. 2, until the integrator output becomes positive. Then, $\bar{Q}$ output of the D FF becomes a logic "1" and enables the up-counter to be incremented. At the same time, it turns M_2 "on" to charge C_1 to the reference voltage V_r through C_2 and M_6. This extracts the quantized reference charge C_1V_r from C_2, thereby forcing the integrator output

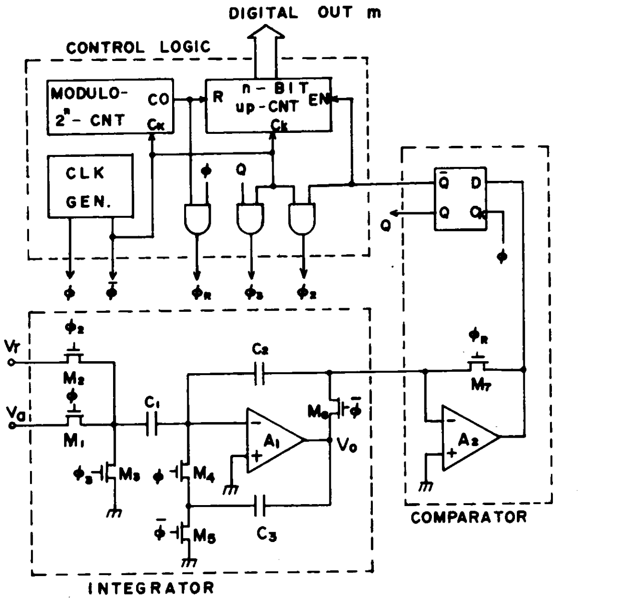

Fig. 1. The charge-balancing A/D converter for unipolar conversion.

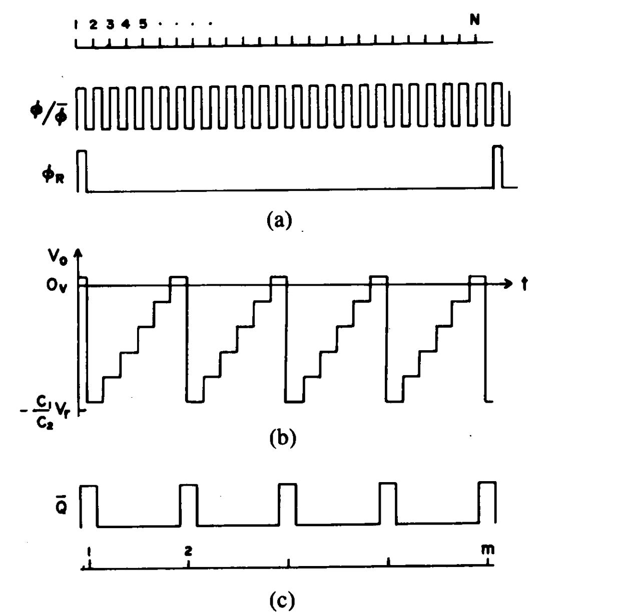

Fig. 2. (a) The clock signals and (b) the output waveforms of op-amp A_1 and of (c) D flip-flop.

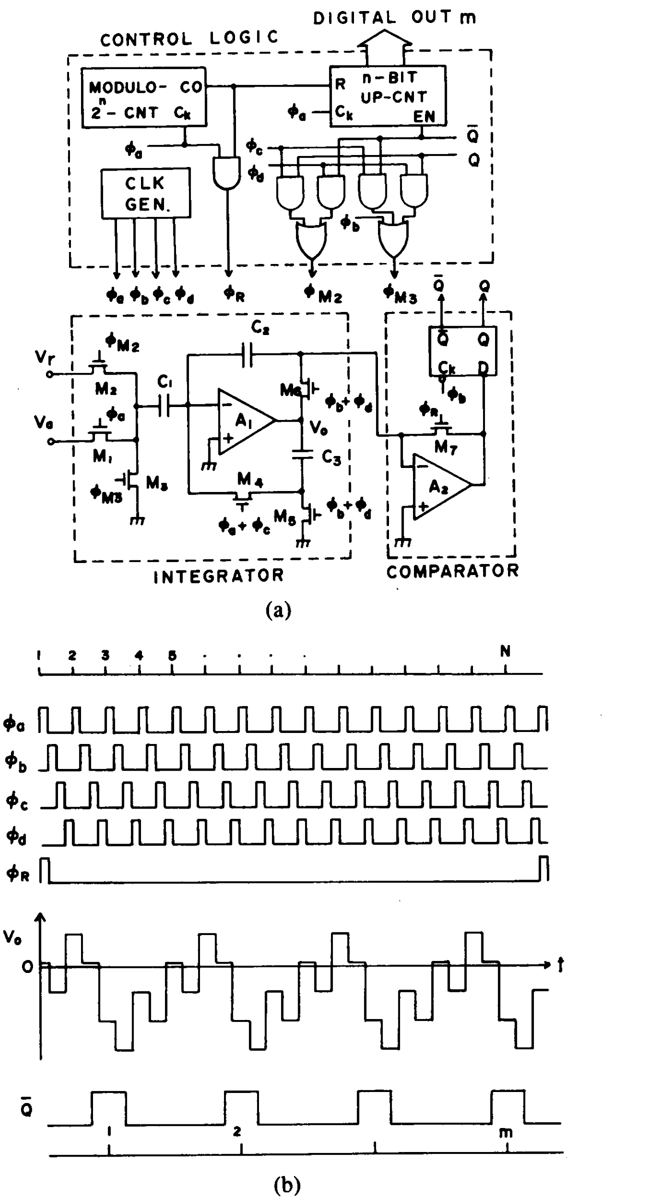

Fig. 3. (a) The charge-balancing A/D converter for bipolar conversion. (b) Timing diagram of the nonoverlapping four-phase clocks and the output voltage waveforms of op-amp A_1 and D flip-flop.

to go negative again to resume the incremental signal charge accumulation. This process of the charge accumulation and extraction is repeated until the next reset pulse ϕ_R initializes the operation.

Let the quantized reference charge C_1V_r be extracted in m times. The total reference charge extracted from C_2 is then mC_1V_r, while the total signal charge accumulated into C_2 is $2^nC_1V_a$. The output voltage of the integrator when one cycle of the A/D conversion is completed is thus given by

$$V_o = (C_1/C_2)(2^nV_a - mV_r). \tag{1}$$

Because $|V_o| < |(C_1/C_2)V_r|$, we obtain

$$(V_a/V_r) - (m/2^n) < 1 \text{ LSB} \tag{2}$$

where 1 LSB $= 1/2^n$.

Thus, counting m using the n-bit up-counter, one can get the digital (binary) representation of the input analog voltage. It is noted in (2) that the conversion is independent of the capacitance ratio C_1/C_2 and that it generates no missing code.

B. Bipolar Conversion

The circuit diagram for bipolar conversion is shown in Fig. 3(a). The analog circuitry is the same as that shown in Fig. 1, but the four-phase clock whose timing diagram is shown in Fig. 3(b) is required for driving each switch. The operation is as follows; in the ϕ_a and ϕ_b phases, op-amp A_1 operates as a noninverting integrator to accumulate the incremental signal charge C_1V_a in C_2. The integrator output in the ϕ_b phase is tested by the comparator A_2. If it is positive ($\bar{Q}$ = '1'), then the quantized reference charge C_1V_r is extracted from C_2 in the ϕ_c and ϕ_d phases and the up-counter is incremented. If the integrator output in the ϕ_b phase is negative (Q = '1'), on the other hand, then C_1V_r is accumulated upon C_2 in the ϕ_c and ϕ_d phases. To identify the operation in each phase, the output voltage V_o of op-amp A_1 and $\bar{Q}$ output of the D FF, assuming $V_a = -V_r/2$, are also depicted in Fig. 3(b). The output voltage V_o decreases by $(C_1/C_2)\,|V_a|$ in each ϕ_b phase since V_a is negative and increases or decreases by $(C_1/C_2)\,V_r$ in each ϕ_d phase depending on the $\overline{Q}$ output. This process of charge accumulation and extraction is repeated for 2^n cycles of the four-phase clock, until the next reset pulse ϕ_R initializes the A/D converter.

Let the quantized reference charge be extracted from C_2 in m counts. Then the total extracted charge is mC_1V_r, while the total charge accumulated upon C_2 is $2^nC_1V_a + (2^n - m)\,C_1V_r$. The integrator output voltage V_o at the end of conversion is thus

$$V_o = (C_1/C_2)\,[2^n(V_a + V_r) - 2mV_r]. \quad (3)$$

Because $|V_o| < |(C_1/C_2)\,V_r|$, we obtain

$$(V_a + V_r)/(2V_r) - (m/2^n) < (1/2)\,\text{LSB}. \quad (4)$$

Therefore, m counted by the up-counter gives the digital (offset binary) representation of an input analog voltage. The input analog voltage range is $-V_r \leqq V_a < V_r$. It should be noted here again that the conversion process is independent of the capacitance ratio and is monotonic.

III. Conversion Accuracy

The description in the previous section neglects such nonideal circuit performances as the offset voltages and finite open-loop gains of op-amps, parasitic capacitances, and clock feedthrough. Their effect upon the conversion accuracy is examined in this section. Only the unipolar conversion is analyzed for simplicity, but the result holds also true for the bipolar conversion.

The offset voltages V_{os1} and V_{os2} of op-amps A_1 and A_2, respectively, are detected in the reset phase by closing M_4 and M_7. The voltage V_{c2} across C_2 is then $V_{os2} - V_{os1}$. Starting with this initial voltage, the integrator produces the output voltage $V_o(i)$ in the ith cycle of unipolar conversion:

$$\begin{aligned} V_o(i) &= V_{c2}(i) + V_{os1} \\ &= (C_1/C_2)\,[iV_a - (m_{i-1} + Q_{i-1})\,V_r]/ \\ &\quad [1 + A^{-1}(1 + C_1/C_2)] + V_{os2} \end{aligned} \quad (5)$$

where m_{i-1} denotes the number of times the quantized reference charge is extracted before the ith cycle, A is the finite open-loop gain of op-amp A_1, and Q_{i-1} is the complimentary output of the D FF which assumes 1 or 0 depending on the integrator output polarity. The voltage $V_o(i)$ is compared with V_{os2} by the comparator A_2 to determine its polarity. Thus, the comparison process is independent of the offset voltages of op-amps. The denominator in (5) indicates the reduction in charge transfer efficiency from C_1 to C_2 due to the finite open-loop gain A. This reduction is common to the incremental signal and quantized reference charges. Therefore, the finite gain A has no effect upon the conversion accuracy either. This is a salient feature of the present A/D converter made possible by incorporating the holding capacitor C_3 into the integrator [11]. The integrator is also configured such that the parasitic capacitance between each node and ground has no effect upon its operation [12]. Thus, the clock feedthrough is only the error source in this converter.

Let the clock feedthrough charge referred to the inverting input terminal of op-amp A_1 be Q_f. Then the integrator output V_o' at the end of conversion is given by

$$V_o' = (C_1/C_2)\,(2^nV_a - m'V_r + 2^nQ_f/C_1) \quad (6)$$

where m' is the content of the up-counter. If $m' - m < 1$, where m is the binary representation of V_a given by (2), then the conversion is accurate down to its LSB. This requires

$$C_1V_r/Q_f > 2^{n+1}. \quad (7)$$

In an IC realization using advanced MOS technologies, the signal-to-noise charge ratio C_1V_r/Q_f as high as 5×10^4 can be obtained by accommodating the clock feedthrough compensation scheme [13] or by using the completely differential scheme [14] or the modified two phase clock [15]. It follows therefore that an accuracy higher than 14 bits can be expected from the integrated version of the present A/D converter. The digital compensation which measures the contribution of the feedthrough charge separately to subtract it from the overall result will improve the accuracy further.

IV. Application

A straightforward application of the present A/D converter is a digital voltmeter (DVM). Actually, the DVM with 0.1-percent accuracy (10-bit resolution) was realized by the prototype A/D converter built using discrete components. Besides this promising application, it can be applied to a wide range of applications which require manipulation of a charge packet. Some of them will be described in the following.

A. Capacitance Meter

The present A/D converter compares the signal charge packet C_1V_a with the reference charge packet C_1V_r to encode their ratio into a binary number. If the signal and reference charges are replaced by C_xV_r and C_sV_r, respectively, then an unknown capacitance C_x can be measured digitally with reference to a standard capacitor C_s:

$$\begin{aligned} C_x/C_s &= m/2^n = b_12^{-1} + b_22^{-2} \\ &\quad + \cdots + b_n2^{-n}. \end{aligned} \quad (8)$$

A portion of the unipolar A/D converter modified for a digital capacitance meter is shown in Fig. 4. The circuit operation is the same as that of the unipolar conversion and the capacitance ratio is given by m stored in the up-counter. Table I shows a measured example, comparing the capacitance C_{DCM} measured by the present digital capacitance meter with those C_{FTB} by a commercial four-terminal-pair bridge.[1] The discrepancies ϵ_r between them

[1]HP model 4275A multifrequency LCR meter.

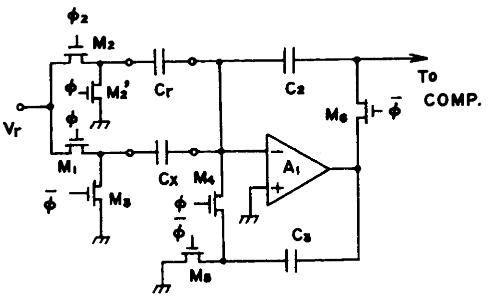

Fig. 4. The switched-capacitor integrator modified for the digital capacitance meter.

TABLE I
COMPARISON BETWEEN THE CAPACITANCE C_{DCM} MEASURED BY THE PRESENT DIGITAL CAPACITANCE METER AND THOSE C_{FTB} BY THE CONVENTIONAL FOUR-TERMINAL-PAIR BRIDGE
(C_{nom} is the nominal capacitance and ϵ_r is the relative deviation between C_{DCM} and C_{FTB})

C_{nom}[pF]	C_{FTB}[pF]	C_{DCM}[pF]	ϵ_r[%]
1	1.034	1.048	1.35
2	2.024	2.005	0.94
4	3.900	3.926	0.67
10	10.27	10.19	0.78
20	20.29	20.46	0.84
47	47.43	47.87	0.93
100	98.30	97.36	0.96
220	215.6	217.2	0.74
470	463.3	460.5	0.60
1000	971.1	966.8	0.44

are almost within 1 percent, which are attributed to the clock feedthrough. Accommodating the clock feedthrough compensation and digital calibration schemes will improve the accuracy drastically. A measurement range can be expanded by incorporating the scaled reference voltage to charge an unknown capacitor.

B. Capacitive Transducer Interface

The digital capacitance meter described above is available for signal processing of a capacitive transducer. The capacitance change of the solid-state transducer, however, is usually very small compared to its offset capacitance [16]. An accurate signal processing of such transducer thus requires its offset capacitance to be cancelled. A portion of the present unipolar A/D converter modified to meet such a requirement is shown in Fig. 5. Here, C_x represents a capacitive transducer, C_r is the reference capacitor with which the capacitance change of the transducer is to be compared, and C_c is the compensation capacitor for cancelling the offset capacitance of the transducer. In each $\bar{\phi}$ phase, the charge $C_x V_r$ stored in C_x in the preceding ϕ phase is transferred, as in the digital capacitance meter, onto C_2. At the same time, the offset charge $C_c V_r$ is extracted from C_2. Thus, the net charge accumulated onto C_2 in each $\bar{\phi}$ phase is $(C_x - C_c) V_r$. The net charge is compared with the quantized reference charge $C_r V_r$ to give the n-bit digital representation m of the capacitance change:

$$(C_x - C_c)/C_r = m/2^n. \qquad (9)$$

This interface has been applied to the humidity transducer composed of a thin polyimide film deposited onto a silicon substrate. Its structure and capacitance C_x measured by the aforementioned four-terminal-pair bridge are shown in Fig. 6(a) and (b), respectively. In the interface shown in Fig. 5, 100- and 380-pF capacitors were used for C_r and C_c, respectively. The reference voltage V_r was set to 1 V. The scale on the right-hand ordinate of Fig. 6(b) indicates the digital output of the interface in hex code representation. The result promises a digital hygrometer with excellent linearity and accuracy.

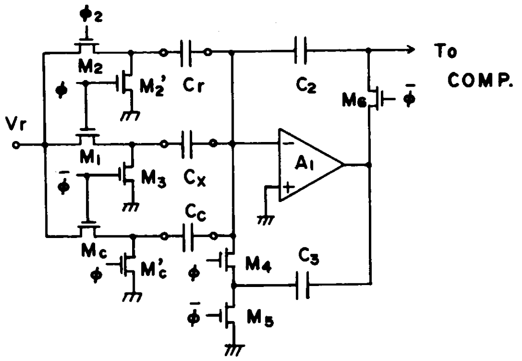

Fig. 5. The switched-capacitor integrator modified for the capacitive transducer.

For another example of the interface, the charge-balancing A/D converter has been applied to signal processing of the differential pressure transducer. The transducer, shown in Fig. 7(a), consists of two metal chambers filled with oil and separated by a diaphragm [17]. Each chamber can be represented electrically by a capacitor. The pressure difference, $\Delta P = P_H - P_L$, is then given by

$$K\Delta P = (C_L - C_H)/(C_L + C_H) \qquad (10)$$

where K is a proportional constant determined by a mechanical structure of the transducer, and C_H and C_L are capacitances of high and low pressure chambers, respectively. Detecting ΔP based on (10) is possible with the present A/D converter, but requires bipolar conversion because the numerator $C_L - C_H$ may take a negative value depending on the offset capacitance of each chamber. To be compatible with the unipolar conversion and thereby to simplify the interface, (10) is modified to

$$C_L/(C_L + C_H) = (K\Delta P + 1)/2. \qquad (11)$$

Fig. 7(b) shows that portion of the A/D converter which is modified to detect the differential pressure based on (11). With m being again the content of the n-bit up-counter, the total charge accumulated onto C_2 from C_L is $(2^n - m) C_L V_r$, while the charge extracted from C_2 is $m C_H V_r$. From the charge balance, we can get

$$K\Delta P = (2m/2^n) - 1. \qquad (12)$$

Multiplying m by 2 is accomplished by shifting the up-counter by 1 bit toward the MSB. The carry, if generated, cancels -1 term in (12). Otherwise, subtracting 1 from the shifted result is accomplished by taking the 1's complement. Therefore, the content m of the up-counter is in itself the offset binary representation of $K\Delta P$. The digital output in hex code versus the pressure difference thus ob-

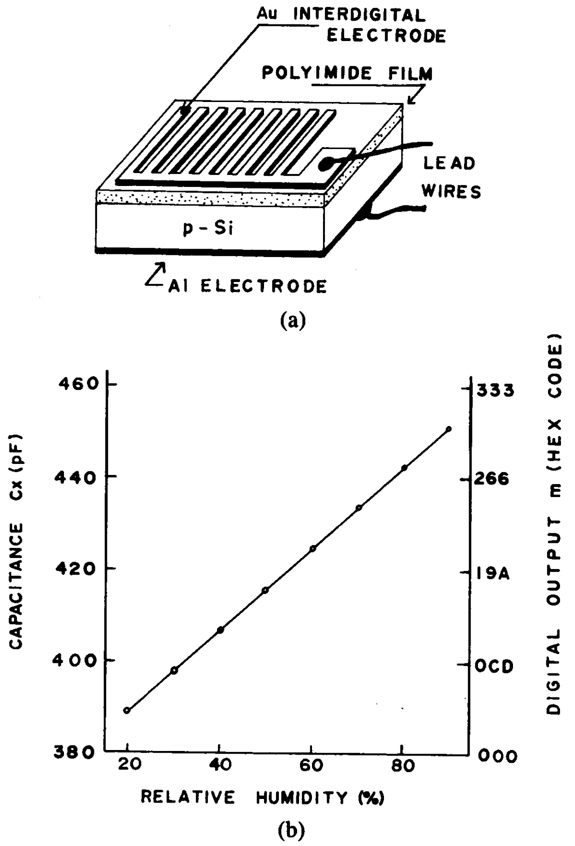

Fig. 6. (a) The structure of the humidity transducer and (b) the humidity versus capacitance C_x measured by a conventional bridge. The right-hand ordinate of (b) shows the digital output obtained by the present interface.

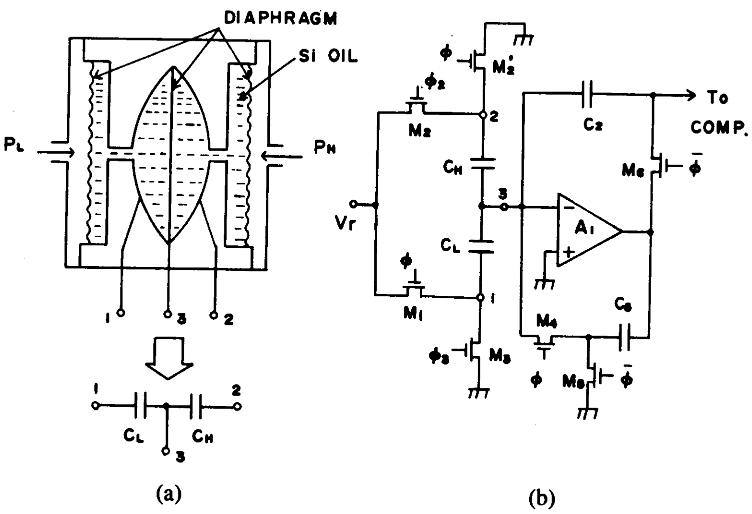

Fig. 7. (a) The structure of the differential pressure transducer and (b) the switched-capacitor integrator modified to detect the differential pressure.

tained is shown in Fig. 8 together with C_H and C_L measured by the aforementioned bridge. The digital results are in close agreement with those calculated using the measured capacitances.

V. Conclusions

A switched-capacitor A/D converter based on the charge-balancing principle has been presented. It features a small device-count integrable onto a small chip area and a high accuracy made possible by the parasitic- and gain-insensitive configuration. These features together with its

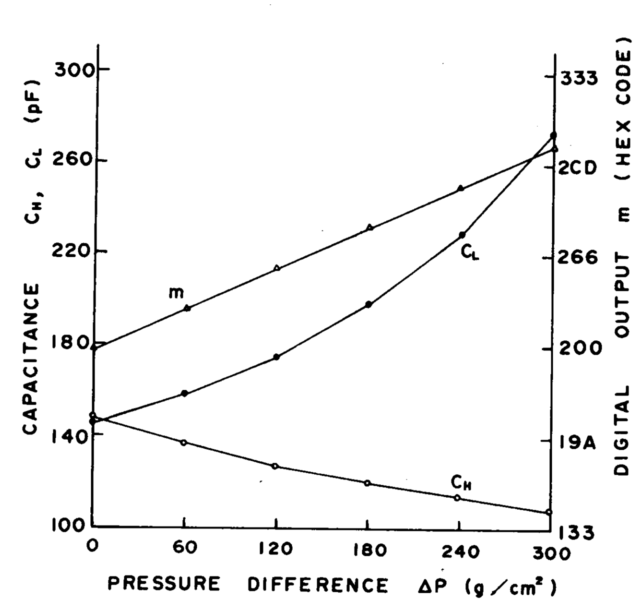

Fig. 8. Capacitances C_H and C_L versus the pressure difference. The digital output m obtained by the present interface is also shown in the right-hand ordinate.

inherent property of manipulating the charge packet make this A/D converter especially useful for interfacing capacitive transducers with a digital system. The circuit modifications and practical performance of such interfaces were also described to demonstrate its capabilities. In these applications, no technique was adopted for compensating the clock feedthrough and thus the accuracy was limited to 10 bits. Incorporating the clock feedthrough cancellation or digital calibration scheme into its integrated realization will open a wider application.

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