A SWITCHED-CAPACITOR DAC WITH ANALOG MISMATCH CORRECTION

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ABSTRACT

This paper describes a background calibration method for enhancing the accuracy and linearity of a switched-capacitor digital-to-analog converter. It can be used alone or in combination with mismatch shaping to achieve very high accuracy and linearity combined with high speed.

1. INTRODUCTION

In a number of important applications such as delta-sigma ADCs or DACs as well as pipeline or segmented data converters, low-resolution but high-linearity DACs are required. Since the linearity of the DAC is limited by the matching accuracy of its nominally equal-valued analog circuit elements (resistors, capacitors, or current sources), for more than 12-bit linearity the required matching precision is difficult to obtain. Alternative techniques have recently been developed which utilize digital circuitry to filter out the errors generated by the mismatch errors of the DAC elements [1]-[3]. However, these mismatch-shaping techniques are effective only if the sampling rate is much higher than the signal bandwidth, i.e., if the signal is greatly oversampled.

In this paper, a switched-capacitor (SC) DAC using a straightforward analog calibration process is described. The calibration is applicable even if the signal is not oversampled, and can be combined with mismatch shaping if it is.

2. SC DAC WITH ANALOG CALIBRATION

Fig. 1 shows the conceptual diagram of a DAC constructed using SC circuitry. The operation of the circuit is as follows. The input word is in a thermometer code with bits $x_1,\ x_2,\ \ldots,\ x_M$ such that if the integer value of the input word is m, the bits $x_1,\ x_2,\ \ldots,\ x_m$ equal 1, and the rest are 0. During the reset phase (Φ_1=1), the feedback capacitor C_f is discharged and all input capacitors are charged to the reference voltage V_{ref}. Next, during the conversion phase (Φ_2=1), the first m input capacitors are discharged into C_f, resulting in an output voltage $V_{out} = (mC/C_f)V_{ref}$. To avoid signal-dependent loading of V_{ref}, capacitors C_{m+1} through C_{M-1} may also be discharged to ground during this phase.

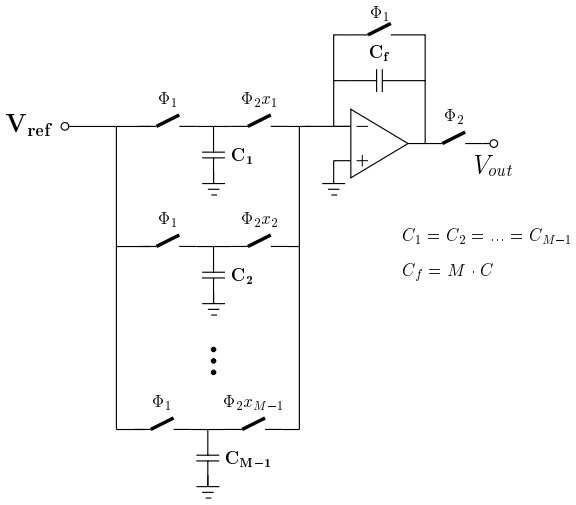

Figure 1: A switched-capacitor DAC

Since in practice the nominally equal-valued input capacitors will be mismatched, a fixed nonlinearity will be introduced. Even for a well-designed integrated circuit, this is likely to cause a total harmonic distortion which is about 0.1 % of the full-scale signal. If the circuit needs to be operated at a fast clock rate, the capacitors need to be made small, and their matching accuracy will be even lower, so not even 10-bit performance is achievable.

Analog correction of the matching errors may be achieved by using the system shown in Fig. 2, where only the second branch converting the bit x_2 is shown in detail. For an M-level DAC, M-1 identical input branches need to be connected to the virtual ground node; the ith branch contains a coarse input capacitor C_{ci} which can deliver a charge $C_{ci}V_{ref}$ into C_f, and a fine input capacitor C_{fi} which can deliver $C_{fi}V_{refi}$, where V_{refi} is an adjustable dc voltage.

During the reset phase (Φ_1=1), all input capacitors are charged to the reference voltages: C_{ci} to V_{ref} and C_{fi} to V_{refi}. Next, during the conversion phase (Φ_2=1), both capacitors C_{ci} and C_{fi} are discharged into C_f if x_i=1. To correct for the mismatch of the nominally equal-valued input capacitors, a calibration stage is used. It contains a transconductor G_m and a reference capacitor C_{ref}, and is

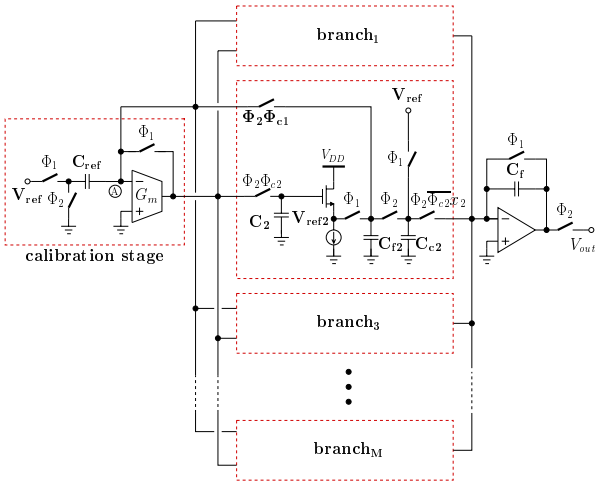

Figure 2: A switched-capacitor DAC with the proposed analog mismatch correction

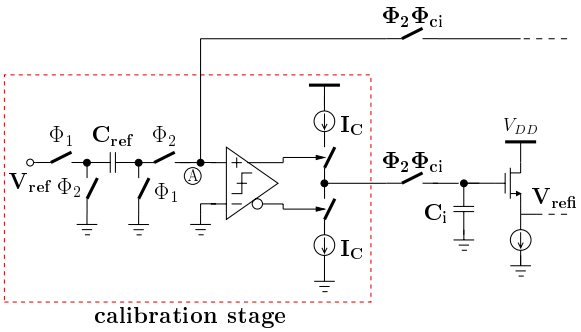

Figure 3: A switched-capacitor DAC with charge-pump calibration

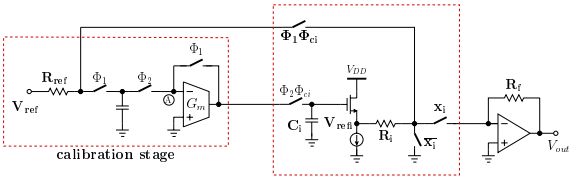

Figure 4: Resistive DAC with analog mismatch correction

shared by all input branches. It readjusts the ith reference voltage V_{refi} once every M clock periods, when the ith calibration clock phase Φ_{ci} is high, so as to make the combined charges stored in C_{ci} and C_{fi} equal to $C_{ref}V_{ref}$. To replace the branch being calibrated, an extra input branch is needed, raising the total number of input branches to M.

The calibration principle is somewhat similar to that proposed earlier by Groeneveld et al. [4], who used current copiers to calibrate the current sources of a DAC. Since it is a background process, it remains active during operation, and is able to correct for a slow drift caused, e.g., by thermal effects.

Alternatively, it is possible to perform a charge-pump-based calibration, in which the G_m stage is replaced by a comparator, as shown in Fig. 3. The calibration stage then delivers fixed amounts of charge to the capacitor C_i every M clock periods, causing V_{refi} to ramp up or down until the optimum value is found.

Although the technique is described for a unit-element DAC, it can be extended also for binary-weighted converters. With some structural changes, it can also be applied to resistive DACs, as illustrated in Fig. 4.

3. ANALYSIS OF THE CALIBRATION PROCESS

The calibration process may be analyzed by applying the law of charge conservation to the input node Ⓐ of the G_m block in the circuit of Fig. 2, at the time of transition between the Φ_1=1 and Φ_2=1 intervals. Assume that the source follower providing V_{refi} has a constant offset voltage and a gain $(1+a)$, where a is a small gain error. Then the pole z_p of the calibration system is given by

$$z_p = 1 - \frac{(1+a)C_{fi}G_mT/2}{C_i \cdot (C_{ref} + C_{ci} + C_{fi})} \qquad (1)$$

where $T = 1/f_c$ is the clock period. For stability, $|z_p| < 1$. This sets upper and lower bounds on G_m:

$$0 < G_m < 4C_i\frac{(C_{ref} + C_{ci} + C_{fi})}{C_{fi}T} \qquad (2)$$

The calibration is carried out as a background operation during the data conversion, so that the speed of its convergence is of only secondary importance. It can be shown, however, that the relative error of V_{refi} decreases by a factor $|z_p|$ in each calibration cycle. Thus, for reasonable pole values ($|z_p| < 0.9$), convergence occurs within a few hundred cycles even for very high specified accuracy. For the fastest convergence speed, the pole can be placed at $z_p = 0$, in which case only one calibration cycle is needed. However, a longer convergence time is desirable, since a higher number of iterations will make the calibration process less sensitive to noise.

The effect of the offset voltage V_{os} of G_m on the DAC linearity can also be found analytically. V_{os} introduces a charge error $V_{os}(C_{ci}+C_{fi})$. Typically, $V_{os} \approx V_{ref}/1000$, and the mismatch error of $C_{ci}+C_{fi}$ is around 0.1 - 0.2 %. Hence, the charge mismatch due to V_{os} is of the order of only a few ppm, negligible in most cases.

Another parasitic effect, which may introduce nonlinearity even for accurately matched capacitors, is the mismatch

of the clock feedthrough and charge injection charges from the switches. Using the formulas given in [5], it can easily be shown that the ratio between the injected charge q_i of a switch and the signal charge is

$$\frac{q_i}{C_{ref}V_{ref}} \approx \frac{10 f_c L^2}{\mu V_{ref}} \tag{3}$$

where L is the channel length of the switch, and μ is the carrier mobility in the channel. For typical values (say f_c = 10 MHz, V_{ref} = 1 V, L = 0.6 μm, μ = 100 cm^2/Vs), this ratio can be found to be around 3.5×10^{-4}. Since only the mismatch of these charges between the input branches affects the linearity, assuming a 10 % mismatch the resulting error will be at least 90 dB below the signal level. This corresponds to a 15-bit performance, and is acceptable for many applications.

4. PRACTICAL CONSIDERATIONS

The above discussion was aimed at explaining the basic concepts of the proposed calibration process for a simplified circuit. Thus, only single-ended circuits were shown, although for high accuracy and dynamic range a fully differential circuitry is needed. In this case, the input branches need to be duplicated, but a single calibration stage can still be used.

The nonideal effects due to the finite gain, offset and $1/f$ noise of the op-amp used in the DAC were also ignored; they can readily be corrected by using correlated double sampling techniques [6]. Finally, the circuits shown are stray sensitive, i.e., the parasitic capacitances loading the top plates of C_i, C_{ci} and C_{fi} have an influence on the operation. However, if these stray capacitances are fairly well matched, then their values and linearity are not critical to the conversion accuracy. If necessary, the circuit may also be modified for stray-insensitive operation.

As mentioned earlier, the proposed technique may be combined with dynamic element matching [3] which assigns the x_i so as to suppress the remaining mismatch errors in the signal band.

5. DESIGN EXAMPLE

To confirm the validity of the proposed technique, a 6-bit DAC circuit containing 64 unit elements was simulated with HSPICE. The circuit used C_{ref} = 1.1 pF, C_i = 1 pF, C_f = 0.2 pF and C_c = 1 pF, for a clock rate of 50 MHz. A random mismatch with a standard deviation of 1% was introduced into the C_{fi} and C_{ci} values. From eq. (2), the maximum G_m is 2.2 mA/V; for this simulation, G_m = 0.88 mA/V was chosen, setting the calibration behavior to a slightly overdamped response.

A full-scale digital ramp was applied to the DAC. Fig. 5a shows the DAC output voltage, Fig. 5b the differential nonlinearity (DNL), and Fig. 5c the integral nonlinearity (INL) characteristics. (The DNL is the variation of the analog output step from the ideal value of 1 LSB; the INL is the maximum deviation of the transfer curve from a straight line, after gain and offset errors are removed.) During the first 64 clock periods the circuit operated without correction, and the DNL and INL were large: referred to the full scale, they were 130 ppm and 258 ppm, respectively. After only 4 calibration periods, they became DNL = 0.72 ppm and INL = 3.71 ppm. This is approximately equivalent to an 18-bit performance.

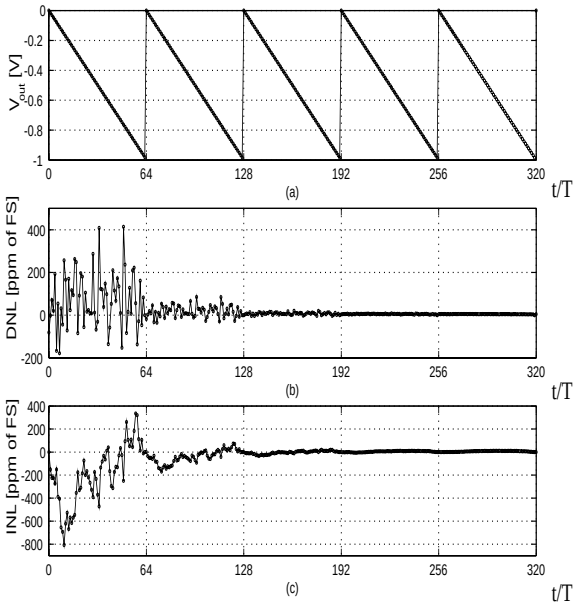

Figure 5: Simulation: a) Output voltage; b) DNL; c) INL

6. CONCLUSIONS

A simple analog background calibration technique was described for switched-capacitor DACs. It compensates for the mismatch of the capacitors, and should allow the realization of fast and accurate data conversion, alone or in combination with a mismatch-shaping algorithm.

Acknowledgement

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7. REFERENCES

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