A Switched-Capacitor Digital Capacitance Bridge

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Abstract—**A switched-capacitor bridge has been developed for capacitance measurements. It consists of four arms connected between the low-impedance output and virtual ground nodes of an op-amp, and hence is insensitive to parasitic capacitances. The capacitance to be measured is first given a proportional charge. This charge is then compared successively with charges quantized by means of a programmable binary-weighted capacitor array, until a balance is reached. This digital balance operation makes it possible to accomodate an automatic calibration scheme, which affords, in conjunction with the parasitic-insensitive configuration, an accurate measurement. Error analysis has shown that a 10-bit quantization accuracy and a relative error as small as 0.1 percent are attainable when the bridge is fabricated in LSI circuit form using present MOS technologies. A prototype bridge built using discrete components has confirmed the principles of operation. Examples of measurement are also given.**

I. Introduction

BALANCING a bridge by nulling a meter is a fundamental procedure for measuring a capacitance using the transformer-ratio-arm or Schering bridge [1]. A measurement accuracy of 1 part/10^6 is attainable by this method, but the procedure is cumbersome and time consuming because of the manual balance operation involved. The four-terminal-pair method [2] has eliminated the manual operation by detecting the voltage across and the current through the impedance to be measured. The price paid for the automated measurement is the complicated signal processing necessary for calculating the impedance. In addition, this method requires a special sample holder because it is susceptible to parasitic capacitances [3]. This makes it difficult to apply this method to the characterization of integrated MOS capacitors in which parasitic capacitances are inevitable.

McCreary and Sealer have proposed a novel technique to characterize binary-weighted MOS capacitor arrays [4]. Based on the voltage-divider principle, their method has facilitated the capacitor ratio measurement, but it cannot measure the absolute value of each capacitor.

In a recent publication [5], a switched-capacitor circuit has been proposed for digital multiplication. This circuit has been modified to form a capacitance bridge which allows quick measurement of the absolute value as well as the ratio of capacitors. This paper describes the bridge configuration, the principles of measurement, and calculates the expected accuracy. A prototype bridge implemented using discrete components and some examples of measurement are also presented.

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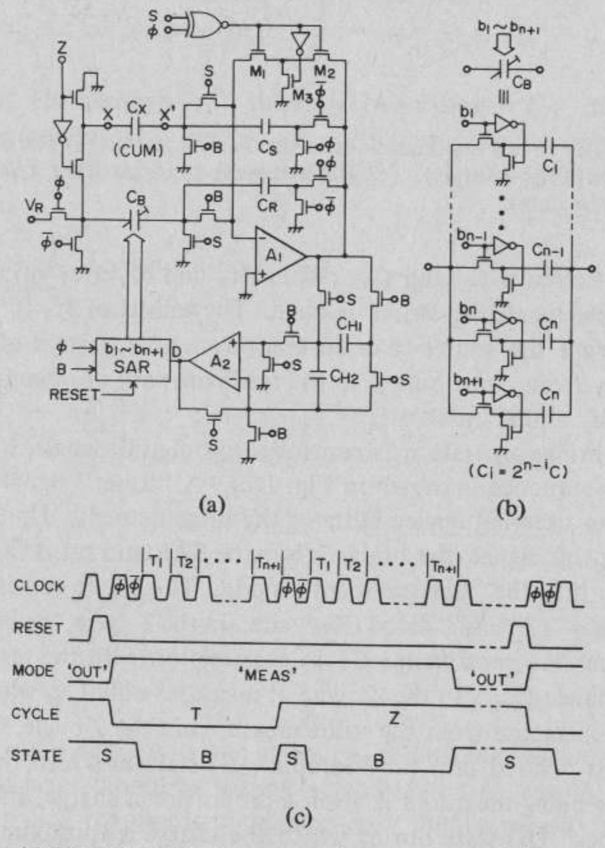
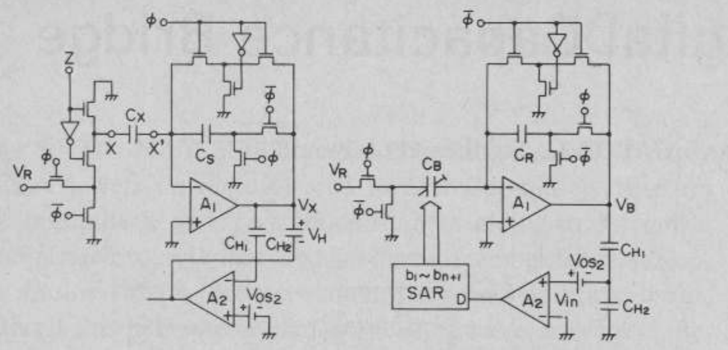


Fig. 1. (a) The schematic diagram of the capacitance bridge. CUM denotes the "Capacitor Under Measurement" and SAR the "Successive-Approximation Register." (b) The configuration of the programmable binary-weighted capacitor array C_B. (c) The timing sequence of the digital signals controlling the bridge operation.

II. The Capacitance Bridge

Fig. 1(a) shows the schematic diagram of the capacitance bridge. The capacitor C_X under measurement (CUM) is connected between the terminals X-X'. Its value is to be measured with reference to C_S. Therefore, C_S must be a standard capacitor of known value when an absolute value measurement is desired. C_B is a programmable binary-weighted capacitor array whose configuration is shown in Fig. 1(b). C_B is related to the reference capacitor C_R. These four capacitors C_X, C_S, C_B, and C_R form the four arms of the bridge. Since each arm is connected between a voltage source and the virtual ground of op-amp A_1, the parasitic capacitances to ground have no effect upon the bridge balance if op-amp A_1 is ideal. The holding capacitor C_{H_2} corresponds to the detector arm of a conventional bridge. Controlled by the signal from op-amp A_2, the successive-approximation registers SAR programs C_B so that the charge on C_{H_2} becomes zero, thereby bringing the bridge into a balance.

The transistors M_1, M_2, and M_3 form a reset switch. When M_1 and M_2 are "on" and M_3 is "off," the switch is closed and



(a) (b)

Fig. 2. The circuit configurations in the S and B states: (a) The offset-free amplifier (S state). (b) The successive-approximation A/D converter (B state).

it short circuits C_S and C_R. When M_1 and M_2 are "off," on the other hand, the switch is open. The transistor M_3 is "on" to prevent the source-to-drain feedthrough capacitors of M_1 and M_2 from contributing to the feedback path of op-amp A_1 when M_1 and M_2 are "off."

The bridge operation is controlled by digital signals, whose timing sequence is shown in Fig. 1(c). A "Reset" signal sent from an external device initiates the measurement. Upon receiving this signal, the bridge clears the SAR and turns the operation into the "Measurement" mode. This mode consists of the "Test" (T) and "Zero" (Z) cycles. In the T cycle, the bridge measures the capacitance C_X in conjunction with the residual capacitance C_{res}. In the Z cycle, it measures only C_{res} which is then subtracted from the value measured in the T cycle. Each cycle is divided into the "Sample" (S) state in which the capacitor being measured is given a proportional charge, and the "Balance" (B) state during which the charge is approximately balanced with a charge quantized by means of a successive-approximation A/D conversion. When the B state in the Z cycle is completed, the operation changes into the "Out" mode. The capacitance value C_X is then available in the SAR in binary form. This mode continues until the next reset signal starts a new cycle of measurement. The operation in the T cycle will be next described in detail.

A. Operation in the S State of the T Cycle

In this state, $S = 1$ and $B = 0$. Thus the capacitors C_X and C_S are connected to the inverting input terminal of op-amp A_1 to form an offset-free noninverting amplifier [6]. Since $Z = 0$, the input of this circuit is the reference voltage V_R in the $\bar{\phi} = 1$ phase, as shown in Fig. 2(a). The output voltage is therefore

$$V_X = (C_X/C_S)\,V_R. \tag{1}$$

The op-amp A_2 forms a voltage follower with a grounded input. Its output is thus its own input-referred offset voltage V_{os_2}. The two holding capacitors C_{H_1} and C_{H_2} are connected in parallel in this state. Their top and bottom plates are driven by op-amps A_1 and A_2, respectively. Therefore, the voltages V_H across C_{H_2} is $V_X - V_{\text{os}_2}$. This voltage represents the initial voltage of C_{H_2} during the subsequent B state if the circuit condition is ideal. The operation under nonideal conditions will be described in Section III.

B. Operation in the B State of the T Cycle

Since now $B = 1$ and $S = 0$, the bridge contains C_B and C_R in place of C_X and C_S, respectively. The op-amp A_1 then forms an offset-free D/A converter. C_{H_1} and C_{H_2} are now connected in series, holding the voltage V_H stored in the previous S state. The op-amp A_2 now operates as a comparator. The whole circuit, including the SAR, is shown in Fig. 2(b). It forms a successive-approximation A/D converter [8]; the voltage to be converted is $V_H + V_{\text{os}_2} = V_X$.

The A/D conversion is performed as follows. In time slot $T_i (i = 1, 2, \cdots, n+1)$, the ith bit of the SAR (b_i) is temporarily set to 1, while the previously tested $i - 1$ values of b are stored. The capacitance of the array C_B is then

$$C_B^{(i)} = \sum_{j=1}^{i-1} b_j \cdot 2^{n-j} C + 2^{n-i} C. \tag{2}$$

Charging this capacitor to the reference voltage V_R in the $\phi = 1$ phase, the D/A converter produces an output

$$V_B = -(C_B^{(i)}/C_R)\,V_R. \tag{3}$$

This tentative output value is divided by capacitors C_{H_1} and C_{H_2}. The input voltage V_{in} of the comparator is then

$$V_{\text{in}} = V_H + V_{\text{os}_2} + \frac{C_{H_1}}{C_{H_1} + C_{H_2}} V_B$$

$$= \left[\frac{C_X}{C_S} - \frac{C_{H_1}}{C_{H_1} + C_{H_2}} \cdot \frac{C_B^{(i)}}{C_R}\right] V_R. \tag{4}$$

Depending on the polarity of V_{in}, the SAR keeps b_i as 1 (if V_{in} is positive) or resets it to 0 (if V_{in} is negative). Repeating this process $n + 1$ times makes V_{in} approximately zero, so that

$$\frac{C_X}{C_S} \simeq \frac{C_{H_1}}{C_{H_1} + C_{H_2}} \cdot \frac{C_B}{C_R} \tag{5}$$

holds, where

$$C_B = \sum_{i=1}^{n} b_i \cdot 2^{n-i} C + b_{n+1} C. \tag{6}$$

When $C_{H_1} = C_{H_2}$ and $C_R = 2^{n-1} C$, the SAR stores the ratio C_X/C_S (i.e., the capacitance C_X scaled by C_S) in binary form

$$C_X/C_S = b_1 \cdot 2^{-1} + b_2 \cdot 2^{-2} + \cdots + b_n \cdot 2^{-n} + b_{n+1} \cdot 2^{-n}. \tag{7}$$

It is worth noting here that the above operation is not affected by op-amp offset voltages if the open-loop gains of op-amps A_1 and A_2 are sufficiently high. Therefore, the bridge can be fabricated in a fully integrated form by MOS IC technologies.

III. Accuracy Estimate

The operation of the practical bridge circuit is affected by many error sources, such as mismatches in the capacitance ratio between C_B and C_R, the offset voltages and finite gains of op-amps A_1 and A_2, parasitic capacitances, and the feedthrough of the clock signals. These nonideal circuit conditions disturb the ideal balance condition, imposing a limit on the measure-

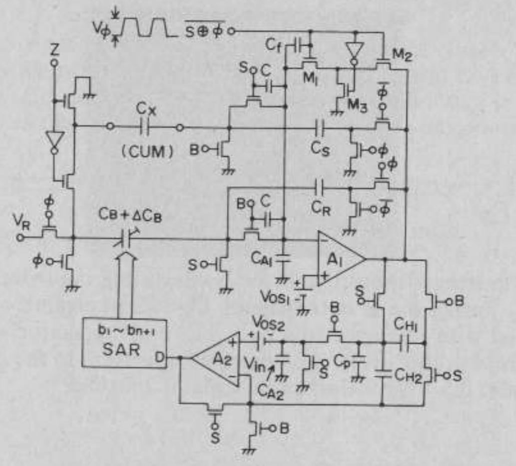


Fig. 3. The practical bridge circuit, including parasitic elements.

ment accuracy. In this section, we calculate the estimated accuracy when all of the bridge circuit (except C_X and C_S) is implemented by MOS IC process.

The bridge in Fig. 1(a) contains, in fact, many parasitic capacitances including the gate-source and gate-drain feedthrough capacitances of the MOS switches. Those residual capacitances, however, which are connected to the low-impedance nodes (except to virtual grounds) have no effect on the bridge balance. Furthermore, some of the feedthrough capacitances have matched couterparts driven by a complementary clock signal, such as C_ϵ and C_δ in Fig. 3. The feedthrough charges due to these paired capacitances can be neglected in a first-order approximation because they tend to cancel each other. Extending the above considerations into the overall circuit and including the other nonideal effects, we find the practical circuit model of the bridge shown in Fig. 3. In this figure, C_f is the feedthrough capacitance of M_1, C_p is the combined top-plate stray capacitance of C_{H_1} and C_{H_2}, and C_{A_1} and C_{A_2} are the input capacitances of op-amps A_1 and A_2, respectively. The mismatch between C_B and C_R is represented by ΔC_B.

The output voltage of op-amp A_1 in the $\overline{\phi} = 1$ phase of the S state is now, assuming $Z = 0$

$$V_X' = \frac{C_X V_R + C_f V_\phi + C_{\mathrm{TS}} V_{\mathrm{os}_1}/(1 + A_1)}{C_S(1 + C_{\mathrm{TS}}/C_S A_1)} \tag{8}$$

where V_ϕ is the amplitude of the clock signal applied to the reset transistor M_1, and

$$C_{\mathrm{TS}} = C_X + C_S + C_f + C_\epsilon + C_\delta + C_{A_1} \tag{9}$$

is the sum of the capacitances connected to the inverting input terminal of A_1 in the S state. The voltage follower A_2 produces the output voltage

$$V_A' = \frac{A_2}{1 + A_2} V_{\mathrm{os}_2}. \tag{10}$$

The voltage across the holding capacitors C_{H_1} and C_{H_2} is thus $V_X' - V_A'$, while that across C_p is V_X'.

When the successive-approximation A/D conversion is completed, op-amp A_1 produces the output voltage

$$V_B' = \frac{-(C_B + \Delta C_B) V_R + C_f V_\phi + C_{\mathrm{TB}} V_{\mathrm{os}_1}/(1 + A_1)}{C_R(1 + C_{\mathrm{TB}}/C_R A_1)}. \tag{11}$$

Here

$$C_{\mathrm{TB}} = C_{\mathrm{BT}} + C_R + C_f + C_\epsilon + C_\delta + C_{A_1} \tag{12}$$

is the sum of the capacitances connected to the inverting input terminal of A_1 in the B state, and $C_{\mathrm{BT}} = 2^n C$ is the total capacitance of the array C_B.

The op-amp A_2 and the SAR balance the bridge so that

$$V_{\mathrm{in}} = \frac{2C_H(V_H' - V_A') + C_p V_X' + C_H V_B'}{2C_H + C_p + C_{A_2}} + V_{\mathrm{os}_2} = 0 \tag{13}$$

holds. In deriving (13), the mismatch between C_{H_1} and C_{H_2} is lumped into C_p and thus $C_{H_1} = C_{H_2} = C_H$ is assumed without loss of generality. Substituting (8), (10), and (11) into (13), we have

$$C_{\mathrm{meas}} = \frac{C_S(C_B + \Delta C_B)}{2C_R} + \epsilon C_X + C_{\mathrm{res}} \tag{14}$$

where

$$\epsilon = \left[1 + \frac{C_p}{2C_H}\right]\left[1 + \frac{1}{A_1}\cdot\frac{C_{\mathrm{TB}}}{C_R}\right] \Big/ \left[1 + \frac{1}{A_1}\cdot\frac{C_{\mathrm{TS}}}{C_S}\right] - 1 \tag{15}$$

$$C_{\mathrm{res}} = \left[1 + \epsilon + \frac{C_S}{2C_R}\right]\frac{C_f V_\phi}{V_R} + \left[1 + \frac{(1+\epsilon)C_{\mathrm{TS}}}{C_S}\right] \cdot \frac{C_S V_{\mathrm{os}_1}}{(1 + A_1)V_R} + \left[\frac{1}{1 + A_2} + \frac{C_p + C_{A_2}}{2C_H}\right]\frac{C_S V_{\mathrm{os}_2}}{V_R}. \tag{16}$$

$C_B + \Delta C_B$ represents the measured capacitance including the digital error caused by the mismatch between C_B and C_R, while $\epsilon C_X + C_{\mathrm{res}}$ represents the analog error due to parasitic capacitances, clock feedthrough, and the nonideal performances of op-amps A_1 and A_2. They will be discussed separately in the following.

A. Digital Error

Each capacitor in the array C_B is assumed to be fabricated by connecting an appropriate number of MOS unit capacitors of magnitude C in parallel. The error in each capacitor is assumed to be random, normally distributed, and uncorrelated. The error charge ΔQ_B in the array C_B due to the capacitance error is then given by

$$\Delta Q_B = \sqrt{\sum_{i=1}^{n+1} (b_i \cdot \Delta C_i)^2}\; V_R \tag{17}$$

where ΔC_i is the standard deviation of each capacitor. If this error charge is smaller than half of that held in the LSB capacitor, then the A/D conversion process is monotonic and the digital output is accurate down to its LSB. Formulating this in terms of the capacitance mismatch, we have the condition

$$\sqrt{\sum_{i=1}^{n+1} (\Delta C_i / C_{\mathrm{BT}})^2} \leqslant 2^{-(n+1)}. \tag{18}$$

Each term under the square root can be estimated by using the data presented by McCreary [7]: $\Delta C_1/C_{\mathrm{BT}} = 0.03$ percent, $\Delta C_2/C_{\mathrm{BT}} = 0.02$ percent, $\Delta C_3/C_{\mathrm{BT}} = 0.015$ percent, and so on. Substituting these values into (18), we find that the quantization accuracy obtainable with present MOS technologies is 10 bits [8].

B. Analog Error

The analog error can be described in terms of the relative error ϵ and the residual (or offset) error C_{res}. Noting that $C_{\text{TB}}/C_R = 2$, we have from (15)

$$\epsilon \simeq C_p/2C_H. \tag{19}$$

The top-plate stray capacitance C_p ranges from 0.1 to 1 percent of C_H, depending on the capacitor size and technology [9]. Therefore, the relative error can be reduced to a value as small as 0.1 percent.

To obtain a rough estimate of the residual capacitance C_{res}, suppose that we are measuring a small capacitance using a 1-pF standard capacitor for C_S. Assume also the following pessimistic values for the op-amp and circuit parameters: $A_1 = A_2 = 60$ dB, $V_{\text{os}_1} = V_{\text{os}_2} = 30$ mV, $C_{A_1} = C_{A_2} = 1$ pF, $C_f = C_\epsilon = C_\delta = 10$ fF, $(C_p + C_{A_2})/2C_H = 10^{-3}$, $V_R = 3$ V, $V_\phi/V_R = 4$, and $C_S << 2C_R$. Then, the residual capacitance due to the clock feedthrough is 40 fF, while that due to the offset voltages of the op-amps is about $5 \times 10^{-5}\ C_S$, although its precise value depends on C_X. This result indicates that the feedthrough component dominates C_{res}, and thus C_{res} is positive irrespective of the offset voltage polarity.

Consider now the bridge operation in the Z cycle. Since now $Z = 1$, C_X is disconnected from the reference source and is grounded. Therefore, the first term in the numerator of (8) vanishes and thus C_{meas} in (14) equals C_{res}; that is, the bridge in the Z cycle measures the residual capacitance which should be subtracted from the value measured in the T cycle. This self-calibrating ability allows the precise measurement of small capacitances.

Summarizing this section, we can conclude that a 10-bit quantization accuracy and a relative error as small as 0.1 percent is attainable with the integrated version of the bridge.

IV. Measurement Examples

A prototype bridge has been built using one half of an LM347 quad JFET op-amp chip, MC14066 CMOS analog switches, and discrete capacitors. The capacitor array was controlled by 10 bits. To reduce the capacitance spread in the array, a split reference source was incorporated into the bridge. The source supplied 3.2 V and 0.1 ($= 3.2/2^5$) V to two 5-bit arrays, each consisting of 4-, 2-, 1-, 0.5-, and 0.25-nF capacitors. These two arrays were combined so that the array driven by 3.2-V source formed the upper half, and that driven by 0.1-V source the lower half, of the 10-bit array. Another 0.25-nF capacitor was incorporated into the lower half of the array, to form another LSB. Capacitors C_R, C_{H_1}, and C_{H_2} were chosen to be 4 nF.

Fig. 4 shows the voltage waveforms observable at the noninverting input terminal of op-amp A_2 during the B state when a ceramic capacitor (nominal value 2 pF) was measured with reference to a $C_S = 11.71$ pF capacitor. In the figure, the $\phi = 1$ phase in time slot T_i ($i = 1, 2, \cdots, 11$) is indicated by b_i so that each bit can be identified by the voltage level. Also shown (indicated by V_X) is the voltage stored in C_{H_2} in the previous S state. The upper trace shows the waveform in the T cycle. Inspecting the voltage levels[1] in the b_i phases, one obtains the ratio $(C_X + C_{\text{res}})/C_S = (00\ 111\ 001\ 100)_B = 115/512$. The lower trace shows the waveform in the Z cycle. Now one obtains the ratio $C_{\text{res}}/C_S = (00\ 001\ 110\ 000)_B = 7/128$. Thus $C_X = 1.99$ pF and $C_{\text{res}} = 0.64$ pF. The measured capacitance of C_X agrees exactly with that measured by a commercially available four-terminal-pair bridge. This bridge displays the result in a four-digit BCD form and its measurement error is 0.1 percent + 3 LSB. The measured residual capacitance, which is ten times larger than that estimated in the previous section, was found experimentally to be mostly due to the large clock feedthrough of the CMOS analog switch used for the reset transistor M_1 which is connected to the virtual ground created by op-amp A_1.

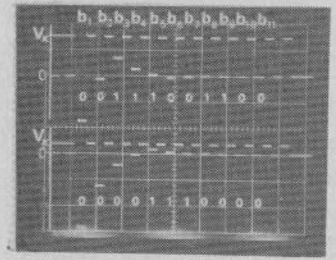


Fig. 4. Waveforms appearing at the noninverting input terminal of op-amp A_2 during the $\bar{B}$ state, when a $C_X \simeq 2$ pf ceramic capacitor was measured with reference to a $C_S = 11.71$ pF capacitor. Upper trace: waveform in the T cycle. Lower trace: waveform in the Z cycle. Vertical scale: 0.5 V/div. Horizontal scale: 0.2 ms/div.

A large number of capacitors were measured, and the results were compared with those obtained by the abovementioned commercial bridge. Capacitors ranging from 10 pF to 1 μF in decade steps were used for C_S, so that C_X/C_S was less than 1. Table I lists some of the results. It can be seen that the discrepancies between the measured results are mostly within 1 percent, although they tend to increase with decreasing capacitance. This probably can be attributed to the large clock feedthrough of the MOS switches, which violates the assumption that the charges due to paired feedthrough capacitances are negligible. In an LSI realization, these error sources will be greatly reduced.

V. Conclusions

An automatic switched-capacitor bridge, which allows the precise measurements of discrete and MOS IC capacitors, has been described. Error analysis has shown that a 10-bit quantization accuracy and a relative error as small as 0.1 percent are attainable by fabricating the bridge using presently available MOS technologies. A prototype bridge, implemented using discrete components, has confirmed the principles of opera-

[1] For b_7–b_{11}, the values are too small to show the sign of the signal. However, they are sufficient to drive the comparator op-amp A_2 unambiguously.

TABLE I
COMPARISON BETWEEN THE CAPACITANCES C_{SCB} MEASURED BY THE PRESENT SWITCHED-CAPACITOR BRIDGE AND THOSE C_{FTB} BY THE COMMERCIAL FOUR-TERMINAL-PAIR BRIDGE
(C_{nom} denotes the nominal capacitance and ϵ_r is the deviation between C_{SCB} and C_{FTB})

C_{nom} (pF)	C_{SCB} (pF)	C_{FTB} (pF)	ϵ_r (%)
1	1.062	1.044	1.72
2	1.960	1.992	1.61
4	4.324	4.227	1.10
10	10.42	10.39	0.29
22	21.74	21.95	0.96
47	45.48	45.42	0.13
100	103.5	102.8	0.68
220	206.1	205.4	0.34
470	455.8	453.3	0.55
1000	960.5	952.4	0.85
2200	2450	2448	0.08
4700	4528	4518	0.22
10000	10616	10530	0.82
22000	23016	23170	0.65
40000	38695	38350	0.90

tion. Incorporating a split reference source, a standard capacitor bank, and an automatic range-selecting circuit will provide the bridge with a wide measurement range. The extension to the measurement of grounded capacitors is another future problem.

The bridge described here features a circuit configuration suitable for LSI realization and high accuracy made possible by the digital balance operation and the parasitic-insensitive configuration. Therefore, it is also useful for the interface for "smart" capacitive transducers.

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