A Switched-Capacitor Digital Capacitance Meter

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Abstract—**A digital capacitance meter has been developed based on the switched-capacitor cyclic analog-to-digital (A/D) converter. It consists of the analog arithmetic and sample/hold (S/H) circuits. The arithmetic circuit first samples the capacitance to be measured in a form of its proportional voltage. This voltage is then converted into a binary number by the A/D converter. The whole operation is insensitive to parasitic capacitances, offset voltages of op amps, and the capacitance mismatch involved in the circuit. Therefore, the proposed meter permits an accurate capacitance measurement. Error analysis shows that 12-bit accuracy can be expected by realizing the meter in an IC form. A prototype meter built using discrete components and examples of measurement are also given.**

I. Introduction

A CAPACITANCE measurement is indispensable for characterizing *RC*-active and switched-capacitor circuits and capacitive transducers. Conventional methods using Schering, transformer-ratio arm, or four-terminal-pair bridge are useful for the measurement of discrete capacitors [1], [2]. They are, however, not applicable to integrated MOS capacitors, because they cannot separate contributions of parasitic capacitances.

The accurate measurement of integrated MOS capacitors is only possible by the on-chip built-in measuring system with digital output. Two such candidates have been reported so far [3], [4], but they are applicable only to floating capacitors. In addition, the chip area required for the implementation is appreciable because of the large device count.

To eliminate these difficulties, a new capacitance meter has been developed based on the switched-capacitor cyclic analog-to-digital (A/D) converter [5]. This paper describes the meter configuration, the principles of measurement, and the expected accuracy when it is realized in an IC form. A prototype meter built using discrete components and examples of measurement are also presented.

II. Meter Configuration

Fig. 1 shows the schematic diagram of the digital capacitance meter. It consists of two main parts: the analog arithmetic circuit formed by op-amp A_1 and two capacitors C_1 and C_2, and the sample/hold (S/H) circuit formed by op-amp A_2 and capacitor C_3. The capacitor under measurement (CUM) is connected between the terminals X_F–X_F' if it is floating, or to the terminal X_G if it is grounded.

Manuscript received October 7, 1985; revised April 7, 1986.

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IEEE Log Number 8610229.

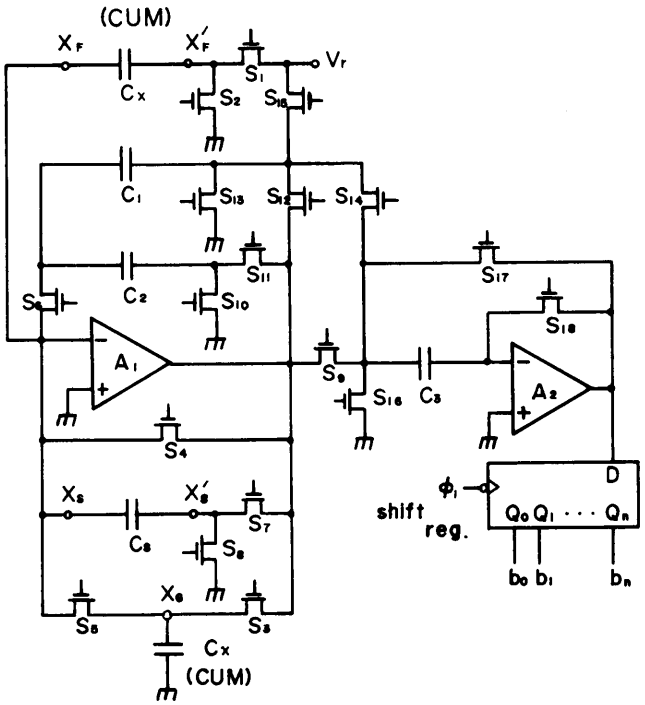

Fig. 1. The schematic diagram of the digital capacitance meter.

Its value is to be measured with reference to the capacitor C_S connected between the terminals X_S–X_S'. V_r is the reference voltage. It may assume any value, but having its voltage as high as possible is preferable to enhance measurement accuracy, unless this causes saturation of the op amps.

Meter operation is controlled by digital signals, whose timing is shown in Fig. 2. A "reset" signal initializes the meter by closing all the even-numbered switches except S_{14} in Fig. 1. The mode signal distinguishes between the "sample" state in which the arithmetic circuit samples the voltage proportional to the capacitance ratio C_X/C_S and the "convert" state in which the whole circuit performs the cyclic A/D conversion of the voltage, sampled in the preceding "sample" state, into a binary number. Driving the switches, the nonoverlapping five-phase clock ϕ_i ($i = 1, 2, \cdots, 5$) manages the operation in each state.

A. Operation in the "Sample" State

The analog arithmetic circuit forms the amplifier in this state. Its configuration depends on which capacitor, a floating or a grounded capacitor, is to be measured.

Fig. 3(a) shows the amplifier configuration for a floating-capacitor measurement. The clock signal which drives each switch is also shown next to its control terminal to identify the following operation in each phase. The switch

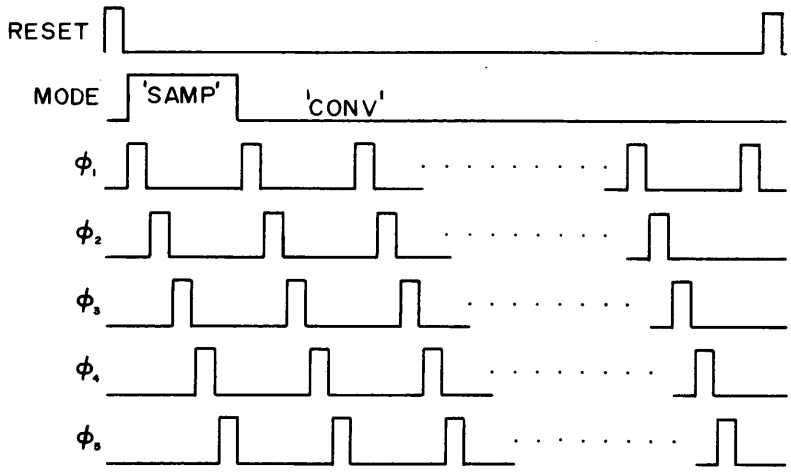

Fig. 2. Timing diagram of digital signals controlling the meter operation.

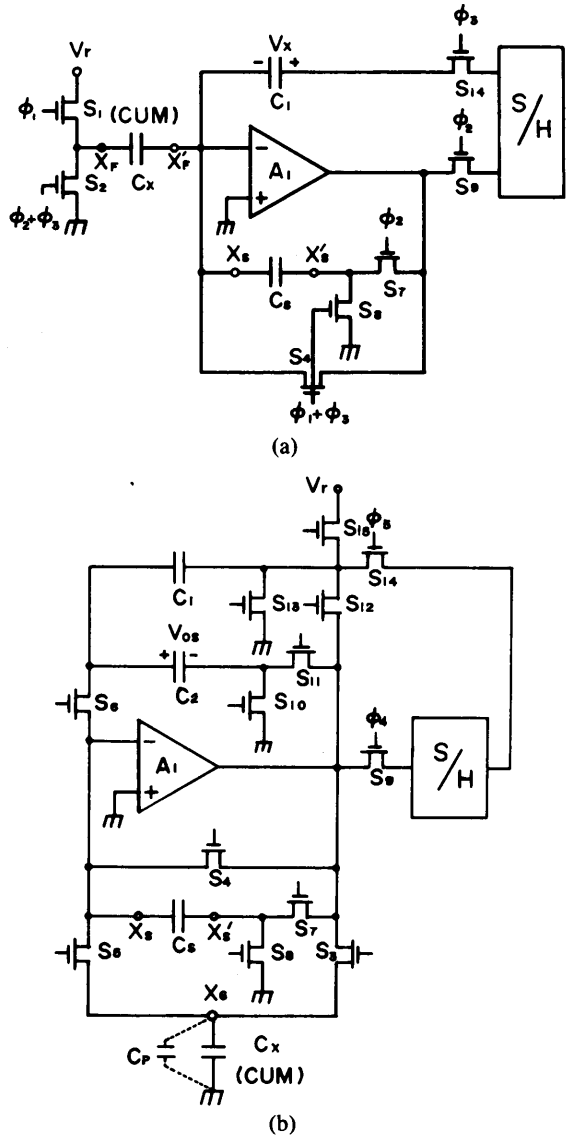

Fig. 3. The circuit configurations in the "sample" state for (a) floating- and (b) grounded-capacitor measurements.

S_6 is kept ON during this state and hence omitted. In the ϕ_1 phase, C_X is charged to the reference voltage V_r, while C_S is discharged to ground. In the next ϕ_2 phase, the charge stored in C_X is transferred to C_S. This produces the voltage V_x:

$$V_x = (C_X/C_S)V_r. \quad (1)$$

TABLE I
SWITCHING SEQUENCE IN THE "SAMPLE" STATE FOR GROUNDED-CAPACITOR MEASUREMENT

ϕ \ S	S_3	S_4	S_5	S_6	S_7	S_8	S_{10}	S_{11}	S_{12}	S_{13}	S_{15}
ϕ_1				1		1		1			1
ϕ_2		1		1		1				1	
ϕ_3	1			1		1	1		1		
ϕ_4			1		1		1				
ϕ_5		1		1		1	1				

This voltage is sampled and held by the S/H circuit. In the ϕ_3 phase, the S/H circuit charges C_1 to V_x through S_{14} and S_4, while the arithmetic circuit discharges C_2 and C_S.

This completes the operation in the "sample" state. The capacitors C_1 and C_3 hold the voltage V_x until the subsequent "convert" state. It is noted here that the above operation is insensitive to both the offset voltages of op amps and parasitic capacitances, and thus V_x does not include these nonideal components [6], [7].

The amplifier configuration for grounded-capacitor measurement is shown in Fig. 3(b). A somewhat elaborate switching sequence, which is shown in Table I, is adopted to assure op-amp A_1 of the offset-free amplification. The "1" in this table marks those switches that are ON in the corresponding phase. Referring to this table, one can identify the operation in each phase.

In the ϕ_1 phase, the arithmetic circuit forms the inverting amplifier. Its input is the reference voltage V_r and its gain is $-\alpha$, where $\alpha = C_1/C_2$. Since C_1 was discharged to 0 while C_2 was charged to the offset voltage V_{os} of op-amp A_1 with the polarity shown in Fig. 3(b) in the preceding "reset" phase, the voltage across C_2 becomes $-\alpha(V_r - V_{os})$. After discharging C_1 through S_4 and S_{13} in the ϕ_2 phase, the arithmetic circuit forms the noninverting amplifier in the ϕ_3 phase. Its input is the voltage stored in C_2 in the preceding ϕ_1 phase and its gain is $1/\alpha$. The output voltage of A_1 is now $-V_r + V_{os}$, which is stored in C_X through S_3. In the ϕ_4 phase, op-amp A_1 forms the inverting amplifier with C_X and C_S being the input and feedback capacitors, respectively. The input is the voltage stored in C_X in the last ϕ_3 phase. This produces the

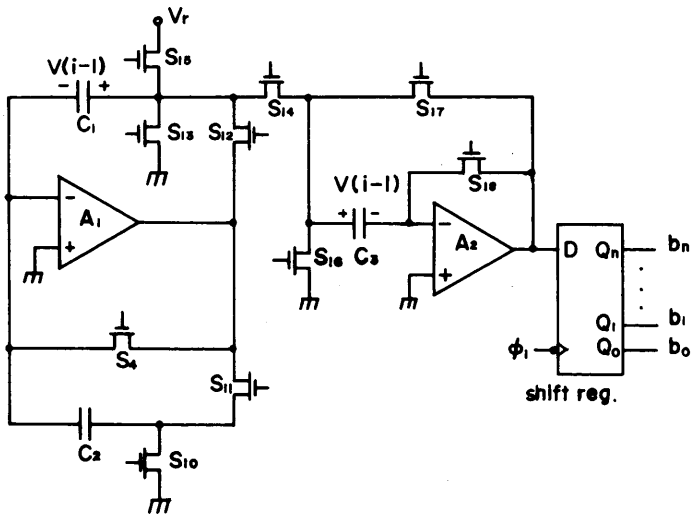

Fig. 4. The circuit configuration in the "convert" state.

output voltage V_x given by (1). It is noted here again that V_x does not include the offset voltage V_{os}. V_x is also stored in C_3 through S_9 and S_{18}. Discharging C_S through S_4 and S_8 and charging C_1 to V_x by the S/H circuit in the ϕ_5 phase, the circuit completes the operation in the "sample" state.

B. Operation in the "Convert" State

In this state, the analog arithmetic and S/H circuits form the cyclic A/D converter shown in Fig. 4 [5]. It converts the voltage V_x produced in the preceding "sample" state into the n-bit binary number b, according to the following algorithm [8]:

$$V(i) = 2V(i-1) + (-1)^{b_{i-1}} V_r \tag{2}$$

$$b_i = \begin{cases} 1, & \text{if } V(i) \geq 0 \\ 0, & \text{otherwise} \end{cases} \qquad (i = 1, 2, \cdots, n) \tag{3}$$

where $V(0) = V_x$, and b_1 and b_n are the most-significant and least-significant bits of b, respectively. The analog arithmetic circuit executes the operation involved in (2), while, operating also as a comparator, the S/H circuit executes the operation involved in (3). Switching sequence for executing the conversion algorithm is listed in Table II.

Let the capacitors C_1 and C_3 store the voltage $V(i-1)$, and let C_2 be discharged to 0. In the ith cycle of operation, $V(i)$ given by (2) is produced by the following steps. (Refer also to Table II to identify the operation in each step.)

1) ϕ_1 phase: The analog arithmetic circuit forms the noninverting amplifier. Its input is $V(i-1)$ stored in C_1. The voltage across C_2 is then $\alpha V(i-1)$. Operating as a comparator, op amp A_2 tests the polarity of $V(i-1)$ stored in C_3. If it is positive, then b_{i-1} is set to 1. Otherwise, it is reset to 0. The shift register stores the value b_{i-1}.

2) ϕ_2 phase: If $b_{i-1} = 1$, then the arithmetic circuit forms the inverting integrator to execute the subtraction involved in (2). Its input is V_r. The voltage across C_2 thus becomes $\alpha\{V(i-1) - V_r\}$. If $b_{i-1} = 0$, on the other hand, the circuit charges C_1 to V_r through S_{15} and S_4. Op-amp A_2 now operates as a hold circuit.

TABLE II
SWITCHING SEQUENCE IN THE "CONVERT" STATE

φ \ S	S_4	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}	S_{17}	S_{18}
ϕ_1			1		1			1		
ϕ_2	$\bar{b}_{i-1}$		b_{i-1}				1		1	
ϕ_3	b_{i-1}		$\bar{b}_{i-1}$		1				1	
ϕ_4	1					1			1	
ϕ_5		1		1		1				1

3) ϕ_3 phase: If $b_{i-1} = 0$, the arithmetic circuit transfers the charge stored in C_1 in the last ϕ_2 phase into C_2. This executes the addition in (2) and the voltage across C_2 now becomes $\alpha\{V(i-1) + V_r\}$. Otherwise, C_1 is discharged to ground through S_4 and S_{13}.

4) ϕ_4 phase: The hold op-amp A_2 charges C_1 to $V(i-1)$.

5) ϕ_5 phase: The arithmetic circuit forms the noninverting integrator. Its input is the voltage stored in C_2 in the previous ϕ_3 phase. The voltage across C_1 then becomes $V(i)$ given by (2). C_3 is also charged to $V(i)$ through S_{14} and S_{18}.

This completes one cycle of operation. Repeating this conversion cycle n times, the circuit generates the n-bit number b, which is related to the capacitance C_X as

$$C_X = \sum_{i=1}^{n} b_i 2^{-i} C_S. \tag{4}$$

The conversion process is also insensitive to offset voltages of op amps, parasitic capacitances, and the capacitance ratio α.

III. Accuracy Estimate

The main error sources in this meter are the feedthrough of digital signals and the finite open-loop gains of op amps. The parasitic capacitance C_p between the node X_G and ground (Fig. 3(b)) also causes the error in grounded-capacitor measurement.

All the switches shown in Fig. 1 involve the feedthrough problem, but only those switches that are connected to the inverting input terminals of op amps are considered here, because their effect is most serious. Let Q_f be the feedthrough charge injected through S_4 and S_{18} when they turn their state from ON to OFF. The switches S_5 and S_6 also inject the charge Q_f when grounded-capacitor measurement is concerned. Their contributions are, however, neglected in a first-order approximation, because they are driven by a complementary digital signal and their feedthrough charges tend to cancel each other.

Taking the feedthrough charge Q_f (the finite open-loop gains A of op-amps A_1 and A_2) and the parasitic capacitance C_p into account, the output voltage of A_1 in the "sample" state and the conversion algorithm executed in the "convert" state can be expressed as follows:

$$V_x' = \left(\frac{C_X}{C_S}\left(\frac{A}{1+A}\right)^2 + \frac{C_{res}}{C_S}\right)V_r \tag{5}$$

where $C_{res} = C_p + Q_f/V_r$, and

$$V(i) = 2\left(\frac{A}{1+A}\right)^2 V(i-1) + (-1)^{b_{i-1}}\left(\frac{A}{1+A}\right)^2 V_r + (2 + \bar{b}_{i-1})\frac{Q_f}{C_1} \quad (i = 1, 2, \cdots, n) \tag{6}$$

where $V'(0) = V_x'$, and a prime denotes the erroneous quantity.

Using (5) and (6), one can estimate separately the contribution of each error source; the capacitance meter measures the residual capacitance C_{res} when C_x is disconnected. Therefore the contribution of C_{res} can be eliminated by subtracting it from the measured capacitance C_X'. The finite gain A reduces the gain of the amplifier in the "sample" state. This reduction in gain is equivalent to scaling the reference voltage V_r by $(A/(1+A))^2$, as indicated in (5). The scaled reference voltage is also included in the second term in the right-hand side of (6). Thus the gain reduction in the "sample" state is canceled by the scaled reference voltage in the cyclic A/D conversion.

Executing the algorithm given by (6) n times, the cyclic A/D converter produces, to a first order, the error voltage

$$\Delta V = \Delta V_A + \Delta V_f = -2\left\{n \cdot 2^n V(0) + \sum_{i=1}^{n}(-1)^{b_{i-1}}(n-i)2^{n-i}V_r\right\}\Big/A + \left(2^{n+1} + \sum_{i=1}^{n}\bar{b}_{i-1}2^{n-i}\right)Q_f/C_1 \tag{7}$$

where ΔV_A and ΔV_f are the error voltages caused by the finite open-loop gain A and the feedthrough charge Q_f, respectively. When $V(0) = V_r$, and hence all b_i's assume 1, ΔV_A becomes maximum

$$[\Delta V_A]_{\max} = 2^{n+2}V_r/A. \tag{8}$$

For the A/D conversion to be accurate down to its LSB, this error voltage should be smaller than V_r. Thus we have

$$2^{n+2} < A. \tag{9}$$

If $A = 80$ dB, the conversion accuracy is estimated to be 12 bits.

The error voltage ΔV_f becomes maximum when all b_i's assume 0:

$$[\Delta V_f]_{\max} = 3 \times 2^{n+1}Q_f/C_1 \tag{10}$$

Thus we can obtain the accuracy condition

$$3 \times 2^{n+1} < C_1 V_r/Q_f. \tag{11}$$

The charge ratio $C_1 V_r/Q_f$ as high as 5×10^4 can be realized with presently available MOS technologies by accommodating the clock feedthrough cancellation scheme and making C_1 as large as practical [9]. The conversion accuracy limited by Q_f is then estimated to be 14 bits.

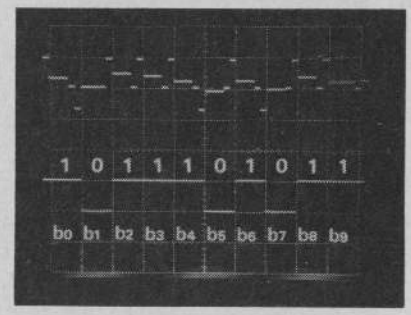

Fig. 5. Experimentally observed waveforms when the meter measured a grounded capacitor of nominal value 470 pF with reference to 1039-pF capacitor. Upper trace: the output voltage waveform of op-amp A_2. Lower trace: the bit pattern obtained. Horizontal scale: 625 μs/div; and vertical scale: 5 V/div.

Summarizing the above discussion, we can conclude that the accuracy of the present capacitance meter is limited by the finite open-loop gains of op amps or the feedthrough charge and a 12-bit quantization accuracy can be obtained by fabricating it in an MOS IC form.

IV. Measurement Examples

A prototype capacitance meter was built using discrete components to confirm the principles of measurement. Op amps and switches used were LF353 and MC14016, respectively. Capacitors C_1, C_2, and C_3 were chosen to be 2.2 nF. The reference voltage V_r was set to 2 V. The clock feedthrough cancellation technique was not used.

Fig. 5 shows waveforms observed during the "convert" state when a capacitor of nominal value 470 pF (its actual value measured by the commercial four-terminal-pair bridge[1] was 463 pF) was subjected to grounded-capacitor measurement using the reference capacitor of 1039 pF. One horizontal division corresponds to one conversion cycle of five phases. The upper trace shows the output voltage of op-amp A_2. The voltage $V(i)$ held in C_3 can be seen during the first three phases of each cycle. The output in the last phase of each cycle indicates the polarity of $V(i)$, which is reflected in the bit pattern $b_0 b_1 \cdots b_n = 1011101011$ shown in the lower trace. The first bit b_0 is the sign bit. The measured capacitance including the residual capacitance 10.1 pF, which was measured separately by disconnecting C_X, was thus $1039 \times (235/512) = 476.9$ pF. The large residual capacitance was attributed to clock feedthrough.

A number of capacitors were measured by both the floating and grounded methods. Table III lists the measured results together with those obtained by the above-mentioned commercial bridge. The discrepancies between them are mostly within 1 percent. Errors which were caused by clock feedthrough will be greatly reduced by accommodating the clock feedthrough cancellation scheme in its integrated realization.

[1]HP Model 4275A multifrequency LCR meter.

TABLE III
COMPARISON BETWEEN THE CAPACITANCES C_{DCM} MEASURED BY THE PRESENT DIGITAL CAPACITANCE METER AND THOSE C_{FTB} BY THE CONVENTIONAL FOUR-TERMINAL-PAIR BRIDGE
The capacitances in parentheses were obtained by the grounded measurement. C_{nom} represents the nominal value and ϵ_r is the relative deviation between C_{DCM} and C_{FTB}.

C_{nom} pF	C_{DCM} pF	C_{FTB} pF	ϵ_r %
1	0.914 (0.885)	0.9	1.5 (1.5)
2	1.91 (1.892)	1.9	1.0 (0.8)
4	3.79 (3.81)	3.8	1.0 (1.0)
10	10.22 (10.21)	10.3	0.78 (0.87)
20	20.37 (20.35)	20.2	0.84 (0.74)
47	47.78 (47.10)	47.4	0.8 (0.63)
100	97.58 (99.13)	98.2	0.63 (0.95)
220	234.5 (233.9)	236	0.64 (0.90)
470	459.0 (466.8)	463	0.86 (0.82)
1000	1075 (1073)	1065	0.94 (0.78)
2200	2870 (2917)	2890	0.69 (0.93)
4700	4730 (4731)	4700	0.64 (0.66)
10000	14270 (14261)	14350	0.8 (0.89)
22000	21910 (21903)	21700	0.97 (0.94)

V. CONCLUSIONS

A digital capacitance meter using switched-capacitor circuitry has been described. It features high accuracy made possible by its offset-tolerant and parasitic-insensitive circuit configuration. Error analysis has shown that 12-bit accuracy can be expected by fabricating the meter in an IC form using present MOS technologies. The chip area required for the fabrication is very small because of the small device count involved. Therefore it would be useful as an on-chip meter to characterize integrated MOS capacitors and also for built-in interfacing of intelligent capacitive transducers.

ACKNOWLEDGMENT

The authors thank Prof. G. C. Temes of UCLA for useful discussions.

REFERENCES

[1] B. M. Oliver and J. M. Cage, *Electronic Measurement and Instrumentation.* New York: McGraw-Hill, 1971, ch. 9.
[2] A. C. Corney, "A universal four-terminal-pair impedance bridge," *IEEE Trans. Instrum. Meas.*, vol. IM-28, no. 3, pp. 211–215, Sept. 1979.
[3] J. L. McCreary and D. A. Sealer, "Precision capacitor ratio measurement technique for integrated circuit capacitor array," *IEEE Trans. Instrum. Meas.*, vol. IM-28, no. 1, pp. 11–17, Mar. 1979.
[4] K. Watanabe and G. C. Temes, "A switched-capacitor digital capacitance bridge," *IEEE Trans. Instrum. Meas.*, vol. IM-33, no. 4, pp. 247–251, Dec. 1984.
[5] H. Matsumoto and K. Watanabe, "Improved switched-capacitor algorithmic analogue-to-digital converter," *Electron. Lett.*, vol. 21, pp. 430–431, May 1985.
[6] R. Gregorian and S. Fan, "Offset free high-resolution D/A converter," in *Proc. 14th Asilomar Conf. Circuits, Systems, and Components*, Nov. 1980, pp. 316–319.
[7] K. Martin, "Improved circuits for the realization of switched-capacitor filters," *IEEE Trans. Circuits Syst.*, vol. CAS-27, pp. 237–244, Apr. 1980.
[8] R. H. McCharles and D. A. Hodges, "Charge circuits for analog LSI," *IEEE Trans. Circuits Syst.*, vol. CAS-25, pp. 490–497, July 1978.
[9] K. Martin, "New clock feedthrough cancellation technique for analog MOS switched-capacitor circuits," *Electron. Lett.*, vol. 18, pp. 39–40, Jan. 1982.