A Switched-Capacitor Interface for Capacitive Sensors with Wide Dynamic Range

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Abstract—**A novel switched-capacitor interface for capacitive sensors has been developed based on a dual-slope analog-to-digital (A/D) conversion technique. The interface consists of a switched-capacitor integrator, a comparator, and digital control circuits. The integrator first samples the sensor capacitance in the form of its proportional charge. A quantized reference charge is then extracted until the output voltage of the integrator becomes zero. An autoranging function is incorporated to achieve a wide dynamic range of sensor capacitance by changing the sampling count in a 2's geometric manner. A prototype interface built using discrete components has demonstrated a capacitance measurement over four decades with an accuracy better than 1 percent.**

I. Introduction

SENSORS are now becoming key components in automatic control of vehicles, robots, and the industrial process. They are usually exposed to noisy environments removed from central control units and thus their outputs are easily disturbed by electromagnetic interference. One promising solution to overcome this problem is to convert the sensed variable into its equivalent digital number by means of built-in signal conditioning circuitry [1]. A variety of interface circuitry has been developed for such "smart" sensors, but the switched-capacitor circuits seem best suited for capacitive sensors because their fabrication process is compatible with most of the sensors [2]–[4]. The dynamic range, and thus the maximum signal-to-noise ratio, of such interfaces proposed so far is limited to 60 dB, which obliges a large offset capacitance of the sensor to be cancelled to detect its small capacitance change accurately. A wider dynamic range for obviating the offset cancellation is possible by increasing the effective number of bits, but this greatly increases the device count.

A more realistic approach for increasing the dynamic range is to use a floating-point technique for quantizing the sensed variable. Such an interface was proposed earlier [5], but the improvement was limited to 10 dB primarily by the finite open-loop gain of a particular op-amp involved. This paper describes another approach based on the dual slope analog-to-digital (A/D) conversion technique [6]. Following this introductory section, its configuration, principles of operation, accuracy estimate, and calibration procedure are given. A prototype interface implemented using discrete components and examples of measurement are also presented.

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II. Circuit Configuration

The interface is a hybrid analog and digital system. The analog part, shown in Fig. 1(a), is basically a dual-slope A/D converter, consisting of the switched-capacitor integrator and the comparator. Here, C_x denotes a capacitive sensor, C_2 is an integration capacitor, and C_3 and C_4 are incorporated to eliminate errors due to the finite open-loop gain and the offset voltage of op-amp A_1, respectively [7], [8]. Capacitor C_M prevents the glitches which would otherwise be generated during the non-overlapping period of the two phase clocks ϕ and $\bar{\phi}$ [9]. The input to the integrator is the reference voltage V_r. V_{ar} is the threshold voltage for autoranging. The operation of this integrator is controlled by the digital part shown in Fig. 1(b).

The timing diagram of the control signals is shown in Fig. 1(c). ϕ and $\bar{\phi}$ are complimentarily non-overlapping two-phase clock pulses. A reset pulse ϕ_R initializes the interface by discharging the integration capacitor C_2 and clearing the counter. The operation is divided into two states; the "Sample" (SMP) state during which the charge proportional to the sensor capacitance is stored into capacitor C_2 and the "Conversion" (CNV) state during which the charge stored in C_2 is converted into its equivalent digital word. $\phi_a(n)$ is the autoranging pulse generated by the counter when it counts 2^n ($n = 0, 1, 2, \cdots, n$) clocks in the SMP state. The SMP state continues until the comparator output CMP becomes high and $\phi_a(n)$ turns the operation into the CNV state. The operation of each state is described in detail in the following sections.

A. Operation in the SMP State

In this state, switches S_2, S_4, S_8, and S_{15} are kept "on", while switches S_1, S_3, S_7, and S_{16} are kept "off." Thus the analog circuit becomes as is shown in Fig. 2. The integrator performs the noninverting integration to accumulate the signal charge C_xV_r onto the capacitor C_2 every $\bar{\phi}$ clock pulse. Op-amp A_2 and flip-flop D_1 form the comparator. This comparator compares the integrator output voltage V_o with the threshold voltage V_{ar}. If $V_o < V_{ar}$,

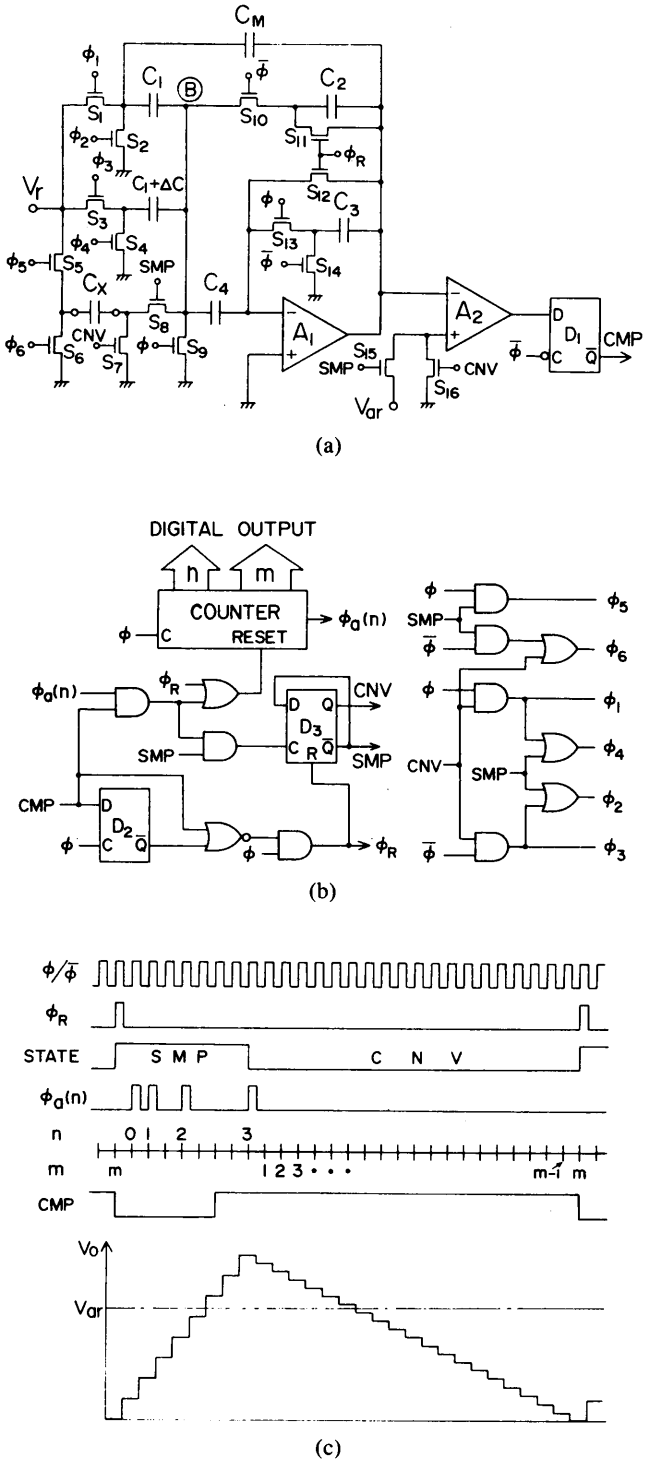

Fig. 1. (a) The analog. (b) Digital circuitry of the interface. (c) Timing diagram of digital control signals and the output waveform of op-amp A_1.

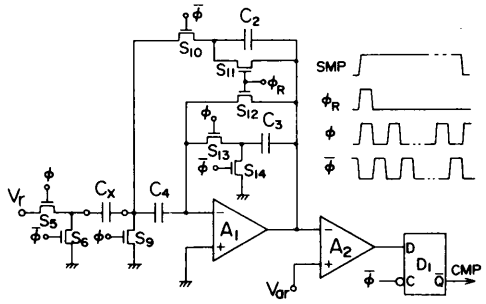

Fig. 2. The analog circuitry in the SMP state.

the sampling operation is continued. If $V_o \geqq V_{ar}$, the autoranging pulse $\phi_a(n)$ turns the operation to the CNV state. Therefore, if the sensor capacitance lies in the range

$$\frac{C_2 V_{ar}}{2^n V_r} \leqq C_x < \frac{C_2 V_{ar}}{2^{n-1} V_r} \tag{1}$$

the accumulation is repeated 2^n times. The accumulated charge at the end of this state is thus

$$Q_{\mathrm{SMP}} = 2^n C_x V_r. \tag{2}$$

B. Operation in the CNV State

In this state, switches S_6, S_7, and S_{16} are kept "on", while switches S_5, S_8, S_{11}, and S_{12} are kept "off." Thus the equivalent analog circuitry represented in this state becomes as is shown in Fig. 3. Op-amp A_1 now performs the noninverting and inverting integration simultaneously. The noninverting integration deposits the $C_1 V_r$ charge to C_2, while the inverting integration withdraws the charge $(C_1 + \Delta C) V_r$ from C_2. Therefore, a net charge $\Delta C V_r$ is extracted from C_2 every $\bar{\phi}$ clock cycle. Let us assume that this charge extraction is repeated m times until V_o reaches zero. Then, the total charge Q_{CNV} extracted from C_2 is

$$Q_{\mathrm{CNV}} = m \Delta C V_r. \tag{3}$$

Since $Q_{\mathrm{SMP}} = Q_{\mathrm{CNV}}$, the sensor capacitance is given by

$$C_x = \frac{m}{2^n} \Delta C = 2^{-n}(m_1 2^1 + m_2 2^2 + \cdots + m_k 2^k) \Delta C \tag{4}$$

where m_i $(i = 1, 2, \cdots, k)$ is the content of the k-bit counter used for counting the number of times the quantum charge is extracted. Therefore, m and n represent the integer and exponent parts, of the binary representation of the capacitance, respectively.

III. Error Analysis and Calibration Method

The switched-capacitor integrator is configured such that the offset voltage, the finite open-loop gain of the op-amp, the parasitic capacitance, and the glitches in the nonoverlapping period of the two phase clocks have negligible effect upon its operation. Therefore, the clock feedthrough associated with the switches and the uncertainty of ΔC are the main error sources.

Let the feedthrough charge at node Ⓑ in Fig. 1(a) be Q_f. Then the total charge accumulated onto C_2 in the SMP state is $2^n(C_x V_r + Q_f)$, while that extracted from C_2 in the CNV state is $m'(\Delta C V_r - Q_f)$, where m' is the erroneous count due to Q_f. Since these charges balance each other, we obtain

$$2^n(C_x V_r + Q_f) = m'(\Delta C V_r - Q_f). \tag{5}$$

Equation (5) is depicted graphically in Fig. 4. Comparing the erroneous response with the ideal one, one notices that the feedthrough charge in the SMP state causes the offset error, and that in the CNV state results in the gain error.

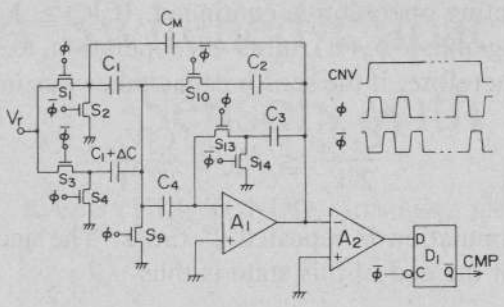

Fig. 3. The analog circuitry in the CNV state.

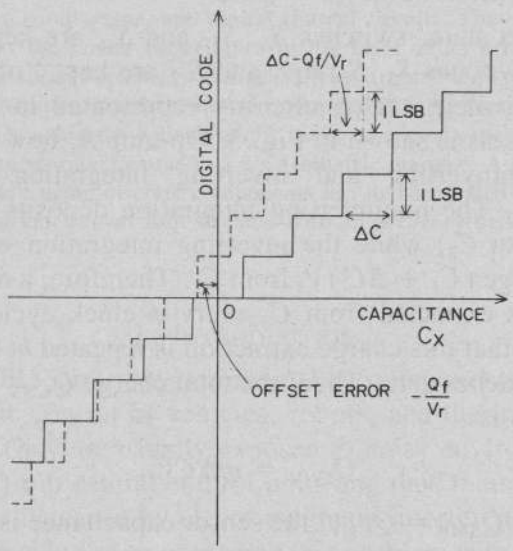

Fig. 4. The error (dotted line) due to the clock frequency charge and the ideal response (solid line).

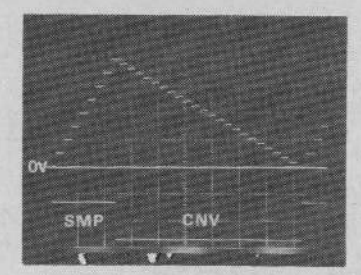

Fig. 5. The output voltage of op-amp A_1 (upper trace) and the state signal (lower trace) observed in a prototype interface. Horizontal scale: 0.1 ms/div; Vertical scale: 1 V/div (upper trace); and 10 V/div (lower trace).

TABLE I
COMPARISON BETWEEN THE CAPACITANCE C_{SCM} AND C_{FTB}. C_{nom} IS THE NOMINAL CAPACITANCE AND ϵ_r IS THE RELATIVE ERROR BETWEEN C_{SCM} AND C_{FTB}

C_{nom} (pF)	C_{SCM} (pF)	C_{FTB} (pF)	ϵ_r (%)
0.5	0.685	0.675	1.48
1	1.173	1.17	0.25
2	2.380	2.39	-0.42
5	4.927	4.97	-0.87
10	10.28	10.25	0.29
18	19.78	19.81	-0.15
50	54.12	54.01	0.20
100	98.7	99.7	-1.00
180	176.5	177	-0.28
360	357.6	359	-0.39
820	823.1	822	0.13
1500	1485	1486	-0.07
3300	3311	3330	-0.57
5600	5625	5670	-0.79

In addition, the uncertainty of ΔC also contributes to the gain error.

To eliminate these errors, a calibration cycle consisting of the following steps is implemented. First, only the feedthrough charge Q_f is detected in the SMP state by setting $V_r = 0$ and then converting it into a binary number with the quantum $\Delta C V_r - Q_f$. Next, a known standard capacitor C_s is substituted in place of the sensor, and its value is measured by the system. Since the feedthrough charge Q_f and the quantum $\Delta C V_r - Q_f$ can be measured independently by these two steps, we can detect the sensor capacitance C_x by

$$C_x = \frac{D_x}{D_s} C_s \tag{6}$$

where D_x and D_s are digital readings for C_x and C_s, respectively.

IV. Experimental Results

A prototype interface was implemented using discrete components. The capacitors were $C_1 = C_2 = C_3 = C_4 = 3.34$ nF, $C_M = 1.56$ nF. The op-amp used was LF347. The reference voltage V_r and the threshold voltage V_{ar} were both set to 2 V. The clock frequency was 30 kHz.

To confirm its principles of operation, this interface was applied to capacitance measurement of discrete capacitors. Fig. 5 shows the integrator output V_o and the state signal when a capacitor of nominal value 824 pF was connected to the interface. The large capcitance difference $\Delta C = 287$ pF was intentionally chosen so that the waveform demonstrates the operation in each state. In the SMP state, the accumulation is repeated eight times and thus $n = 3$. In the CNV state, the charge extraction is repeated 23 times and thus $m = 23$. Therefore, the measured capacitance is $C_x = (23/2^3) \times 287 = 825$ pF, which agrees well with the nominal value.

A number of capacitors were measured by the system to test the dynamic range of the interface. In this measurement, ΔC is set to 5 pF. Table I compares the capacitance C_{SCM} measured by the present interface with C_{FTB} by a commercial four-terminal-pair bridge. The measurement uncertainty of this bridge is 0.1 percent of the full scale or 3 LSB of the four digit display. The discrepancies between them are almost within 1 percent. These results demonstrate that a dynamic range of 80 dB is possible with the present interface and thus it is also useful as a capacitance meter.

V. Conclusions

A switched-capacitor interface incorporating the autoranging function has been presented. It features a small device count integrable onto a small chip area, and a high accuracy made possible by the offset, parasitic, and gain-

insensitive configuration. A prototype interface implemented using discrete components has confirmed the principles of operation. The wide dynamic range demonstrated by the measurement examples obviates the need for offset cancellation and makes this interface also useful as a capacitance meter.

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