A Switched-Capacitor Interface for Intelligent Capacitive Transducers

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Abstract—**A novel switched-capacitor circuit has been developed for interfacing capacitive transducers with digital systems. It consists of a differential integrator and a cyclic analog-to-digital converter (ADC). The capacitive transducer is first charged in proportion to its capacitance. This charge is next compared with that stored on a reference capacitor and their difference is converted to a voltage by a differential integrator. The sensitivity of this capacitance-to-voltage conversion is controlled by the rate of the charge accumulation. A binary output is obtained from the resultant voltage by analog-to-digital conversion.**

The whole operation is insensitive to parasitic capacitances, offset voltages of op amps, and the capacitor values involved in the circuit. Thus the proposed circuit permits an accurate differential capacitance measurement. An error analysis has shown that the resolution as high as 14 bits can be expected by realizing the circuit in a monolithic IC form. Besides the accuracy, it features the small device count integrable onto a small chip area. The circuit is thus suited particularly for the on-chip interface. Its application to a humidity sensor is also presented.

I. Introduction

THE development of intelligent sensors is now one of the main concerns of control systems and automation. To provide sensors with intelligence, an interface circuit, which converts the sensed variable into a digital number, is indispensable because linearization, compensation, and calibration are accomplished with a microprocessor. In capacitive transducers for sensing humidity, pressure, flow, and so on, the standard method of analog-to-digital conversion is capacitance-to-frequency conversion [1], [2]. This frequency encoding allows simple and robust data transmission [3], but high resolution cannot be expected in a solid-state sensor because its capacitance variation is small and offset by a large fixed capacitance [4], [5].

Encoding the capacitance variation only into a digital number can be accomplished by a capacitance bridge followed by an amplifier, a detector, and an analog-to-digital converter (ADC), although its frequency encoding is also possible. It is impractical, however, to incorporate such a hybrid analog and digital signal processing system into a sensor using presently available circuits, because its implementation requires a large number of trimmed components. Thus an alternative means should be exploited for an intelligent transducer.

Accurate hybrid analog and digital signal processing can easily be performed by switched-capacitor circuits fabricated with advanced MOS technologies. Therefore the switched-capacitor technology is best suited for implementing the interface of a capacitive transducer. Several such candidate techniques have been reported so far, but some of them are applicable only to capacitance ratio measurements [6], [7] and the others have no provision for digital output [8], [9].

This paper describes a novel switched-capacitor circuit which detects the capacitance difference between a capacitive sensor and a reference capacitor and then converts it into a binary number. Following this introductory section, its configuration and principles of operation are given in Section II. An estimate of the resolution attainable when it is realized in a monolithic IC form, some experimental results, and an application are present in subsequent sections.

II. Circuit Description

Fig. 1(a) shows the circuit diagram of the switched-capacitor interface. Here, C_x represents a capacitive sensor and C_r is the reference capacitor with which the capacitance of a sensor is to be compared. The operation of the circuit can be divided into four states, whose sequence is shown in Fig. 1(b). In the "reset" state, the circuit clears the shift register and discharges all the capacitors by turning all the grounded switches and S_5 and S_{12} on. In the subsequent "sense" state, it senses the capacitance difference ΔC between C_x and C_r, to produce the voltage V_0 proportional to ΔC. After scaling the sensed voltage V_0 and storing the scaled voltage V_s into appropriate capacitors in the "scale" state, the circuit converts V_s into a binary number in the "conversion" state. The detailed operation in each state will be described next.

A. Sense State

The circuit diagram for this state is shown in Fig. 2(a). The capacitive sensor C_x, the reference capacitor C_r, and op amp A_1 form the differential integrator. Its operation is controlled by the two phase clocks ϕ and $\bar{\phi}$ with the nonoverlapping period t_d. Their timing is shown in Fig. 2(b). When $\phi = 1$, C_x is charged to the reference voltage V_r through S_1 and S_5, while C_r is discharged to ground. In

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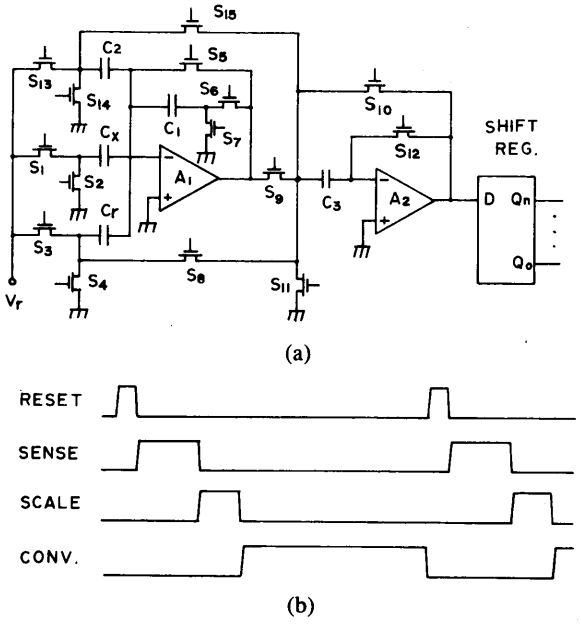

Fig. 1. (a) Circuit diagram of the switched-capacitor interface and (b) the state signals controlling its operation.

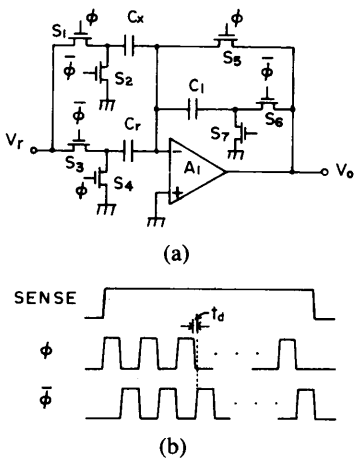

Fig. 2. (a) Circuit configuration and (b) timing diagram of the nonoverlapping two-phase clock in the "sense" state.

the next $\bar{\phi} = 1$ phase, the charge stored in C_x is transferred into the feedback capacitor C_1, while C_r is charged to V_r through S_3. Since the charge $C_r V_r$ also flows through C_1 in the direction opposite to that due to C_x, the net charge stored in C_1 is $(C_x - C_r)V_r$. This process is repeated m times, until op amp A_1 produces the voltage V_0

$$V_0 = m(C_x - C_r)V_r/C_1 = m\Delta C V_r/C_1 \qquad (1)$$

where $\Delta C = C_x - C_r$. The op amp A_2 is inactive during this state.

B. Scale State

The capacitance difference ΔC sensed in the preceding state is referenced to C_1. Since C_1 is not always defined, it should be scaled by C_r. This is accomplished in scale state by the circuit shown in Fig. 3(a). Op amp A_1 now forms, in conjunction with C_1 and C_r, the noninverting amplifier, while op amp A_2 operates as a sample/hold (S/H) circuit. Each switch involved is driven by the nonoverlapping four-phase clock, whose timing is shown in Fig. 3(b).

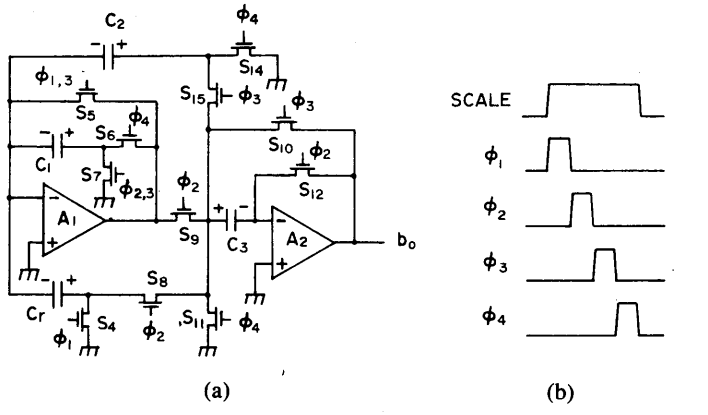

Fig. 3. (a) Circuit configuration and (b) timing diagram of the four-phase clock in the "scale" state.

The operation in each phase can be identified by the clock signal indicated next to the control terminal of each switch. Here, $\phi_{1,3}$ denotes $\phi_1 + \phi_3$. In the $\phi_1 = 1$ phase, the circuit discharges C_r to ground. In the next $\phi_2 = 1$ phase, it transfers the charge stored in C_1 in the preceding "sense" state into C_r. Op amp A_1 then produces the voltage given by

$$V_s = m\Delta C V_r/C_r. \qquad (2)$$

This voltage is sampled and stored in C_3 with the polarity indicated in the figure. In the $\phi_3 = 1$ phase, op amp A_2 operates as a hold circuit and charges C_2 to V_s through S_{10}, S_{15}, and S_5. The charge thus stored in C_2 is next transferred into C_1 in the $\phi_4 = 1$ phase, while op amp A_2 operates as a comparator to test the polarity of V_s held in C_3. If it is positive, then one is stored in the sign bit b_0. Otherwise, zero is stored in b_0. The capacitors C_1, C_2, and C_3 store the voltages γV_s, 0, V_s, respectively, where $\gamma = C_2/C_1$. This completes the operation in this state and the circuit is now ready for the next state.

C. Conversion State

In this state, the interface circuit converts the capacitance difference ΔC scaled by C_r into the n-bit binary number b by iterating the following arithmetic operation [10]:

$$V(i) = 2V(i-1) + (-1)^{b_i - 1}V_r \qquad (3)$$

$$b_i = \begin{cases} 1, & \text{if } V(i) > 0 \\ 0, & \text{otherwise} \end{cases}$$

$$(i = 1, 2, \cdots, n) \qquad (4)$$

where $V(0) = V_s$, and b_1 and b_n are the most-significant bit (MSB) and least-significant bit (LSB) of b, respectively.

The circuit diagram for executing the algorithm (3) is shown in Fig. 4(a). Controlled by the nonoverlapping five-phase clock whose timing is shown in Fig. 4(b), op amp A_1, C_1, and C_2 form the arithmetic circuit to perform the operation involved in (3), while op amp A_2 operates as a S/H and comparator circuit to determine the value of b_i according to (4). Let the voltages $\gamma V(i-1)$, 0, and $V(i$

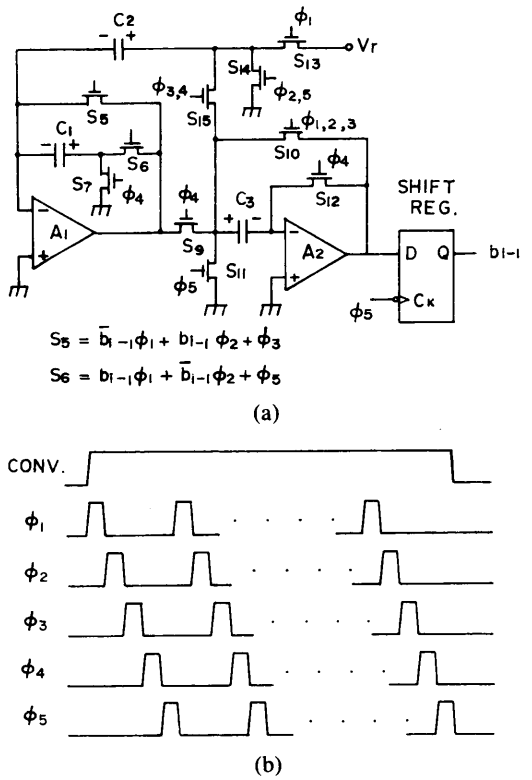

Fig. 4. (a) Circuit configuration and (b) timing diagram of the five-phase clock in the "conversion" state.

-1) be stored in C_1, C_2, and C_3, respectively, and the value of b_{i-1} be stored in the shift register by the $(i-1)$th cycle of operation. In the next ith cycle, the voltage $V(i)$ is produced and the value of b_i is determined as follows [11].

ϕ_1 phase: If $b_{i-1} = 1$, then the arithmetic circuit forms the inverting integrator. Its input is V_r. The voltage across C_1 then becomes $\gamma\{V(i-1) - V_r\}$. The subtraction involved in (3) is thus executed. If $b_{i-1} = 0$, on the other hand, C_2 is charged to V_r through S_{13} and S_5. The voltage across C_1 then remains unchanged. Op amp A_2 holds the voltage $V(i-1)$ across C_3 until the $\phi_4 = 1$ phase.

ϕ_2 phase: The arithmetic circuit forms the noninverting integrator if $b_{i-1} = 0$. Its input is the voltage V_r stored in C_2 in the last ϕ_1 phase. The voltage across C_1 then becomes $\gamma\{V(i-1) + V_r\}$. The addition involved in (3) is thus executed. If $b_{i-1} = 1$, then C_2 is discharged to ground through S_5. The voltage across C_1 then remains unchanged.

ϕ_3 phase: The hold op amp A_2 charges C_2 to $V(i-1)$ through S_{15} and S_5.

ϕ_4 phase: The arithmetic circuit forms the noninverting integrator. Its input is the voltage across C_1. The voltage across C_2, and thus the output of op amp A_1, then becomes $V(i)$ given by (3). This voltage is also sampled into C_3.

ϕ_5 phase: Forming the noninverting amplifier, the arithmetic circuit transfers the charge stored in C_2 in the last ϕ_4 phase back into C_1. The voltages across C_1, C_2, and C_3 are now $\gamma V(i)$, 0, and $V(i)$, respectively. Operating as a comparator, op amp A_2 tests the polarity of $V(i)$ stored into C_3, to determine the value of b_i. This completes one cycle of operation.

This conversion cycle is repeated n times, until the capacitance difference ΔC scaled by C_r is converted into the n-bit number with an additional sign bit b_0:

$$m\Delta C/C_r = (-1)^{\bar{b}_0}(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n}). \tag{5}$$

III. Resolution Estimate

In this section, we estimate the resolution attainable with this interface when all of the circuit (except C_x and C_r) is implemented in the MOS IC process.

Inspecting Fig. 1(a), one can easily find that the operation of the interface is not affected by the offset voltages of op amps and the parasitic capacitance between each node and ground [12], [13]. The A/D conversion process does not depend upon the capacitance ratio γ either. Therefore the main error sources are the feedthrough of clock signals through gate–source and gate–drain capacitors of MOS switches and the finite open-loop gains of op amps. All the switches in Fig. 1(a) are, in fact, involved in the clock feedthrough, but those switches which are connected to the inverting input terminals of op amps cause the most serious effect. Let the switches S_5 and S_{12} inject the charge Q_f towards the inverting input terminals when they turn their states from ON to OFF. Let also A be the open-loop gain of op amps A_1 and A_2. Then the output voltage of op amp A_1 in the "scale" state is given by

$$V_s' = \frac{\alpha(\Delta C V_r + Q_f)\dfrac{1-\alpha^m}{1-\alpha} + Q_f}{C_r\{1 + (C_T - C_x)/AC_r\}}$$

$$\simeq \frac{m\Delta C}{C_r}\frac{V_r}{1 + 2/A} + (m+1)Q_f/C_r \tag{6}$$

where

$$\alpha = \frac{1 + 1/A}{1 + C_T/AC_1} \tag{7}$$

and $C_T = C_r + C_x + C_1$ is the total capacitance connected to the inverting input of op amp A_1 in the "sense" state. In deriving the final expression of (6), $C_x \simeq C_r$ and $C_T \simeq 2C_1$ are assumed. The first term of (6) indicates that the reduction of the op-amp gain is equivalent to scaling the reference voltage V_r by $1/(1 + 2A^{-1})$. The second term, and hence the contribution of the clock feedthrough charge in the "sense" and "scale" states, can be measured separately by setting $V_r = 0$. Therefore the resolution defined as the ratio between C_r and the minimum detectable capacitance difference is limited by the accuracy in the A/D conversion.

Taking the finite open-loop gain A and the feedthrough charge Q_f into account, one can derive the following iterative equation for the conversion algorithm executed in the "conversion" state:

$$V'(i) = \frac{2V'(i-1)}{1 + 2/A} + (-1)^{b_{i-1}}\alpha\frac{V_r}{1 + 2/A} + (2 + \bar{b}_{i-1})Q_f/C_1 \tag{8}$$

where a prime denotes the erroneous quantity. It is noted in (8) that the scaled reference voltage is included explicitly to compensate for the reduction in gain in the "sense" and "scale" states. Executing (8) n times, the ADC produces, to a first order, the error voltage

$$\Delta V = \Delta V_A + \Delta V_f = 2^n((1 - 2/A)^n - 1)V(0) + \sum_{i=0}^{n-1} (-1)^{b_i} 2^i((1 - 2/A)^i(1 - 1/A) - 1)V_r + \left(2^{n+1} + \sum_{i=1}^{n} \bar{b}_{i-1} 2^{n-i}\right) Q_f/C_1 \quad (9)$$

where ΔV_A and ΔV_f are the error voltages caused by the finite gain A and the feedthrough charge Q_f, respectively. When $V(0) = V_r$, and hence all b_i's assume 0, the error voltage ΔV becomes maximum:

$$[\Delta V]_{\max} = 2^n(3A^{-1} + 4Q_f/C_1V_r)V_r. \quad (10)$$

For the A/D conversion to be accurate down to its LSB, this error voltage should be less than V_r. Assume $A = 80$ dB and the signal-to-noise charge ratio $C_1V_r/Q_f = 2 \times 10^4$, which is obtainable with presently available MOS technologies if the clock feedthrough cancellation scheme is accommodated [12]. Then, the accuracy of the A/D conversion is estimated to be 11 bits.

The minimum detectable capacitance difference is then given by

$$\frac{[\Delta C]_{\min}}{C_r} > \frac{1}{2^{11}m}. \quad (11)$$

The resolution can be increased by increasing m, but it increases the relative error in V_s' in turn. Expanding (6) into the Taylor series, one can find that the relative error in V_s' is given by $(m - 1)/2A$. To keep this error within 1/2 LSB of 11 bits, m should be smaller than 6. Thus the resolution obtainable by realizing this interface in an IC form is estimated to be 13–14 bits.

IV. Experimental Results and Application

Based on the scheme shown in Fig. 1(a), a prototype interface was built using discrete components. The op amps and switches used were LF356 and CD4066, respectively. The capacitors C_1, C_2, and C_3 were chosen to be 2.2 nF. The reference voltage V_r was set to 2 V. To confirm the principles of operation, a variable capacitor 513 ± 30 pF was used for C_x and its capacitance change was measured with reference to $C_r = 513$ pF. Instead of measuring the contribution of the clock feedthrough to V_s separately, the clock-feedthrough compensation scheme in Fig. 5 was incorporated to minimize it. No technique, however, was adopted to cancel the clock feedthrough in the "conversion" state.

Fig. 6 shows experimentally observed waveforms when the interface sensed the capacitance difference $\Delta C = 30$ pF and converted it into the 8-bit binary number. The accumulation frequency m was set to 10. The upper trace shows the output voltage of op amp A_1. The step voltage

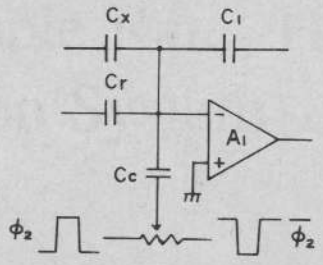

Fig. 5. Offset compensation scheme in the "scale" state.

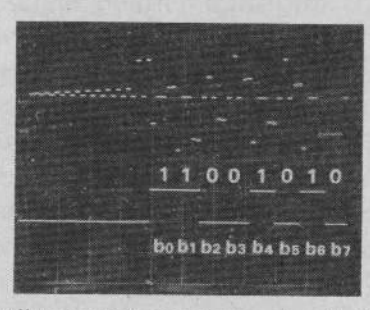

Fig. 6. Experimentally observed waveforms when the interface measured the capacitance difference $\Delta C = 30$ pF with reference to $C_r = 513$ pF. (Upper trace: the output voltage of op amp A_1. Lower trace: the bit pattern generated. Vertical scale: 1 V/div (upper trace) and 5 V/div (lower trace). Horizontal scale: 0.2 ms/div.)

in the "sense" state can be seen in the left part increasing with the charge accumulation. After being amplified by $C_1/C_r = 4.29$ in the "scale" state, the sensed voltage is subjected to the A/D conversion. The voltage $V(i)$ produced in the "conversion" state can be seen from the center to the right. The polarity of $V(i)$ is reflected on the bit pattern shown in the lower trace. Each bit is identified in the figure. The first bit $b_0 = 1$ indicates $C_x > C_r$. The binary number $(1001010)_B$ obtained differs by 1 LSB from that calculated using the capacitance measured by a commercially available four-terminal-pair bridge. This difference was attributed to the clock feedthrough in the "conversion" state.

The output codes obtained by varying C_x are plotted in Fig. 7 with the accumulation frequency m as a parameter. Here, 1 LSB for $m = 10$ corresponds to $\Delta C = 0.4$ pF and that for $m = 3$ to $\Delta C = 1.33$ pF. The results are in good agreement with those predicted by the capacitance difference measured by the four-terminal-pair bridge, although the error due to the clock feedthrough amounts to a 1 LSB for $m = 10$ at $\Delta C = 30$ pF. In an IC realization, this error will be greatly reduced by accommodating the clock feedthrough cancellation scheme.

This prototype interface was applied to the signal processing of the humidity sensor made of a thin cellulose acetate film deposited on a glass substrate. The sensor can be represented electrically by a parallel circuit of the capacitor C_p and the resistor R_p. Their values measured at 40°C at 100 kHz by the commercial bridge are listed in Table I. The reference capacitor $C_r = 555$ pF was used for cancelling the offset capacitance of the sensor. The accumulation frequency m and the binary digit n were set to 10 and 9, respectively. The binary value in hex code versus relative humidity is plotted in Fig. 8. The solid line

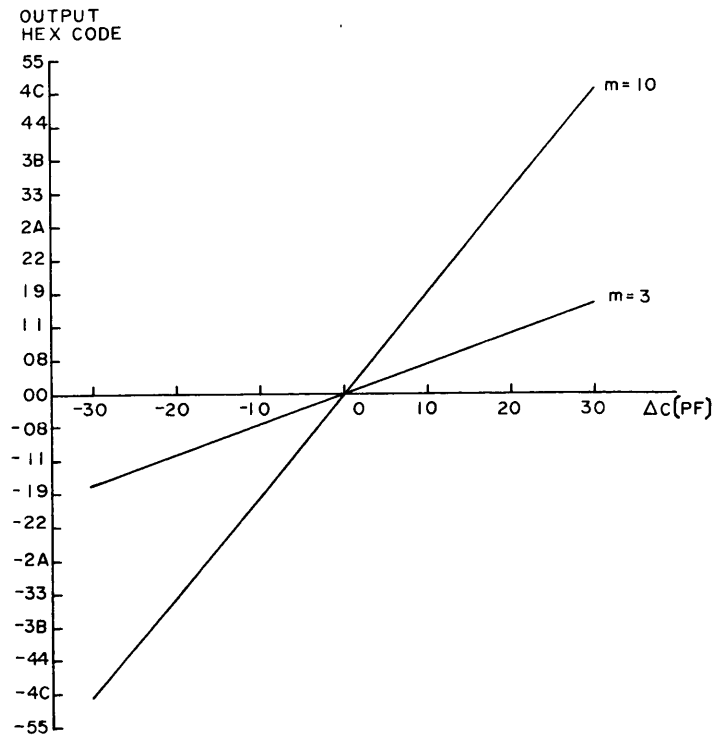

Fig. 7. Output binary number versus the capacitance difference with the accumulation frequency m as a parameter.

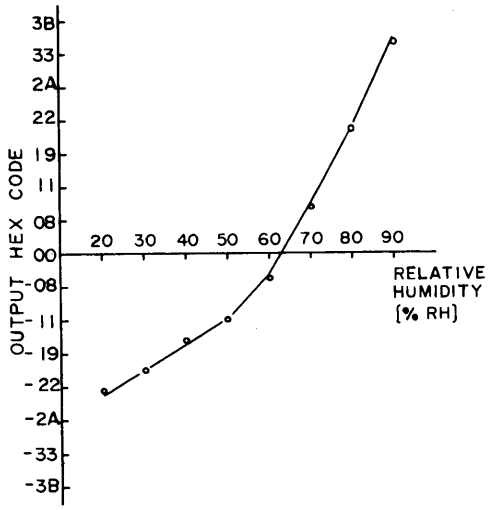

Fig. 8. Output hex code versus relative humidity obtained using a thin cellulose acetate film humidity sensor.

shows the value calculated using the capacitance listed in Table I. Both are again in good agreement, which indicates that a small capacitance change can be detected accurately in spite of the large offset capacitance. The linearization can be easily accomplished by means of ROM.

V. Conclusions

A switched-capacitor circuit for interfacing a capacitive transducer with a digital system has been described. Because of a small device count, the interface circuit can be realized in a monolithic IC form using presently available MOS technologies. Its operation is insensitive to both parasitic capacitances, op-amp offset voltages, and component variation. Thus it allows high-precision processing of the transducer output signal. The error analysis has shown that the resolution as high as 14 bits can be expected from the integrated version of the interface circuit. Therefore the circuit presented here is best suited for a built-in interface of a solid-state capacitive sensor.

TABLE I
Electrical Characteristics of the Humidity Sensor

RH (%)	C_p (pF)	R_p (kΩ)
20	547.7	$>2\times10^4$
30	548.8	$>2\times10^4$
40	550.3	$>2\times10^4$
50	551.6	$>2\times10^4$
60	553.9	$>2\times10^4$
70	557.6	$>2\times10^4$
80	561.3	1279
90	566.2	564

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References

[1] T. Saigusa and S. Gotoh, "UNIΔ series electronic differential pressure transmitter" (in Japanese), *Yokogawa Tech. J.*, vol. 22, pp. 23–29, Mar. 1978.
[2] P. J. Ross, "A water-level sensor using a capacitance to frequency converter," *J. Phys. E: Sci. Instrum.*, vol. 16, pp. 827–828, 1983.
[3] J. E. Brignell, "Interfacing solid state sensors with digital systems," *J. Phys. E: Sci. Instrum.*, vol. 18, pp. 559–565, 1985.
[4] Y. S. Lee and K. D. Wise, "A batch-fabricated silicon capacitive pressure transducer with low temperature sensitivity," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 42–48, Jan. 1982.
[5] A. Hanneborg, T. E. Hansen, P. A. Ohlckers, E. Carlson, B. Dahl, and O. Holwech, "A new integrated capacitive pressure sensor with frequency modulated output," in *Dig. Int. Conf. Solid-State Sensors and Actuators*, 1985, pp. 186–188.
[6] J. M. McCreary and D. A. Sealer, "Precision capacitor measurement technique for integrated circuit capacitor arrays," *IEEE Trans. Instrum. Meas.*, vol. IM-28, pp. 11–17, Mar. 1979.
[7] K. Watanabe and G. C. Temes, "A switched-capacitor digital capacitance bridge," *IEEE Trans. Instrum. Meas.*, vol. IM-33, pp. 247–251, Dec. 1984.
[8] Y. E. Park and K. D. Wise, "An MOS switched-capacitor readout amplifier for capacitive pressure sensors," in *Proc. Custom Integrated Circuits Conf.*, 1983, pp. 380–384.
[9] G. J. Yeh, I. Dendo, and W. H. Ko, "Switched-capacitor interface circuit for capacitive transducers," in *Dig. Int. Conf. Solid-State Sensors and Actuators*, 1985, pp. 60–63.
[10] R. H. McCharles and D. A. Hodges, "Charge circuits for analog LSI," *IEEE Trans. Circuits Syst.*, vol. CAS-25, pp. 490–497, July 1978.
[11] H. Matsumoto and K. Watanabe, "Improved switched-capacitor algorithmic analogue-to-digital converter," *Electron. Lett.*, vol. 21, pp. 430–431, May 1985.
[12] K. Martin, "New clock feedthrough cancellation technique for analog MOS switched-capacitor circuits," *Electron. Lett.*, vol. 18, pp. 39–40, Jan. 1982.
[13] R. Gregorian and S. Fan, "Offset free high-resolution D/A converter," in *Proc. 14th Asilomar Conf. Circuits, Systems, Components*, Nov. 1980, pp. 316–319.