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A Switched-Capacitor-Voltage-Doubler Based Boost Inverter for Common-Mode Voltage Reduction

TAN-TAI TRAN[1], MINH-KHAI NGUYEN[2], (Senior Member, IEEE), TRUONG-DUY DUONG[1], JOON-HO CHOI[1], (Member, IEEE), YOUNG-CHEOL LIM[1], (Member, IEEE), AND FIRUZ ZARE[3], (Senior Member, IEEE)

[1]Department of Electrical Engineering, Chonnam National University, Gwangju 500-757, South Korea
[2]School of Electrical Engineering and Computer Science, Queensland University of Technology, Brisbane, QLD 4000, Australia
[3]School of Information Technology and Electrical Engineering, The University of Queensland, Brisbane, QLD 4072, Australia

Corresponding author: Young-Cheol Lim (yclim@chonnam.ac.kr)

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ABSTRACT In this paper, a modified three-phase two-level voltage source inverter is proposed. By combining the conventional three-phase H-bridge inverter with a switched-capacitor-voltage-doubler network, the DC-link voltage of the proposed inverter is double with respect to the input DC voltage. As a result, the output voltage of the proposed inverter can be higher than the input DC voltage. Furthermore, a common-mode voltage (CMV) of the proposed inverter can be reduced through controlling the two additional switches based on the space vector pulse-width modulation. Compared to the existing modulations and topologies, the variation in CMV can only be up to 16.6% of DC-link voltage. Furthermore, the voltage stress across additional switches and diodes is equal to half of DC-link voltage. Mathematical analysis, operating principles, and comparison of the proposed three-phase two-level voltage source inverter with the conventional three-phase voltage source inverters are presented. The simulation results based on PLECS software verify a good performance of the proposed inverter. Finally, a laboratory prototype based on a TMS320F280049 DSP is developed and experimental tests are carried out to validate the effectiveness of the proposed three-phase inverter topology.

INDEX TERMS Three-phase inverter topology, common-mode voltage, transformerless PV system, space-vector pulse-width modulation, leakage current.

I. INTRODUCTION

The conventional three-phase two-level voltage source inverters (VSIs) have been typically used in various industrial applications such as distributed power systems and ac motor drive systems [1]–[5]. However, the common-mode voltage (CMV) with high frequency and amplitude produced by the conventional VSIs causes a variety of unwanted issues from electromagnetic interference (EMI) emissions to ground leakage and bearing currents [6]–[12]. To solve the CMV problems in the conventional VSIs, a lot of constructive solutions have been discussed in the previous works such as improving system topology and PWM modulation techniques as well as installing EMI filters [13]–[17]. A passive EMI filter which utilizes RLC networks to damping out the high-frequency leakage current because of the grounded motor frame and the grounded heat sink was discussed in [13]. To compensate for variations of the CMV, an active common-mode filter has been introduced in [15] by combining the H-bridge circuit with the common-mode transformer. However, these filter topologies have demerits of being complex or bulky.

Recently, the modulation-based solutions have been discussed to limit the CMV. To be able to understand clearly how these solutions are constructive, it is essential to define the CMV of the conventional VSIs. Fig. 1 presents schematic diagram and common-mode loop model of the conventional three-phase two-level voltage source inverter. The CMV is

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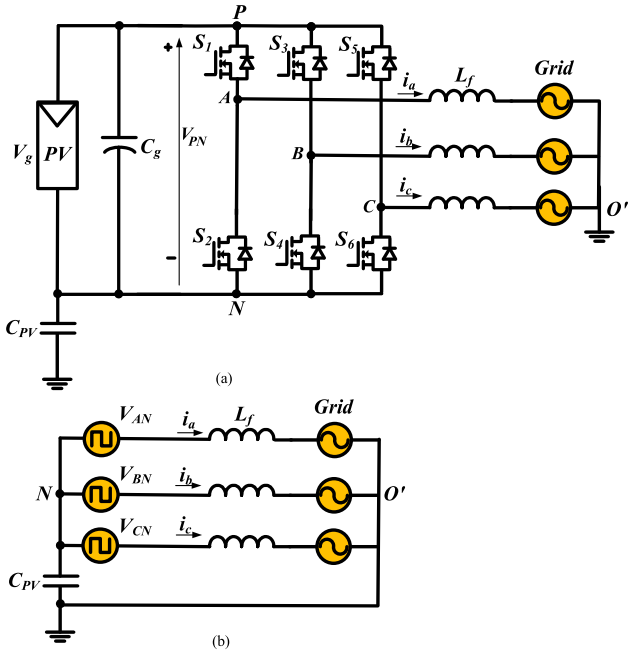

FIGURE 1. Conventional three-phase two-level voltage source inverter topology. (a) Conventional three-phase inverter topology and (b) Common-mode model of conventional three-phase inverter.

TABLE 1. CMV value under different switching states.

Switching State		Bridge States	V_{CM}
Zero states	State 0	000	0
	State 7	111	V_{PN}
odd states	State 1	100	$V_{PN}/3$
	State 3	010	$V_{PN}/3$
	State 5	001	$V_{PN}/3$
even states	State 2	110	$2V_{PN}/3$
	State 4	011	$2V_{PN}/3$
	State 6	101	$2V_{PN}/3$

where V_{PN} is the DC-link voltage across the H-bridge circuit.

calculated as the average of the voltages between the nodes *A-N*, *B-N*, and *C-N* and is given by:

$$V_{CM} = V_{O'N} = \frac{(V_{AN} + V_{BN} + V_{CN})}{3}. \quad (1)$$

where the point "*N*" defines the negative input DC source, while V_{AN}, V_{BN}, and V_{CN} are three-phase voltages indicated in Fig. 1.

Because of eight switching states in the conventional VSIs, the different values of CMV are generated. As presented in Table 1, it can be noted that the CMV varies from $V_{PN}/3$ to $2V_{PN}/3$ during active states as well as V_{PN} and 0 in zero states (state 0 and state 7). As a result, the CMV varies widely from 0 to V_{PN}. Based on Table 1, we can see that the peak value of CMV can be suppressed by avoiding using zero states. With the active zero-state PWM strategies (AZSPWM) as discussed in [18]–[21], zero vectors were replaced by two opposite active vectors with the same time as zero vector. The selection of these vectors based on the region of the reference voltage vector. Therefore, AZSPWM strategies use a group of four active vectors to synthesize the output voltage vector. As a result, the CMV varies from $V_{PN}/3$ to $2V_{PN}/3$ (33.3% of V_{PN}). The voltage linearity characteristics of AZSPWM strategies is the same as that of the conventional space vector PWM (SVPWM) and discontinuous PWM (DPWM) strategies. Unlike AZSPWM strategies, the near state PWM (NSPWM) strategies [22] only used a group of three active vectors to synthesize the output voltage vector. Also, the CMV varies from $V_{PN}/3$ to $2V_{PN}/3$ (33.3% of V_{PN}) like AZSPWM strategies. Furthermore, the current ripple of NSPWM strategy was lower than that of AZSPWM strategies. Compared to AZSPWM strategies, the switching losses in NSPWM strategy is reduced dramatically. However, the NSPWM strategy only operated linearly with modulation index ($Mi = \sqrt{3}\ V_m/V_{PN}$) in range of 0.66 to 1, where V_m is the amplitude of reference voltage, and V_{PN} is DC-link voltage. The remote state PWM (RSPWM) strategies which have been introduced in [23] used three odd active vectors or three even active vectors to synthesize the output voltage vector. The CMV was constant at $V_{PN}/3$ or $2V_{PN}/3$ with the RSPWM1 and RSPWM2 strategies while CMV was constant every 60^o with the RSPWM3 strategy. However, the RSPWM strategies only operated linearly with *Mi* in range of 0 to 0.57. Hybrid SVPWM strategies were proposed in [24] to reduce both amplitude and frequency of CMV. The voltage linearity characteristics of hybrid SVPWM strategies is the same as that of the AZSPWM strategies. The CMV amplitude was reduced to $V_{PN}/3$ and the CMV frequency was equal to three times of fundamental frequency. However, hybrid SVPWM strategies have demerits of being complex and the high switching loss.

On the other hand, various inverter topologies have been introduced for the CMV reduction. In [25], a voltage-clamping H8 topology which used two additional active switches and a voltage-clamping network to limit CMV was proposed. By controlling two additional active switches, the CMV did not change when entering and exiting the zero states. Therefore, the CMV varies from $V_{PN}/3$ to $2V_{PN}/3$. However, using a voltage-clamping network increased the complexity and size of the system. In [26], [27], another H8 topology that only uses two additional active switches to reduce CMV was proposed. So, the volume of the system is reduced in comparison to the voltage-clamping H8 topology. By controlling two additional active switches to float the inverter from the DC voltage source in zero states, the variation in CMV is 33.3% of DC-link voltage. Amit Kumar Gupta *et al.* [28] introduced an improved H8 topology. The CMV during zero states in the improved H8 topology kept constant at $2V_{PN}/5$ while The CMV during active states varies from $V_{PN}/3$ to $2V_{PN}/3$. A constant CMV can be achieved by zero-voltage-state rectifier (ZVR) topology [29]. However, the ZVR topology utilized more power switches. So, size/cost and loss of the system were increased.

Inspired by the previous researches, a three-phase switched-capacitor-voltage-doubler based boost inverter (SCVD-B^{2}I) is discussed in this paper. The proposed

structure is a combination of the conventional three-phase inverter and a voltage-doubler network. Unlike the previous solutions, The CMV in the proposed inverter only varies from $V_{PN}/6$ to $V_{PN}/3$ during active-vector states. Compared to [25], the proposed topology uses a voltage-doubler network to reduce the CMV instead of a voltage-clamping network. So, the output voltage in the proposed inverter can be higher than the DC input voltage. Furthermore, the voltage stress across two additional switches and two additional diodes is only equal to half of DC-link voltage. Also, a comparison between the proposed SCVD-B²I and the previous solutions is performed to validate the performance of the proposed topology. Section II presents the proposed SCVD-B²I. The PWM strategies applied in the proposed topology are discussed in Section III. Simulation and experimental results are included in Section IV and Section V.

II. PROPOSED THREE-PHASE SWITCHED-CAPACITOR-VOLTAGE-DOUBLER BASED BOOST INVERTER (SCVD-B²I)

The schematic circuit of the proposed SCVD-B²I is indicated in Fig. 2. A switched-capacitor-voltage-doubler (SCVD) network which includes two capacitors, two diodes, and two switches is inserted into between the dc input voltage source and the conventional H-bridge circuit. The common-mode loop model of the proposed SCVD-B²I is highlighted in Fig. 3

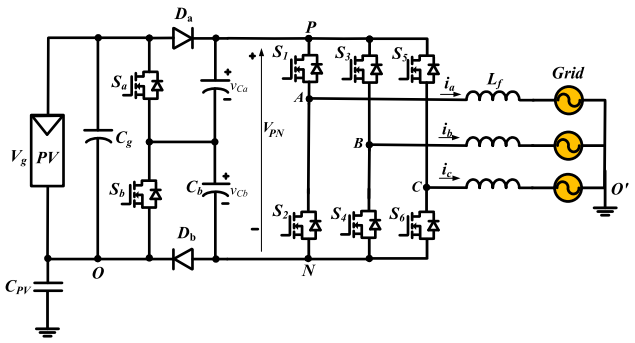

FIGURE 2. Proposed three-phase switched-capacitor-voltage-doubler based boost inverter.

From Fig. 4, the typical voltage across diode $D_b(V_{NO})$ is calculated as follows

$$V_{NO} = \begin{cases} -V_{Cb} & \text{switch } S_b \text{ is turned on} \\ 0 & \text{switch } S_b \text{ is turned off.} \end{cases} \quad (2)$$

The CMV (V_{CM}) of the proposed SCVD-B²I can be calculated as follows:

$$V_{CM} = V_{O'O} = V_{O'N} + V_{NO} = V_{NO} + \frac{(V_{AN} + V_{BN} + V_{CN})}{3}. \quad (3)$$

From (2), (3) and Table 1, all the switching states and the corresponding CMV of the proposed SCVD-B²I are highlighted in Table 2.

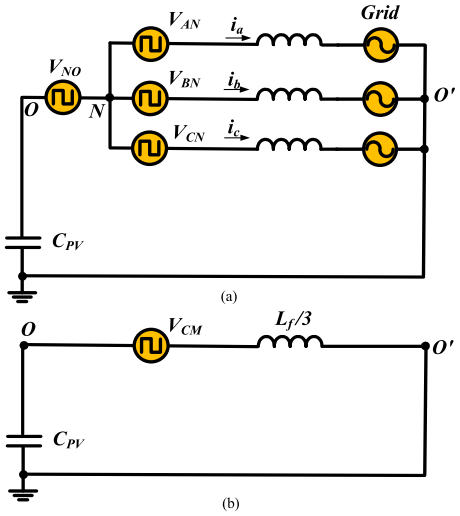

FIGURE 3. Common-mode model of proposed three-phase switched-capacitor-voltage-doubler based boost inverter. (a) Simplified common-mode model of proposed Inverter and (b) Simplified diagram.

Like the conventional VSIs, the proposed SCVD-B²I has eight switching states as presented in Fig. 4. The operating principle of the proposed SCVD-B²I is explained as follows.

During zero state (state 0) [see Fig. 4 (a)]: S_a is switched on while S_b is switched off. As a result, the diode D_a is blocked while diode D_b conducts. The capacitor C_a is discharged as well as the capacitor C_b is charged. The capacitor C_b voltage is equal to V_g. The corresponding CMV during this state is zero like that in the conventional VSIs.

During odd active states (state 1, state 3 and state 5) [see Fig. 4 (b), Fig. 4 (d), and Fig. 4 (f)]: S_a is switched on while S_b is switched off. So, diode D_a is blocked while diode D_b conducts. Capacitor C_a is discharged while capacitor C_b is charged. Capacitor C_b voltage is equal to V_g. The corresponding CMV during this state is $V_{PN}/3$.

During even active states (state 2, state 4 and state 6) [see Fig. 4 (c), Fig. 4 (e), and Fig. 4 (g)]: S_a is switched off while S_b is switched on. As a result, diode D_b is blocked while diode D_a conducts. Capacitor C_a is charged while capacitor C_b is discharged. Capacitor C_a voltage is equal to V_g. The corresponding CMV during this state is $V_{PN}/6$.

During zero state (state 7) [see Fig. 4 (h)]: S_a is switched off while S_b is switched on. So, diode D_a conducts while diode D_b is blocked. Capacitor C_a is charged while capacitor C_b is discharged. Capacitor C_a voltage is equal to V_g. The corresponding CMV during this state is $V_{PN}/2$.

We can see that the two capacitors (C_a and C_b) are charged every switching period. So, in order to guarantee that the two capacitors voltage are the same as the input voltage, the high switching frequency is required.

Therefore, the DC-link voltage of SCVD-B²I is

$$V_{PN} = V_{Ca} + V_{Cb} = 2V_g. \quad (4)$$

From operating principles of the proposed SCVD-B²I, it can be noted that the CMV varies from $V_{PN}/6$ to $V_{PN}/3$ (16.6% of V_{PN}) during powering mode (odd active states and

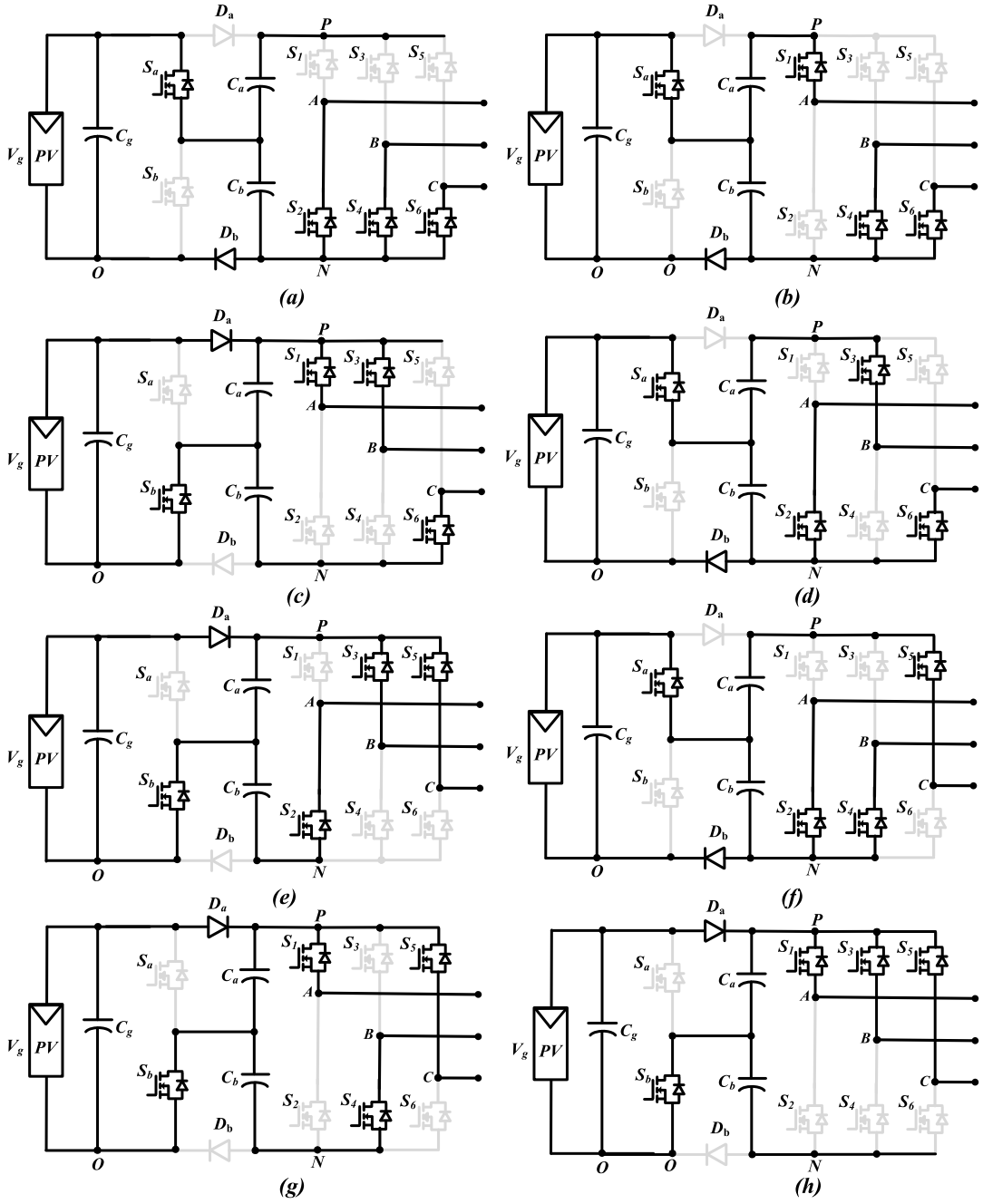

FIGURE 4. Configuration of the proposed SCVD-B^{2}I for eight switching State. (a) State 0 (000); (b) State 1 (100); (c) State 2 (110); (d) State 3 (010); (e) State 4 (011); (f) State 5 (001); (g) State 6 (101); (h) State 7 (111).

even active states). Besides, for the same input DC voltage, the DC-link voltage of the proposed SCVD-B^{2}I is double of that of the conventional VSIs.

III. CONTROL STRATEGIES FOR SCVD-B^{2}I TOPOLOGY

Based on characteristics CMV of the proposed SCVD-B^{2}I, we can see that the CMV varies from $V_{PN}/6$ to $V_{PN}/3$ (16.6% of V_{PN}) during powering mode. Therefore, Some PWM Strategies for SCVD-B^{2}I are discussed in this section.

A. DPWM STRATEGY FOR PROPOSED SCVD-B^{2}I

For the conventional VSIs, the conventional DPWM method plays good performances in DC-link current ripple, THD of output current, voltage linearity, and switching losses. However, the conventional DPWM method performs poor characteristics CMV.

Fig. 5 indicates DPWM strategy for the proposed SCVD-B^{2}I. In the proposed SCVD-B^{2}I, the DPWM strategy which avoids using one zero state (state 7) is applied

TABLE 2. State of each of semiconductor device and CMV of proposed inverter under different switching states.

`State	Switch								Diode		Output Leg Voltage			V_{CM}
	S_1	S_2	S_3	S_4	S_5	S_6	S_a	S_b	D_a	D_b	V_{AN}	V_{BN}	V_{CN}	
State 0	Off	On	Off	On	Off	On	On	Off	Off	On	0	0	0	0
State 1	On	Off	Off	On	Off	On	On	Off	Off	On	V_{PN}	0	0	$V_{PN}/3$
State 2	On	Off	On	Off	Off	On	Off	On	On	Off	V_{PN}	V_{PN}	0	$V_{PN}/6$
State 3	Off	On	On	Off	Off	On	On	Off	Off	On	0	V_{PN}	0	$V_{PN}/3$
State 4	Off	On	On	Off	On	Off	Off	On	On	Off	0	V_{PN}	V_{PN}	$V_{PN}/6$
State 5	Off	On	Off	On	On	Off	On	Off	Off	On	0	0	V_{PN}	$V_{PN}/3$
State 6	On	Off	Off	On	On	Off	Off	On	On	Off	V_{PN}	0	V_{PN}	$V_{PN}/6$
State 7	On	Off	On	Off	On	Off	Off	On	On	Off	V_{PN}	V_{PN}	V_{PN}	$V_{PN}/2$

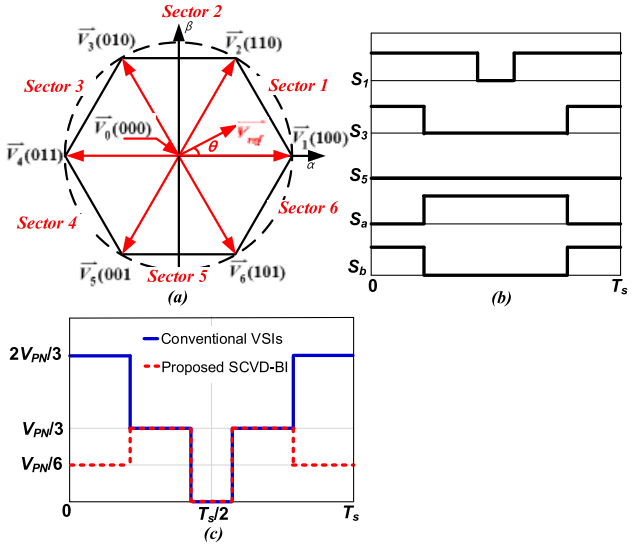

FIGURE 5. DPWM strategy for proposed inverter. (a) Space vector in output of three-phase inverter; (b) Switching pattern of proposed SCVD-B2I in sector 1; (c) CMV of the conventional VSIs compared to the proposed SCVD-B2I under DPWM strategy.

into H-bridge circuit. Besides that, during even active states, the switch S_a is turned off as well as the switch S_b is turned on. During odd active states, the switch S_a is turned on as well as the switch S_b is turned off as shown in Fig. 4 (b). This guarantees that the CMV only takes values of $V_{PN}/3$, $V_{PN}/6$ or 0. As highlighted in Fig. 5 (c), CMV of the proposed SCVD-B^{2}I is dramatically reduced with DPWM strategy. The variation of CMV is 33.3% of DC-link voltage like that in [25]–[28]. So, besides the inherent features of the VSIs under DPWM strategy such as low DC-link current ripple, low THD of output current, full modulation range ($0 \leq Mi \leq 1$), and low switching losses, the proposed SCVD-B^{2}I under DPWM strategy has additional merit of low variation in CMV.

B. ZERO-EVEN PWM (ZEPWM) STRATEGY FOR PROPOSED SCVD-B^{2}I

Fig. 6 presents the ZEPWM strategy for SCVD-B^{2}I. As shown in Fig. 6 (a), the ZEPWM strategy uses a group of two even active vectors and one zero vector to synthesize the output voltage vector. Besides that, during even active states, the switch S_a is turned off as well as the switch S_b is turned on. During zero state (State 0), the switch S_a is turned on as well

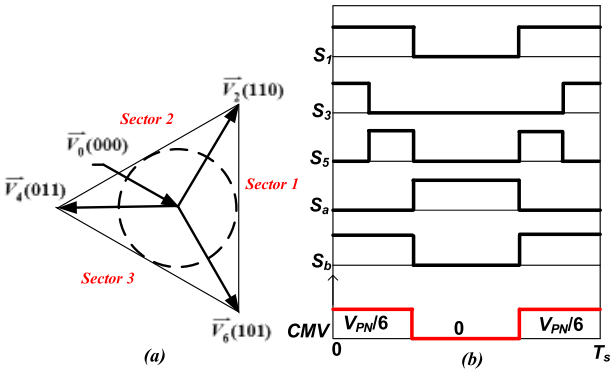

FIGURE 6. ZEPWM strategy for proposed inverter. (a) Space vector in output of three-phase inverter; (b) Switching pattern and CMV of proposed SCVD-B2I in sector 1.

as the switch S_b is turned off as shown in Fig. 6 (b). This guarantees that the CMV only takes values of $V_{PN}/6$ or 0. As highlighted in Fig. 6 (b), the amplitude and high frequency of CMV of the proposed SCVD-B^{2}I is dramatically reduced. The variation of CMV is 16.6% of DC-link voltage.

In sector 1 as shown in Fig. 6(a), the three vector $\vec{V}_0$, $\vec{V}_2$ and $\vec{V}_6$ is used to synthesize the reference vector ($\vec{V}_{ref}$). According to the volt-second balance principle, we get:

$$\vec{V}_{ref} T_s = \vec{V}_2 T_2 + \vec{V}_6 T_6 + \vec{V}_0 T_0 \tag{5}$$

where T_s is the switching period, T_0, T_2 and T_6 are dwell times of $\vec{V}_0$, $\vec{V}_2$ and $\vec{V}_6$, respectively.

The time intervals of T_0, T_2 and T_6 can be calculated as:

$$\begin{cases} T_2 = Mi \cdot T_s \cdot \sin(\theta + \pi/3) \\ T_6 = Mi \cdot T_s \cdot \cos(\theta + \pi/6) \\ T_0 = T_s - \sqrt{3} Mi \cdot T_s \cdot \cos(\theta). \end{cases} \tag{6}$$

Similarly, in sector 2 as shown in Fig. 6 (a), the three vector $\vec{V}_0$, $\vec{V}_2$ and $\vec{V}_4$ are used to synthesize the reference vector ($\vec{V}_{ref}$).

Dwell times of $\vec{V}_0$, $\vec{V}_2$ and $\vec{V}_4$ can be calculated as:

$$\begin{cases} T_2 = Mi \cdot T_s \cdot \sin(\theta) \\ T_4 = Mi \cdot T_s \cdot \sin(\theta - \pi/3) \\ T_0 = T_s + \sqrt{3} Mi \cdot T_s \cdot \cos(\theta + \pi/3). \end{cases} \tag{7}$$

Similarly, in sector 3 as shown in Fig. 6 (a), the three vector $\vec{V}_0$, $\vec{V}_4$ and $\vec{V}_6$ are used to synthesize the reference vector ($\vec{V}_{ref}$).

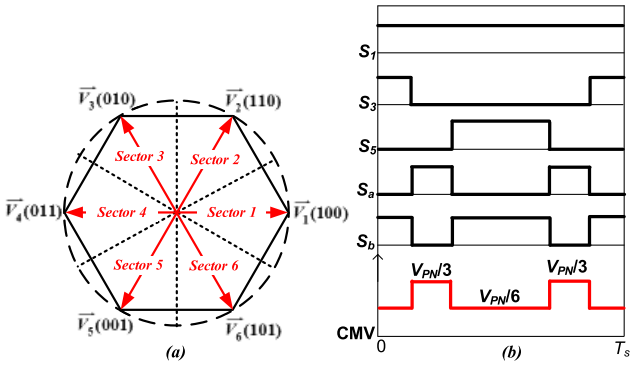

FIGURE 7. NSPWM strategy for proposed inverter. (a) Space vector in output of three-phase inverter; (b) Switching pattern and CMV of proposed SCVD-B^{2}I in sector 1.

Dwell times of $\vec{V}_0$, $\vec{V}_4$ and $\vec{V}_6$ can be calculated as:

$$\begin{cases} T_6 = Mi \cdot T_s \cdot \cos(\theta + \pi/2) \\ T_4 = Mi \cdot T_s \cdot \cos(\theta + 5\pi/6) \\ T_0 = T_s + \sqrt{3}Mi \cdot T_s \cdot \sin(\theta + \pi/6). \end{cases} \quad (8)$$

The ZEPWM strategy operates only linearly at low modulation index ($Mi < 0.57$).

C. NEAR STATE PWM (NSPWM) STRATEGY FOR PROPOSED SCVD-B^{2}I

Fig. 7 presents the NSPWM strategy for SCVD-B^{2}I. As shown in Fig. 7 (a), the NSPWM strategy uses a group of three active vectors to synthesize the output voltage vector like the NSPWM strategy [22] for conventional VSIs. Besides, similar to DPWM strategy for SCVD-B^{2}I, the switch S_a is turned off as well as the switch S_b is turned on during even active states. The switch S_a is turned on as well as the switch S_b is turned off during odd active states as shown in Fig. 7 (b). As a result, the CMV only takes values of $V_{PN}/6$ or $V_{PN}/3$. As highlighted in Fig. 7 (b), CMV of the proposed SCVD-B^{2}I is dramatically reduced. The variation of CMV is 16.6% of DC-link voltage.

Similar to the NSPWM strategy [22] for conventional VSIs, the NSPWM strategy for SCVD-B^{2}I operates only linearly at high modulation index ($Mi > 0.66$).

Table 3 highlights the comparison of the number of components, overall variation in CMV, input voltage and voltage linearity between the proposed SCVD-B^{2}I and the recent three-phase topologies using different PWM strategies. Compared to the conventional VSIs, the proposed SCVD-B^{2}I uses two more switches, two more diodes and two more capacitors as shown in Table 3. Compared to the existing three-phase inverter topologies under different PWM strategies, the required input of the proposed SCVD-B^{2}I is lowest and half of that in the other topologies for the same DC-link voltage as presented in Table 3. As a result, for the same input voltage, the output voltage of the proposed SCVD-B^{2}I can be higher than that of the existing three-phase inverter topologies under different PWM strategies. The variation in CMV of the proposed SCVD-B^{2}I under ZEPWM and NSPWM strategies is 16.6% of DC-link voltage while that of the conventional VSIs [20], [22], [23] and H8 topologies [25]–[28] is 33.3% of DC-link voltage. Compared to voltage-clamping H8 topology [25], the proposed SCVD-B^{2}I uses one less capacitor. Compared to modified H8 topology [26], the proposed SCVD-B^{2}I uses two more capacitors as shown in Table 3. The variation in CMV of the ZVR topology [29] is lowest. However, the ZVR topology uses so many switches and diodes as highlighted in Table 3.

IV. SIMULATION RESULTS

Simulations are established in PLECS software to verify the operating principle and the effectiveness of the proposed SCVD-B^{2}I as shown in Fig. 2. The main parameters of the

TABLE 3. Comparison between the proposed SCVD-B^{2}I and existing topologies for the same DC-link voltage (V_{PN}).

	Switches	Diodes	Capacitors	Overall variation in CMV	Input voltage	Voltage linearity
Conventional VSIs under AZSPWM [20]	6	0	0	$V_{PN}/3$ to $2V_{PN}/3$	$2V_g$	0 to 1
Conventional VSIs under NSPWM [22]	6	0	0	$V_{PN}/3$ to $2V_{PN}/3$	$2V_g$	0.66 to 1
Conventional VSIs under RSPWM [23]	6	0	0	$V_{PN}/3$ to $V_{PN}/3$	$2V_g$	0 to 0.57
Voltage-clamping H8 topology [25]	8	2	3	$V_{PN}/3$ to $2V_{PN}/3$	$2V_g$	0 to 1
Modified H8 topology [26]	8	2	0	$V_{PN}/3$ to $2V_{PN}/3$	$2V_g$	0 to 1
Modified H8 topology [27]	8	0	0	$V_{PN}/3$ to $2V_{PN}/3$	$2V_g$	0 to 1
Modified H8 topology [28]	8	0	0	$V_{PN}/3$ to $2V_{PN}/3$	$2V_g$	0 to 1
ZVR topology [29]	9	12	0	0	$2V_g$	0 to 1
Proposed SCVD-B^{2}I under DPWM	8	2	2	0 to $V_{PN}/3$	V_g	0 to 1
Proposed SCVD-B^{2}I under ZEPWM	8	2	2	0 to $V_{PN}/6$	V_g	0 to 0.57
Proposed SCVD-B^{2}I under NSPWM	8	2	2	$V_{PN}/6$ to $V_{PN}/3$	V_g	0.66 to 1

proposed SCVD-B^{2}I used for simulation are listed as follows: $V_g = 150$ V, $C_a = C_b = 220$ μF. The switching frequency is 10 kHz. And, the fundamental frequency is 50 Hz

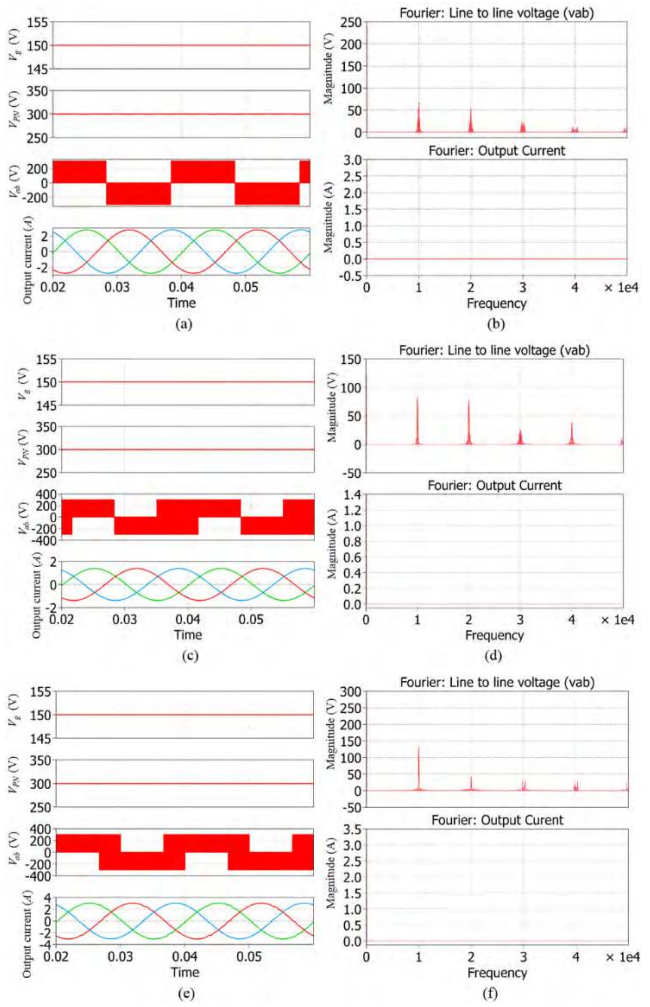

FIGURE 8. Waveforms of proposed inverter under (a)(b) DPWM strategy, (c)(d) ZEPWM strategy, and (e)(f) NSPWM strategy. From top to bottom: (a)(c)(e) input voltage, DC-link voltage, line-to-line voltage and output currents; (b)(d)(f) FFT of line-to-line voltage and FFT of output current.

First, an inductive load with $R_l = 50$ Ω and $L_l = 8$ mH is considered to test the proposed SCVD-B^{2}I. In this case, the output of inverter is filtered by an LC filter with $L_f = 3$ mH and $C_f = 10$ μF. Simulation waveforms of input voltage, DC-link voltage, line-to-line voltage, and output currents are illustrated in Fig. 8. We can see that the DC-link voltage of the proposed SCVD-B^{2}I under various PWM strategies is double of input DC voltage. As shown in Fig. 8 (a), Fig. 8 (c) and Fig. 8 (e), the DC-link voltage of the proposed SCVD-B^{2}I is stepped up to 300 V. As shown in Fig. 8 (a) and Fig. 8 (b), the proposed SCVD-B^{2}I under DPWM strategy produces unipolar output line-to-line voltage. The fundamental harmonic value of output line-to-line voltage is 240 V at modulation index, $Mi = 0.8$. The RMS value of output currents are 1.95 A as well as THD of output currents are about 0.4%.

Unlike DPWM strategy, the proposed SCVD-B^{2}I under ZEPWM strategy produces bipolar output line-to-line voltage. As observed in Fig. 8 (c), the output line-to-line voltage changes from $+V_{PN}$ to -V_{PN} during interval time of sector 3. The fundamental harmonic value of output line-to-line voltage is 120 V at modulation index, $Mi = 0.4$.

The RMS value of output currents are 0.98 A as well as THD of output currents are about 0.7%. Similar to ZEPWM strategy, the proposed SCVD-B^{2}I under NSPWM strategy also produces bipolar output line-to-line voltage. As observed in Fig. 8 (e), the output line-to-line voltage changes from $+V_{PN}$ to $-V_{PN}$ during interval time of sector 3. The fundamental harmonic value of output line-to-line voltage is 270 V at modulation index, $Mi = 0.9$. The RMS value of output currents are 2.2 A as well as THD of output currents are about 0.9%.

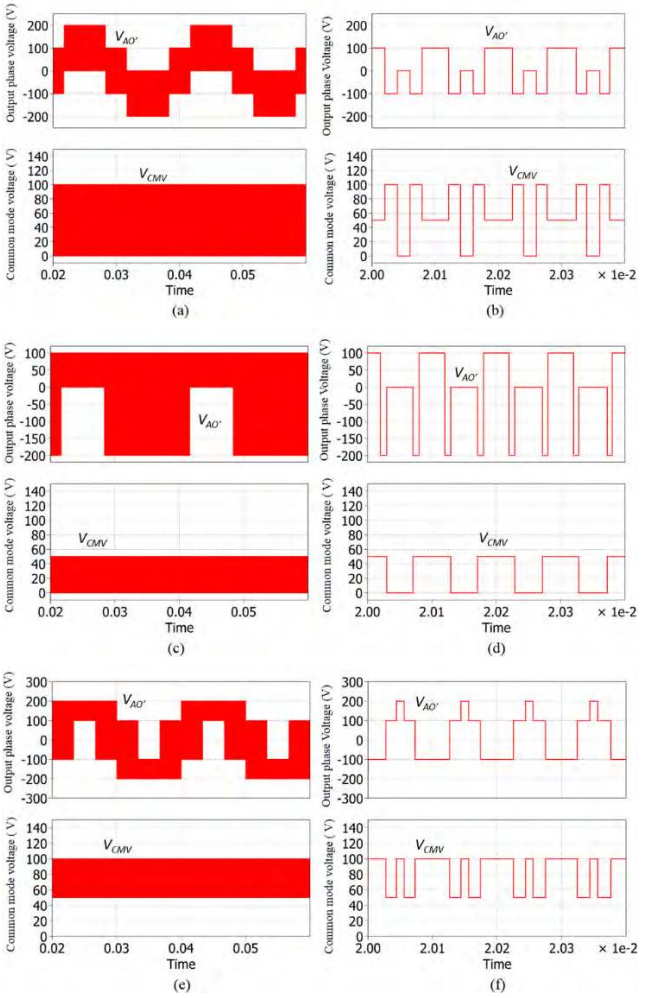

FIGURE 9. Phase-A voltage and common-mode voltage of proposed inverter under (a)(b) DPWM strategy, (c)(d) ZEPWM strategy, and (e)(f) NSPWM strategy.

Fig. 9 shows simulation waveforms of phase-A voltage and CMV under various PWM strategies. As shown in Fig. 9 (a) and Fig. 9 (b), the magnitude of CMV of the proposed SCVD-B^{2}I under DPWM strategy is equal to 100*V*,

i.e., *33.3%* V_{PN}. A zoom version of The variation of CMV is highlighted in Fig. 9 (b). We can see that the CMV during powering modes is 50 V or 100 V, and the CMV during freewheeling mode is 0 V as highlighted in Fig. 9 (b).

The magnitude of CMV of the proposed SCVD-B^{2}I under ZEPWM strategy is equal to 50*V,* i.e.,16.6%V_{PN}. A zoom version of the variation of CMV is highlighted in Fig. 9 (d). We can see that the CMV changes from 0V to 50V as highlighted in Fig. 9 (d). The magnitude of CMV of the proposed SCVD-B^{2}I under NSPWM strategy is equal to 50*V,* i.e.,16.6% V_{PN}. A zoom version of the variation of CMV is highlighted in Fig. 9 (e). Unlike ZEPWM strategy, we can see that the CMV of proposed SCVD-B^{2}I under NSPWM strategy changes from 50 V to 100 V as highlighted in Fig. 9 (f).

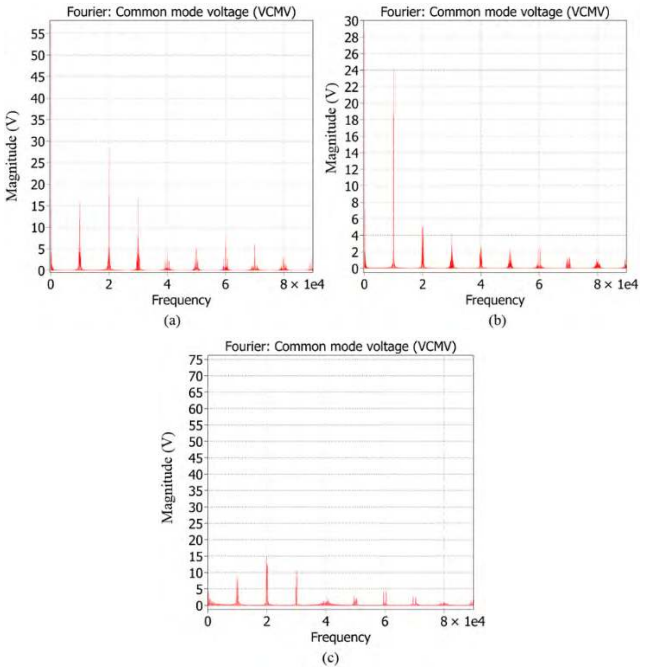

FIGURE 10. FFT of common-mode voltage. (a) DPWM strategy, (b) ZEPWM strategy, and (c) NSPWM strategy.

Fig. 10 shows the corresponding frequency spectrum of CMV of proposed SCVD-B^{2}I under various PWM strategies. From Fig.10, we can see that the amplitudes of CMV at high frequency of proposed SCVD-B^{2}I under ZEPWM and NSPWM strategies are lower than that of proposed SCVD-B^{2}I under DPWM strategy.

Second, the proposed SCVD-B^{2}I is tested in the grid-tied mode. The grid voltage is 110 V/50 Hz. Three-phase L_f filter with $L_f = 8$ mH is used between the grid and the inverter. The stray capacitor, C_{PV} is 330 nF. Because DC-link voltage of the proposed SCVD-B^{2}I is double of input voltage while DC-link voltage of the proposed SCVD-B^{2}I is the same as input voltage. For the same DC-link voltage, the input voltage for the proposed SCVD-B^{2}I and conventional VSIs are 150 V and 300 V, respectively. Fig. 11 shows simulation waveforms of grid voltage, grid current and leakage current for conventional VSIs and proposed SCVD- B^{2}I. As shown

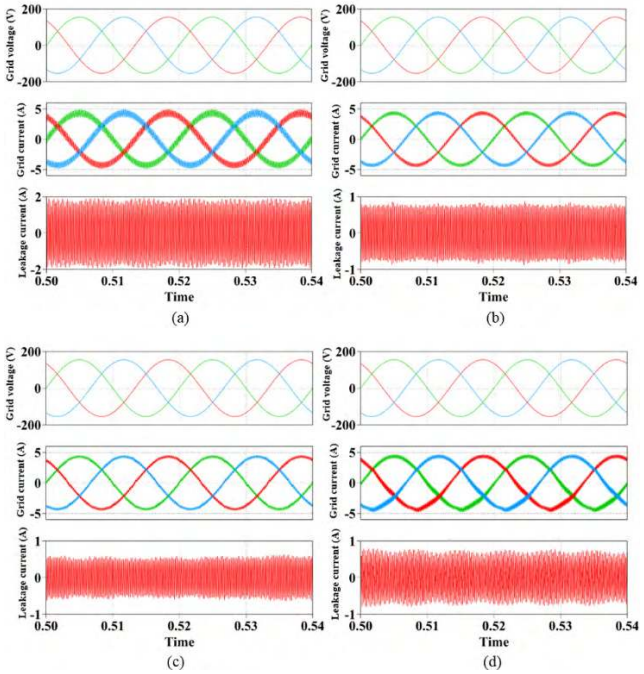

FIGURE 11. Grid voltage, output current and leakage current for (a) the conventional VSIs with DPWM strategy; (b) proposed inverter with DPWM strategy; (c) proposed inverter with NSPWM strategy; and (d) proposed inverter with ZEPWM strategy.

in Fig. 11 (a), the output current ripples of VSIs under DPWM method are very high because of high leakage current. THD of the output current is 11%. The magnitude of leakage current is 1.8 A.

With proposed SCVD-B^{2}I, the magnitude of leakage current is limited due to the reduced CMV. As shown in Fig. 11 (b), the output current ripples of proposed SCVD-B^{2}I under DPWM method are reduced. THD of the output current is 5%. The magnitude of leakage current is significantly limited to 0.8 A. Similarly, the output current ripples of proposed SCVD-B^{2}I under NSPWM method are significantly reduced as shown in Fig. 11 (c). THD of the output current is 2.6%. The magnitude of leakage current is significantly limited to 0.49 A. Unlike DPWM method and NSPWM method, The ZEPWM method operates only linearly at low modulation index ($Mi < 0.57$). So, the input voltage for proposed SCVD-B^{2}I under ZEPWM method is 300 V. As shown in Fig. 11 (d), the output current ripples of proposed SCVD-B^{2}I under DPWM method are high. THD of the output current is 8%. The magnitude of leakage current is significantly limited to 0.9 A. The leakage current of proposed SCVD-B^{2}I under ZEPWM method is higher than that under NSPWM method because of operating at low modulation index.

V. EXPERIMENTAL RESULTS

A laboratory prototype of proposed SCVD-B^{2}I has been constructed to prove the effectiveness of the proposed SCVD-B^{2}I. Fig. 12 shows a photograph of the experimental setup. The parameters of the proposed SCVD-B^{2}I used for the experiment are the same as those in the simulation. Due to

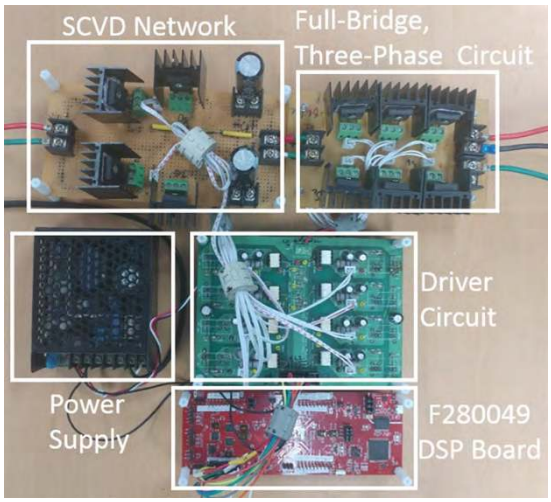

FIGURE 12. Prototype photo of the proposed SCVD-B^{2}I.

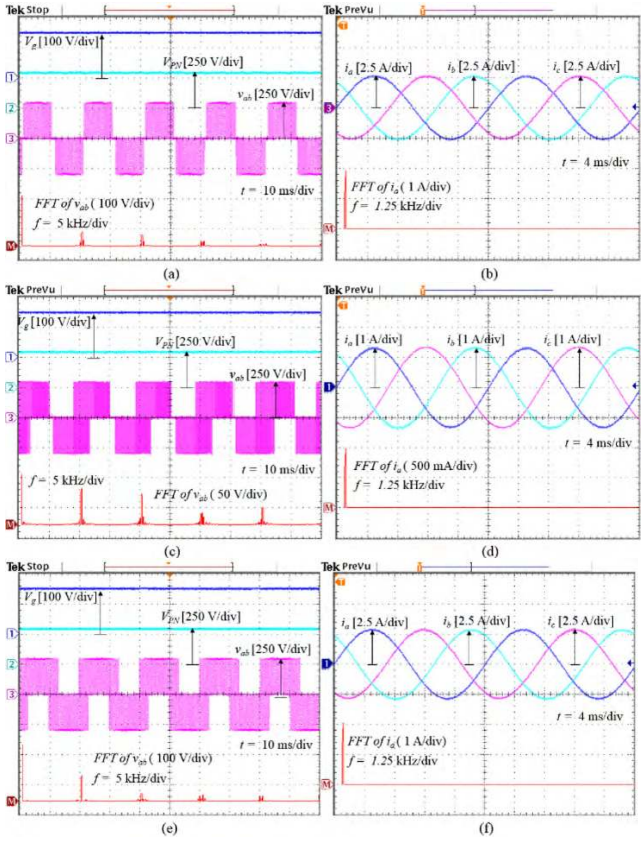

FIGURE 13. Experimental output waveforms of proposed inverter under (a)(b) DPWM strategy, (c)(d) ZEPWM strategy, and (e)(f) NSPWM strategy. From top to bottom: (a)(c)(e) input voltage, DC-link voltage, line-to-line voltage and FFT of line-to-line voltage; (b)(d)(f) output currents and FFT of output current.

limitation of laboratory, the inductive load is only used to verify the performance of the proposed SCVD-B^{2}I.

Fig. 13 shows the experimental results of input voltage, DC-link voltage, line-to-line voltage and output currents under various PWM strategies. As highlighted in Fig. 13 (a), Fig. 13 (c) and Fig. 13 (e), the DC-link voltage of the proposed SCVD-B^{2}I is stepped up to 297 V from the input

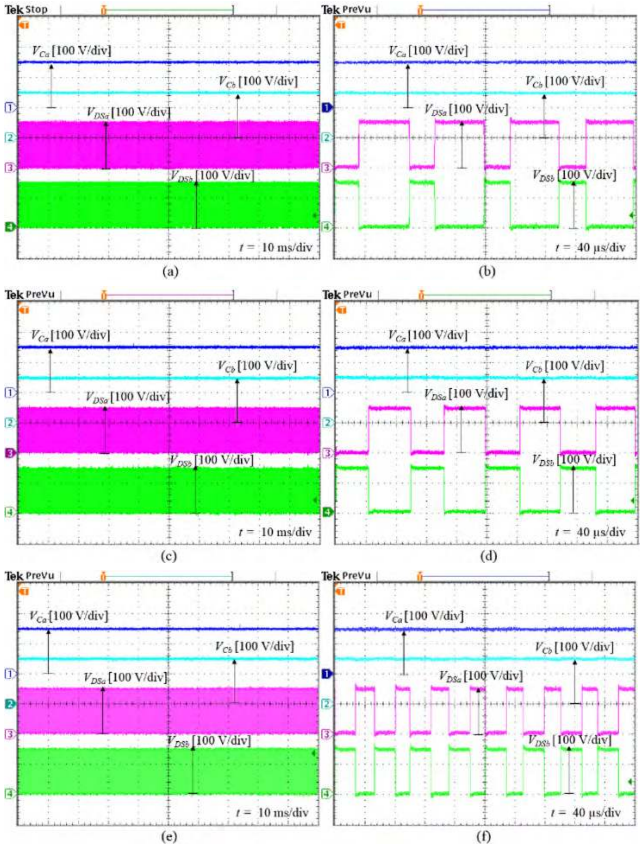

FIGURE 14. Experimental output waveforms of proposed inverter under (a)(b) DPWM strategy, (c)(d) ZEPWM strategy, and (e)(f) NSPWM strategy. From top to bottom: capacitor Ca voltage, capacitor Cb voltage, voltage across switch S_a and voltage across switch S_b.

voltage of 150 V. As shown in Fig. 13 (a), the proposed SCVD-B^{2}I under DPWM strategy produces unipolar output line-to-line voltage. The fundamental harmonic value of output line-to-line voltage is 169 Vrms at modulation index, $Mi = 0.8$. The RMS value of output currents are 1.95 Arms as well as THD of output currents are about 0.9% as shown in Fig. 13 (b). Under ZEPWM strategy, the proposed SCVD-B^{2}I produces bipolar output line-to-line voltage. As observed in Fig. 13 (c), during interval time of section 3, the output line-to-line voltage changes from 297 V to -297 V. The fundamental harmonic value of output line-to-line voltage is 84 Vrms at modulation index, $Mi = 0.4$. The RMS value of output currents are 0.97 Arms as well as THD of output currents are about 1%. Like ZEPWM strategy, we can see that the proposed SCVD-B^{2}I under NSPWM strategy also produces bipolar output line-to-line voltage. As observed in Fig. 13 (e), the output line-to-line voltage changes from $297V$ to $-297V$ during interval time of sector 3. The fundamental harmonic value of output line-to-line voltage is 189 Vrms at modulation index, $Mi = 0.9$. The RMS value of output currents are 2.18 Arms as well as THD of output currents are about 1.2%. The measured efficiency of proposed SCVD-B^{2}I is around 97.4% at 710 W.

Fig. 14 shows the experimental results of the capacitor C_a voltage, the capacitor C_b voltage, drain-source voltages of

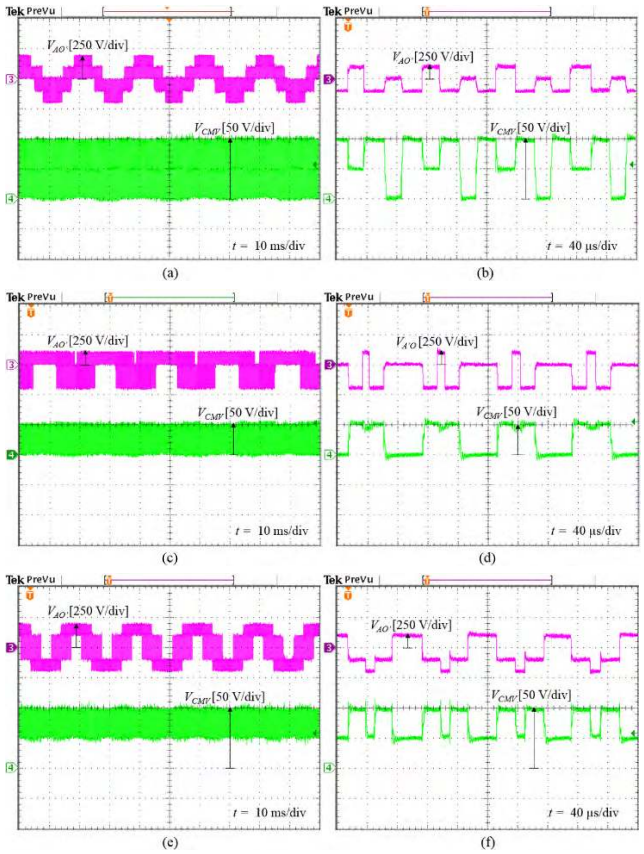

FIGURE 15. Phase-A voltage and common-mode voltage of proposed inverter under (a)(b) DPWM strategy, (c)(d) ZEPWM strategy, and (e)(f) NSPWM strategy.

S_a and S_b. As shown in Fig. 14, the capacitor C_a voltage, the capacitor C_b voltage and drain-source voltages of S_a and S_b are equal to the input voltage V_g. From Fig. 14, we can see that the switching frequency of S_a and S_b under NSPWM strategy is higher than that under ZEPWM strategy and DPWM strategy. So, switching loss under NSPWM strategy is high.

Fig. 15 shows experimental results of phase-A voltage and CMV under various PWM strategies. As indicated in Fig. 15 (a) and Fig. 15 (b), the magnitude of the CMV of the proposed SCVD-B^{2}I under DPWM strategy is equal to 100*V*, i.e., 33.3%V_{PN}. As shown in Fig. 15 (b), the CMV during powering modes is 50 V or 100 V, and the CMV during freewheeling mode is 0 V. The magnitude of CMV of the proposed SCVD-B^{2}I under ZEPWM strategy is equal to 50*V*, i.e.,16.6%V_{PN}. The CMV changes from 0V to 50V as highlighted in Fig. 15 (d). The magnitude of common-mode voltage of the proposed SCVD-B^{2}I under NSPWM strategy is equal to 50*V*, i.e.,16.6% V_{PN}. Unlike ZEPWM strategy, as highlighted in Fig. 15 (f), the CMV of proposed SCVD-B^{2}I under NSPWM strategy changes from 50 V to 100 V.

Fig. 16 shows the corresponding frequency spectrum of CMV of proposed SCVD-B^{2}I under various PWM strategies. From Fig. 16, we can see that the amplitudes of CMV at high frequency of proposed SCVD-B^{2}I under DPWM strategy are

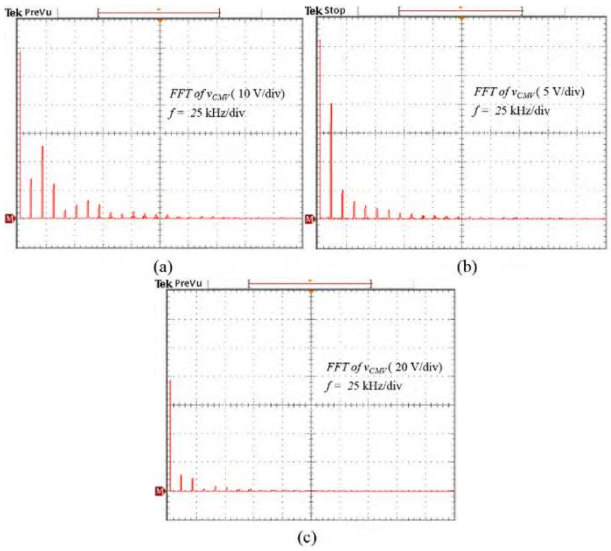

FIGURE 16. FFT of common-mode voltage. (a) DPWM strategy, (b) ZEPWM strategy, and (c) NSPWM strategy.

higher than that of proposed SCVD-B^{2}I under ZEPWM and NSPWM strategies.

VI. CONCLUSION

This paper has presented a modified three-phase two-level voltage source inverter topology for common-mode voltage reduction. By adding at dc side of the conventional three-phase H-bridge inverter a SCVD network which includes two switches, two diodes, and two capacitors, the DC-link voltage of proposed inverter is double of input voltage. Therefore, the output voltage of the proposed SCVD-B^{2}I can be higher than the input voltage. Like the previous works, the magnitude of common-mode voltage of the proposed SCVD-B^{2}I under DPWM strategy is equal to 33.3% V_{PN}. The common-mode voltage of the proposed SCVD-B^{2}I under DPWM strategy changes from 0 to $V_{PN}/3$. Furthermore, for higher modulation index, NSPWM strategy can be utilized. The magnitude of common-mode voltage of the proposed SCVD-B^{2}I under NSPWM strategy is only equal to 16.6% V_{PN}. For lower modulation index, ZEPWM strategy can be utilized. Similar to NSPWM strategy, Under ZEPWM strategy, the magnitude of common-mode voltage of the proposed SCVD-B^{2}I is also equal to 16.6% V_{PN}. Mathematical analysis, operating principles, and simulation results using PLECS software are presented. Also, a comparison of the proposed three-phase two-level voltage source inverter with the conventional three-phase voltage source inverters are presented. A laboratory prototype based on a TMS320F280049 DSP is built to validate the performance of the proposed three-phase inverter topology.

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TAN-TAI TRAN received the B.S. degree in electrical and electronic engineering technology and the M.S. degree in electronic engineering from the Ho Chi Minh City University of Technology and Education, Ho Chi Minh City, Vietnam, in 2012 and 2016, respectively. He is currently pursuing the Ph.D. degree with the Department of Electrical Engineering, Chonnam National University, Gwangju, South Korea. His current research interests include renewable energy systems, automation systems, dc-dc converters, and dc-ac inverters.

MINH-KHAI NGUYEN (S'09–M'12–SM'18) received the B.S. degree in electrical engineering from the Ho Chi Minh City University of Technology, Ho Chi Minh City, Vietnam, in 2005, and the M.S. and Ph.D. degrees in electrical engineering from Chonnam National University, Gwangju, South Korea, in 2007 and 2010, respectively. He was a Lecturer with the Ho Chi Minh City University of Technology and Education, Ho Chi Minh City, and an Assistant Professor with Chosun University, Gwangju, South Korea. He is currently with the School of Electrical Engineering and Computer Science, Queensland University of Technology, Australia. His current research interests include impedance-source inverters and power converters for renewable energy systems. He had served as a Guest Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS special issue on the impedance source converter topologies and applications. He is currently an Associate Editor for the *Journal of Power Electronics* and the *International Journal of Power Electronics*.

TRUONG-DUY DUONG received the B.S degree in electronic telecommunication engineering from the Ho Chi Minh City University of Technology and Education, Ho Chi Minh City, Vietnam, in 2015, and the M.S. degree in electrical engineering from Chonnam National University, Gwangju, South Korea, in 2018, where he is currently pursuing the Ph.D. degree with the Department of Electrical Engineering. His current research interests include the topologies and control of dc-dc converters and dc-ac inverters.

JOON-HO CHOI (S'98–M'02) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Soongsil University, Seoul, South Korea, in 1996, 1998, and 2002, respectively. Since 2003, he has been a Professor with Chonnam National University, Gwangju, South Korea. His research interests include operation and integration and control strategies of distributed generation, distribution automation, and modelling and operation algorithms of the smart grid. He is a Life Member of the KIEE and The Korean Institute of Illuminating and Electrical Installation Engineers, and a Committee Member of IBS Korea. Since 2004, he has been an Associate Editor of the *Transactions of the KIEE*.

YOUNG-CHEOL LIM (M'85) was born in Chonnam, South Korea, in 1953. He received the B.S. degree in electrical engineering from Chonnam National University, Gwangju, South Korea, in 1975, and the M.S. and Ph.D. degrees from Korea University, Seoul, South Korea, in 1977 and 1990, respectively.

In 1981, he became a Professor at Chonnam National University, where he was the Director of the Research Center for High-Quality Electric Components and Systems, from 1998 to 2007. He was the President of the Korea Institute of Power Electronics (KIPE), in 2009. He has been involved in various academic societies, such as the KIPE, the Korean Institute of Electrical Engineers, and the Institute of Control, Automation, and Systems Engineers, South Korea. He is the coauthor of three books. He has authored or coauthored more than 200 published technical papers. His current research interests include power electronics, control instruments, and neurofuzzy control. He has received a number of awards, including the 2000 KIPE Best Paper Award, and the 2001 KIPE Academic Award.

FIRUZ ZARE (S'98–M'01–SM'06) received the Ph.D. degree in power electronics from the Queensland University of Technology, Australia, in 2002. He has spent several years in industry as a Team Leader, working on power electronics and power quality projects. He is currently an Academic Staff with The University of Queensland, Australia, and a Task Force Leader of Active Infeed Converters within the Working Group one at the IEC Standardization TC77A. He has published over 220 journals and conference papers and technical reports in the area of power electronics. His main research interests include power electronics topology, control and applications, power quality, and regulations and pulsed power applications. He has received several awards, such as the Australian Future Fellowship, the Symposium Fellowship by the Australian Academy of Technological Science, the Early Career Academic Excellence Research Award, and the John Madsen Medal from Engineers Australia. He is the Editor-in-Chief of the *International Journal of Power Electronics* and an Associate Editor of the IEEE ACCESS and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS.