17.1 A System-on-Chip EPC Gen-2 Passive UHF RFID Tag with Embedded Temperature Sensor

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A system-on-chip passive UHF RFID tag with embedded temperature sensor is developed in a standard 0.18μm CMOS process for the EPC Gen-2 protocol from 860-960MHz [1]. Flip-chip technology is used to bond the developed tag IC to an antenna to realize a complete tag inlay, which is successfully demonstrated and evaluated in real-time wireless communications with commercial RFID readers.

Figure 17.1.1 shows the block diagram of the tag IC. Multiple supply voltages, generated by a power management unit (PMU) using a separate-storage-capacitor technique to save area, are employed to optimize the performance of individual building blocks, while minimizing the total power consumption. A dual-path clock generator is used to generate on-chip clocks for signal processing to support both applications with either very accurate link frequency or very low power consumption. A low-power temperature sensor is also embedded with a gain-compensation technique that makes use of current correlation from the same bandgap reference (BGR) for the clock generator to reduce the temperature sensing error due to process variations.

Figure 17.1.2 shows the PMU. The rectifier (RECT1) supplies the 670nA BGR while the core RF-DC conversion is performed by a triple-output rectifier (RECT2). Further supply regulation is done using low-dropout regulators (LDRs). For the duration of PW (=Tari/2) [1], as the RF input is significantly attenuated due to the data modulation, the rectifier becomes inactive, and a storage capacitor C_S is employed to supply both the load current I_L and the reverse leakage current I_{leak} that flows back to the rectifier, which results in a ripple voltage of $VR_{CS}=(I_L+I_{leak})\times PW/C_S$. In existing work [2], all the blocks share one single capacitor C_S, which needs to be large enough to meet the ripple voltage requirement of the most noise-sensitive block. To provide a highly stable current for the dual-path clock generator, the BGR is required to have a small supply ripple of 0.1V, and, as a result, the single C_S would need to be at least 1.75nF to supply the nominal total I_L of 14μA when Tari=25μs. In our work, three separate capacitors, C_{Sx} (x=1,2,3), are employed for different blocks with different optimal ripple voltages (0.4V, 0.25V, 0.1V, respectively), which helps to significantly reduce the total capacitance to 805pF, even with >10% margins. The switches S_x (x=1,2,3) are controlled by the demodulator's output to cut off I_{leak} during PW, which helps further reduce both the sizes of C_{Sx} and the required input power for replenishing. M_{ST1} and M_{ST2} are used for start-up. High voltages of 3.5V and 7.8V, used for programming the OTP memory, are generated by three charge pumps (QPs). During the WRITE operation, a VCO is activated to regulate the QP_VPP's output at 7.8V with an output current up to 20μA. With sufficient input power, the power detector (PD) sends a Power-Good (PG) signal to turn on S_4 to power up LDR_3 for the injection-locked frequency divider (ILFD) in the dual-path clock generator.

Figure 17.1.3 shows the dual-path clock generator. In the first path, to achieve the stringent link frequency accuracy (<±4%) over PVT variations specified by the EPC Gen-2 protocol, a proposed 19.5μW divide-by-3 ILFD followed by a cascade of divide-by-2 dividers is employed to derive an on-chip clock (~2.3MHz) directly from the RF input. A 1V current-starved ring oscillator with 300MHz self-oscillation frequency is used as the divider core, which is biased by a temperature-independent current I_{REF} from BGR to reduce frequency sensitivity due to temperature variations. A voltage limiter is inserted between the antenna and the ILFD input to handle large input signals. The output swing of the first ILFD and the supply voltages of the succeeding lower-frequency dividers are designed to be 0.5V to minimize power consumption. However, the ILFD working at the RF frequency consumes relatively large power. For applications that require better sensitivity, a low-power temperature-compensated oscillator (TCO) is also employed in a second clock path to trade off power dissipation with frequency accuracy. Different from [3], the TCO frequency is made to be proportional to the BGR current, which allows a co-design with the temperature sensor for gain compensation. Moreover, a temperature-independent frequency can be obtained by adjusting the temperature coefficient of the bias current I_{BIAS}. As shown in Figure 17.1.5, the measured TCO's frequency variation is within ±2.65% with a much smaller power (1.5μW) than existing solutions [3][5]. Clock-path selection is automatically done by the power detector to turn the ILFD clock path ON or OFF depending on the available input power.

Existing solutions for embedded temperature sensors in passive RFID tags mainly suffer from a severe trade-off between accuracy and power. The sensor in [4] achieves an error of +2.4/–2.0°C by using a ΣΔ ADC readout with one-point calibration but consumes 9.2μW, which is 80% of the whole tag's power. In [5] and [6], the sensors consume merely 1.6μW and 0.22μW, respectively, but both require 2-point calibration to achieve errors of ±2.4°C and +3.0/–1.6°C, respectively. Figure 17.1.4 shows the presented embedded sensor using only 1-point calibration to achieve good sensing accuracy. Time-domain readout is employed to eliminate the power-hungry ADCs. A temperature-modulated pulse-width signal sen_PW is generated by integrating the PTAT and the CTAT currents and is then quantized using the TCO clock. The sensor and the TCO use the PTAT and CTAT currents generated from the same BGR in PMU so that the current changes due to process variations in the two blocks track each other. The sensor gain, which is defined as the digitized difference of sen_PW at the maximum and minimum temperature divided by the temperature range, is inversely proportional to the BGR current while the TCO clock frequency is proportional to the BGR current, which allows gain compensation due to current variation. Flicker noise is reduced by resetting the current signals after each conversion, and is averaged out together with wideband noise using on-chip averaging. At room temperature, the power of the sensor block is 104nW at 25S/s. The measured results of three samples demonstrate an accuracy of +0.4/–1.1°C after 1-point calibration (Fig. 17.1.5), which is small enough for food-monitoring applications. The ENOB of the sensor is 8b, and the corresponding resolution is about 0.35°C.

A 16×8b one-time-programmable (OTP) memory array based on gate-oxide anti-fuse technology in a standard CMOS process with no extra mask, is also embedded. The baseband implements an EPC-compliant custom command to perform the complete SENSE-WRITE-READ operation (Fig. 17.1.4) in addition to all the mandatory commands required by the EPC Gen-2 protocol.

The complete tag chip with 1.1mm^2 area is fabricated in a standard 0.18μm CMOS process. As shown in Figure 17.1.7, the tag IC is aligned and bonded onto the antenna printed on PET film using flip-chip technology with Au stud bumps for low cost. Tested with an RFID tester and commercial RFID handheld readers, the tag inlay shows a sensitivity of –6dBm and a sensing error of +0.4/–1.1°C with 1-point calibration. The measured performance is summarized in Figure 17.1.6.

Acknowledgements:
This work was supported by the grant ITP/027/07LP funded by Hong Kong Innovation and Technology Fund (ITF) with support from the Hong Kong R&D Center for Logistic Supply Chain Management.

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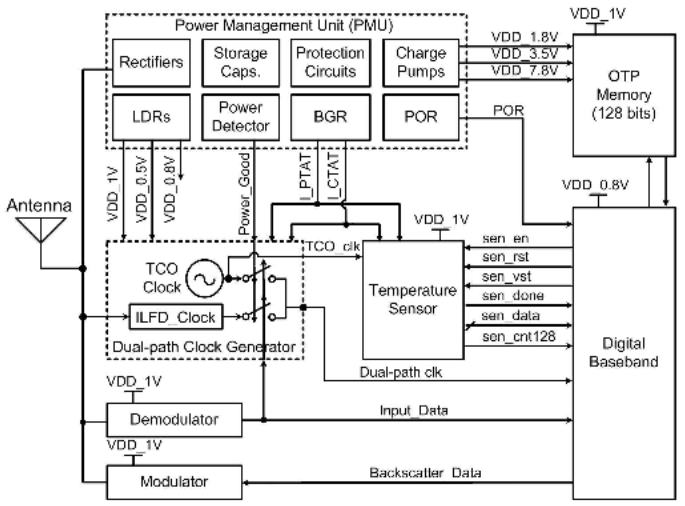

Figure 17.1.1: Block diagram of the developed passive RFID tag IC.

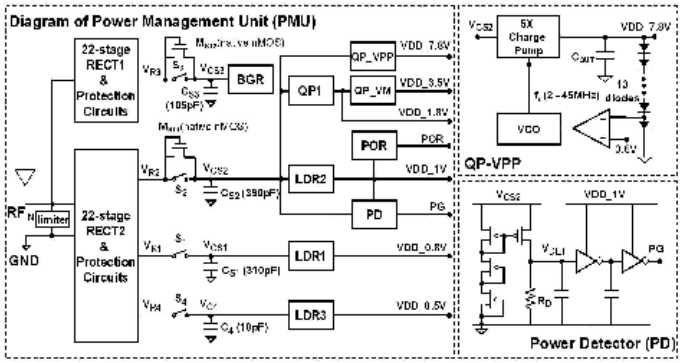

Figure 17.1.2: Block diagram and schematics of the proposed power-management unit.

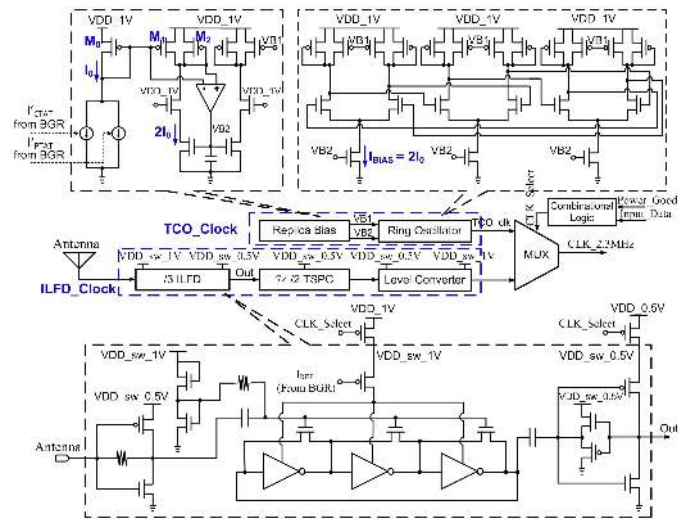

Figure 17.1.3: Block diagram and schematics of the proposed dual-path clock generator.

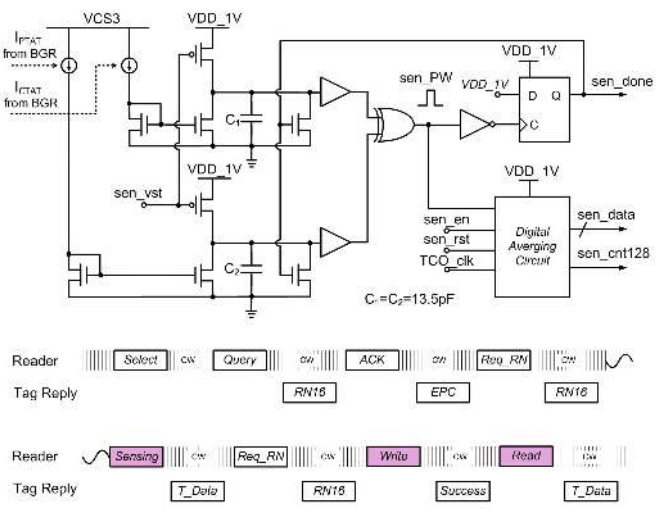

Figure 17.1.4: Simplified schematic of the integrated temperature sensor and the SENSE-WRITE-READ working flow.

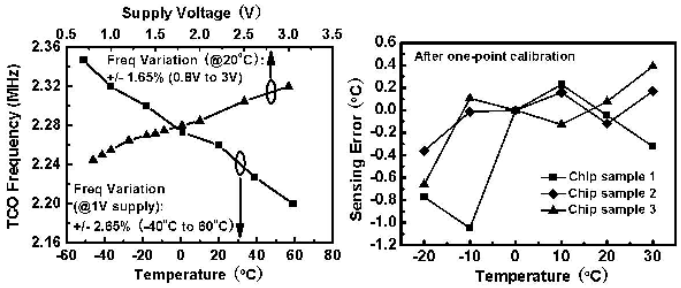

Figure 17.1.5: Measured TCO frequency variation and temperature sensing error after one-point calibration.

	This work	[4]	[5]	[6]
Process	0.18μm CMOS	Not available	0.25 μm CMOS	0.18 μm CMOS
Tag chip Area	1.1 mm²	1.4 mm²	0.42 mm²	Not applicable
Frequency range	860-960MHz	100-150kHz	860-960MHz	Not applicable
Commercial standard supported	EPCglobal Gen 2 Compliant	Not available	Not available	Not applicable
Tag Type	Passive	Passive	Passive	Not applicable
Tag Loading Power Consumption	12μW (only TCO clock activated)	12 μW (10μA/Assuming 1.2V supply)	5.1μW	Not applicable
Sensitivity	-6 dBm (only TCO clock activated)	Not available	Not available	Not applicable
Reading and Temperature Sensing Distance	4 m (Reader EIRP 4W, only TCO clock activated)	10-25cm	Not available	Not applicable
Internal Clock Frequency (local oscillator)	2.2MHz	100-150kHz	330kHz	100kHz
Sensor	Temperature sensor	Temperature sensor	Temperature and photo sensors	Temperature sensor
Power Consumption of Temperature Sensor	(0.104 +0.8 +1.5)μW (Sensor+BGR+TCO)[1]	9.6 μW (8μA/Assuming 1.2V supply)	(1.2+1.8)μW (Sensor+TCO)[1]	0.22 μW
Temperature Sensing Range	-20°C to 30°C	0°C to 100°C	0°C to 80°C	0°C to 100°C
Sensing Error	+0.4/-1.1 °C [2]	+2.5/-2 °C [2]	+/-2.4 °C [3]	+3/-1.6 °C [3]
ENOB	8 bits @25 samples/s	Not available	Not available	6.5 bits @100 samples/s

[1] The BGR and TCO are also required by other functions of tag, and are not dedicated for temperature sensor.
[2] After one-point calibration.
[3] After two-point calibration.

Figure 17.1.6: Measured tag performance and comparison with other tags and temperature sensors.

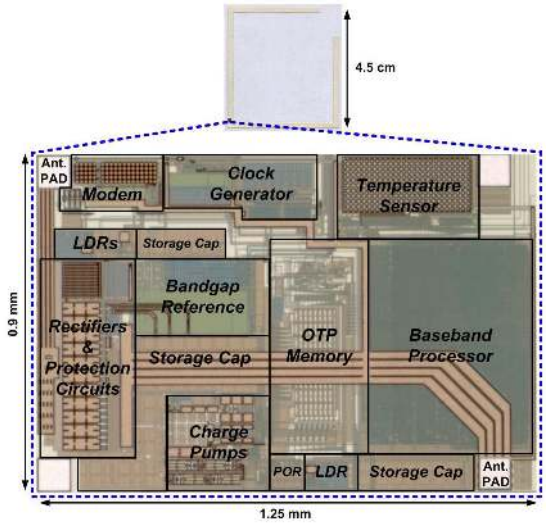

Figure 17.1.7: Chip micrograph of the presented passive RFID tag IC and the complete inlay with tag IC flip-chip bonded to antenna.

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