A T-Coil-Enhanced 8.5 Gb/s High-Swing SST Transmitter in 65 nm Bulk CMOS With < -16 dB Return Loss Over 10 GHz Bandwidth

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Abstract—A source-series-terminated (SST) transmitter in a 65 nm bulk CMOS technology is presented. The circuit exhibits an eye height greater than 1.0 V for data rates of up to 8.5 Gb/s. A thin-oxide pre-driver stage running at 1.0 V drives 22 parallel connected thick-oxide SST output stages operated at 1.5 V that feature a 5-bit 2-tap FIR filter whose adaptation is independent of the impedance tuning. To achieve a return loss of < -16 dB up to 10 GHz a 40 μm × 40 μm T-coil complements the transmitter output. This half-bit-rate clock SST transmitter has a duty-cycle restoration capability of 5x, and the common-mode voltage noise is below 10 mV rms for high-, mid- and low-level terminations. The chip consumes 96 mW at 8.5 Gb/s and occupies 180 μm × 360 μm. In addition to the transmitter design, guidelines for the T-coil design are presented.

Index Terms—De-emphasis, impedance tuning, return loss, source series termination, T-coil.

I. INTRODUCTION

IN HIGH-SPEED data transmission, current-mode-logic (CML) style transmitters are frequently employed because they support high data rates and have an inherently low susceptibility to power supply noise. These advantages, however, come along with some drawbacks, such as the static power consumption and the inability to support different dc termination voltages as the CML output always refers to one of the two power supply rails. Source-series-terminated (SST) signaling overcomes these disadvantages with a CMOS-oriented design style, supporting many different termination voltages combined with a higher signal swing. A conceptually similar design style has been proposed in series-terminated line drivers [1]–[3] or in the stub-series-terminated logic commonly used in double-data-rate (DDR) memory circuits [4]. Recent work on transmitters with voltage-mode output stages can be found in [5], [6]. Reference [6] also proposes an independent control of the impedance tuning and the equalization, but in contrast to our transmitter that approach is not based on enhancing the sliced output stages with a complete set of de-emphasis weights.

Apart from the high versatility due to the support of many different common mode voltages at the receiver with the same transmitter circuit, the advantages of the SST concept lie in its potential for low-power operation, good technology scaling due to the high content of digital circuitry, and the comparatively large signal swing. These factors make SST line drivers particularly suitable for multi-standard I/Os. Some standards however-especially those with optical extensions or legacy constraints to earlier signaling schemes with higher voltage levels-call for larger vertical eye openings that require raising the dc supply voltage from the typical 1.0 V limit for thin-oxide FETs in 65 nm technology to 1.5 V or even higher. These high-swing requirements are addressed in the proposed SST transmitter by combining a thin-oxide pre-driver stage running at 1.0 V with successive parallel connected thick-oxide SST output stages operated at 1.5 V. Key features of this design include the implementation of tri-statable output slices for impedance tuning and a 2-tap equalization with 5-bit resolution whose adaptation is independent of the impedance tuning control. To the best knowledge of the authors, this paper describes the first application of T-coils to an SST transmitter in order to achieve an outstanding output return loss performance. Another important building block of this design is the level-shifter between the thin-oxide pre-driver and the successive thick-oxide output stages.

The high-swing SST transmitter presented is derived from an earlier regular swing design [7], from which architectural concepts for the design of the clock path and in parts for the pre-driver have been adopted. Throughout this paper cross-references and comparisons to this earlier work are made to point out the relevant differentiations between this high-swing SST transmitter and the earlier regular-swing version.

The paper is organized as follows. Section II describes the basic principle of source-series-termination. A general discussion on the impedance tuning and the equalization of SST transmitters is given in Section III. In Section IV the high-swing SST transmitter implemented is presented. Section V describes the ESD protection scheme applied and the T-coil design, for which design considerations are outlined as well. In Section VI the measurement results are discussed. Section VII presents a summary and the conclusions of this work.

II. CONCEPT OF SOURCE-SERIES-TERMINATION

Fig. 1 illustrates the basic topology of an SST transmitter. The driver output stage is subdivided into a pull-up and a
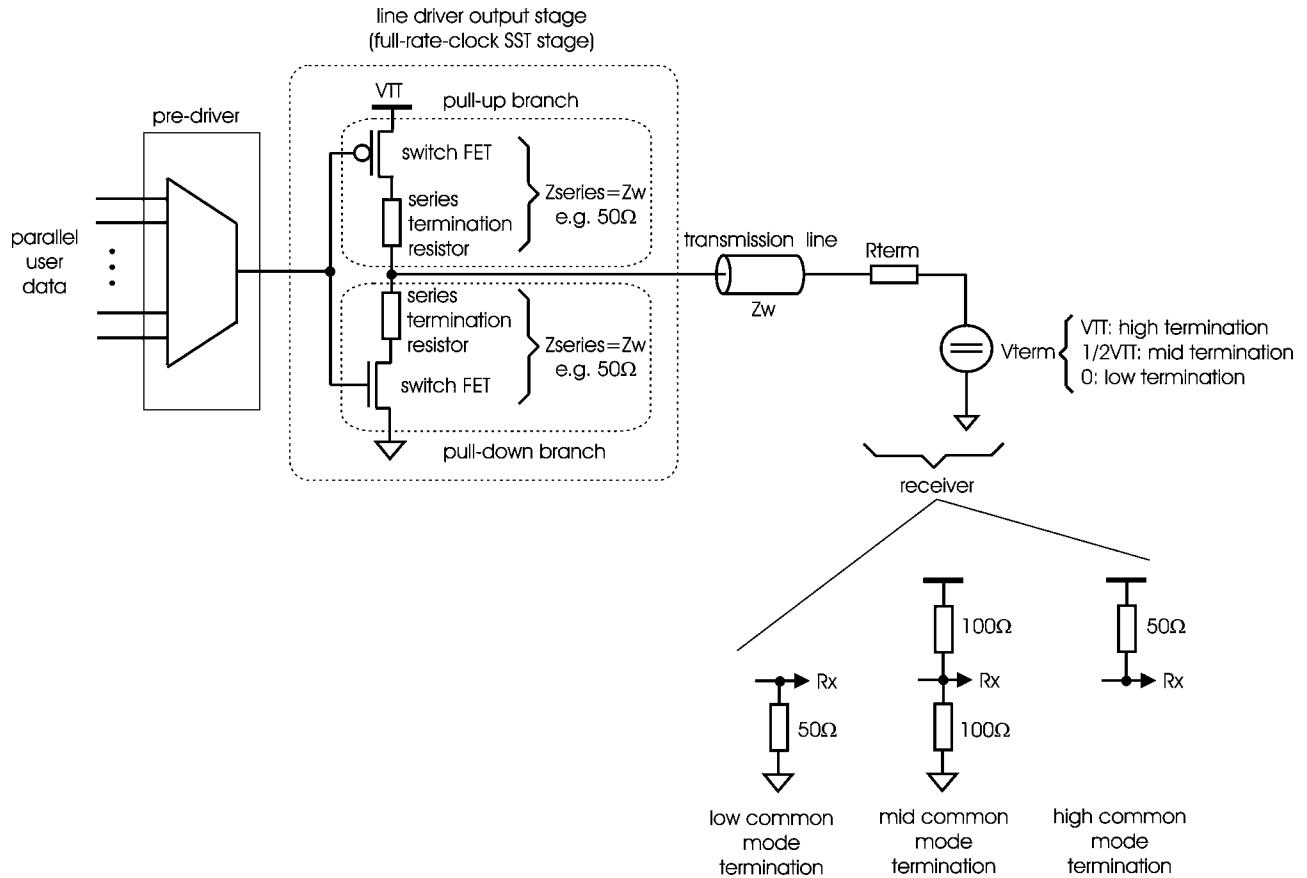
Fig. 1. Basic principle of source series termination.

pull-down branch implemented as a PMOS or NMOS switch transistor followed by a series termination resistor. Each of the two branches is impedance-matched to the transmission line impedance, which is typically 50 Ω. The term 'source' in SST refers to the fact that the transmitter can be regarded as being "self-terminated" because the far-end termination at the receiver does not necessarily have to be part of the transmitter termination. Ideally, the resistance of the pull-up/pull-down branches should be dominated by the corresponding series termination resistor because the resistance of the switch FETs is rather nonlinear and susceptible to process variations. However, to obtain a negligible resistance of the FETs in the on-state, their widths must be rather big and consequently the FETs provide a high load capacitance for the pre-driver, which contradicts the design target of high-speed and low-power signaling. In practice, a trade-off between the size of the switch FETs and the series termination resistor must be made to lower the pre-driver loading at the cost of a slightly reduced accuracy of the pull-up/pull-down branch resistance.

An inherent advantage of the SST concept is its capability to support many different dc termination voltages at the receiver input. An example of three different receiver terminations is given in Fig. 1. In all three cases, the signal swing is half of the supply voltage if the branch impedances of the line-driver output stage are impedance-matched to the transmission line impedance.

The SST topology of Fig. 1 operates at the full-bit-rate clock. As will be shown in Section IV in the discussion of the high-swing SST transmitter design implemented, a half-bit-rate design can be obtained by enhancing the switch transistors with two stacked FETs in each of the pull-up/pull-down branches, where the first FET is driven by the half-bit-rate clock and the second FET is driven by the data. This implements a 2:1 multiplexer within the series termination of the transmitter.

III. IMPEDANCE TUNING AND EQUALIZATION

To account for process variations in the line-driver stage or deviations from the nominal transmission line impedance, the transmitter output impedance is made tunable. Fig. 2 shows the two basic concepts of how this can be accomplished.

In Fig. 2(a), a digitally controlled set of binary-weighted FETs is series-connected to the top and the bottom of the actual line-driver stage. The equivalent resistance of these impedance-tuning FETs is used to adjust the line-driver impedance to the desired value [3]. The impedance tuning by series-stacked FET banks (a.k.a. footer devices) allows the implementation of relatively small impedance steps around the nominal impedance. The additional FETs, however, limit the voltage headroom available, which must be compensated for by an increased width of the switch transistors, if the same ratio of FET on-resistance and series-termination resistance is to be maintained.
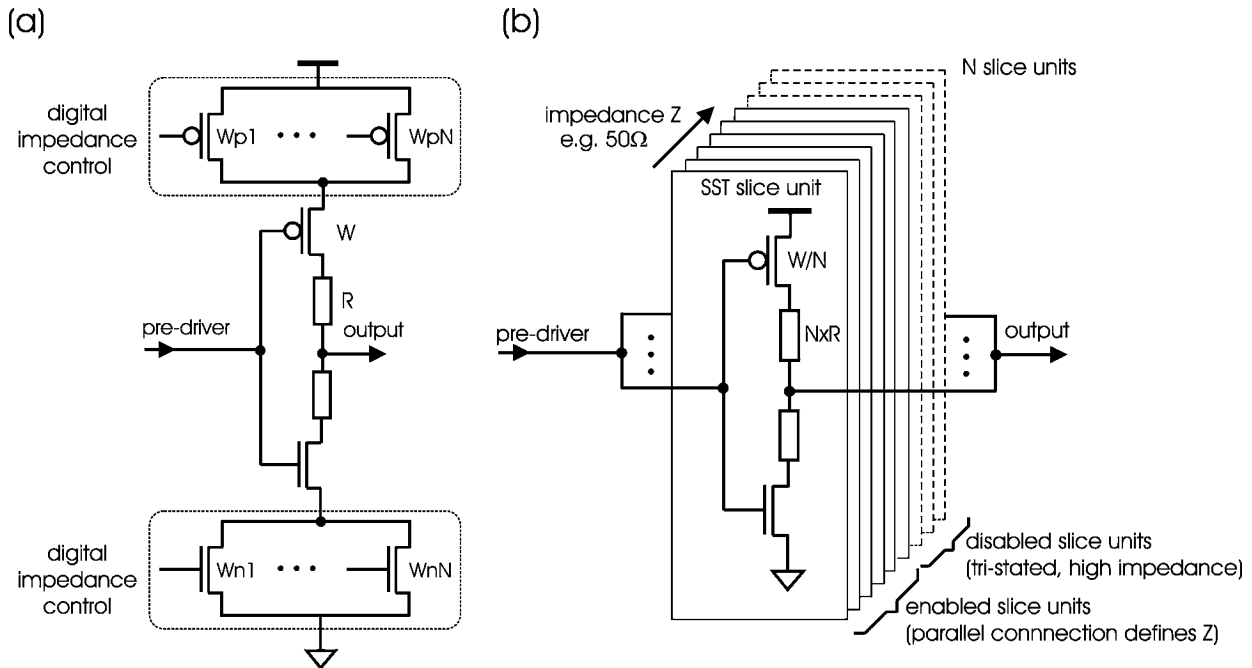
Fig. 2. Impedance tuning concepts: (a) FET impedance tuning banks at top and bottom of SST stage; (b) parallel connection of impedance scaled SST stages.

Another impedance tuning concept that has been implemented in [7] and is also applied to our transmitter is shown in Fig. 2(b). The original line-driver output stage of Fig. 1 is impedance-scaled and N times duplicated such that the parallel connection of all line-driver stages, i.e., the slice units, results in the desired transmission-line impedance. If the resulting impedance is too low, some of the slice units are disabled to increase the impedance to the desired value. This concept has the advantage that the impedance tuning control and the slice units can be kept simple and small. Furthermore there is no voltage headroom penalty if the disablement or tri-stating of the slice units is performed via the data path, which is explained in more detail in [7]. Because the maximum number of slice units must be selected so as to be able to cover the worst-case process variations and deviations in the transmission-line impedance, several slice units may be disabled during nominal operation, which leads to an overhead in silicon area and partially also in pre-driver power. The partitioning of the output stage into slices also allows amplitude margining to be performed, which means that within the enabled output slices, individual slices are configured to statically either pull-up or pull-down. Amplitude margining is beneficial, for example at system start-up to determine appropriate launch levels for the transmit signal. Amplitude margining does not alter the output impedance of the transmitter as the statically operated slice units merely replace the dynamically switched slices, and hence only the signal swing changes but not the impedance.

In addition to providing impedance tuning capability, versatile transmitters are often needed to perform appropriate channel equalization with sufficient resolution in terms of the number of taps and the amplitude step size. The proposed transmitter architecture can independently control impedance tuning and equalization. It is a further development of the SST equalization

concept presented in [7], which did not have this feature. Fig. 3 shows a comparison between two SST equalization schemes [7], [8]. For clarity, the example uses only a 2-tap equalizer with a main tap and one post-cursor tap and 3-bit resolution.

In Fig. 3(a) all N slice units are identical and composed of the basic full-bit-rate SST structure as shown in Fig. 1. Furthermore it is assumed that the nominal transmission-line impedance is obtained by connecting K out of N slice units in parallel. The 2-tap equalization is implemented by assigning I slice units to the main tap and J slice units to the post-cursor tap, where $I + J = K < N$. For instance if $K = 8$ and the channel needs to be equalized for instance with 6 dB, this means that I is 75% of K and J is 25% of K because $-20 \log_{10}((I - J)/K) = -20 \log_{10}((6 - 2)/2^3) \approx 6$ dB. The main tap slice units are driven by the data sequence $d[k]$, whereas the slice units associated to the post-cursor tap are driven by the 1-bit-delayed and inverted data sequence $\overline{d[k - 1]}$. The problem with this topology is that the transmitter impedance cannot be tuned independently of the equalization setting because a change in the number of parallel connected slice units also affects the number of slice units assigned to the main and post-cursor taps. For instance, if K needs to be increased with 4 enabled slice units to meet the new transmission-line impedance, I needs to be increased by 3 and one slice unit must be added to J to maintain the required 6 dB channel equalization. In this example the selected equalization settings cannot be maintained if the increase in K is not a multiple of 4.

This drawback is circumvented with the equalization concept shown in Fig. 3(b). The transmitter topology consists of N identical slice units. Again K slice units connected in parallel are required to obtain the desired transmission-line impedance. In contrast to the preceding equalization concept, the individual slice units are composed of three binary-scaled SST stages
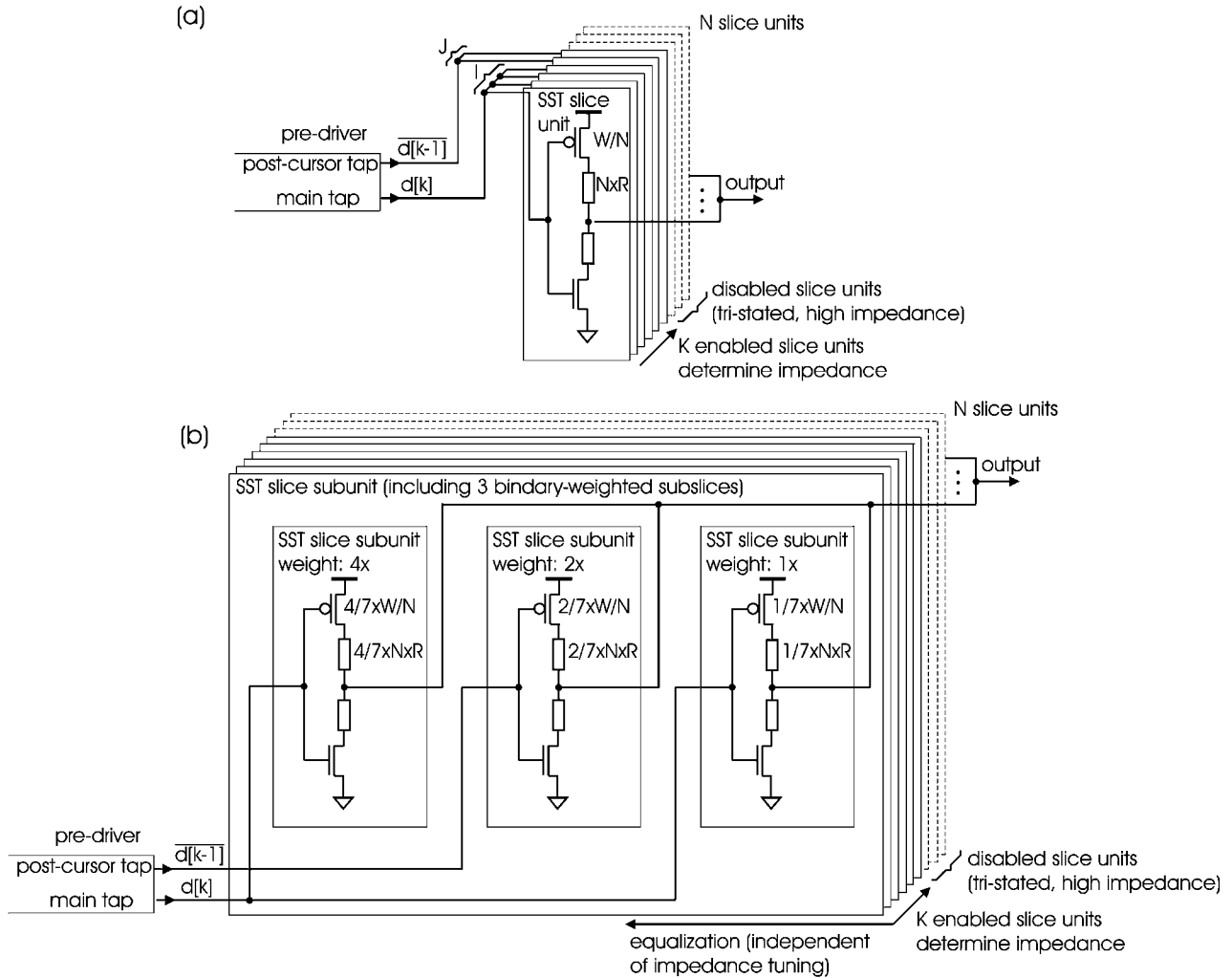
Fig. 3. Equalization concepts: (a) assignment of equalization taps to parallel connected SST slice units [7]; (b) SST slices composed of binary-weighted SST slice subunits to obtain an independent control of equalization and impedance tuning [8].

according to the 3-bit amplitude resolution of the equalization, which results in a amplitude step size of $V_{pp}/(2^3 - 1)$, where V_{pp} denotes the voltage swing. If for example the largest and the smallest weights are assigned to the main tap and the middle weight is driven by the post-cursor, an equalization of $-20 \cdot \log_{10}((5 - 2)/7) \approx 7.4$ dB results. The advantage of this topology is that the selected equalization setting is maintained independently of what the actual number of K is. Hence the control of the impedance tuning and the equalization are mutually decoupled, which significantly simplifies the control logic of the SST transmitter.

IV. TRANSMITTER ARCHITECTURE

A high-level schematic of the high-swing half-bit-rate SST transmitter implemented is shown in Fig. 4. It consists of a thin-oxide pre-driver operated at 1.0 V followed by 22 thick-oxide output stages connected in parallel, which operate at the half-bit-rate clock from a 1.5 V supply. The thin-oxide devices have a drawn gate length of 50 nm, and the thick-oxide devices are 100 nm long. The pre-driver includes the clock path and implements the multiplexing of the four parallel quarter-rate data

to the FIR-filtered differential half-bit-rate even and odd data streams, which are globally distributed together with the differential half-bit-rate clock to the 22 output slices. Because of the 2-tap equalization with 5-bit resolution, a total of 2×5 differential data streams are provided by the pre-driver. In the following two subsections the thin-oxide pre-driver and the thick-oxide output stages including the level shifters are discussed in more detail.

A. Thin-Oxide Pre-Driver

Fig. 5 shows a detailed schematic of the pre-driver. It is assumed that the transmitter receives a CML half-bit-rate clock. In the clock path first a source-degenerated and replica-biased CML buffer stage is employed to perform duty-cycle restoration, which is especially important for the operation of this half-bit-rate architecture as discussed in [7]. A more detailed schematic of the clock path is shown in Fig. 6. The capacitive source degeneration leads to a zero in the buffer transfer characteristic [9] and results, together with the two poles, in a bandpass characteristic. This in turn suppresses the signal's dc component and avoids a direct translation of the dc offset voltage mismatch of the individual differential input signals
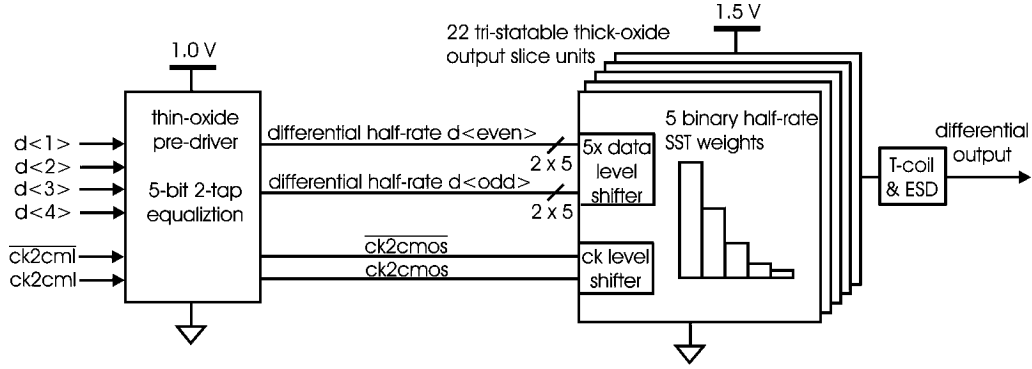
Fig. 4. High-level schematic of high-swing half-bit-rate clock SST transmitter.
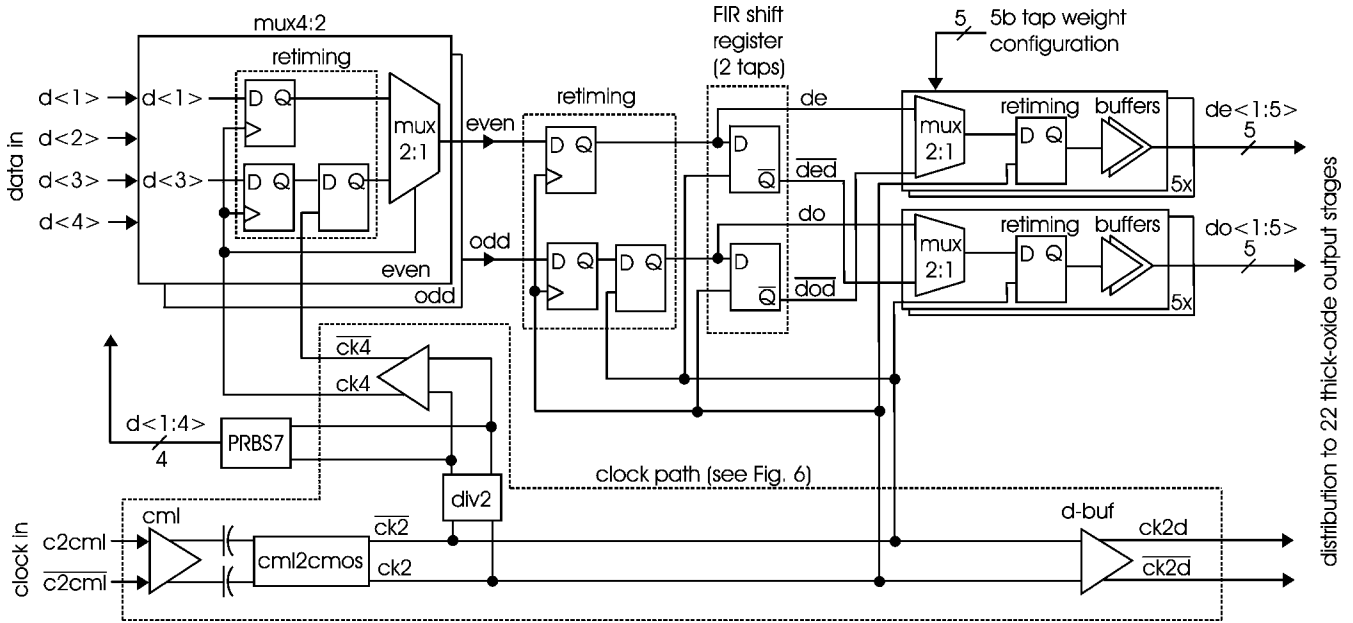

Fig. 5. Pre-driver of high-swing SST transmitter.

into duty-cycle distortion. The zero and pole locations can be approximated by

$$s_z = \frac{1}{R_{0,N1} \cdot C_s} \tag{1}$$

$$s_{p1/p2} \approx \frac{1}{2 R_L C_L} \left(1 \pm \sqrt{1 - 4 \frac{R_L C_L}{R_{0,N2} C_s}} \right) \tag{2}$$

where $R_{0,N1}$ is the output resistance of the current source $N1$, $R_{0,N2}$ is the output resistance of the switch $N2$, R_L is the load resistance, C_L is the load capacitance and C_s is the source degeneration capacitance.

The amplified and duty-cycle-restored half-bit-rate CML clock signal is then converted into a CMOS clock by a CML-to-CMOS converter consisting of an ac-coupled inverter with resistive feedback to operate the inverter at its trip point. The differential CMOS clock $\mathrm{ck2}/\overline{\mathrm{ck2}}$ is further buffered for distribution to the parallel connected output stages. In addition, the outputs of the CML-to-CMOS converter are fed to a divide-by-2 stage and subsequent buffers to generate the differential quarter rate clock $\mathrm{ck4}/\overline{\mathrm{ck4}}$. One of the divider

outputs serves as clock signal for the on-chip PRBS-7 generator that provides the 4-bit quarter rate data for the input of the transmitter.

As is seen from Fig. 5, first the data $d < 1 : 4 >$ are retimed to the quarter rate clock $\mathrm{ck4}$ with a retiming flip flop in the data path of $d\langle 1 \rangle$ and $d\langle 2 \rangle$. The retiming of $d\langle 3 \rangle$ and $d\langle 4 \rangle$ is done with a flip flop followed by a latch clocked with $\overline{\mathrm{ck4}}$. A 4:2 multiplexer implemented as two parallel connected 2:1 multiplexers clocked with $\mathrm{ck4}$ generates an even and an odd data stream out of the 4-bit input. A timing diagram example in Fig. 9 illustrates the operation of the individual transmitter components. The signal labels $s1$ through $s4$ illustrate the multiplexing operation. To keep the timing diagram simple, the retiming-related time shift of $d\langle 2 \rangle$ and $d\langle 4 \rangle$ is not explicitly drawn, and hence $s2$ and $s4$ are aligned to $s1$ and $s3$.

The even and odd data streams at the output of the 4:2 multiplexer are first retimed to the half-bit-rate clock $\mathrm{ck2}$ before they are fed to the subsequent FIR shift register. Because this transmitter has a 2-tap equalization scheme, the FIR shift register consists of only two latches. The latch clocked with $\overline{\mathrm{ck2}}$ outputs the inverted even signal $\overline{\mathrm{ded}}$ with a delay of half of the $\mathrm{ck2}$
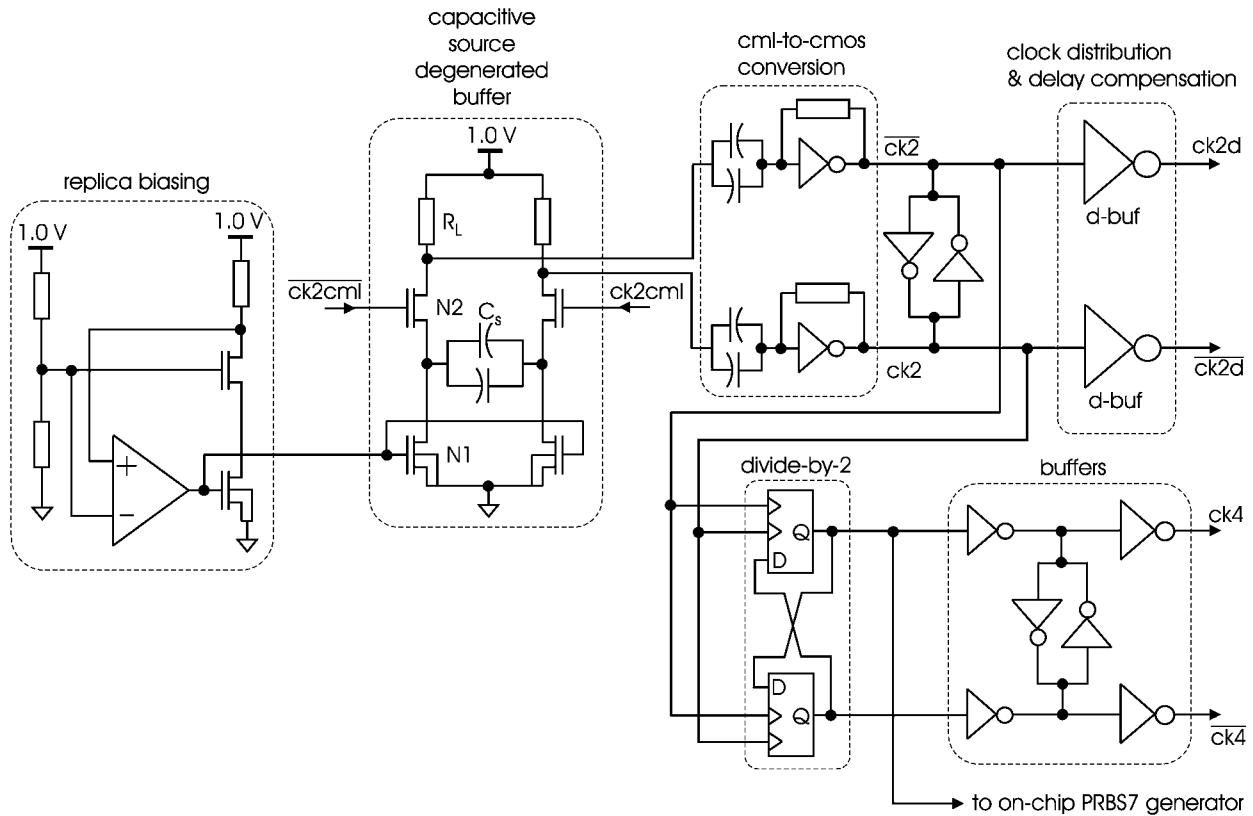
Fig. 6.   Clock path in thin-oxide part of high-swing SST transmitter.

period with respect to the even data de. The other latch is clocked with ck2 and outputs the inverted and delayed odd data $\overline{dod}$. The signals $\overline{ded}$ and $\overline{dod}$ represent the post cursor, whereas de and do are the main tap components of the half-bit-rate even and odd data streams. In Fig. 9 examples of the signals de, do, $\overline{ded}$ and $\overline{dod}$ are shown. The last letter 'd' in $\overline{ded}$ designates the delay of half a clock cycle with respect to the signal de. The same notation also applies to other delayed data and clock signals.

As shown in Fig. 3(b) an independent control of impedance tuning and equalization can be achieved by enhancing the SST output slices with binary-weighted subslices. In our architecture five binary-weighted subslices are implemented to achieve a 5-bit output resolution of the equalization. Hence 2×5 2:1 multiplexers operated in parallel are used after the FIR shift register to switch either the main tap signal or the post-cursor data to the corresponding binary-weighted subslices located further down the data path in the thick-oxide transmitter part. Because of the half-bit-rate operation, the main tap even signal de is multiplexed with the post-cursor odd signal $\overline{dod}$ in one of the two 2:1 multiplexers and similarly do and $\overline{ded}$ are multiplexed in the other 2:1 mux. The operation of the 2:1 multiplexers also ensures that the main and post-cursor taps are always complementary to each other as the post-cursor weights are implicitly deduced from the sum of the binary-weighted main-tap weights. This complementary tap-weight assignment significantly simplifies the de-emphasis control.

Each of the 2×5 2:1 multiplexers is followed by a retiming latch, whose output is buffered and distributed to the subsequent 22 thick-oxide output stages. To keep the design sym-

metrical and achieve short signal paths ($\sim$150 μm), 11 output stages are located on each side of the pre-driver (see Fig. 16). Even more important than the single-ended data routing is the distribution of the differential half-bit-rate clock to minimize duty-cycle distortion. The last buffer labeled d-buf in the clock path of the pre-driver has to fulfill two tasks. First it provides sufficient buffering to distribute the differential clock signal to the 22 output stages. Second its delay matches the delay in the data distribution so that no retiming must be performed in front of the final multiplexing stages in the thick-oxide output stages. This delay compensation saves power with respect to a local retiming in all of the 22 output stages. However, it comes at the cost of limiting the maximum data rate because the inserted delay does not scale with the data rate, whereas in a retiming stage, delay differences between clock and data can be better eliminated at very high data rates.

B. Thick-Oxide Output Stages and Level Shifters

Fig. 7 shows the schematic of the thick-oxide output stages. There are in total 22 tri-statable SST output slices, each consisting of 5 binary-weighted SST stages with 2×5 data level shifters and one clock level shifter per slice. The distributed half-bit-rate clock and data signals are first level-shifted from the 1.0 V power supply domain of the thin-oxide pre-driver to the 1.5 V domain of the thick-oxide output stages.

Fig. 8 shows the schematic of the differential level shifter used in the clock and data path. In the data path, the level shifters are scaled according to the binary weights they have to drive. In addition a single-ended to differential conversion of the data
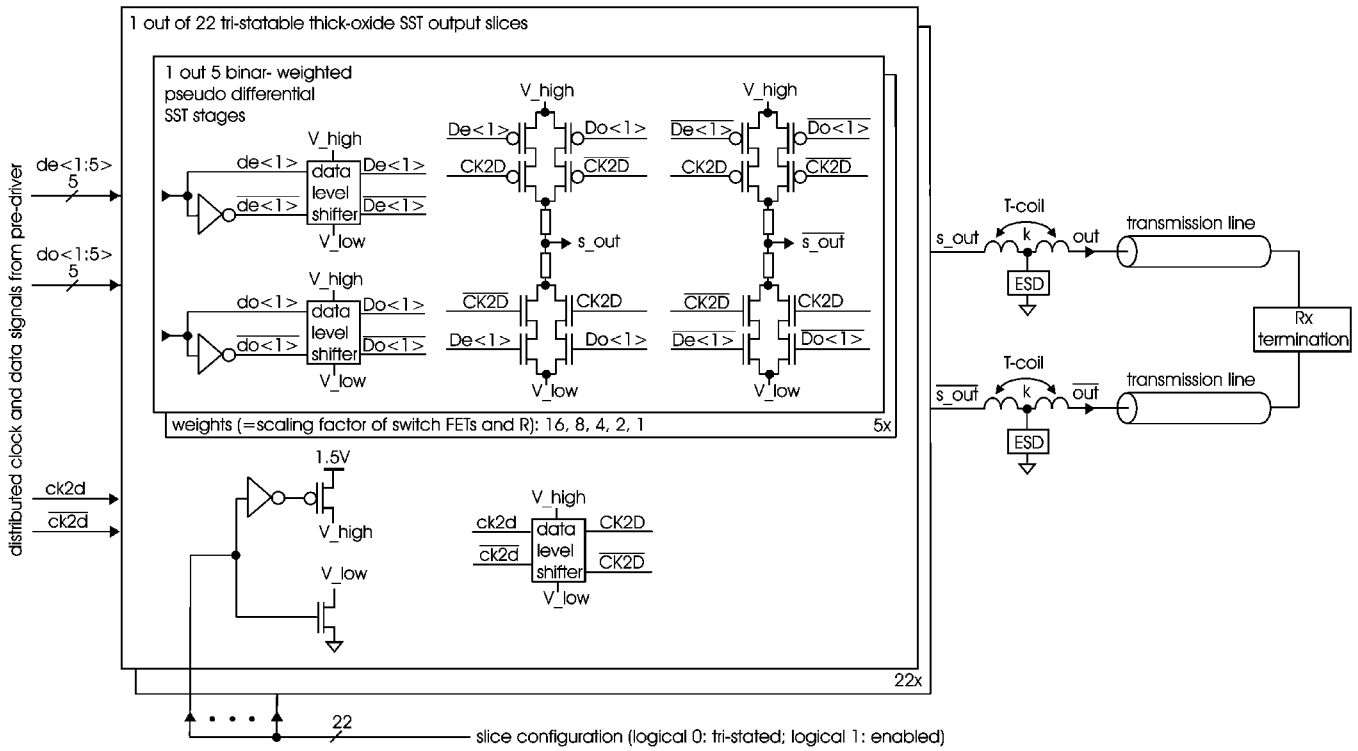
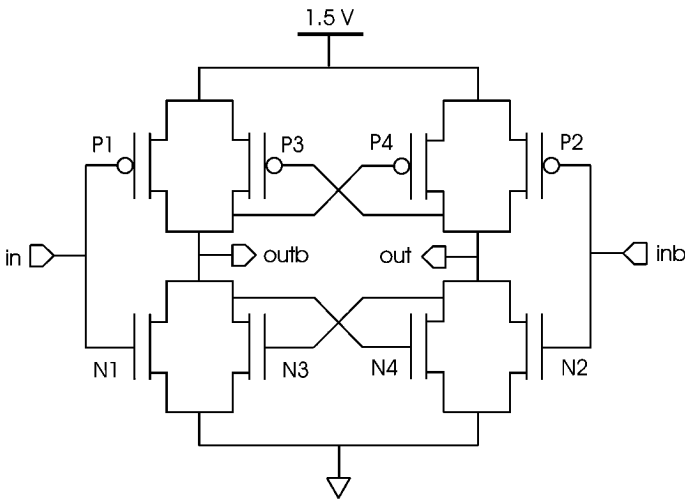Fig. 7. Schematic of thick-oxide half-bit-rate output stages.

Fig. 8. Level shifter consisting of thick-oxide FETs to perform a 1.0 V to 1.5 V conversion of the clock and data signals.

signal is performed by means of an inverter in front of each data level shifter, as is shown in Fig. 7. The actual level-shifting from 1.0 to 1.5 V is performed by the cross-coupled PMOS transistors P3 and P4 in Fig. 8. To appropriately convert the trip point of the input signal to the corresponding higher level at the output, P3 and P4 have to be dimensioned smaller than the cross-coupled NMOS transistors N3 and N4. This however reduces the capability of P3 and P4 to raise the output at a low-to-high transition sufficiently fast. To solve this inherent problem of level-shifting, inverter-like structures consisting of the devices P1, N1 and P2, N2 are connected in parallel to the cross-coupled transistors. These additional circuits constitute a feed-forward path with respect to the feedback-path-like cross-coupled

FETs and thus help pre-bias the outputs such that the cross-coupled PMOS transistors can switch faster despite their smaller size. The threshold voltage of P1 and P2 must be higher than the amount of voltage level-shifting because otherwise leakage currents will flow when the input is at a logical high.

The level-shifted differential half-bit-rate clock $CK2D, \overline{CK2D}$ and the differential half-bit-rate even data $De\langle 1 \rangle, \overline{De\langle 1 \rangle}$ and odd data $Do\langle 1 \rangle, \overline{Do\langle 1 \rangle}$ are fed to two pseudo-differential SST drivers. As can be seen from Fig. 7, each of these pseudo-differential SST drivers consists of a pull-up and pull-down branch with one pair of stacked FETs and one series termination resistor per branch. The pairs of stacked FETs implement the final 2:1 multiplexer to generate the full-bit-rate differential output signals. A key feature of this output multiplexer is its perfect symmetry with respect to PMOS/NMOS slew rate mismatches as the clock and data signals always have to drive identical pairs of PMOS and NMOS FETs. Examples of an output signal without de-emphasis (0 dB) and with 6.3 dB de-emphasis are shown in Fig. 9. The signal labels $s7$ and $s8$ illustrate how the 2:1 multiplexing is performed based on the distributed even and odd data streams de, $\overline{ded}$, do and $\overline{dod}$. The assignment of these signals to the individual tap weights is not explicitly shown in Fig. 9. In the 6.3 dB de-emphasis case, the main tap signals de and do would be assigned to tap weights 16, 4, 2, 1 of Fig. 7 and the post cursor signals $\overline{ded}$ and $\overline{dod}$ would be fed to tap weight 8, which results in a de-emphasis of $-20 \log_{10}((23 - 8)/31) \approx 6.3$ dB.

V. ESD PROTECTION AND T-COIL IMPEDANCE MATCHING

The SST-driver output stages are protected against ESD events by means of silicon-controlled rectifiers (SCR). They
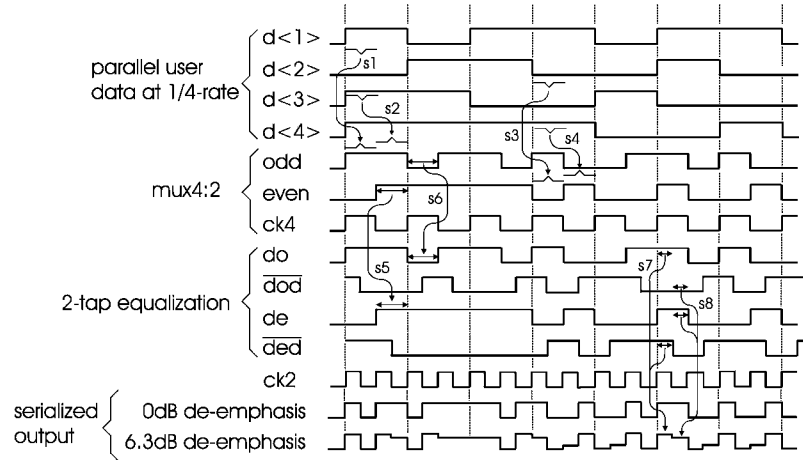
Fig. 9. Signaling example of serialization and de-emphasis in transmitter.

TABLE I
T-COIL MODELING PARAMETERS

Parameters: $L_b = 360$ pH, $L_b = 240$ pH, $k = 0.4$, $M = 118$ pH, $C_b = 15$ fF, $C_t = 600$ fF, $C_p = 70$ fF, $R_{Tx} = R_{Rx} = 50\ \Omega$			
$D(s) = C_b(L_a + L_b + 2M) \cdot s^2 + C_b(R_a + R_b) \cdot s + 1$			
$v_1 = C_b(R_a + R_b)$	$v_2 = R_a R_b C_b C_e + C_b(L_a + L_b + 2M) - MC_e$	$v_3 = C_b C_e(L_a R_b + L_b R_a)$	$v_4 = C_b C_e(L_a L_b - M^2)$
$u_1 = C_e$	$u_2 = C_b C_e(R_a + R_b)$	$u_3 = C_b C_e(L_a + L_b + 2M)$	

are suitable devices for this application because of their low holding voltage, low on-resistance and the relatively low parasitic capacitance. Because we aimed at providing a standard ESD compliance of 2 kV human-body model, a relatively large SCR was required ($\sim 300\ \mu$m total perimeter). To handle negative ESD events an N+ P-well diode of the same size was connected in parallel. To reduce the junction capacitance of the SCR during normal operation, the N-well at gate G2 is tied to VDD via a high-ohmic resistor of 17 kΩ in our design (see Fig. 11). Still, the parasitic capacitance C_e of the combined SCR and diode during operation is ~ 300 fF. Thus the total output capacitance of the SST driver is the sum of the parasitics of the output stages (~ 600 fF), above ESD capacitance and the pad capacitance (~ 70 fF), and amounts to ~ 1 pF. Typical transmitter return loss specifications require $|S11| < -8$ dB at the frequency corresponding to half of the maximum data-rate (e.g., HT3, [10]). Consequently a load capacitance of ~ 1 pF limits transmitter operation to below 5 Gb/s, as is illustrated in Fig. 12(a). To improve the transmitter return loss and enable operation at higher data rates, the differential output signals of the SST driver are connected to two T-coils. Using T-coils for broadband impedance-matching ESD-protection devices was also proposed in [11]. The basic design equations and an analytical discussion of the (symmetric) T-coil can be found in [11]–[14].

The T-coil consists of two coupled inductors with the ESD protection devices connected to the center tap (Fig. 10(a)). Its equivalent circuit is shown in Fig. 10(b). The bridging capacitance C_b required to obtain the broadband compensation is in our case not a dedicated component but is implicitly accounted

for with the parasitic fringing capacitance between the turns of the T-coil. Representative for the many parallel connected SST slices, only one half-bit-rate SST subslice is shown in Fig. 10(a), which is replaced in the equivalent circuit of Fig. 10(b) with the termination resistor R_{Tx} in parallel to the parasitic capacitance C_t. The capacitance C_t at the output stage is mainly due to the parasitic sheet capacitance of the polysilicon resistors in the pull-up/pull-down branches but includes also wiring parasitics. The mutual inductance M is a function of the coupling coefficient k:

$$M = k \cdot \sqrt{L_a \cdot L_b}, \qquad (3)$$

where L_a, L_b denote the self-inductances of the two inductor branches. In Fig. 10(b)–(d), the SCR and ESD diode are also replaced by their common parasitic capacitance C_e. Furthermore, in Fig. 10(b)–(d) the pad parasitic capacitance C_p is included together with the line impedance R_{Rx}. Because our SST transmitter was only on-wafer-tested, packaging effects are not accounted for.

To obtain an analytical expression for the transmitter output return loss, the T-coil is transformed to a network without inductive coupling in Fig. 10(c), [12], [13]. A further simplification is obtained by applying a π-to-T conversion to the encircled network in Fig. 10(c), which results in the circuit of Fig. 10(d). Now the output impedance $Z_{Tx,out}$ can be derived. First the output impedance Z'_{Txout} without pad parasitics C_p is determined:

$$Z'_{Tx,out} = \frac{Z_T \cdot Z_3 + Z_1 \cdot Z_3 + Z_1 \cdot Z_2 + Z_2 \cdot Z_3 + Z_2 \cdot Z_T}{Z_1 + Z_3 + Z_T}$$
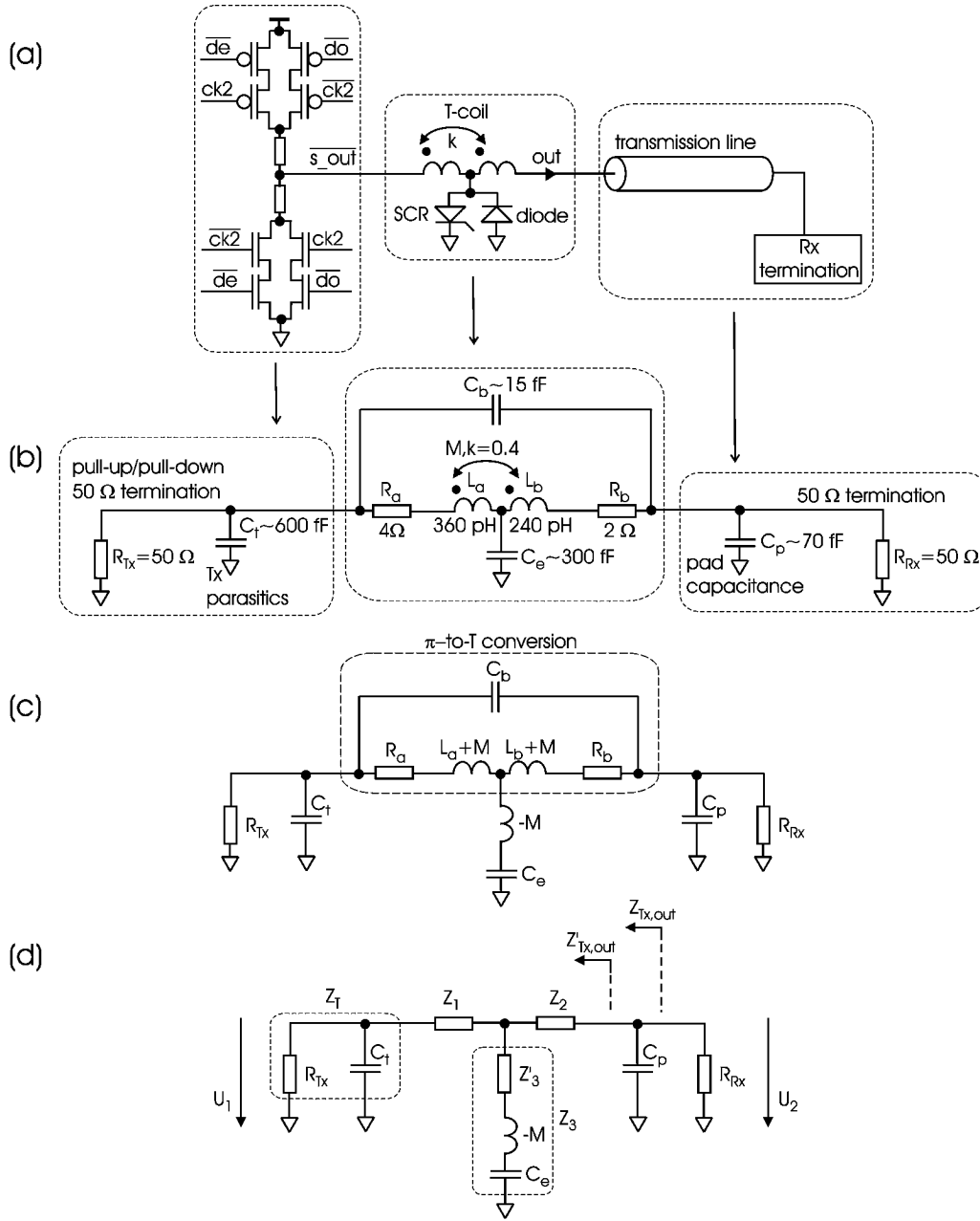
$$(4)$$

Fig. 10. Application of a T-coil at the transmitter output and different small-signal-equivalent circuits used to perform the analytical analysis of the asymmetric T-coil.

where

$$Z_1 = \frac{(L_a + M) \cdot s + R_a}{D(s)} \quad (5)$$

$$Z_2 = \frac{(L_b + M) \cdot s + R_b}{D(s)} \quad (6)$$

$$Z_3 = \frac{v_4 s^4 + v_3 s^3 + v_2 s^2 + v_1 s + 1}{u_3 s^3 + u_2 s^2 + u_1 s} \quad (7)$$

$$Z_T = \frac{R_{\text{Tx}}}{1 + s R_{\text{Tx}} C_T}. \quad (8)$$

The coefficients in the expressions of Z_1, Z_2 and Z_3 are defined in Table I. Taking C_{p} into account, the output impedance of the SST transmitter can be written as

$$Z_{\text{Tx,out}} = \frac{Z'_{\text{Tx,out}}}{1 + s C_p Z'_{\text{Tx,out}}}. \quad (9)$$

The output reflection factor is defined as

$$r = \frac{Z_{\text{Tx,out}} - 50\,\Omega}{Z_{\text{Tx,out}} + 50\,\Omega} \quad (10)$$

and the return loss is given by

$$|S_{11}| = 20 \cdot \log_{10}(|r|). \quad (11)$$

With (3)–(11) the return loss of the T-coil-compensated SST transmitter can be computed and is shown in Fig. 22 for comparison with measurements. The simulated return loss curve also
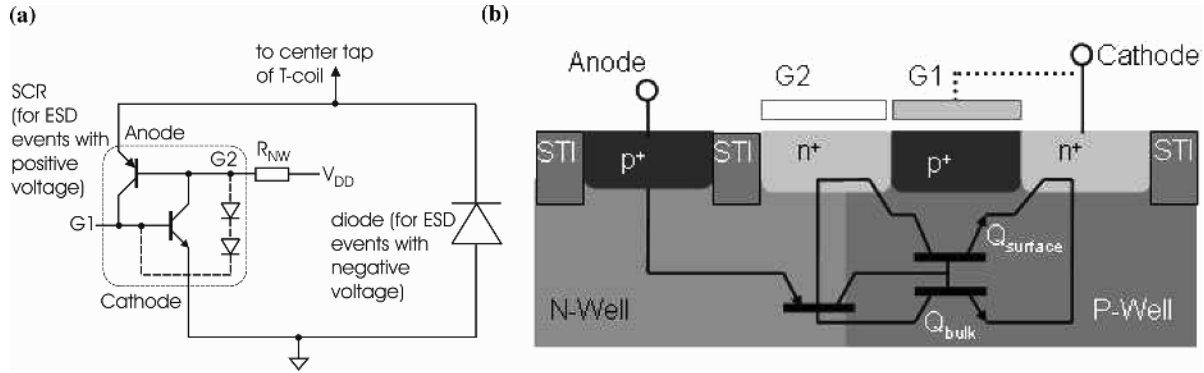
Fig. 11. (a) SCR-equivalent circuit and ESD diode, (b) SCR cross section with parasitic bulk-NPN transistor (ESD diode not shown); STI = shallow trench isolation.
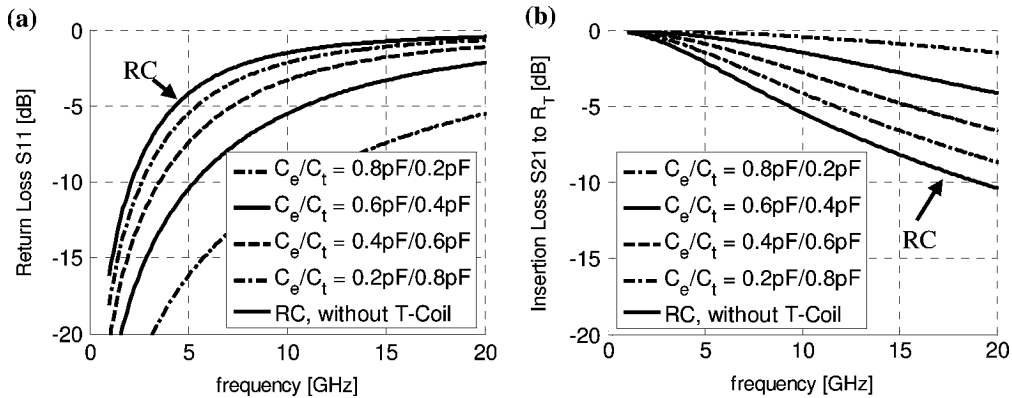

Fig. 12. (a) Return loss degradation and (b) insertion loss degradation for a compensated I/O circuit using a perfect, symmetrical bridged T-coil but with a varying capacitance distribution between C_e and C_t.

includes inductive wiring parasitics within the distributed SST slices (not shown in Fig. 10 for clarity). The SST transmitter presented has a relatively large parasitic output capacitance C_t with respect to the ESD capacitance C_e, thus using symmetric T-coils yields unsatisfactory return-loss improvements as is apparent from Fig. 12(a). Fig. 12(a) depicts the results from an analysis that has been performed-based on the lumped element equivalent circuit of Fig. 10(b)—on how much asymmetry a symmetric T-coil can tolerate with respect to C_t. It shows that the return loss $|S_{11}|$ degrades as the ratio C_e/C_t becomes smaller. With an asymmetric T-coil instead, much better return loss values can be achieved, as will be explained below when we discuss the measurements. However, the simple design equations from [12], [14] for the symmetrical T-coils are no longer applicable, and numerical methods must be applied. For the asymmetric T-coil, L_a increases with increasing C_t. However, the more asymmetric the T-coil is, the smaller L_b becomes. With L_b converging to zero, a simple π-circuit remains, where the sum of $C_p + C_e$ is separated from C_t by a simple inductor L_a. As L_b is the coil branch that must be laid out to carry the high ESD currents, these typically small values of L_b facilitate a compact T-coil layout.

The T-coil design has been verified with a 3D full-wave electromagnetic field solver (ANSOFT HFSS) from which s-parameters have been exported to be included in the transistor-level simulations of the driver. Fig. 13 shows the simulated 3-D model, which is approximately 40 μm × 40 μm and exploits the top five metal layers of the available metal stack to obtain a low

series resistance and a compact size. In general, a low series resistance is desired as otherwise the MOSFET to polysilicon resistor ratio degrades, which is undesirable for the reasons discussed in Section II. Moreover a minimum inductor trace width is required to meet electromigration design rules, and particularly L_b has to be dimensioned appropriately to carry the high ESD currents. The T-coil resistance is approximately 6 Ω and the series termination resistors in the SST slices are reduced accordingly. Because of the large spacing required between metal patches on the top metal layer (i.e., DRC rules), only a single turn is implemented on this layer. To further reduce the series resistance, the two bottom 2x-thick metals are connected in parallel. By employing a helical rather than a flat wiring scheme for the T-coil (Fig. 13(a)), the effect of the parasitic fringing capacitance between the layers (i.e., vertically) can be reduced, which improves the T-coil self-resonance frequency.

As mentioned above, our SST transmitter was designed for on-wafer measurements because no packaged chips were available. So that we can nevertheless evaluate how a package would impact the return and insertion loss performance, the model of the T-coil and SST output stages shown in Fig. 10(b) is applied to measured scattering parameters of a FCPBGA package with 16 mm package conductor length and 3 mm board microstrip. The simulation results are shown in Fig. 14. With respect to the return loss performance, the application of the T-coil results in a significant improvement towards lower frequencies (<6 GHz), whereas at higher frequencies the lossy package predominates.
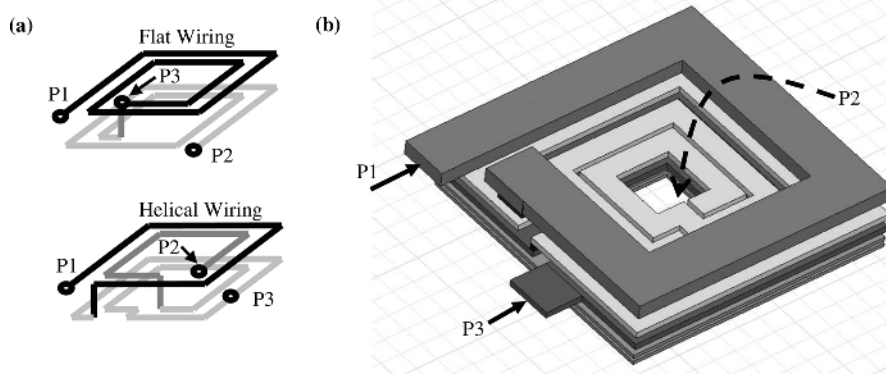
Fig. 13. (a) Different coil wiring schemes and (b) 3D model for full-wave EM simulation.
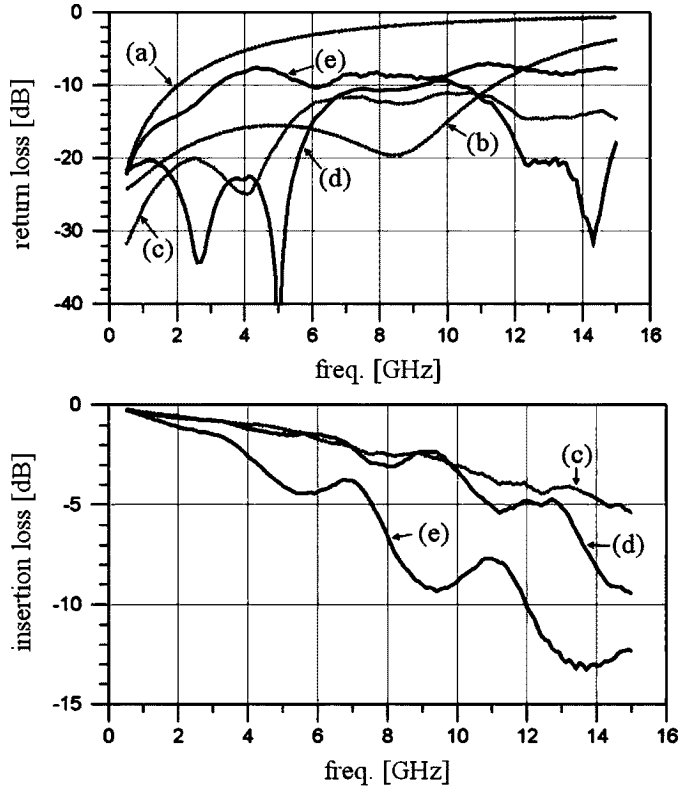

Fig. 14. Return and insertion loss: (a) Tx without T-coil; (b) Tx with T-coil; (c) package only; (d) package attached to Tx with T-coil, (e) package attached to Tx without T-coil.

In terms of insertion loss, the transmitter with T-coil achieves a better performance over the entire frequency range.

VI. EXPERIMENTAL RESULTS

Test chips with 2-channel transmitters and different T-coil and ESD configurations at the output were fabricated. The die micrograph of a 2-channel transmitter test chip is depicted in Figs. 15 and 16 shows the layout of a single transmitter. Fig. 17 shows the measured output impedance versus the number of enabled SST slice units, with a static data pattern applied to the transmitter input. The required 50 Ω impedance is obtained with 18 enabled slice units out of 22. In Fig. 18, a 10-bit long section of a PRBS-7 sequence at 5.2 Gb/s is shown, where all
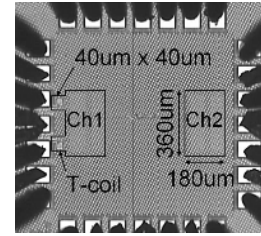

Fig. 15. Die micrograph of a two-channel SST transmitter test chip, in which the left transmitter has a T-coil and SCR ESD protection at the output, whereas the right transmitter has neither.
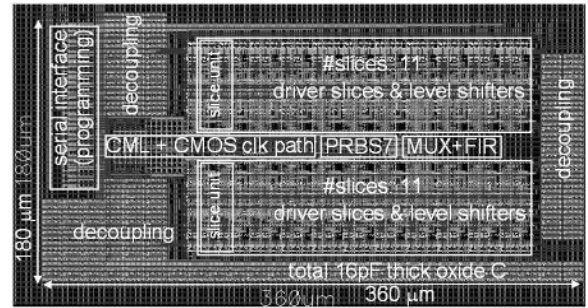

Fig. 16. Layout of high-swing SST transmitter (1 channel without ESD and T-coil).

16 de-emphasis settings are overlaid on the oscilloscope screen. The de-emphasis values are given by

$$de-emphasis[dB] = 20 \cdot \log_{10}\left(\frac{2^5 - 1 - 2 \cdot i}{2^5 - 1}\right) \quad (12)$$

with $i = 0, \ldots, 15$, and result in a single-ended amplitude step size of approximately 24.2 mV at a supply voltage of 1.5 V.

Fig. 19 shows a typical eye diagram with -1.9 dB de-emphasis applied to a 7.5 Gb/s PRBS-7 signal and measured over a measuring section with 1.8 dB channel loss (probes, cables) plus a 3 dB attenuator used as overvoltage protection at the input of the oscilloscope. The total jitter at a bit-error rate (BER) of 10^{-12} is 16.6 ps; 80% thereof is deterministic jitter mainly due to ISI and the random jitter is about 1.8 mUIrms. The required eye opening greater than 1.0 V is specified at the transmitter output ports, and hence the measured eye height of approximately 625 mV must be de-embedded at a data rate of 7.5 Gb/s
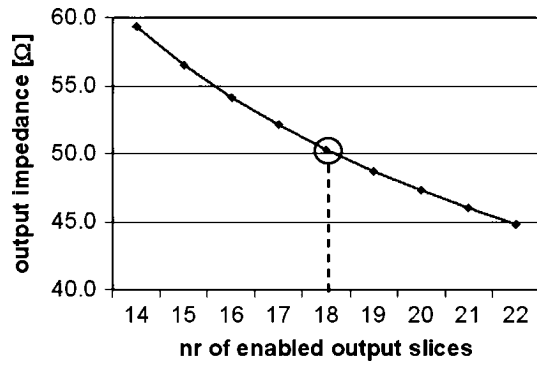
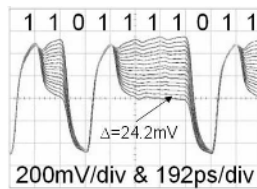Fig. 17.   Output impedance versus number of enabled SST slice units.

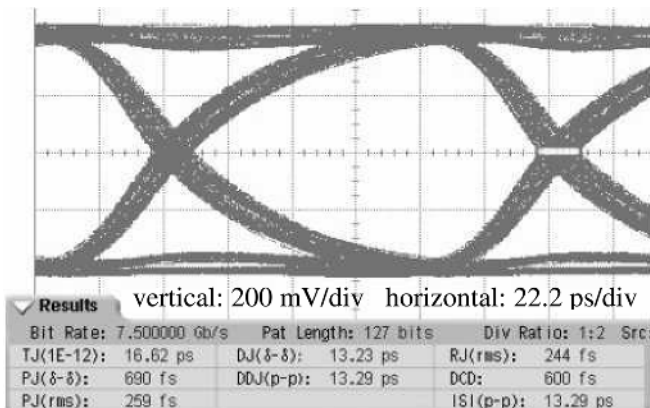Fig. 18.   Overlay of 16 de-emphasis settings at 5.2 Gb/s.

Fig. 19.   Differential eye diagram at 7.5 Gb/s with -1.9 dB de-emphasis measured over a measuring section with 1.8 dB channel loss (probes, 3.5 m long cable) and a 3 dB attenuator at the input of the oscilloscope.
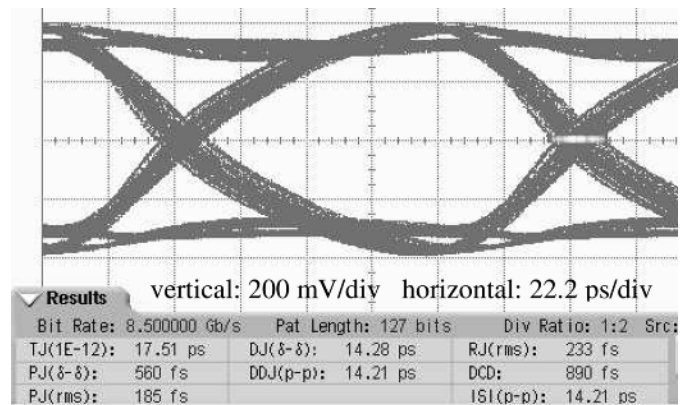

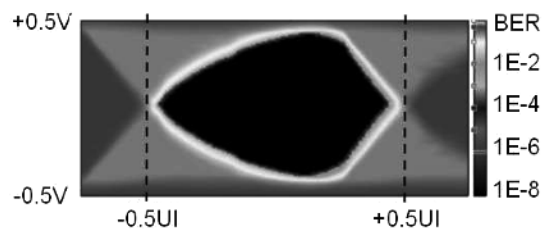Fig. 20.   Differential eye diagram at 8.5 Gb/s with -2.6 dB de-emphasis.

Fig. 21.   Eye diagram at 6.0 Gb/s measured with a BERT.

be expressed as $\mathrm{S11[dB]} = 20\log_{10}(|-j\omega C_{\mathrm{tot}}50\ \Omega/(2 + j\omega C_{\mathrm{tot}}50\ \Omega)|)$. By fitting the curve to the response of a lumped element equivalent circuit, $C_t = 600$ fF and $C_p = 70$ fF can be extracted (see Fig. 10(a)). Curve (b) was measured on an uncompensated ESD-protected SST transmitter (i.e., SCR but no T-coil). The additional parasitic capacitance of the ESD-protection devices deteriorates the return loss performance. Again, by curve-fitting, the equivalent parasitic capacitance of the SCR was extracted to be $\sim$300 fF. Curve (c) was measured on a T-coil compensated ESD-protected SST transmitter. Because of the T-coils, a wideband output impedance matching is achieved with a return loss below 16 dB at up to 10 GHz. These experimental results clearly demonstrate the high potential of T-coils to improve the return loss performance of transmitters.

Furthermore, for comparison with our 65 nm bulk CMOS design, the return loss curve of a previously designed regular swing SST transmitter in 65 nm SOI CMOS [7] is shown in Fig. 22, curve (d). The SOI CMOS transmitter has 44 half-bit-rate SST slice units and a total parasitic output capacitance of $\sim$760 fF, including pad, wiring and ESD protection. Although the SOI CMOS design has larger ESD structures, its return loss is much better than that of the bulk design (curve (b)). This better return loss can be explained by the much lower parasitic capacitances of the polysilicon resistors in SOI CMOS technology. Consequently, SST transmitters with a large number of slice units should preferably be implemented in SOI CMOS rather than in bulk CMOS.

In the preceding section, it has been stated that the asymmetric T-coil may result in a better return loss performance than is achievable with a symmetric T-coil. A quantitative statement can be made when comparing the graphs of Figs. 12(a) and 22 at 10 GHz. Under the load conditions typical for our design (i.e., $\sim$300 fF at the center tap and $\sim$700 fF at the termination tap),

with a multiplication factor of $10^{4.8\ \mathrm{dB}/20}$, which results in an effective differential eye opening of 1.1 V. An example of an eye diagram at 8.5 Gb/s, where the de-embedded eye height crosses the 1.0 V limit, is shown in Fig. 20. It is measured over the same measuring section with a slight over-equalization. Fig. 21 depicts the eye diagram obtained with a BER tester (BERT) under the same measurement conditions but at 6.0 Gb/s. This two-dimensional BER scan has been performed with a confidence level of 90% [15], which limits the minimum achievable BER value to $\sim$10^{-9} but shortens the required test time to approximately 32 h for this BERT eye diagram.

Fig. 22 compares the measured return loss curves of different transmitter output configurations. In curve (a) the transmitter output has no ESD protection and no T-coil. Its return loss is dominated by the parasitic capacitances of the SST slice units and to a smaller extent by the pad parasitics. If these two parasitic capacitances are combined to C_{tot} and the transmitter's dc output impedance is adjusted to 50 Ω, the return loss can
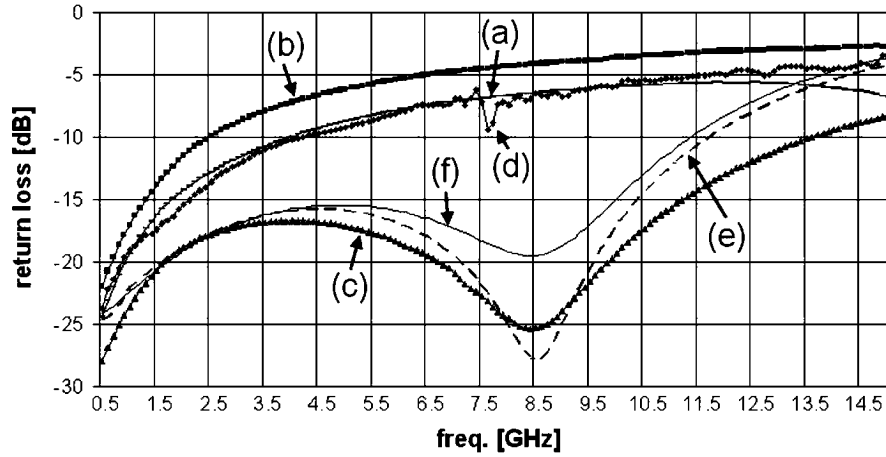
Fig. 22. Measured return loss curves: (a) without ESD and without T-coil; (b) with SCR used as ESD, but no T-coil; (c) with SCR and asymmetric T-coil; (d) SOI CMOS SST transmitter [7] with ESD. Simulated return loss curves: (e): HFSS EM model; (f) mathematical model.
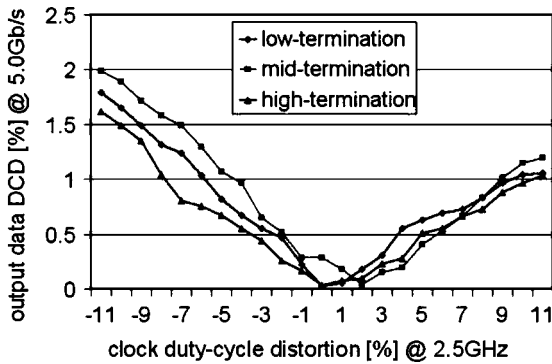

Fig. 23. Measured improvement of duty-cycle distortion because of the application of source-degenerated buffering in clock path. The duty cycle restoration capability corresponds to a factor of 5.

Fig. 24. Measured and de-embedded differential eye height (a) without de-emphasis and (b) with -3.4 dB de-emphasis; (c) total power consumption of (d) thick-oxide output stages and (e) thin-oxide pre-driver and clock path.

the symmetric T-coil of Fig. 12(a) yields $|S_{11}| > -4$ dB (take the value between the two curves of $C_e/C_t = 0.2/0.8$ pF and $0.4/0.6$ pF) whereas with the asymmetric T-coil (see Fig. 22) a return loss better than -15 dB or an improvement of >10 dB at 10 GHz is achieved.

Fig. 23 shows the measured output-versus-clock duty-cycle distortion (DCD). The measured output DCD at all termination voltages remains below 2% peak-to-peak at an input DCD of $\pm10\%$. Owing to the fully differential clock path with a capacitive source-degenerated buffer as first stage (see Fig. 6), a duty-cycle distortion restoration capability of $5x$ is achieved. In Fig. 24 the de-embedded eye height and the power consumption versus data rate are depicted. The differential eye height at the output pins is greater than 1.0 V at up to 8.5 Gb/s. The power consumption changes linearly with data rate and amounts to 96 mW at 8.5 Gb/s.

Table II shows additional measurement results. An inherent drawback of CMOS clocking is the higher power supply sensitivity compared with, for example, a CML design. To counteract this drawback either a power supply regulator needs to be used or the clock path has to be kept as short as possible such that limited power supply noise, which is directly transferred into jitter, can still be tolerated. Motivated by the good results of [7], the design presented here pursues the strategy of limiting the clock
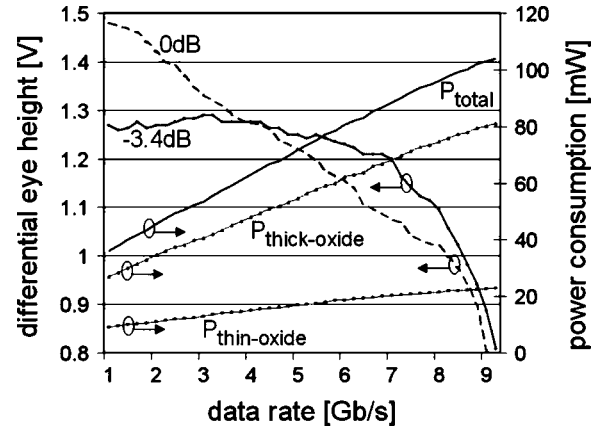
TABLE II
MISCELLANEOUS MEASUREMENTS

DC supply sensitivity:			
Thick-oxide part of transmitter at VTT = 1.5 V: $S = -1.13$ ps/100 mV			
Thin-oxide part of transmitter at VDD = 1.0 V: $S = -6.84$ ps/100 mV			
Cross-talk on neighbor channel at 7.5 Gb/s with 16 pF on-chip decoupling			
bit pattern	RJ [ps]	DJ [ps]	ISI [ps]
0000	0.34	12.33	10.82
1010	0.35	12.47	10.64
PRBS-7	0.34	15.73	14.06
Common-mode voltage noise:			
High termination ($V_{cm} = 0.75 \times$VTT): 4.99 mV rms			
Mid termination ($V_{cm} = 0.5 \times$VTT): 6.39 mV rms			
Low termination ($V_{cm} = 0.25 \times$VTT): 9.09 mV rms			

path length and does not use power supply regulation. When adding the two supply sensitivities specified in Table II, it turns out that, e.g., at 8.5 Gb/s the power supply noise induced jitter is about 70 mUI pk-to-pk. To reduce this value, a power supply

TABLE III
PERFORMANCE SUMMARY OF SST TRANSMITTER AND COMPARISON WITH PREVIOUS WORK

Reference	Technology	Max. data rate [Gb/s]	Differential eye height [Vpp]	Efficiency [mW/Gb/s]	Return loss [dB] at $f_0/2$
[21]	0.11 µm CMOS	20	0.2	12.6[2)]	-
[20]	65 nm CMOS	15	0.16	2.3[2)]	-
[19]	0.13 µm CMOS	6.4	0.35	15.6[2)]	-10
[18]	0.13 µm CMOS	8	0.65	20.5[2)]	-10
[17]	90 nm CMOS	10	0.9	17.4[2)]	-
[16]	90 nm CMOS	10	1.0	7[2)]	-
[5]	90 nm CMOS	6.4	0.125	0.8[1)]	-12
[6]	0.18 µm CMOS	3.6	0.25	2.7[1)]	-
[7]	65 nm SOI CMOS	16	0.5	3.6[1)]	-7
This work	65 nm bulk CMOS	8.5	1.0	11.3[1)]	-16

1) SST-like transmitter, 2) CML-like transmitter

regulator would be required. The dc supply sensitivity measurements were carried out by first measuring the total jitter (TJ) at $\mathrm{BER} = 10^{-12}$ with an Agilent Infiniium DCA-J 86100 oscilloscope under nominal dc supply conditions ($\mathrm{VDD} = 1.0$ V, $\mathrm{VTT} = 1.5$ V). Next the jitter measurements were repeated with different supply voltage settings (e.g., $\mathrm{VDD} = 0.9$ V, $\mathrm{VTT} = 1.5$ V). Based on these measurements, the dc sensitivities specified here are defined as the ratio of the TJ-difference to the voltage step applied (e.g., $S = \Delta\mathrm{TJ}/\Delta\mathrm{VDD}$). Note that the sensitivity values have a negative sign because the TJ values decrease with increasing supply voltages. This kind of dc supply sensitivity measurements based on statically varying the dc supply voltages instead of applying a real power supply noise source can only be performed because no supply voltage regulator is used in the transmitter and the latency in the clock path, which is most relevant for the induced jitter, is directly dependent on the actual supply voltage.

Table II also shows some cross-talk measurements that reveal a 33% increase of ISI-related jitter when both channels operate with PRBS-7 data. The on-chip power supply decoupling used in these measurements is 16 pF and results in a cut-off frequency of ~640 MHz. The final measurement in Table II is related to the common-mode voltage noise, which remains below 10 mV rms for all three termination voltages. The performance summary of this SST transmitter and a comparison with previous work are given in Table III.

VII. CONCLUSION

In this paper, a high-swing SST transmitter implemented in 65 nm bulk CMOS technology has been proposed. Inner eye openings greater than 1.0 V at up to 8.5 Gb/s have been demonstrated. This was made possible by combining a thin-oxide pre-driver stage running at 1.0 V dc supply and subsequent thick-oxide SST output stages operating in parallel from a 1.5 V supply. The clock and data signal conversion between the two power supply domains is performed with dc-coupled level shifters. To relax the timing constraints in the pre-driver stage, a half-bit-rate design of the thick-oxide output stages is employed, where the final 2:1 multiplexing is done at the transmitter output within the pull-up and pull-down branches. The tuning of the output impedance is achieved by tri-stating some of the parallel connected SST slice units. To decouple the impedance tuning from the equalization, every slice unit comprises a complete set of binary-weighted SST weights. The

half-bit-rate SST transmitter implements a 2-tap de-emphasis scheme with 5 bit amplitude resolution whose adaptation is independent of the impedance tuning control. A capacitive source-degenerated buffer is used to restore the duty cycle of the input clock signal.

Outstanding return loss results are achieved by applying impedance-matching T-coils at the outputs of the transmitter. The T-coil cancels the parasitic capacitance of the ESD-protection devices and separates the parasitic capacitances of the SST output stages from the actual output port of the transmitter over a wide frequency range. Silicon-controlled rectifiers are used as ESD-protection devices. In combination with the T-coils, this high-swing half-bit-rate SST transmitter proves to be suitable in supporting multi-standard I/Os because of the large range of supported termination voltages, the relatively large eye opening and the excellent output impedance match.

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