A T-type Switched-Capacitor Multilevel Inverter with Low Voltage Stress and Self-Balancing

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***Abstract*- This paper proposes a novel T-type multilevel inverter (MLI) based on the switched-capacitor technique. The proposed inverter not only achieves that the maximum voltage stress of the switches is less than the input voltage but also has a voltage boost capability, which makes it suitable in high voltage applications. It is worth mentioning that the proposed inverter features two topology extension schemes which help it achieve a higher output level and voltage gain. With the merit of low voltage stress and reduced power devices, a seven-level inverter can be achieved using only two capacitors. Moreover, capacitor voltage self-balancing capability can simplify the complexity of the circuit and control. The topology, operating principle, modulation strategy and analysis of the capacitor of the inverter are presented. The superiorities of the proposed inverter are investigated by comparing with recently proposed hybrid MLIs and switched-capacitor MLIs. Finally, a seven-level prototype is constructed to validate the correctness of the theoretical analysis and the feasibility and effectiveness of the proposed inverter. [1]**

***Index Terms*—Multilevel inverter, switched-capacitor, low voltage stress, self-balancing, extension.**

NOMENCLATURE

A_c	Amplitude of the triangular carriers
f_c	Frequency of the triangular carriers
A_{ref}	Amplitude of the sinusoidal modulation wave
f_o	Frequency of the sinusoidal modulation wave
V_o	Output voltage
V_{dc}	Voltage of dc source
V_s	Voltage stress of the switch
C_i	Capacitor number i
C_s	Parasitic capacitance of the switch
ΔV_{C2}	Voltage ripple of C_2
V_{C2}	The voltage of C_2
ΔQ_1	Discharge amount of C_2 during the period of 0-t_1
ΔQ_2	Discharge amount of C_2 during the period of t_2-t_3
ΔQ_{C2}	The maximum discharge amount of C_2
Q_u	The discharge amount of the capacitor when it works at $V_{dc}/2$
Q_m	The maximum discharge amount of the capacitor
K	The factor of the maximum acceptable voltage ripple
P_{rip}	Ripple losses
P_{con}	Conduction losses
P_{sw}	Switching losses
P_o	Output power
N	Output levels
x	Number of the connected inverters
n	Number of the extended H-bridges
y	Number of the switches
N_s	Switching transitions in one period
M	Fundamental wave modulation index
R_o	Load resistance
ESR_C	Equivalent series resistance of each capacitor
r_s	Equivalent resistance of the switch
f_s	Switching frequency of the switches
I_o	Output current
r_{eq}	Equivalent parasitic resistance
η	Efficiency of the nine-level inverter
t_s	Working time of the switches in one period
T_s	Time of one cycle
t_i	Intersection time instant of the ith sine and triangle waves
m	Step number of half-cycle
TSV	Total standing voltage
THD	Total harmonic distortion

This work was supported in part by the National Natural Science Foundation of China under Grant 51507155, and in part by the Youth Key Teacher Project of Henan Higher Educational Institutions under Grant 2019GGJS011. (*Corresponding author: Gen Li.*)

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I. INTRODUCTION

Multilevel inverters (MLIs) play an important role in power electronics systems thanks to their excellent features in high power capacity, low switching voltage stress, low harmonics, modular and scalable design [1]-[5].

The development of MLIs can be traced back to the late 1960s [6]. Traditional MLIs can be divided into three types: neutral point clamp (NPC), flying capacitor (FC) and cascade H-bridge (CHB). These inverters have a wide range of applications due to the advantages of low voltage stress, low switching frequency and capability for high voltage applications [7]-[9].

1) Motivation and incitement

Based on the three types of inverters, numerous new inverters have been designed and proposed to enhance their performance in the past decades. To achieve a higher output level and improve extensibility, the topology combines the NPC and FC is one of the attractive alternatives to [10]-[12]. The CHB inverter has also been modified to reduce the number of switching devices [13]. These improvements enrich the variety

of MLIs. They have a common advantage of limiting the voltage stress of all semiconductor devices to the dc input voltage. However, these inverters do not have voltage boosting capability. In addition, the capacitor voltage balance is still a challenge for NPC inverters [14]. The existence of flying capacitors requires additional complex control circuits [15]. CHB circuits require multiple independent power sources [16]. These shortcomings limit their widespread applications. The inverters in [17] and [18] use different switch combinations to connect multiple dc power sources in series to supply the load and output multiple voltage levels. Different dc voltage ratios can be achieved, which increases their flexibility. However, the MVS of their switches is at least the voltage of two dc sources. Moreover, they do not have voltage boosting capability and have only one topology extension scheme.

The switched-capacitor technique provides a good way to solve the above-mentioned shortcomings. There is no additional complicated control circuit in the switched-capacitor multilevel inverters (SCMLIs) [19]. They are able to boost small input dc voltages to high ac voltages by switching the pre-charged capacitors in series [20]-[21]. Such inverters also benefit from their small size, light weight, large power density and low harmonic components.

2) Literature review

Various SCMLIs have been proposed in the open literature. The SCMLIs presented in [22]-[25] can maintain the balance of capacitor voltages. In addition, they are featured that only one dc power source is employed with the capability of voltage boosting. However, using H-bridges to achieve the voltage polarity conversion will limit their application because the H-bridge increases the maximum voltage stress (MVS) of the switches and also, increases the capital cost.

The H-bridge has been removed in [26]-[29] without affecting the voltage polarity conversion. However, there are still switches need to withstand the peak value of the output voltage, which may also limit their applications in high voltage systems. The topology proposed in [30] reduces the MVS of switches, however, the MVS of switches is still twice the dc source voltage. The topologies proposed in [31]-[32] can effectively reduce the voltage stress of the switches. However, a large number of switches and independent power sources are required by the ones in [31] and [32], respectively. In [33]-[36], the proposed inverters limit the MVS of switches to the input power voltage utilizing proper devices. However, more improvement can be made to use fewer capacitors in the topologies proposed in [33]-[35].

3) Contribution and paper organization.

To overcome the shortcomings of the above-mentioned inverters in terms of using numerous devices, high MVS of switches, and lacking voltage boosting and capacitor voltage self-balancing, an MLI based on the switched-capacitor technique has been proposed in this paper. Comparing with conventional MLIs, the proposed inverter can boost the input power voltage and realize capacitor voltage self-balancing. Moreover, the MVS of inverter switches is limited to less than the input power voltage. The components used in the proposed MLI are reduced compared to low voltage stress SCMLIs. In addition, the proposed inverter is also superior in its flexible extensibility and capability of supplying inductive loads. The low voltage stress is one of the excellent features that made the proposed inverter an attractive alternative for medium- and high-voltage photovoltaic power generation applications.

The rest of the paper is organized as: the circuit configuration and operation principles of the proposed inverter and analysis of capacitors are described in Section II. Section III gives an analysis of power losses and efficiency. The topology extension and comparison analysis are presented in Section IV. In Section V, the feasibility and effectiveness of the proposed MLI have been validated through experiment. Section VI draws the conclusion and closes the paper.

II. Proposed Multilevel Inverter

A. Circuit Configuration

The topologies proposed in [33]-[36] are shown in Fig. 1. The common feature of them is that they only use one dc power source, two T-type voltage-dividing capacitors to achieve a seven-level inverter. The two T-type capacitors are used to generate a voltage level of $V_{dc}/2$, making the step voltage of the output waveforms have a smaller value than V_{dc}, which can effectively reduce the total harmonic distortion (THD) of the output voltage. However, the two T-type capacitors are not fully utilized because they are only used for voltage division and cannot be connected in series with the dc power source to supply the load. Therefore, these topologies require additional capacitors to achieve multilevel outputs.

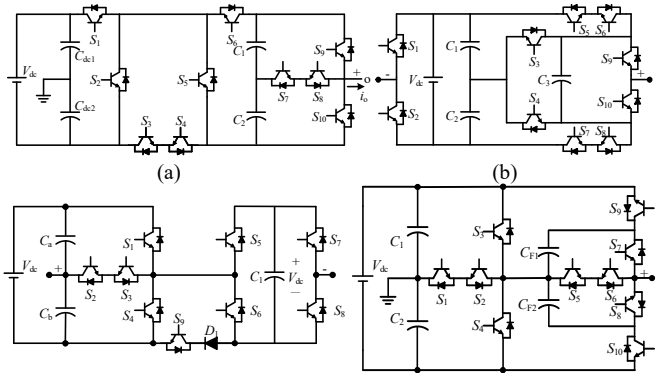


Fig. 1. Topologies proposed in [33]-[36]. (a) Topology in [33]; (b) Topology in [34]; (c) Topology in [35]; (d) Topology in [36].

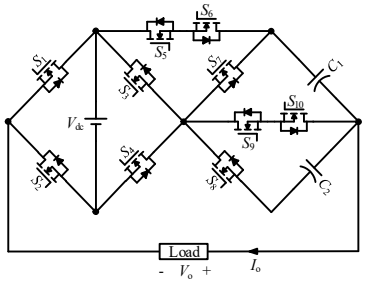


Fig. 2. The topology of the proposed seven-level inverter.

In order to reduce the number of capacitors and thereby maximize the utilization of the two T-type capacitors, a new T-type switched-capacitor inverter has been proposed in this

paper, as shown in Fig. 2. In this topology, the two capacitors are not only employed to generate the voltage level of $V_{dc}/2$, but also act as the switched capacitors, which eliminates the need for additional capacitors. In addition, the proposed topology can be regarded as a reconstruction of the topology proposed in [35]. The dc source and two T-type voltage-dividing capacitors are integrated to reduce the additional switched capacitor. Comparing to the topology in [35], the front-to-front connected switches S_5 and S_6 are needed to achieve a bidirectional current path. However, the proposed topology, in turn, reduces one capacitor at the expense of adding one switch. It is worth mentioning that the topology proposed in [35] has the potential to further reduce the number of capacitors. For instance, the two T-type voltage-dividing capacitors could be replaced by two split dc sources. In this case, only one capacitor is needed to achieve a seven-level output. Similar changes can be made in [33], [34] and [36]. However, the use of multiple dc sources may limit the applications of such designs. This is because that one important driving force of using the switched capacitor technique for multilevel inverters is to reduce the use of independent dc sources.

In the proposed inverter, the dc power source (e.g. photovoltaic panels, batteries, and fuel cells) supplies the capacitors and load. The switched-capacitor structure guarantees the boost capacity and enables a voltage boost gain of 1.5. With the help of the H-bridge, the two capacitors can operate alternately to achieve the voltage polarity conversion on the load. In this case, the H-bridge used for changing the voltage polarity in conventional SCMLIs can be removed. This feature leads to a remarkable decrease of the MVS of switches. The proposed inverter can a seven-level output: $\pm 3V_{dc}/2$, $\pm V_{dc}$, $\pm V_{dc}/2$ and 0.

B. Operating Principle

This section describes the operating principle of the seven-level inverter. Different output levels are obtained by controlling the on and off states of each switch. All operating states under different modes are shown in Table I. It is noted that 0 and 1 refer to the off and on states of the related switches. The states of the capacitors are shown by "C", "D" and "—", which indicate the charging, discharging and rest states.

TABLE I
SWITCHING AND CAPACITORS STATES AT DIFFERENT OUTPUT LEVELS

V_o	Switches	Capacitors	
	$S_1S_2S_3S_4S_5S_6S_7S_8S_9S_{10}$	C_1	C_2
$3V_{dc}/2$	0110000100	—	D
V_{dc}	0110000011	—	—
$V_{dc}/2$	0101100100	C	D
0	0101000011	—	—
$-V_{dc}/2$	1001110000	D	C
$-V_{dc}$	1001000011	—	—
$-3V_{dc}/2$	1001001000	D	—

The current paths in each operating mode are shown in Fig. 3. It is noted here, the two operating modes with the output voltage of $\pm V_{dc}/2$ contain two current paths. One path is that the capacitor supplies the load. The other is that the power source charges the capacitors in series. It can be seen from Fig. 3 that the load current can flow reversely under each operating mode and the reversed current path is the same as the forward current path. It proves that the proposed inverter has the capacity of supplying inductive loads.

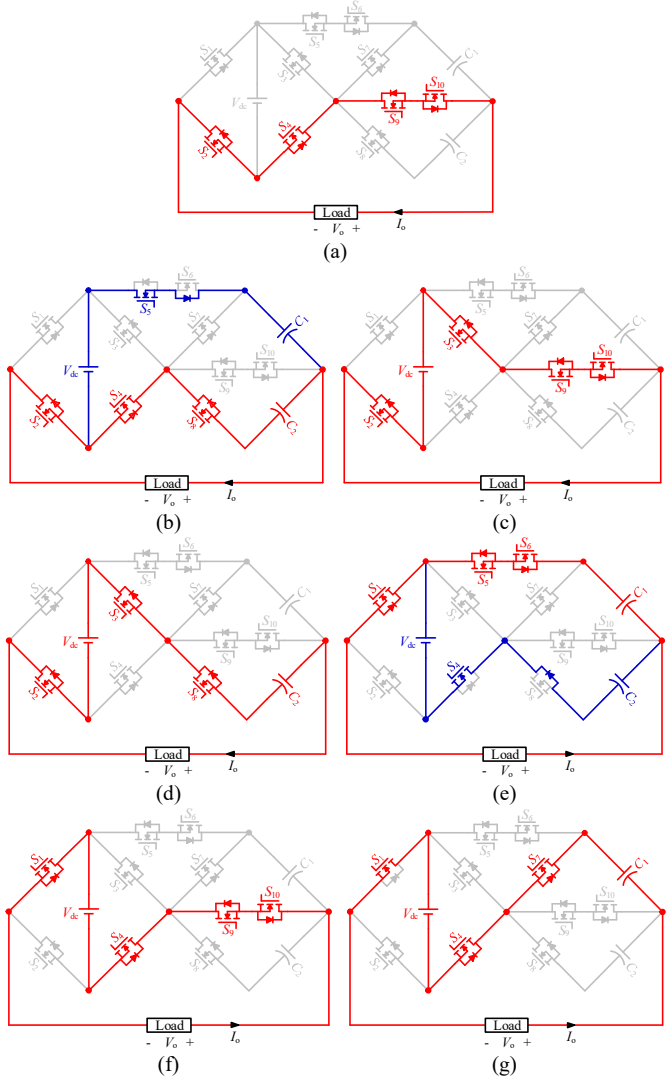


Fig. 3. Operation modes. (a) 0. (b) $V_{dc}/2$. (c) V_{dc}. (d) $3V_{dc}/2$. (e) $-V_{dc}/2$. (f) $-V_{dc}$. (g) $-3V_{dc}/2$.

C. Modulation Strategy

The pulse width modulation (PWM) is mainly divided into three types: carrier wave PWM, selective harmonic eliminated PWM (SHE-PWM) and the space-vector PWM (SV-PWM) [37]-[38]. The SHE-PWM can reduce the switching frequency, thereby reducing the switching losses, and improving the utilization of the dc voltage. However, it is complicated to implement. The SV-PWM method is suitable for inverters which output three to five voltage levels. However, it is not suitable for inverters output more than five voltage levels due to its complexity. In this paper, the phase disposition PWM (PD-PWM), which is one type of carrier wave PWMs, is

adopted to generate the driving signals for all switches. The advantage of this method is that it is easy to implement, thereby greatly reducing the complexity of the control circuit. For a seven-level inverter, six triangular carriers and a sinusoidal modulation wave are required to generate pulses. Different logical combinations of these pulses control the on and off states of each switch. The schematic diagram of the PD-PWM is shown in Fig. 4. The six triangular carriers have the same amplitude (A_c) and frequency (f_c) but different offsets. The amplitude of the sinusoidal modulation wave is A_{ref} and the frequency is f_o. The modulation index is determined by the amplitude of the carrier and reference waveforms. Hence, the modulation index M can be defined as

$$M = \frac{A_{ref}}{3A_c}. \quad (1)$$

The proposed inverter is able to adjust its output accordingly when M changes. The relationship between different values of M and the output level is shown in Table II.

TABLE II
THE RELATIONSHIP BETWEEN OUTPUT LEVEL AND M

M	Output level
$0 < M \le 1/3$	3
$1/3 < M \le 2/3$	5
$2/3 < M \le 1$	7

D. Analysis of Capacitor Balancing

As shown in Table I, C_1 is charged when the output voltage is $V_{dc}/2$ and discharged when the output voltage is $-V_{dc}/2$ and $-3V_{dc}/2$. C_2 is charged when the output voltage is $-V_{dc}/2$ and discharged when the output voltage is $V_{dc}/2$ and $3V_{dc}/2$. It can be seen from Fig. 4, the working states of the two capacitors are symmetrical in one cycle. C_2 works in the positive half-cycle, then the voltage will drop and the voltage of C_1 rises. This is because the two capacitors are connected in series with the dc power source when they are charged. C_1 works in the negative half-cycle, then the voltage will drop and the voltage of C_2 rises. The voltages of two capacitors can return to the initial state after a cycle deviating from the set voltage. Hence, the voltages of the two capacitors are self-balanced which is one of the features of this inverter.

E. Analysis of the Capacitors

The capacitors in SCMLIs play an important role in power transmission and conversion. Their voltage ripples should be controlled within a reasonable range. The voltage ripple of capacitors is related to their capacitance, load value and discharging periods. A low voltage ripple can improve the quality of the output voltage, reduce ripple losses and improve the efficiency of inverters. The two capacitors in the proposed seven-level inverter have the same capacitance. The selection of the two capacitors are the same and therefore, only capacitor C_2 is analyzed as follows.

To determine the capacitance of a capacitor, it is necessary to learn its maximum discharge amount. It can be seen from Fig. 4 that C_2 is discharged when the output voltage is $3V_{dc}/2$ and $V_{dc}/2$. Therefore, the maximum discharge amount of C_2 is

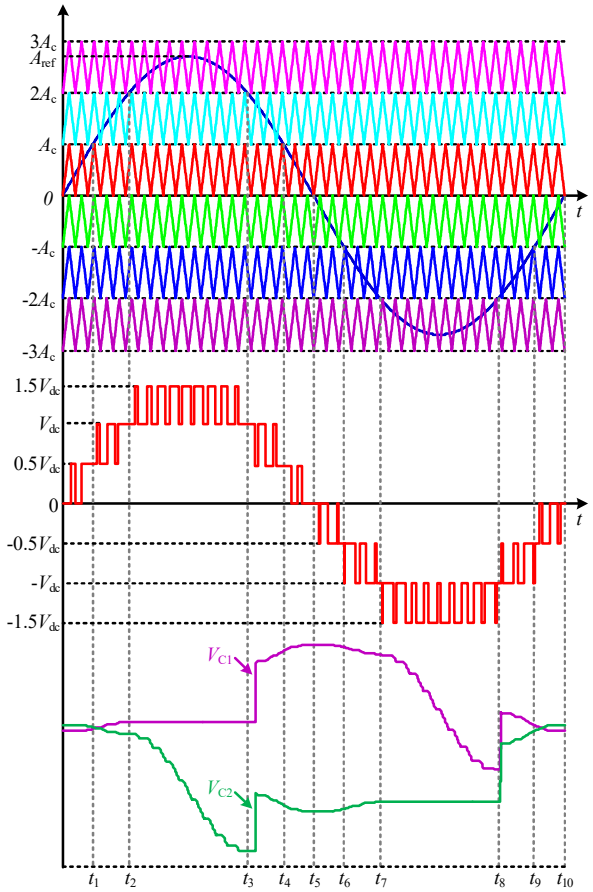


Fig. 4. Schematic diagram of the PD-PWM and the capacitor voltages in one cycle.

the sum of the discharge amount in the three periods of 0-t_1, t_2-t_3 and t_3-t_4.

The instants t_i (i=1,2,3,4,5) are intersection points of the sine and triangle waves, which can be calculated by the following equations:

$$t_1 = \frac{\arcsin\left(\frac{1}{3M}\right)}{2\pi f_o}, \quad (2)$$

$$t_2 = \frac{\arcsin\left(\frac{2}{3M}\right)}{2\pi f_o}, \quad (3)$$

$$t_3 = \frac{\pi - \arcsin\left(\frac{2}{3M}\right)}{2\pi f_o}, \quad (4)$$

$$t_4 = \frac{\pi - \arcsin\left(\frac{1}{3M}\right)}{2\pi f_o}, \quad (5)$$

$$t_5 = \frac{\pi}{2\pi f_o}. \quad (6)$$

In (2)-(6), M is the modulation index (M=0.9 is used in this study) and f_o is output frequency. The discharge amount of the capacitor during the period from 0 to t_1 can be calculated by:

$$\Delta Q_1 = \int_0^{t_1} I_o \sin(2\pi f_o t) dt \,, \tag{7}$$

where ΔQ_1 is the discharge amount during the period of 0-t_1, I_o is the output current. Using the same calculation method, the discharge amount ΔQ_2 during the period of t_2-t_3 can be obtained as:

$$\Delta Q_2 = \int_{t_2}^{t_3} I_o \sin(2\pi f_o t) dt \,. \tag{8}$$

The variables in (8) are the same as the ones in (7). As the operating status of the capacitor is the same during 0-t_1 and t_4-t_5, the discharge amount during the two periods is the same as well. Therefore, the maximum discharge amount of C_2 is given by:

$$\Delta Q_{C2} = 2\Delta Q_1 + \Delta Q_2 \,. \tag{9}$$

Assuming k is the factor describing the maximum acceptable voltage ripple, the capacitance can be obtained:

$$C_2 \geq \frac{\Delta Q_{C2}}{k V_{C2}} \,, \tag{10}$$

where V_{C2} is the rated voltage of C_2.

Considering the symmetrical characteristics of the working states of C_1 and C_2 in the positive and negative half-cycles, the voltage ripples of the two capacitors are the same. Thus, C_2 is chosen as an example. It can be seen from (9) that the maximum continuous discharge amount of C_2 is ΔQ_{C2}. Therefore, the voltage ripple of C_2 can be given by:

$$\Delta V_{C2} = \frac{\Delta Q_{C2}}{C_2} \,, \tag{11}$$

where ΔV_{C2} is the voltage ripple of C_2. As can be seen from (11), the ripple can be controlled within a reasonable range by setting a proper capacitance.

III. Power Losses Analysis

Three types of losses are considered for the switched-capacitor inverters, which include the ripple losses of capacitors (P_{rip}), conduction losses (P_{con}) and switching losses (P_{sw}).

A. Ripple Losses of Capacitors

P_{rip} is caused by the voltage fluctuation of the capacitors. C_2 is still taken as an example, due to the symmetrical working states of the two capacitors. As shown in (11), the voltage ripple of C_2 is ΔV_{C2}, therefore the P_{rip} can be calculated from:

$$P_{rip} = f_o C_2 \Delta {V_{C2}}^2 \,. \tag{12}$$

A further calculation can be obtained as:

$$P_{rip} = f_o \frac{{\Delta Q_{C2}}^2}{C_2} \,. \tag{13}$$

B. Conduction Losses

The conduction losses of the inverters are caused by the parasitic parameters of devices, such as the on-state resistance of the switches (r_s), and the equivalent series resistance of each capacitor (ESR_C). Fig. 5 shows the equivalent circuit of supplying the load. In Fig. 5, V_o, r_{eq} and R_o are the output voltage, the equivalent parasitic resistance of the devices and the load resistance, respectively.

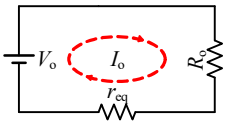


Fig. 5. The equivalent circuit of supplying the load.

The equivalent parameters in the three working modes of the positive half cycle are shown in Table III. The value of j in Table III indicate that the output V_o is i times of $V_{dc}/2$.

TABLE III
THE EQUIVALENT PARAMETERS IN THE THREE WORKING MODES

j	V_o	r_{eq}
0	0	$4r_s$
1	$V_{dc}/2$	ESR_C+3r_s
2	V_{dc}	$4r_s$
3	$3V_{dc}/2$	ESR_C+3r_s

According to Fig. 4, in the interval of [0, t_1], the output level changes between 0 and $V_{dc}/2$. Therefore, the power losses during [0, t_1] can be calculated from:

$$P_{0\&0.5V_{dc}} = \int_0^{t_1} [I_o \sin(2\pi f_o t)]^2 \times [(ERS_C + 3r_s)\frac{A_{ref}\sin(2\pi f_o t)}{A_c} + 4r_s(1 - \frac{A_{ref}\sin(2\pi f_o t)}{A_c})] dt \,. \tag{14}$$

Similarly, the power losses of the other two working modes can be obtained in the same way.

$$P_{0.5V_{dc}\&V_{dc}} = \int_{t_1}^{t_2} [I_o \sin(2\pi f_o t)]^2 \times 4r_s \frac{A_{ref}\sin(2\pi f_o t) - A_c}{A_c} + (ERS_C + 3r_s)(1 - \frac{A_{ref}\sin(2\pi f_o t) - A_c}{A_c})] dt \,. \tag{15}$$

$$P_{V_{dc}\&1.5V_{dc}} = \int_{t_2}^{0.01} [I_o \sin(2\pi f_o t)]^2 \times (ERS_C + 3r_s)\frac{A_{ref}\sin(2\pi f_o t) - 2A_c}{A_c} + 4r_s(1 - \frac{A_{ref}\sin(2\pi f_o t) - 2A_c}{A_c})] dt \,. \tag{16}$$

Therefore, the P_{con} can be obtained as:

$$P_{con} = 4(P_{0\&0.5V_{dc}} + P_{0.5V_{dc}\&V_{dc}} + P_{V_{dc}\&1.5V_{dc}}) \,. \tag{17}$$

C. Switching Losses

The switching losses can be calculated according to the charging and discharging processes of the parasitic capacitor C_s in the switches, it is assumed that the capacitance of the parasitic capacitor is linear. The voltage of the parasitic capacitor is gradually charged to V_s when the switches are turned off, where V_s is the MVS of the switches, and the V_s of each switch is shown in Table IV.

TABLE IV
THE MVS OF EACH SWITCH IN THE PROPOSED INVERTER

Switches	S_1-S_8	S_1-S_8
MVS	V_{dc}	$V_{dc}/2$

Therefore, the P_{sw} can be calculated from:

$$P_{sw} = C_s {V_s}^2 f_s \,, \tag{18}$$

where f_s is the switching frequency of the switches, and it can be obtained from:

$$f_s = N_s f_o , \tag{19}$$

where N_s is the switching transitions in one period of the reference waveform.

As can be seen from Fig. 4, the switches are repeatedly turned on or off in the corresponding intervals. The N_s of each switch can be roughly obtained as the ratio of f_c and f_o if the switch works in the whole period. However, the switches in the proposed inverter only work in the specific intervals. Therefore, the N_s of each switch can be calculated as:

$$N_s = \frac{t_s f_c}{T_s f_o}, \tag{20}$$

where t_s is the working time of the switches, and it can be obtained from Figs. 3 and 4, T_s is the time of one cycle. Therefore, P_{sw} can be calculated from:

$$P_{sw} = 50\sum_{i=1}^{10} C_{si} V_{si}^{\ 2} t_{si} f_c . \tag{21}$$

In summary, the efficiency of the proposed inverter can be calculated as:

$$\eta = \frac{P_o}{P_o + P_{rip} + P_{con} + P_{sw}}, \tag{22}$$

where η and P_o are the efficiency and output power of the proposed inverter.

The aforementioned losses can be obtained numerically at different output power. It should be noted that r_s, ESR_C, f_o, f_c, C_s are considered 5mΩ, 60mΩ, 50Hz, 5KHz, and 500pF, respectively, for the losses calculations. The theoretical efficiency of the proposed seven-level inverter is shown in Fig. 6(a). Under the condition of a 30 V dc source and 30 Ω load, the three types of losses can be obtained as: P_{rip} = 0.49 W, P_{con} = 0.12 W and P_{sw} = 0.3 W. The ratio of the three types of losses is illustrated in Fig. 6(b).

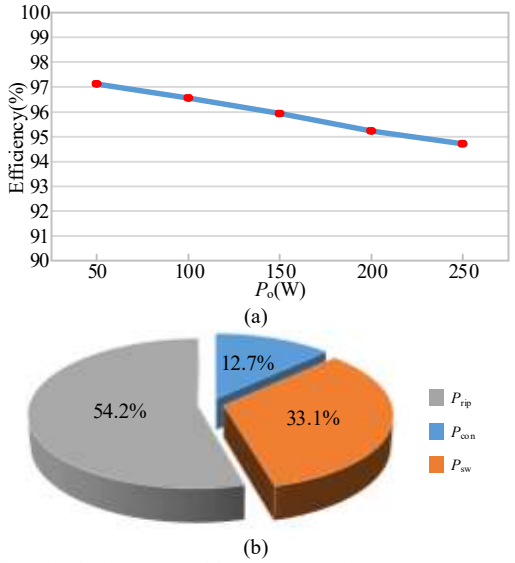


Fig. 6. Theoretical efficiency and losses. (a) Efficiency at different power; (b) the ratio of three types of losses.

IV. Topology Extension and Comparison Analysis

An advantage of the proposed inverter is that it is extensible. There are two ways to extend the topology. Each type has its own characteristics and can be used for different applications.

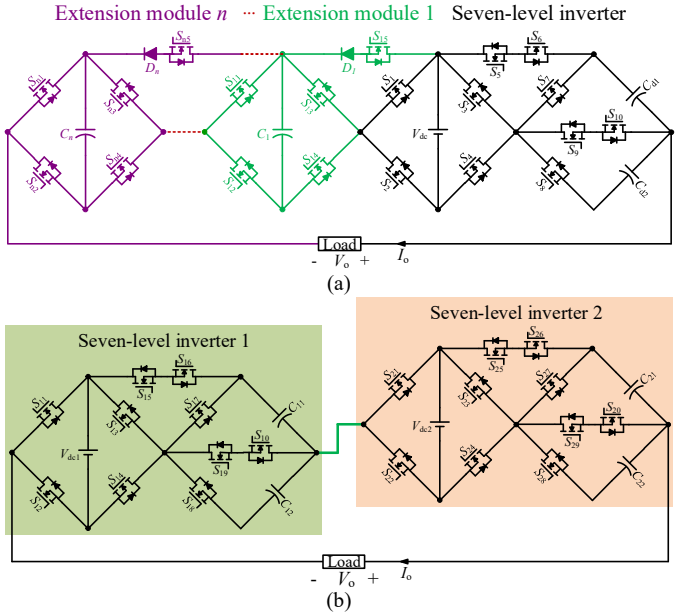


Fig. 7. Two types of extension. (a) Extension of the left H-bridge. (b) Connecting multiple inverters in Series.

A. Extending the H-bridge

It can be seen from Fig.2 that the left side of the proposed inverter is an H-bridge. The first type of extensions is achieved by using multiple H-bridges which are connected through switches and diodes, as shown in Fig. 7(a). It is worth mentioning that the independent power sources inside the extension H-bridges can be replaced by capacitors, which can enhance the applicability of the proposed inverter. In addition, thanks to the right-side capacitors, the output level under this extension can be significantly increased compared to conventional CHB MLIs. In fact, the total output level can be increased by 4 for every additional H-bridge. In the extended topology, the output level of the inverter, N_{level1}, has a quantitative relationship with the number of the extended H-bridges (n) and the number of switches (y):

$$N_{level1} = 4n + 7 = \frac{4y - 5}{5} . \tag{23}$$

B. Connecting Multiple Inverters in Series

The other way to extend the inverter is to connect multiple inverters in series. The extended topology with two inverters is shown in Fig. 7(b). Modular design can be achieved without using additional power devices, such as the switches and diodes used in the above extension, which is one of the benefits of this extension. According to the analysis in the last section, the highest output level of a single inverter is $3V_{dc}/2$. Then, the dc source voltage of the series-connected inverters can be set in proportion to increasing the output levels. To ensure the output voltage increases step-by-step, a suitable ratio is 1:7. Assuming x inverters are connected in series, the proportional relationship between each power source is:

$$V_{dc1} : V_{dc2} : \cdots : V_{dcx} = 1 : 7 : \cdots : 7^{x-1}. \quad (24)$$

Similarly, the quantitative relationship between the output level N_{level2} with the number of connected inverters (x) and the number of switches (y) is:

$$N_{level2} = 7^x = 7^{\frac{y}{10}}. \quad (25)$$

C. Comparison of the Two Extensions

Both extensions have their pros and cons. First of all, in the first extension, the output level increases linearly with the number of H-Bridges and switches. The output level in the second extension increases exponentially with the number of the connected inverters and switches. Although the growth rate of the first extension is considerable, the one of the second extension is significantly higher. Secondly, in both extensions, the voltage stress of each switch does not exceed the input source voltage. However, in the second extension, the voltage stress of the switches will increase gradually with the increase of the number of the connected inverters. It is because that the voltage of the dc sources in the series-connected inverter will increase. Finally, the first extension requires only one dc source, while the second requires multiple dc sources. The advantages of the two extensions make them suitable for different applications.

D. Topology Comparison

Table V shows the comparison of the proposed inverter with the recently proposed hybrid MLIs. The comparison has been made under the condition that all inverters have the same output level. These hybrid MLIs are able to limit the voltage stress on the switches to a low value, which is also a feature of the proposed inverter. However, more devices are used in the hybrid MLIs compare to the proposed inverter. In addition, most of them do not have the ability to boost the input voltage. It can be seen from Table V, the proposed inverter solves the above shortcomings, and has a better comprehensive performance.

TABLE V
COMPARISON WITH HYBRID MULTILEVEL INVERTERS

Items	[10]	[11]	[12]	7L-CHB	Proposed
Levels	7	7	7	7	7
Switches	18	16	8	12	10
Capacitors	4	3	3	0	2
DC sources	1	1	1	3	1
Voltage boosting	no	no	no	no	yes

In order to further evaluate the superiority of the proposed inverter, it has been comprehensively analyzed and compared with other recently proposed SCMLIs. The main indicators for the comparison are the number of power devices, MVS, and total standing voltage (TSV), etc. The comparison analysis has been carried out under the condition that their output level is $2m$+1 (or m steps). The results are shown in Fig. 8 and Table VI. "E_I" and "E_{II}" represent the first and second types of the extension. V_{step} is the voltage of each step.

It can be seen from Table VI and Fig. 8 that the proposed inverter shows excellent performance amongst the SCMLIs, especially in terms of the switch MVS. Although the value of MVS in [31] is the smallest, V_{step} in [31] is twice the V_{step} of the proposed inverter, and therefore, both inverters have the same MVS. However, with the extension of the inverter, the

TABLE VI
COMPARISON WITH DIFFERENT SCMLIS

Items	[22]	[23]	[26]	[31]	E_I	E_{II}
Voltage Gain	m	m	m	m	m/2	m/2
Switches	$3m$+1	$2m$+3	$3\log_2^m+3$	$5m$-1	$5m$+5/ 2	$10\log_7^{2m+1}$
Diodes	0	m-1	$\log_2^m$	m-1	m-3/ 2	0
Capacitors	m-1	m-1	$\log_2^m$	m-1	m+1/ 2	$2\log_7^{2m+1}$
Dc Source	1	1	multiple	1	1	multiple
MVS($\times V_{step}$)	m	m	m	1	2	$4m$+2/ 7
TSV($\times V_{step}$)	$7m$-3	(m^2+11m+4)/ 2	$7m$-4	$5m$-1	$5m$+3	$6m$
Inductive-load	yes	no	yes	yes	yes	yes

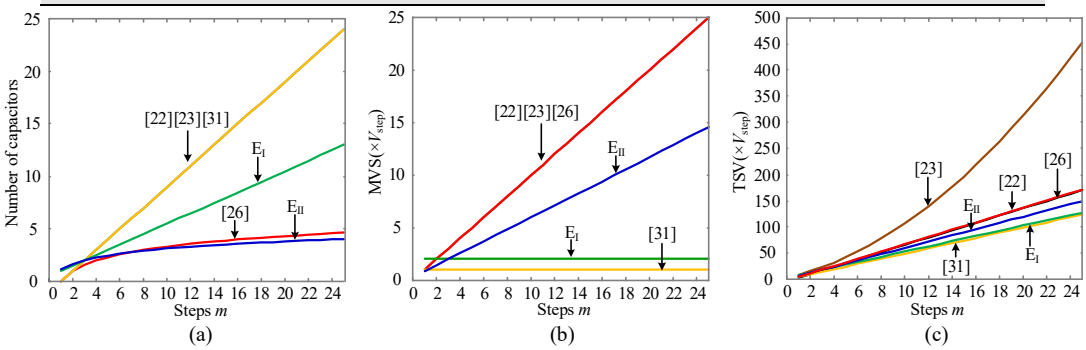


Fig. 8. The results of the comparison with different SCMLIs. (a) number of capacitors. (b) MVS. (c) TSV.

number of switches in [31] increases significantly, and the number of capacitors is also higher than the proposed inverter. In terms of the used capacitors, the topology in [23] is also excellent. However, [23] and the second extension of the proposed inverter need to use multiple dc power sources, which limits its application. Only the SCMLIs in [31] are superior to the proposed inverter in terms of TSV. However, the SCMLI in [31] requires a large number of switches.

The gain of the proposed inverter is half that of other inverters when the output is at the same level due to the existence of the voltage-dividing capacitors. If the same output voltage is achieved, the dc power source of the proposed inverter has to be doubled. However, the presence of the voltage-dividing capacitors makes it possible to effectively increase the number of output levels when the components used are equivalent, thereby substantially achieving the same gain. In addition, the two proposed extensions have their advantages which can be seen from Table VI. The first extension is better in reducing the voltage stress of the switches, while the second extension is better in reducing the number of devices. This shows good agreement with the previous analysis of the topology extension.

Table VII shows the comparison of the proposed inverter with the recently proposed SCMLIs feature low voltage stress and T type capacitors. The comparison is performed under the condition that the output level of all inverters is seven. It can be seen from Table VII that the proposed SCMLI is the optimal one in terms of the number of devices. In addition, the Q_m in Table VII is the discharge amount of capacitors, the benchmark discharge amount of the capacitor working at $0.5V_{dc}$ is defined as Q_u. Then, the capacitor discharge amount will be $2Q_u$ when it works at V_{dc}, and so forth. It can be seen from the Q_m of these inverters that the proposed inverter is superior in terms of the number of capacitors and the maximum discharge capacity. Therefore, the proposed inverter has the advantage of using a smaller capacitance.

TABLE VII
COMPARISON WITH LOW VOLTAGE STRESS SCMLIS

Items	[33]	[34]	[35]	[36]	proposed
Levels	7	7	7	7	7
Switches	10	10	10	9	10
Diodes	0	0	0	1	0
Capacitors	4	3	4	3	2
MVS	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}
Q_m	$6Q_u$	$5Q_u$	$5Q_u$	$5Q_u$	$4Q_u$

V. SIMULATION VERIFICATION AND EXPERIMENTAL VALIDATION

A. Simulations

To verify the effectiveness of the proposed inverter, a model of a seven-level inverter is built in MATLAB/Simulink. Parameters in the simulations are shown in Table VIII.

The simulation results are shown in Figs. 9 and 10. It can be seen from Fig. 9 that the inverter outputs 7-level PWM waves, and the current lags the voltage by about 8.9°. The fast Fourier transform (FFT) of the output voltage is given in Fig. 10. The THD is 16.26%. The 20th harmonic components are larger than others because the carrier frequency is 2 kHz. As other harmonics are much less than the 20th harmonics, this can simplify the filter design.

TABLE VIII
SIMULATION PARAMETERS

Parameters	Values
Input DC source (V_{dc})	30 V
Output frequency (f_o)	50 Hz
Carrier frequency	2 kHz
Modulation index (M)	0.9
Capacitors (C_1, C_2)	2200 μF
Loads	30 Ω & 15 mH

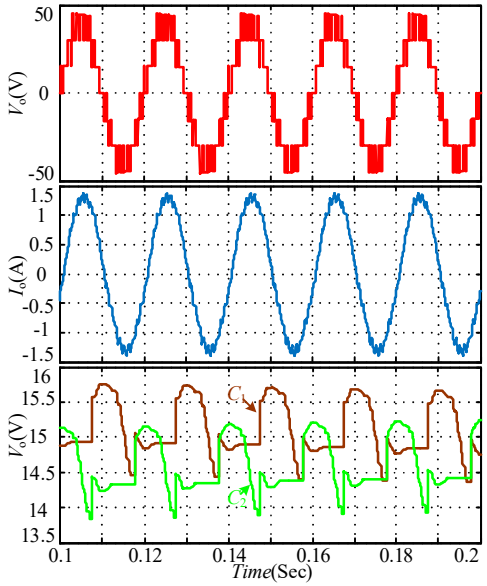


Fig. 9. Simulation results of the output voltage, current and capacitor voltage.

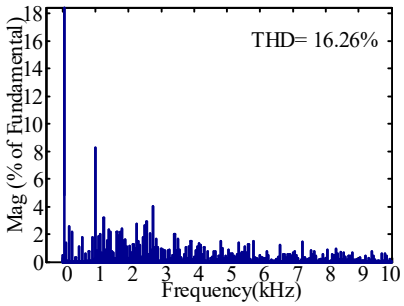


Fig. 10. THD of the output voltage.

B. Steady-state Analysis

In order to validate the feasibility of the proposed inverter, a seven-level prototype has been constructed to test its steady-state and dynamic performance. The parameters of the prototype are listed in Table IX and the experimental platform is shown in Fig. 11. The waveforms of voltage and current, the voltage waveforms of the two capacitors and the voltage stress of switches are studied.

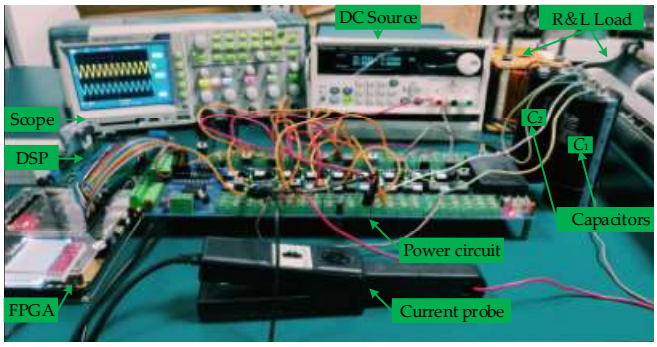


Fig. 11. Experimental platform.

TABLE IX
EXPERIMENTAL PARAMETERS

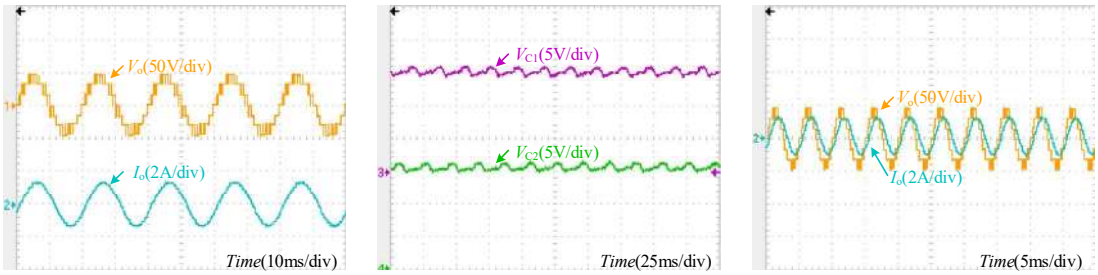
Parameters	Values
Input DC source (V_{dc})	30 V
Output frequency (f_o)	50 Hz
Switching frequency	2 kHz
Capacitors (C_1, C_2)	4700 μF
Loads	30 Ω & 15 mH or 50 Ω or 100 Ω
Switches (MOSFET)	SPP20N60C3
Optocoupler-driver	TLP250
Current probe	Tektronix A622

Experiment has been conducted in an *R-L* load (30 Ω & 15 mH) to test the steady-state performance of the proposed inverter. The waveforms of voltage and current are shown in Fig. 12(a). The voltage of each step is 15 V and the maximum output voltage is 45 V. As the voltage of the input source used is 30 V, a boost gain of 1.5 is achieved which matches the previous analysis. The steady-state capacitor voltages are shown in Fig. 12(b). It can be seen that the two capacitors are self-balancing with small voltage ripples, which is consistent with the analysis of capacitor voltage balancing. Under the same resistance condition, increase the inductance value to 60mH. The results are shown in Fig. 12(c). It is obvious that the output current lags behind the voltage which proves the capability of supplying inductive loads.

Fig. 13 shows the voltage stress of the switches. The MVS of the switches is limited to the input power voltage V_{dc}, which is an advantage of the proposed inverter. A total of ten switches are used in the proposed seven-level inverter. The voltage stress of S_1 to S_8 is V_{dc}, and is $V_{dc}/2$ of S_9 and S_{10}.

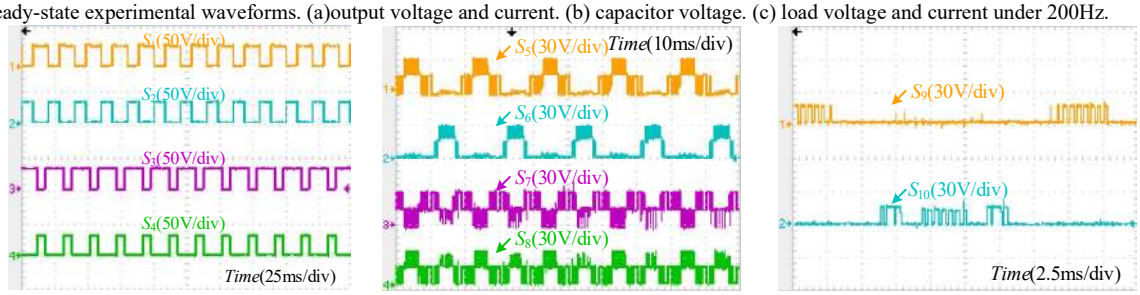
The experimental results of the current stress of the switches are shown in Fig. 14. Thanks to the small voltage ripples of the capacitors, all switch current stress is small. The peak value of the current stress of the switches in the capacitor charging circuit is only about 1 A.

C. Dynamic Analysis



(a) (b) (c)

Fig. 12. Steady-state experimental waveforms. (a)output voltage and current. (b) capacitor voltage. (c) load voltage and current under 200Hz.



(a) (b) (c)

Fig. 13. Voltage stress of switches. (a) S_1, S_2, S_3, S_4; (b) S_5, S_6, S_7, S_8; (c) S_9, S_{10}.

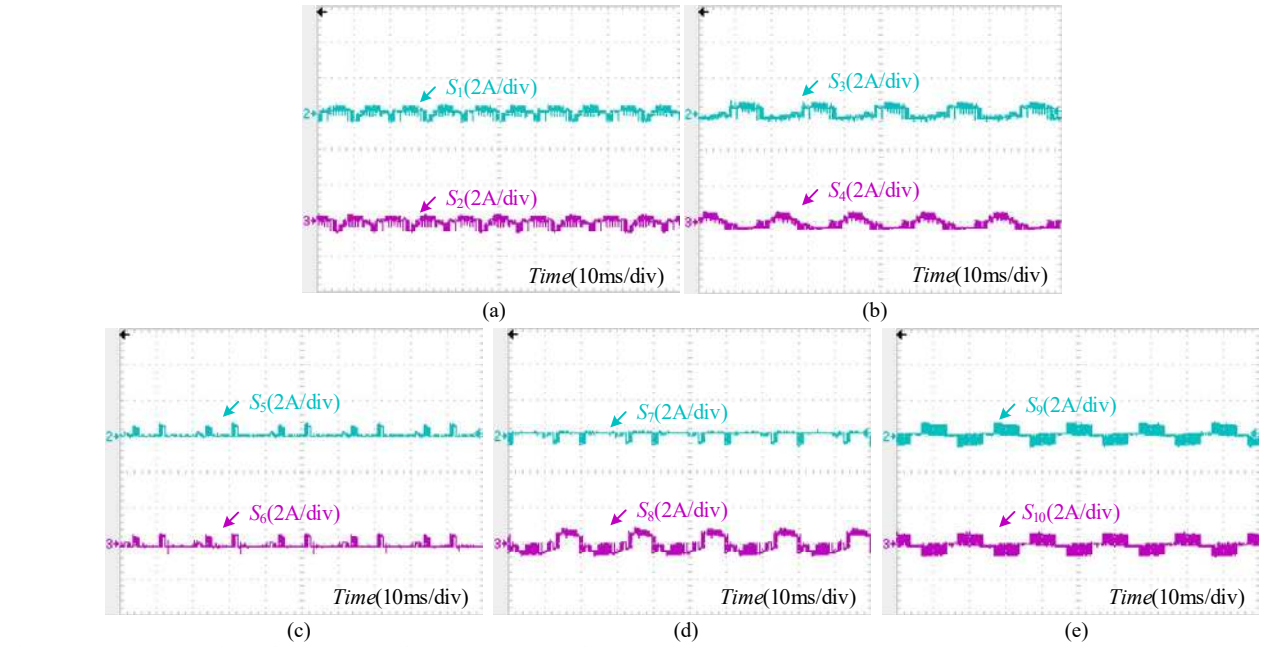


Fig. 14. Current stress of switches. (a) S_1, S_2; (b) S_3, S_4; (c) S_5, S_6; (d) S_7, S_8; (e) S_9, S_{10}.

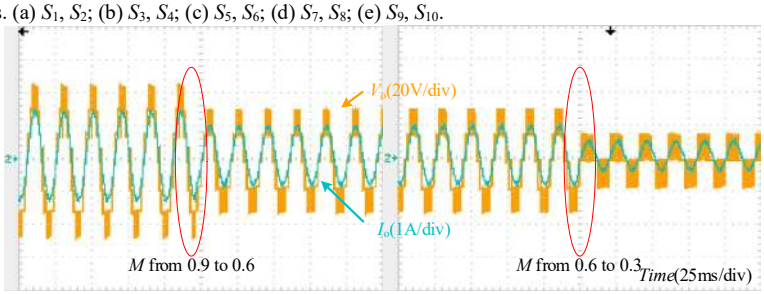


Fig. 15. Dynamic responses of the output voltage and current when the modulation index M changes.

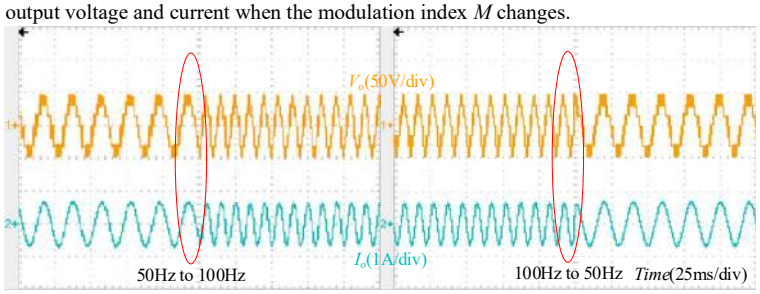


Fig. 16. Dynamic responses of the output voltage and current when the frequency f_o changes.

An inverter with excellent performance should be tolerant to the changes of working conditions, such as sudden changes of the load, input voltage, frequency and amplitude of modulation waves, etc. To further test the performance of the inverter in dynamic conditions, the following experiments have been performed. Fig. 15 shows the output voltage under the condition that the amplitude of modulation wave changes. It can be seen from Fig. 15 that the output voltage changes from seven-level to five-level and then to three-level when M changes from 0.9 to 0.6 and then to 0.3. The transient processes complete fast, which proves the excellent dynamic performance of the proposed inverter. The experimental results also show good agreement with the analysis in Table II.

The proposed inverter can properly adapt to the conditions when the frequency of the modulation wave changes. The output voltage and current when frequency changes are shown in Fig. 16. It is observed that the inverter can transit accordingly with a fast transient response in both cases (50 to 100Hz and 100 to 50Hz).

The experimental results under the condition of a sudden change of the load are shown in Fig. 17. The setting of the load change is: from no-load condition changes to an R-L load (30Ω & 15mH), and then changes to a resistive load (50Ω). The results illustrate that the inverter performs well when the load changes.

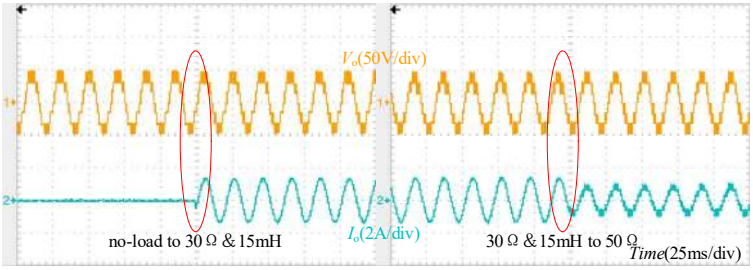
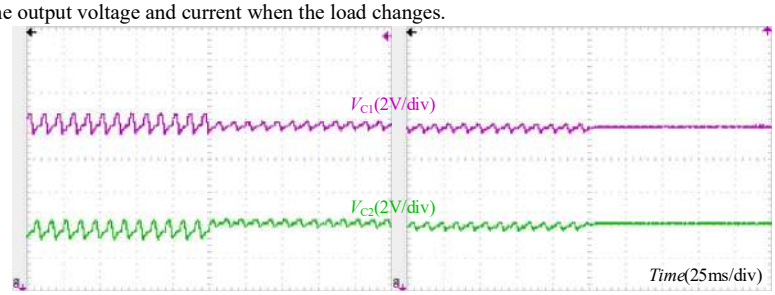
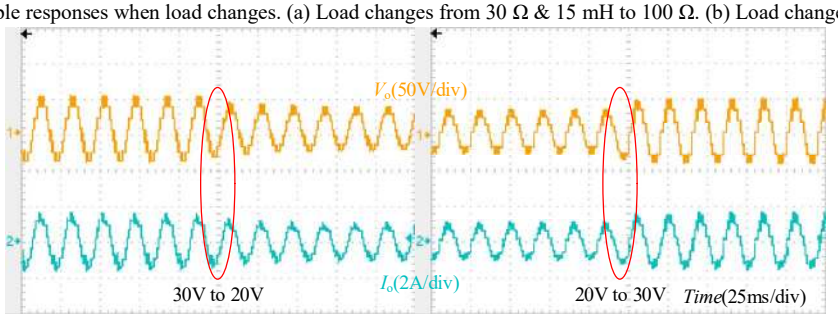


Fig. 17. Dynamic responses of the output voltage and current when the load changes.



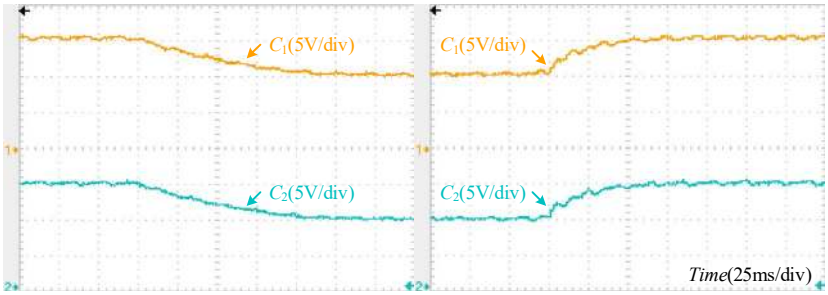
(a) (b)

Fig. 18. Capacitor voltage ripple responses when load changes. (a) Load changes from 30 Ω & 15 mH to 100 Ω. (b) Load changes from 100 Ω to no-load.



(a) (b)

Fig. 19. Responses of load voltage and current when the dc source voltage changes. (a) Dc voltage changes from 30 V to 20 V; (b) Dc voltage changes from 20 V to 30 V.



(a) (b)

Fig. 20. Responses of capacitor voltages when dc source voltage changes. (a) Dc voltage changes from 30 V to 20 V; (b) Dc voltage changes from 20 V to 30 V.

Load affects the discharging current of the capacitors, and therefore, affects the discharge amount of the capacitors, which will, in turn, affects the voltage ripples of the capacitors. Fig. 18 shows the voltage ripples of capacitors when the load changes. It can be seen that the voltage ripples of capacitors decrease with the increase of impedance.

The charging and discharging of C_1 and C_2 when the dc source voltage changes from 30 V to 20 V and the reverse processes, which can emulate the abrupt changes of the input voltage (e.g. a power source of a solar cell), has been carried. As shown in Figs. 19 and 20, the inverter performs well during the abrupt change of its input voltage. It can be seen from the experimental results that the inverter can quickly reach to a new steady-state and has good dynamic performance in adapting to changes of the input voltage.

D. Efficiency analysis

The efficiency *v.s.* load power curves at different supply voltages are shown in Fig. 21. The efficiency is higher than 95% when the output power does not exceed 250 W. When the inverter output power is 200 W under an input voltage of 30 V, the efficiency is 95.5%, which is higher than the 95.3% in [25] and 89% in [26]. In addition, it can be seen from Fig. 21 that the efficiency increases as the input voltage increases

under the same load power. This is because the load current will decrease, and therefore reduce power losses.

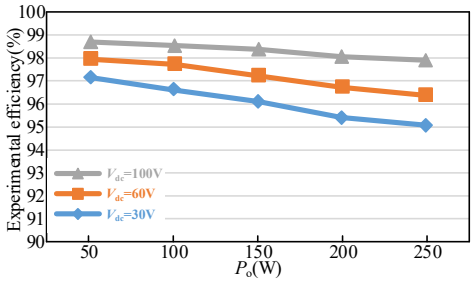


Fig. 21. The efficiency *v.s.* load power curves at different supply voltages.

E. Discussion

The voltage boosting, capacitor self-balancing and capability of supplying inductive loads of the proposed inverter have been investigated through simulation verification and experimental validation. The experimental results show that with an input dc voltage of 30 V, the amplitude of output voltage is 45 V, achieving a voltage gain of 1.5. The experiment also proves that the capacitor voltages can achieve self-balancing. In addition, the capability of supplying the inductive load is validated through tests under a load of 30 Ω and 60 mH. Compared with other SCMLIs, the proposed inverter features low MVS: the voltage stress of all switches does not exceed the dc source voltage. Moreover, the working conditions may change when the inverter is operating. For example, the amplitude and frequency of the sinusoidal modulation wave, and sudden changes in the load and voltage of input dc source. These scenarios are also tested through experiments of dynamic changing, which show that the proposed inverter is capable to respond to dynamics and stabilize in a new working state quickly.

VI. Conclusion

A novel T-type switched-capacitor multilevel inverter with low voltage stress and capacitor voltage self-balancing capability has been proposed in this paper. Only two capacitors are used to achieve a seven-level output without affecting the switch count.

Outcomes and features of this topology include: 1) Compared to conventional SCMLIs, the maximum voltage stress of the switches in the proposed inverter can be limited to less than the input dc voltage V_{dc}. The low voltage stress is one of the excellent features that make the proposed inverter an attractive alternative for medium- and high-voltage photovoltaic power generation applications. 2) With the merit of the low voltage stress, a voltage boost gain of 1.5 can be achieved as well. 3) Two topology extension schemes have been proposed to achieve a higher voltage boost gain and higher output level, which is superior in its flexible extensibility and capability of supplying inductive loads. 4) The capacitor voltages of the proposed inverter can be self-balanced which can simplify its control complexity. 5) The capacity of supplying the inductive load is ensured by the bidirectional energy loop in each working mode.

The above features of the proposed inverter have been validated through a seven-level experimental prototype. The experimental results indicate that the inverter has an excellent performance in both steady-state and dynamic conditions.

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