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A Technology Overview of the PowerChip Development Program

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***Abstract*—The PowerChip research program is developing technologies to radically improve the size, integration and performance of power electronics operating at up to grid-scale voltages (e.g., up to 200 V) and low-to-moderate power levels (e.g., up to 50 W), and demonstrating the technologies in a high-efficiency light-emitting diode (LED) driver, as an example application. This paper presents an overview of the program and of the progress towards meeting the program goals. Key program aspects and progress in advanced nitride power devices and device reliability, integrated high-frequency magnetics and magnetic materials, and high-frequency converter architectures are summarized.**

***Index Terms*—Intergrated power converter, LED driver, PwrSoC, integrated magnetics, Gallium Nitride, HF**

I. Introduction

Power electronics is a key technology for improving functionality and performance and reducing energy consumption in many kinds of systems. However, the size, cost, and performance constraints of conventional power electronics currently limit their applications and ability to realize this potential. This is especially true in relatively high-voltage, low-power applications (e.g., voltages of up to a few hundred volts and power levels of up to tens of watts), such as off-line power supplies, light-emitting diode (LED) drivers, converters and inverters for photovoltaic panels, and battery interface converters, among myriad other applications. Advances in miniaturization and integration of energy-conversion circuitry in this voltage and power range would have tremendous impact on many such applications, and are the topic of the work described here.

Through examining the present state of the art in this area, we found much room for improvement. We examined commercial line-interfaced (120 Vac) LED drivers in the 3–30 W output range. For the collection of drivers studied, efficiency was in the range of 64–83%, and power factor was in the range of 0.59–0.96, with no design exhibiting both good power factor and good efficiency. Switching frequencies of these drivers were in the range of 57–104 kHz, and all designs exhibited low power densities below 5 W/in^3 (0.3 W/cm^3) and contributed substantially to the overall system size. Reconfiguring these designs for wide-range dc input at similar peak voltage levels might be expected to provide modest improvements in some cases (e.g., by reducing the capacitor volume for attenuating twice-line-frequency ripple), but would not significantly change the picture: the volume of each of these designs was dominated by discrete magnetic components. Recently published academic designs are harder to fully evaluate, but appear to provide generally similar performance with moderate improvements in individual aspects, e.g., [1]–[3]. These results indicate that power electronics continues to be a significant limitation in solid-state lighting [4], and that there is a need for major improvements in miniaturization and performance in this voltage and power range. We seek to improve power densities in this space by more than an order of magnitude (e.g., to beyond 100 W/in^3) while preserving or enhancing other performance aspects. Such advances would facilitate, and require, high degrees of integration, and would make power electronics much less dominant as a system constraint. Our current projections indicate that the final integrated demonstration system we are developing will exceed this target.

Miniaturization of power electronics and integration of magnetics require reductions in energy storage that can only be realized through dramatic increases in switching frequency [5]. Recent work has shown the potential of high-frequency operation in systems operating to beyond 100 MHz at tens of watts and tens of volts (e.g., [5]–[7]), and there has been preliminary work at up to a few tens of MHz at hundreds of

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watts and volts (e.g., [8]). However, achieving the necessary frequency increases at high voltages and modest powers (e.g., at up to hundreds of volts and tens of watts) and realizing the desired miniaturization and integration remains a major technical challenge that we seek to address[1].

In this paper, we present an overview of the PowerChip research program[2], a four-university research effort seeking to achieve significant breakthroughs in integrated high-frequency power electronics [9]. This research program focuses on advancing three key elements that presently limit the performance of power electronic circuits – semiconductor devices, magnetics, and circuits – and on harnessing these advances through co-optimization of circuit topology and component design for the key application of drivers for high-efficiency solid-state lighting (SSL). This endeavor encompasses advances in GaN power devices, nano-structured magnetic materials and microfabricated magnetic designs, and high-frequency power circuit design. Section II of the paper describes the overall design considerations, the conversion architecture employed to address these considerations, and the topology selected for the demonstrator system. Sections III–VI describe the multi-pronged research effort into improved magnetic materials and integrated magnetic components. Section VII presents an overview of the research into advanced high-voltage nitride power devices and power device reliability, and Section VIII concludes the paper.

II. System Architecture and Circuit Design

A. Design Considerations

We begin by considering the overarching design considerations for miniaturizing and integrating power electronics at high voltages and low powers. For a given switching power converter topology, the values of inductors and capacitors and the total required energy storage vary inversely with switching frequency, directly motivating increases in frequency to achieve miniaturization. However, the scaling of passive component *size* with frequency is a far more complex issue. For example, in magnetic components — which dominate the size of most designs — scaling depends on winding loss effects, magnetic material core loss characteristics, and heat transfer limits among other considerations (e.g., see [5], [10]–[14]). Consequently, size does not necessarily decrease monotonically with frequency. Achieving substantial miniaturization through high-frequency operation thus requires a combination of: 1. Designing the system to minimize demands placed upon the passives, and especially upon the magnetic components; 2. Developing and exploiting magnetic materials that work well at high frequencies; 3. Careful modeling and design of magnetic components to best exploit the HF materials and inductor geometries; and 4. Co-optimization of the circuit and passive components to achieve the best size/efficiency tradeoff. The level of miniaturization we are targeting requires combining all four of these approaches, described in more detail below and in Sections III, IV, V, and VI.

Unfortunately, the rate at which the physical sizes of passive components decrease with frequency is slow, such that the effects of interconnect parasitics become increasingly important as frequencies increase. Moreover, some parasitic elements (such as semiconductor device parasitic capacitances and inductances) do not scale at all with operating frequency[3]. As a result, parasitics become a dominant factor in high frequency designs. To achieve miniaturization through extreme high-frequency operation, one must choose circuit topologies that inherently absorb important parasitic components in their operation (and so are tolerant of large parasitics), rather than simply trying to minimize the effects owing to such parasitics, as may be undertaken at conventional frequencies.

A third consideration pertains especially to converters at high voltages and low currents. As the desired operating voltage is increased and/or current is decreased in a particular circuit topology, inductor values increase and capacitor values decrease (e.g., characteristic impedance $Z_0 = \sqrt{L/C}$ scales as V/I) [5]. Consequently, for high voltages and low currents (and low powers), one must operate with relatively large inductors and small capacitors. At the same time, inductor and capacitor values both scale down as frequency is increased (e.g., $\omega_0 = 2\pi f = 1/\sqrt{LC}$). Scaling up too far in frequency may require capacitance values that are too low to be feasible, placing practical limits on frequency and miniaturization. In high voltage, low-power designs, it is thus desirable to seek architectures and circuit topologies that exploit relatively low characteristic impedance values (i.e., small inductances and large capacitances) to reduce constraints on scaling up in frequency.

Lastly, operating range and control are important architectural considerations. We consider designs that are suited to operating either from a wide input dc voltage range or from an ac input at high power factor. In either case, operation over a wide range of voltage conversion ratios is a requirement. At the same time, to achieve extreme high-frequency operation at high voltages, one typically adopts zero-voltage soft switching techniques to reduce capacitive discharge losses. However, soft switching is often difficult to maintain over very wide voltage conversion ratios, because of the ways that circuit waveforms change with operating point. It is thus an important challenge to develop designs that maintain the desired soft-switched operation (or close to it, such that efficiency remains high) across wide voltage conversion ranges.

B. System Architecture

To address the above considerations, we have adopted a merged-two-stage converter architecture, as illustrated in Fig. 1 [15], [16]. The first stage is a variable-topology switched-capacitor converter; because it employs only capacitors and switches, it can attain high power density and efficiency at

[1]The performance we seek is attainable with switching frequencies in the HF frequency range (3-30 MHz) and above.

[2]This research project is sponsored by the Advanced Research Project Agency–Energy at the U.S. Department of Energy.

[3]Device parasitics can be partially mitigated by moving to devices with inherently smaller size for a given voltage and current rating, as accomplished in our adoption of nitride devices. Nevertheless, parasitics become increasingly important as frequency is increased.

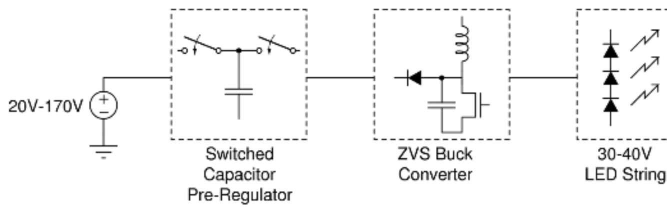

Fig. 1. A merged two-stage converter architecture having a first switched capacitor stage that provides voltage transformation and crude preregulation, and a second high-frequency magnetic stage that provides fine regulation of the output.

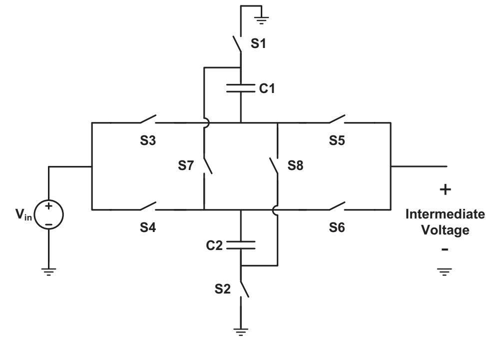

Fig. 2. Schematic of the switched-capacitor stage of the merged two-stage converter.

TABLE I
CONTROL OF SWITCHED-CAPACITOR CIRCUIT.

Case	S1	S2	S3	S4	S5	S6	S7	S8
1:2	q	$\overline{q}$	q	$\overline{q}$	$\overline{q}$	q	$\overline{q}$	q
1:1	off	off	on	on	on	on	off	off
2:1	q	$\overline{q}$	$\overline{q}$	q	q	$\overline{q}$	$\overline{q}$	q

modest operating frequencies, but cannot efficiently achieve fine voltage regulation [17]. This stage serves to both reduce the range of voltage conversion ratios over which the second stage must run, and to reduce the maximum voltage level (and hence impedance level) that the second stage must handle, both of which are favorable for the second stage, as discussed above. The second stage is a magnetics-based stage that provides both additional voltage transformation and regulation of the output, and is operated at high frequency (HF) to minimize magnetic component size. To again follow the considerations identified above, the second stage is designed to employ a small value of inductance (which facilitates the use of integrated inductors) and to inherently incorporate parasitics (particularly parasitic capacitance) as part of its operation. The stages in this architecture are selected so as to minimize device voltage stress (important in high-voltage applications), and to enable partitioning of the device requirements into "slow, high-voltage" and "fast low-voltage" device categories in cases where that is necessary or desirable. Such partitioning is advantageous in quickly realizing the advantages of the new device technologies we are developing, for example. Moreover, the two stages are designed to operate together ("merged") in a manner that enables higher efficiency and power density than could be achieved in a conventional architecture having separate stages [15], [16]. We describe each of these stages in more detail below, and present experimental results highlighting the promise of this architecture.

C. Switched-Capacitor Stage

The first stage of the merged two-stage converter is a variable-topology switched capacitor (SC) circuit that requires only two energy transfer capacitors and provides nearly continuous input and output currents. This SC circuit is illustrated in Fig. 2 and its control is described in Table I. It provides high efficiency over a wide power range and achieves high power density even at relatively low operating frequencies (e.g., 30-100 kHz). An added benefit of the "merged two-stage architecture" [15], [16] used here is the "soft charging" operation of the SC stage through interactions with the high-frequency magnetics stage. The high-frequency stage effectively charges and discharges the SC stage as a current source, thereby enabling the low conduction losses of the SC fast-switching limit while operating at the low frequencies of the SC slow-switching limit [17], [18]. One can thus obtain a combination of higher efficiency and higher power density from the SC circuit than is otherwise possible.

The SC circuit serves multiple functions. First, by switching among different conversion modes, it can take a widely ranging input voltage (25–200 V) and provide an intermediate voltage having a greatly reduced voltage range (50–100 V). That is, an 8:1 input voltage range is narrowed to a 2:1 intermediate voltage range. This enables the second high-frequency stage to operate efficiently over a much wider range of input-side conditions than would otherwise be possible. Second, by operating in voltage-halving mode for high input voltages, the SC stage reduces the peak input voltage into the HF second stage. This reduces device voltage stress, and provides the desired voltage range for the magnetic regulation stage. Moreover, it improves the impedance levels the HF stage must operate at (i.e., increasing allowable capacitance levels and reducing the required inductance value in the magnetic stage). Lastly the SC circuit provides a tremendous degree of flexibility to the system. The driver can be operated across a very wide 8:1 dc input voltage range (25–200 V), or can be combined with a line-frequency rectifier at its input to operate from a 120 V rms ac input. Note that in our overall system development, very high power densities and efficiencies are available by employing existing discrete ceramic capacitors in the SC stage; consequently we have not undertaken development of more advanced capacitor technology.

D. High-Frequency Regulation Stage

The second stage of the converter, shown in Fig. 3, is a resonant-transition discontinuous-mode inverted buck converter operating around 10 MHz, with ZVS soft switching over part of its range and near soft switching over the rest of

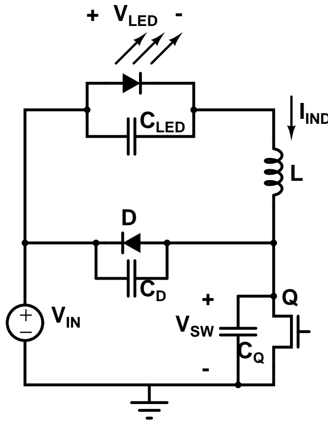

Fig. 3. Schematic of the second magnetic stage of the merged two-stage converter. This converter stage is designed to operate at high frequency.

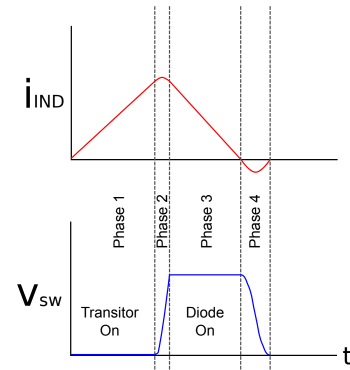

Fig. 4. Operating stages of the high-frequency resonant transition inverted buck converter. The converter achieves zero-voltage switching over most of its range, and low-loss near-zero-voltage switching over the remainder of the operating range. Power control is readily achieved by varying the on-state duration of the switch (phase 1).

the range[4].

This design has several benefits. First, it operates with low-loss switching using a single common-referenced switch, making it suitable for operation at high frequencies (HF, 3-30 MHz)[5]. Because it operates at HF, this stage approximates a current-source load to the first stage, enabling soft charging and discharging of the capacitors in the first stage. Second, it requires only a single, small-valued inductor, facilitating the use of integrated magnetics. Furthermore, it has very fast response (near single cycle) to input voltage transients and changes in the output current command. Finally, for a given input voltage, the output current is roughly proportional to transistor on-time, allowing a variety of control schemes to be employed.

The buck converter goes through four phases of operation in an HF switching cycle, as shown in Fig. 4. In Phase 1, the transistor is on, and i_{IND} ramps up linearly. In Phase 2, the transistor turns off, and the switch voltage, v_{SW}, rings up to the input supply. In Phase 3, the diode conducts, and the i_{IND} ramps down to zero. In Phase 4, both devices are off, and the inductor rings with the net capacitance at the switch drain node. i_{IND} rings negative and v_{SW} rings down to zero or near zero volts. At this point, the transistor is turned back on and the cycle repeats.

E. Example Experimental Results

Initial tests of the proposed architecture and circuit topology have been undertaken using available commercial GaN devices and wire-wound magnetic components. Fig. 5 shows experimental waveforms for an implementation of the second stage operating at approximately 7.8 MHz from a 100 V intermediate voltage. The circuit components are indicated in Table II ; more detail is available in [20], [21]. Fig. 6 shows the

Fig. 5. Waveforms for a prototype HF magnetic stage operating at a frequency of approximately 7.8 MHz from an input voltage of 100 V. Top: Gate voltage (2 V/div); Middle: Drain voltage (50 V/div); Bottom: Inductor current (1 A/div); Horiz: 40 nS/div. At the top end of the input voltage range, the HF stage loses true zero-voltage turn on, but switch turn on is at a sufficiently low voltage that efficiency remains high.

TABLE II
COMPONENT VALUES AND TYPES IN THE PROTOTYPE CONVERTER.

Element	Value	Type
Switches (all)	200 V, 3 A	EPC1012
Diode (HF stage)	2 x 5 A, 170 V	STPS10170CB-TR
L (HF stage)	844 nH	2 x 422nH Maxispring
C (SC stage)	1 μF, 100 V	X7R, 1210 package

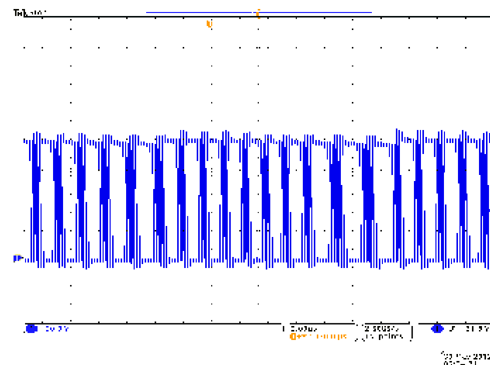

Fig. 6. Modulation of the HF stage caused by switched capacitor droop.

[4]By "inverted", we mean that the converter is designed with "common positives", such that the switch is referenced to a fixed potential. This is of great practical importance in designs that must operate at high frequencies [5]. Control methods aside, for the portion of its operating range for which it is truly soft switched, the topology acts much like a quasi-square-wave ZVS buck converter with a low ratio of switching to resonant frequency [19].

[5]At the high end of the input-voltage range, the HF stage loses ZVS at switch turn on. However, the switch voltage at turn on is always low such that efficiency remains high even under these conditions.

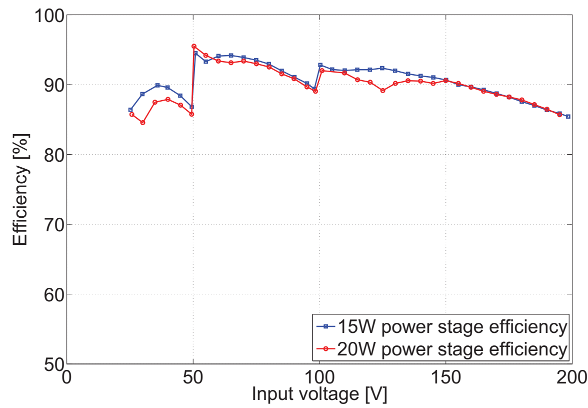

Fig. 7. Power stage efficiency of a merged two stage converter prototype configured to operate from a wide-range dc input of 25-200 V. Power stage efficiency is shown for two regulated output power levels (15 W and 20 W) across the input voltage range. Table II indicates circuit component values.

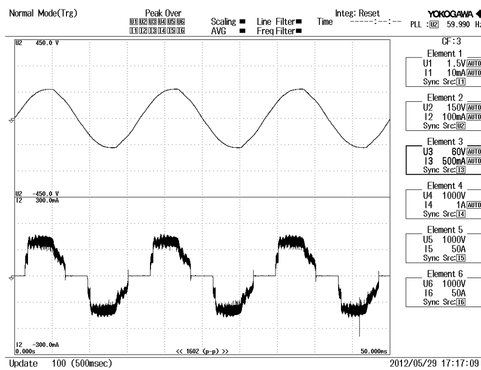

Fig. 8. Input voltage and current of a prototype merged two-stage converter operated from the ac line. The prototype achieves a power stage efficiency of 88% and a 0.93 power factor using only commercially-available devices and components.

envelope of the HF stage switch voltage over a much longer time scale. Variations in the envelope of the switch voltage due to the charging and discharging of the capacitors in the first stage (which is switching at approximately 50 kHz) are clearly visible; this illustrates the "soft charging" of the SC stage by the HF magnetic stage. For a 2:1 stepdown, our prototype SC stage provides greater than 98% efficiency at the requisite loading, and nearly 100% efficiency in bypass (1:1) mode.

Fig. 7 shows the power stage efficiency of a prototype merged two stage converter configured to operate from a wide-range dc input of 25–200 V. Fig. 8 shows the behavior of a second prototype converter configured to operate from the 120 V, 60 Hz AC line. This prototype converter provides an overall power stage efficiency of 88% efficiency with a 0.93 power factor using available commercial devices and components.

III. Magnetics Technology

As discussed in Section II-A, magnetics (inductors and transformers) are often the largest and most expensive components in power electronic circuits and are responsible for a large portion of the power loss. As operating frequencies are increased, the physical size of the passive components can, in theory, be correspondingly reduced while maintaining or improving efficiency [5]. Realizing this reduction in size and corresponding improvement in efficiency requires improvements in magnetics technology. We are exploring several approaches to microfabricating high-efficiency power magnetics.

As the switching frequencies of the power electronics rise and the size of the magnetics falls, new fabrication strategies for the magnetics become possible. On-chip or similar-scale inductors built for power converters in the multi-megahertz region include [22]–[39] and are reviewed in [40], [41]. With sufficiently small volume, the magnetics can be embedded in the substrate of the power circuit or within a secondary substrate and flip-bonded above the power circuit. If the inductor is embedded in the power-circuit substrate, dead space of the substrate is then used for magnetics, eliminating the high profile of the magnetics and helping to reduce the volume of the system.

We have been pursuing development of several types of microfabricated inductors, as described below. In order to facilitate co-optimization of inductor and circuit designs, we have developed extensive models addressing each of these inductor types. The models predict inductance, winding losses and, in magnetic-core inductors, the core losses, as described in Section IV. The loss models are employed in a multi-objective co-optimization algorithm to determine inductor designs and circuit parameters which minimize power loss while maximizing power density, as described in Section V. Inductor fabrication processes and experimental results, including development of new magnetic materials, are described in Section VI.

A. Toroidal air-core inductors

Air-core magnetics offer the advantages of avoiding magnetic core losses as well as avoiding the need for a fabrication process incorporating special materials [5], [42]–[44]. Planar spiral and solenoidal air-core inductors produce significant external fields which may cause losses in nearby conductors and electromagnetic interference problems, but toroidal geometries can mitigate these concerns. Microfabricated toroidal inductors have been fabricated above substrates [45], [46], as well as embedded in substrates, most commonly in printed circuit boards in which toroidal magnetics are formed using copper traces and plated-through vias [47], [48]. Similar inductors and transformers have also been successfully electroplated in copper on Pyrex substrates [49], [50]. Thick spiral inductors [51] and toroidal inductors [52], [53] have also been embedded in silicon and other substrates.

We present three-dimensional microfabricated toroidal air-core inductors with thick electroplated windings for high-power operation. These inductors are fabricated using advanced microfabrication technologies, which enables finer winding features, higher copper packing density, higher inductor aspect ratios, and thus higher inductor quality factors compared to previously-reported inductors. Inductors are either microfabricated on low-loss substrates for maximum performance, or inside the volume of a silicon wafer to facilitate integration with on-silicon CMOS circuitry.

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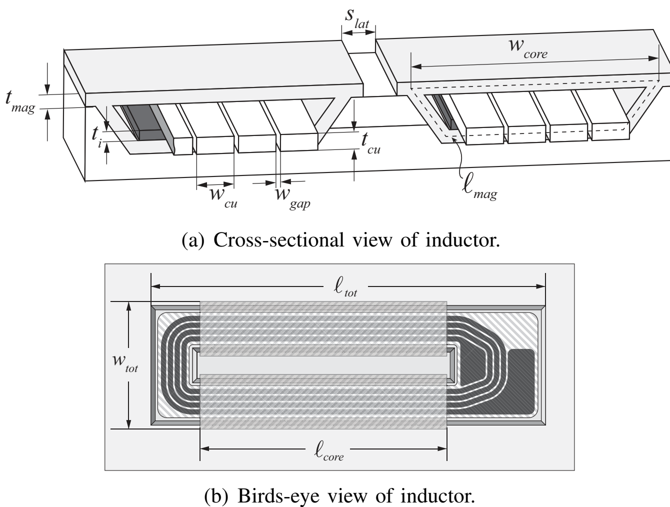


(a) Cross-sectional view of inductor.

(b) Birds-eye view of inductor.

Fig. 9. Illustrations of the silicon-integrated racetrack inductor geometry.

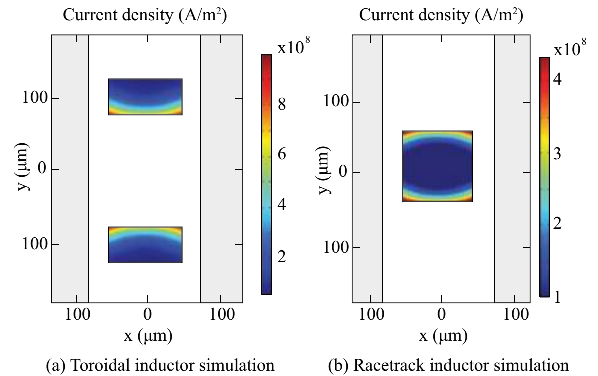


Fig. 10. Examples of finite-element simulations for toriodal **(a)** and racetrack **(b)** windings. Shown for each is one section of a periodic multi-turn structure with side-by-side turns, simulated by the use of symmetry boundary conditions at the left and right of the white region.

B. Magnetic-core inductors

As discussed in [42], thin-film magnetic materials make it possible to reduce the height needed to achieve high efficiency in power magnetics. Most soft thin-film magnetic materials that are attractive for power applications exhibit uniaxial anisotropy, and so must be designed for magnetic flux in only one direction [23]. One popular approach to making use of such a material is to use a "racetrack" geometry. In this geometry, planar-spiral windings are extended along one axis to form an elongated spiral. The elongated section of the spiral can be surrounded by an anisotropic-magnetic material to achieve low loss and high power density. Previous chip-scale racetrack inductor designs have typically focused on micro-fabricating components above the silicon wafer surface [54]–[56].

We present a racetrack-integration approach in which the inductor windings are fabricated within anisotropically-etched trenches in a silicon wafer, as illustrated in Fig. 9. A Co-Zr-O thin-film magnetic material is reactively sputtered to form a magnetic core surrounding the plated-copper windings [57].

While the racetrack geometry allows effective use of an anisotropic material with the easy axis of magnetization oriented in a single direction, toroidal geometries have significant advantages, particularly in combination with the advanced toroidal coils developed in this project. Designs such as the racetrack inductor incur extra losses where flux transitions between upper and lower sections of the core, because in these regions the flux direction is perpendicular to the magnetic layers and induces eddy-current loss [29], [58]. This problem is eliminated in toroidal inductors because all flux is parallel to the plane of the magnetic layers. However, using anisotropic magnetic materials such as Co-Zr-O effectively in a toroid requires an unusual radial orientation of the anisotropy. Using an approach first proposed in [59], we have fabricated toroidal cores with radial anisotropy (i.e. a radial easy axis and a circumferential hard axis) and integrated them within micro-fabricated toroidal windings.

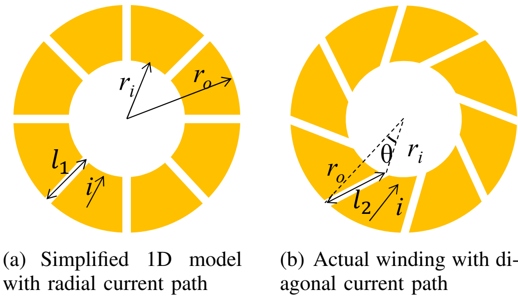
IV. Magnetics Modeling

A. Winding Loss Models

All of the magnetics designs under consideration include a multi-turn single-layer winding with conductors thick compared to a skin depth. A basic model of such a winding would consider currents flowing in one skin depth on the surfaces facing a region with a magnetic field. However, current flow is not perfectly uniform across that surface. As shown in Fig. 10, current is concentrated at the corners of each turn, and also flows on surfaces facing the gaps between turns. Thus, more accurate models are needed for this fundamental geometry. Additional loss effects are important in specific inductor types, and models have been developed for each type of inductor that match finite-element analysis or experiments to within 5% over their intended ranges of application; the match is often much better. First, we discuss two approaches for modeling single-layer windings with side-by-side turns, both of which have proven to be accurate and useful.

1) Improved winding loss model: curve-fit method: Components of the ac losses in toroidal and racetrack windings can be accurately predicted through 2-D finite-element models as shown in Fig. 10 for both inductor geometries. FEA simulations were performed over a wide range of inductor geometries and the resulting ac resistance characteristic was tabulated for each test case. These loss tables, with more than 10,000 entries each, were used to estimate resistances for any geometry within a prescribed range by interpolation [58]. This method enables accurate modeling while providing computational efficiency during the design optimization process.

2) Improved winding-loss model: energy method: Energy methods, which underlie finite-element analysis [60], typically segment space into small regions, and express potential by a simple function over each segment. In our approach, we employ an analytic energy functional that is valid throughout an entire toroid, including the slots between the winding. Such an approach has also been used successfully to analyze electrical machines [61]. The magnetic field in the toroid can be found directly from the minimized energy functional, and from this field, the inductance and surface currents, and thus loss on the inside of the windings, follow directly [62].



(a) Simplified 1D model with radial current path

(b) Actual winding with diagonal current path

Fig. 11. Schematics of a N-turn toroid (top or bottom layer).

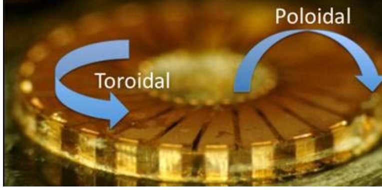


Fig. 12. Toroidal inductor with toroidal and poloidal directions labeled.

B. Special issues in toroids

1) Geometrical effects of diagonal current paths: Fig. 11 shows the winding layout of a N-turn toroid with inner radius r_i and outer radius r_o. The top and bottom layers are symmetric. Fig. 11(a) shows a model based on radial current paths, and Fig. 11(b) shows the actual toroid with diagonal current paths. A simple geometrical factor is used to account for the longer length of the diagonal paths.

2) External currents: As shown in Fig. 12, the winding of a toroidal inductor spirals around the toroid in the poloidal direction as the spiral progresses in the toroidal (circumferential) direction. Thus there are two current components involved: a single-turn toroidal current and a multi-turn poloidal current. At high frequencies, these currents are forced to the surface of the conductors by skin effects. The poloidal currents flow on the inner surface of the winding and terminate the toroidal magnetic flux that travels around the toroid core. The toroidal currents flow on the outer surface of the winding and terminate the poloidal magnetic flux that passes through the donut hole of the toroid. When either of these currents meets the edge of a winding turn, they flow down that edge and become the other current on the opposite side.

Fig. 13 shows a finite-element simulation of the toroidal current component. We have also used the energy method of Section IV-A2 to separately find the external poloidal magnetic fields, their contribution to the inductance, and the losses from their toroidal currents.

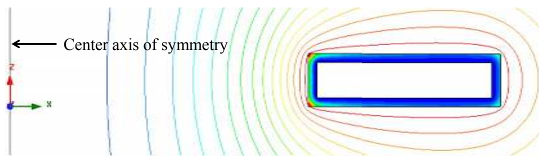


Fig. 13. Finite-element simulation of the toroidal (circumferential) current component in a toroid, which gives rise to a poloidal field. Colored shading in the toroidal winding (shown as a rectangle in this cross section) corresponds to current density; field lines of the poloidal field are shown outside the toroid.

By combining the loss models discussed in Sections IV-A1 or IV-A2 with the two effects discussed above, we obtain accurate winding loss models for toroids.

C. Edge effects in racetrack geometries

Accurate winding loss models for racetrack inductors must consider effects at the outer and inner-most edges of the winding that create unbalanced magnetic fields leading to a different current distribution in each turn of the winding [58], [63]. The finite-element-based loss model described in Section IV-A1 is therefore augmented with a one-dimensional analytical model which uses magnetic field values along the winding edges to predict the current distribution in the winding [63].

The losses along the vertical edges of the winding are then estimated using the analysis in [64] and [65]. The losses along the horizontal edges of the winding are interpolated from the loss table described in Section IV-A1. These two loss components are then superimposed to provide a complete model of the ac winding losses for racetrack inductors [63].

D. Capacitance and Substrate Losses

For parasitic inter-turn capacitance, two cases are considered: the case in which the substrate is insulating, such as for a glass or polymer substrate, and the case in which the turns are near a magnetic core or conducting substrate, such as a silicon substrate. In the former case, a lumped capacitance is placed between each turn. In the latter case, a lumped capacitance is placed from each turn to the substrate or core. All turns are assumed to couple to a common magnetic flux, and hence are treated as a multi-winding transformer [62].

When the inductor is on or embedded in silicon, it is necessary to also model and calculate the additional losses in silicon. These include magnetically-driven losses from induced eddy currents, and electrically-driven losses that result from the spatially-varying potential at each turn. To calculate the electrically-driven losses for a toroid we solve Maxwell's equations in 2-D polar coordinates. To calculate the magnetically-driven losses we assume axial symmetry and solve Maxwell's equations in 1-D [62].

E. Magnetic Core Losses

Losses in the multi-layer Co-Zr-O/Zr-O_2 core include eddy-current and hysteresis loss. Experiments reported in [66], [67] confirm that any other "anomalous" losses in these materials are small. For hysteresis loss we use the simplified approximation introduced in [68] as described in [69]. For eddy-current loss induced by flux parallel to the layers of the Co-Zr-O core, we use the model discussed in [70], [71] that includes displacement currents through the dielectric between layers. In the racetrack design, flux must travel perpendicular to these layers in the region of the "magnetic via" where the top and bottom magnetic layers connect [72]. A model for this phenomenon was developed based on a curve-fit to finite element results, as presented in [58].

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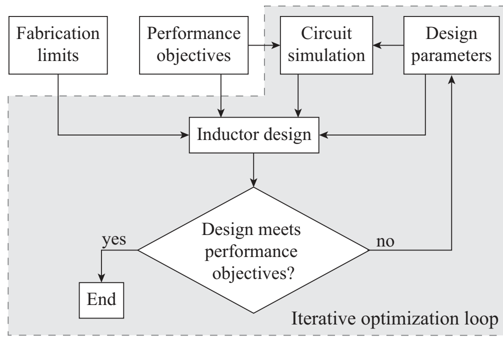

Fig. 14. Co-optimization approach for circuit and inductor designs.

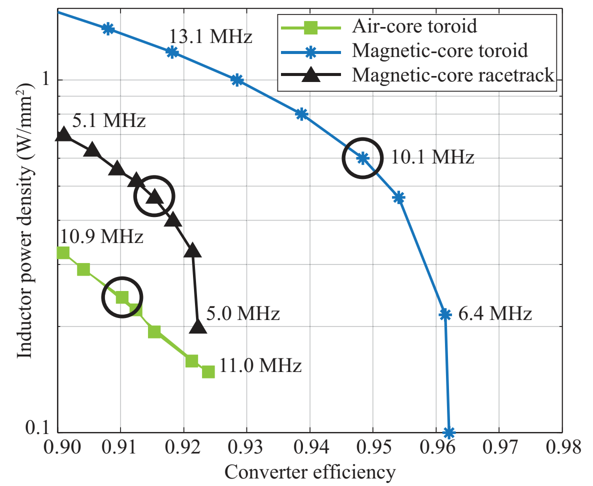

Fig. 15. Design optimization results and Pareto frontiers for three inductor types. Fixed design parameters for each are:
Air-core toroid: overall height $h = 1$ mm, conductor thickness $t_{Cu} = 75$ μm, and spacing $w_{gap} = 50$ μm between turns.
Magnetic-core toroid: $h = 300$ μm, $t_{Cu} = 50$ μm, $w_{gap} = 100$ μm, and total magnetic material thickness $t_{mag} = 80$ μm.
Magnetic-core racetrack: $t_{mag} = 35$ μm in each of the top and bottom cores, $t_{Cu} = 50$ μm, and $w_{gap} = 12.5$ μm. Total height varies between 140 and 180 μm.

V. Co-Optimization of Circuit and Magnetics Design

The models developed in Section IV allow optimization of magnetics designs based on objectives such as minimizing substrate area and maximizing efficiency and constraints such as those arising from the fabrication processes discussed in Section VI. Because the magnetics size and loss depend strongly on the circuit design parameters, and the circuit performance depends strongly on the inductance value and loss, simultaneous optimization of circuit and magnetics parameters is superior to optimizing each separately.

In order to realize this potential we have implemented the models for loss, capacitance and inductance described in Section IV as well as an analysis of the power circuit, in computationally efficient functions in the MATLAB programming language. The use of computationally efficient models permits numerical optimization, using the general co-optimization approach shown in Fig. 14.

For designs using magnetic-core inductors, a particle swarm multi-objective optimization algorithm is employed. Each candidate solution in the search space is assigned a cost C according to the function $C = P_{loss} + Y \cdot V_{ind}$ where P_{loss} is the total power loss in the converter, Y is a weighting factor, and V_{ind} is the inductor volume. The parameter Y is swept over a range of values to assemble a set of Pareto-optimal designs maximizing efficiency and power density.

For air-core inductors, sets of parameters are randomly synthesized for thousands of designs. Next the performance of each design is evaluated. Finally, Pareto-optimal filtering is applied to reduce the feasible design set to those on the multi-objective optimality frontier [73].

The design approach described above was applied to co-optimization of high-frequency regulation stage described in Section II-D and illustrated in Fig. 3 with each of the three inductor types. The results are shown in Fig. 15, where each curve represents a particular inductor technology, and each point of a given curve represents a different inductor geometry and set of circuit parameters optimized for a different trade-off between power density and total losses in the circuit, including the inductor, all for the same converter dc input voltage (100 V) and output voltage and current (35.8 V and 0.7 A). Additional parameters of sample designs from Fig. 15 are shown in Table III. All of the technologies are predicted to be capable of meeting our design objectives of greater than 90% efficiency at high power density. Comparing racetrack magnetic-core inductors to toroidal air-core inductors, we see that the air-core designs are expected to provide better efficiency below 0.5 W/mm^2 power density, but that racetrack designs are expected to provide better power density below 91% system efficiency. Toroidal magnetic-core designs are expected exhibit better performance in both respects, but require more complex fabrication that is in earlier stages of development.

TABLE III
Calculated design parameters for points circled in Fig. 15.

Parameter	Air-core toroid	Magnetic-core toroid	Magnetic core racetrack
Switching frequency (MHz)	10.6	10.1	5.0
Inductance (μH)	1.0	0.51	1.4
Q (at switching freq.)	40	67	42
DC resistance (Ω)	1.0	0.06	0.43
Circuit loss (W)	0.50	0.51	0.66
Inductor loss (W)	1.69	0.84	1.45
Power density (W/mm^2)	0.22	0.60	0.46
Efficiency	91.2%	94.8%	91.5%

To illustrate the advantages of co-optimization of the circuit with the inductor, Fig. 15 includes switching frequencies for representative designs. The different switching frequencies used with the different inductor technologies allow taking advantage of the unique characteristics of each technology to derive the maximum system performance with each.

Within a given microfabricated magnetics technology, cost can be assumed to be proportional to substrate area, so our use of power density as an objective can serve as a proxy for

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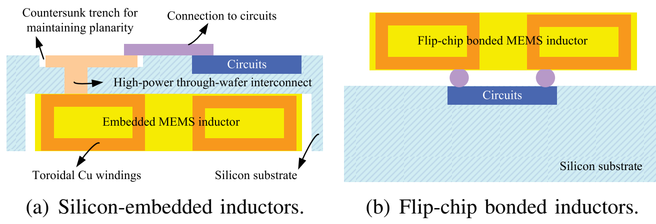


(a) Silicon-embedded inductors. (b) Flip-chip bonded inductors.

Fig. 16. Conceptual renderings of silicon-embedded and flip-chip bonded inductors.

minimizing cost. However, this only applies to comparisons between designs within a given technology. Although cost comparisons between technologies will ultimately be very important, we are unable to estimate cost with any accuracy at this early stage of the technology development.

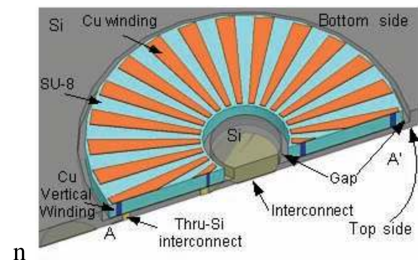
VI. Magnetics Fabrication Methods & Results

A. Air-core toroids

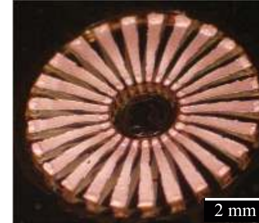
Two general approaches that we have been investigated for microfabricating air-core toroidal inductors are conceptually illustrated in Fig. 16. Both technologies rely on high-aspect-ratio molding and electroplating to form three-dimensional copper windings. The first approach, which emphasizes system compactness, embeds inductors within the volume of a silicon wafer and uses high-power through-wafer interconnects [74], similar to the way a back-side spiral inductor was embedded and connected in [39]. The second approach, which maximizes quality factor on loss-less substrates, uses metal-encapsulated polymer vias to realize high-aspect-ratio vertical conductors [75]. The sample 6-mm-diameter copper-electroplated inductors had 25 turns and heights ranging from 300 to 650 μm.

1) Silicon-embedded toroidal inductors: A CMOS-compatible process for fabrication of 3D toroidal inductors embedded in the volume of a silicon wafer, and capable of interconnection to circuitry on the wafer surface, has been demonstrated [74]. A significant challenge in embedding the structure within the wafer volume was the difficulty of processing inside deep silicon trenches. We overcome this difficulty by means of several key techniques: multilevel wafer etching to form silicon trenches and vias; cavity shaping to facilitate uniform deposition of photoresist; fine proximity lithography to pattern at the bottom of trenches [76]; and laminated dry-film lithography on complex 3D structures. These techniques enabled us to fabricate a 450-μm-tall toroidal inductor in a 300-μm-deep oxidized silicon recess, coupled to the wafer surface with high-power electroplated through-wafer interconnects, as shown in Fig. 17.

2) Toroidal inductors with metal-encapsulated polymer vias: This fabrication technology, which is based on previous work for RF inductors [77], and is now extended to power inductors, results in greatly reduced fabrication time by combining an SU-8 dry film process to create high-aspect-ratio solid polymer vias with metallization of the external surfaces of these polymer vias to create an interlayer conducting path, as shown in Fig. 18(a). The dry film SU-8 via approach provides a magnetic path with high cross-sectional area by allowing large vertical dimensions (0.5–1 mm) with minimal

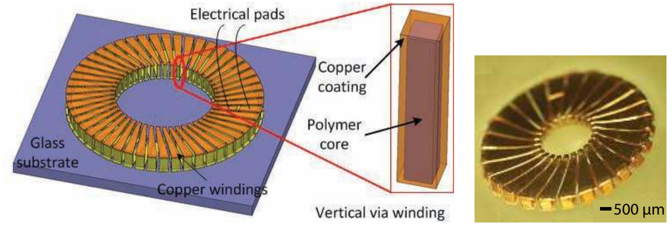


(a) Bottom-view with cross-sectional cut.



(b) Microfabricated and functional silicon-embedded inductor.

Fig. 17. Schematic and image of the silicon-embedded toroidal inductor.



(a) Schematic diagram of a toroidal inductor with metalized polymer vias. (b) Microfabricated and functional inductor.

Fig. 18. Schematic diagram and image of a microfabricated and functional toroidal inductor with metalized polymer vias.

soft baking time compared to solvent casting. It also greatly reduces the electroplating time required to bridge these large vertical dimensions by electrodepositing conducting paths on the outer surface of the SU-8 pillars. A significant challenge in this process is making defect-free pillar arrays and uniform photoresist coatings on these high-aspect-ratio pillars. We overcome this difficulty by means of several key techniques: a back-side UV exposure scheme; fine spray coating; and proximity lithography for simultaneous patterning on the bottom and on the vias. To minimize substrate losses, we microfabricated these inductors on glass substrates. Fig. 18(b) shows a functional 650-μm-tall on-glass inductor.

3) Measurements: Fig. 19 shows the measured and modeled electrical performance of 650-μm-tall on-glass inductors with metal-encapsulated polymer vias. Electrical characterization of the microfabricated inductors was performed with an impedance analyzer (HP 4194). A quality factor as high as 36 at 100 MHz and inductances of approximately 80 nH were measured for test devices. The modeled and measured inductance compare favorably up to 100 MHz. The modeled quality factor, shown by the red solid line, fits well within the measurement error bounds depicted by green dash-dot lines, up to 30 MHz, while the simple skin-depth model under-estimates

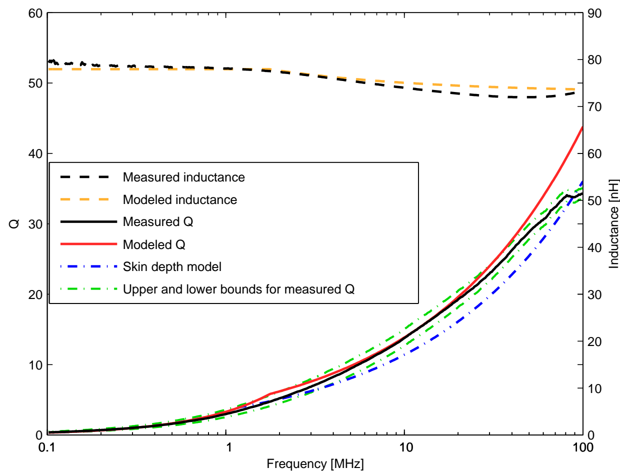
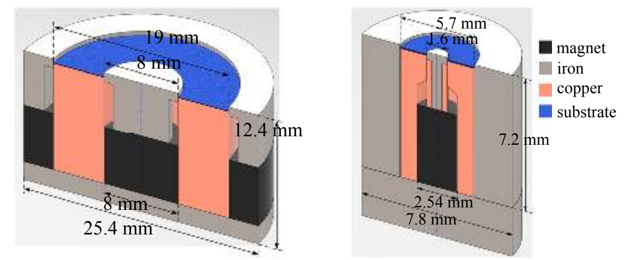


Fig. 19. Comparison of measured inductance and resistance to the predictions of the models described in Sections IV-A, IV-B, and IV-D.



(a) Fixture enabling toroidal core deposition with inner diameter down to 8 mm and outer diameter up to 19 mm, introduced in [59]

(b) Fixture enabling toroidal core deposition with inner diameter down to 1.6 mm and outer diameter up to 5.7 mm, introduced in [79]

Fig. 20. Cross-section view of the magnetic field orientation fixtures for radial-anisotropy magnetic material deposition.

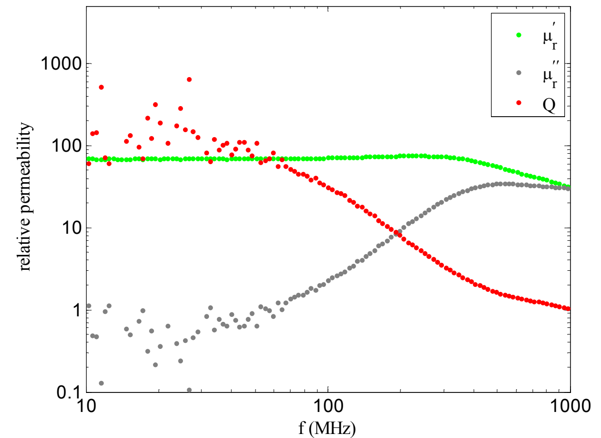


Fig. 21. Measured complex permeability of fabricated thin-film toroidal cores deposited using the smaller fixtures.

the quality of the fabricated inductor.

B. Racetrack fabrication

The microfabrication approach we developed for racetrack inductors (Fig. 9) [58] starts with silicon wafers anisotropically etched in a potassium hydroxide (KOH) solution to produce deep trenches with sloping sidewalls [78]. Next, a thick Co-Zr-O core is sputtered along the bottom and sidewalls of the trenches. A dielectric layer of SU-8 epoxy precedes copper turns electroplated through a negative resist mold. An SU-8 dielectric layer fills the remainder of the trench and the component is planarized. A second layer of magnetic material is sputtered to complete the magnetic path surrounding the windings.

We have processed silicon wafers through various stages of the embedded inductor fabrication sequence to confirm the feasibility of each individual procedure. Magnetic material was deposited and copper was electroplated within deep anisotropically-etched silicon trenches. The use of an anisotropic etch for a flat-bottom trench required adjusting processing parameters to avoid excessive roughness and thereby obtain a smooth surface at the bottom of the trenches.

C. Toroidal magnetic core

Magnetic material with radial anisotropy can be obtained by depositing or annealing in an applied magnetic field with a radial direction. We designed magnetic orientation fixtures to produce a radial field for radial-anisotropy material deposition (Fig. 20) [59], [79]. To minimize perpendicular anisotropy, which could result in poor hysteresis behavior [80], the fixture was designed to produce a field highly parallel to the substrate through the use of iron pole pieces in a configuration optimized by finite-element simulations. The fixture shown in Fig. 20(a) can be used for toroidal deposition with inner diameter down to 8 mm and outer diameter up to 19 mm. The design in Fig. 20(b) uses only one cylindrical magnet and replaces the ring magnet in Fig. 20(a) with an iron piece. This makes it practical to build a smaller fixture for producing smaller radial-anisotropy toroidal cores. To further shrink the fixture size, a "shared-magnet" design was proposed in [79] to allow the use of a small number of magnets to deposit a large array of toroidal samples.

Radial-anisotropy Co-Zr-O thin-film toroidal cores deposited using fixtures in Fig. 20 exhibited the desired anisotropy [59], [79], with a narrow hard-axis hysteresis loop in the circumferential direction, to provide low loss under the excitation used in a toroidal inductor. The real and imaginary parts of the complex permeability were measured with an impedance analyzer (Agilent E4991A) using an approach similar to that described in [81]. Fig. 21 shows the measured complex permeability and quality factor (ratio of real to imaginary permeability) of cores deposited in the smaller fixture. Both sizes of cores (see Fig. 7 in [59] for the larger cores), exhibit good performance (e.g. quality factor >100 and real permeability higher than 60) in the frequency range of interest, below 100 MHz.

D. New Magnetic Materials

Although the Co-Zr-O magnetic material we are now using provides excellent performance, practical thicknesses are lim-

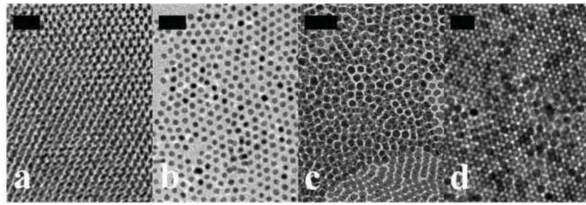


Fig. 22. Magnetic nanocrystals: (a) FePt, (b) $CoPt_3$, (c) $NiFe_2O_4$, (d) $Ni_{\frac{1}{2}}Zn_{\frac{1}{2}}Fe_2O_4$. The scale bar on the upper left in each image represents 20 nm, 20 nm, 60 nm, and 30 nm from (a) to (d).

ited to tens of μm with present deposition technology. New nanocrystal magnetic materials fabricated by wet-chemical processes may offer similar performance characteristics while making thicknesses of 100 μm or more inexpensive to manufacture. Although these materials are in the early stages of development, they offer exciting opportunities.

Magnetic nanoparticles are attractive candidates to be used in inductor cores [82], [83]. Below the critical size, magnetic nanoparticles have a single magnetic domain and become superparamagnetic with zero coercivity at room temperature. The wet chemical synthesis methods allow good control of size, shape, and chemical composition of magnetic nanoparticles. For example, Fig. 22 shows TEM images of monodisperse FePt, $CoPt_3$, $NiFe_2O_4$, and $Ni_{\frac{1}{2}}Zn_{\frac{1}{2}}Fe_2O_4$ nanoparticles. These wet-chemical synthesized magnetic nanoparticles are all capped with organic ligands on the surface, which provides an insulating layer, and therefore can reduce eddy currents. Hysteresis curves for $NiFe_2O_4$ nanoparticles measured by a vibrating sample magnetometer (VSM) confirm soft magnetic properties with low hysteresis, which, combined with low eddy current, is expected to provide low loss for high-frequency inductor cores.

To fabricate magnetic nanocrystal (NC) films with tunable thickness, we have used both dip-coating and doctor-blade methods. Fig. 23a illustrates the steps of the dip-coating method. First, a substrate is dipped into NC solution to build layers of NCs on the substrate. Second, the film undergoes ligand exchange to fix the NC film on the substrate. Finally, the excess ligands are washed away with acetone. The NC solution concentration, dipping speed and time in each step were adjusted to obtain the optimum NC film thickness and uniformity. The thickness of the nanoparticle film was analyzed by Atomic Force Microscopy (AFM), showing a Ni nanoparticle film thickness of 300 nm (Fig. 23a). The dip-coating method is a good way to deposit thin films with various compositions.

An alternative, the "doctor-blade" method, is more convenient for depositing thick and uniform nanocrystal films [84]. This method is simply to scrape out the nanocrystal solution onto a substrate. A thick film can be deposited by allowing the solvent to evaporate and repeating the process multiple times. By repeating the procedure, we formed a 130 μm thick NP film as shown in Fig. 23b.

VII. Nitride Power Device Technology

The targeted development of highly integrated power converters requires greatly improved power switches. We are demonstrating the potential of nitride-based transistors to leapfrog current devices and enable unprecedented performance in integrated power circuits operating at high voltages. The very high critical electric field of GaN (10× higher than in Si), in combination with the high electron mobility (3× higher than in Si) and charge density (2× higher than in Si) enables the fabrication of very compact power switches with specific on resistances potentially >1000× lower than in Si devices (Fig. 24). In addition, the more compact geometry also increases the achievable operating frequency of these switches, potentially into the VHF range (30-300 MHz), allowing important reductions in the dimensions of the passive components.

The substrate on which the GaN structures are grown (SiC, sapphire, Si or bulk GaN) strongly determines the final cost and influences the ability to integrate other components and circuits with the transistors. In this project, we focus on GaN transistors grown on Si (111) wafers. Several companies have recently announced the commercialization of GaN-on-Si devices. However, the performance of these early devices is

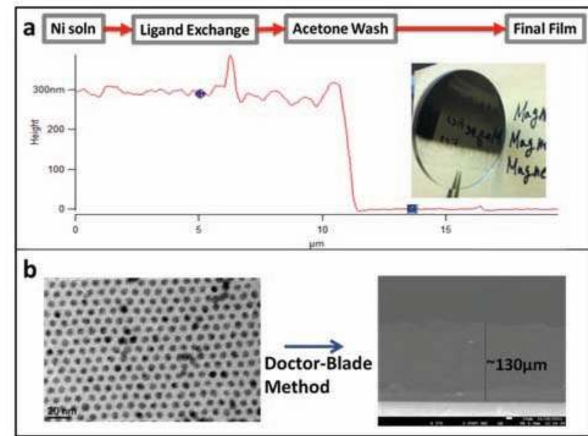


Fig. 23. (a) Schematic procedure of the dip-coating deposition method on the top. The image on the right is the nanoparticle film deposited by the dip-coating method and AFM result shows that the thickness of the film is around 300 nm. (b) 130 μm thick film deposited by the doctor-blade method with 6 nm Ni nanoparticle shown on the left.

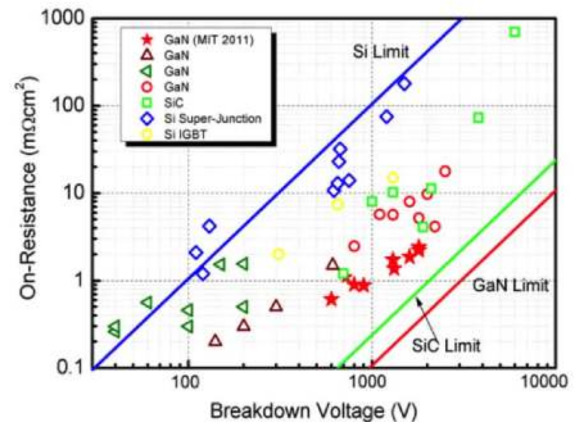


Fig. 24. Specific on resistance (R_{on}) as a function of breakdown voltage (V_{bk}) in Si, SiC and GaN power devices.

still very far from the theoretical maximum. For example, most of the available GaN transistors show critical electric fields of 0.5–1 MV/cm, very far from the maximum fields measured in GaN vertical structures (3 MV/cm). Also, typical contact resistances are 0.4-0.5 Ω·mm, almost one order of magnitude higher than the best values reported for GaN RF amplifiers [85]. In addition, the GaN epilayers used by commercial devices have sheet resistances of 400-600 $\Omega/$sq, much higher than the 200 $\Omega/$sq reported in InAlN/GaN structures [86]. Finally, the on resistance of existing devices increases with switching frequency. This phenomenon, known as dynamic on resistance, severely reduces the efficiency of GaN transistors at high frequencies, which has limited the frequency range over which GaN power circuits are effective. To overcome the challenges that currently limit GaN power devices, we have developed new approaches to improve their performance, focusing on transistors optimized for 200 V to 600 V blocking voltages and enabling switching frequencies to beyond 10 MHz. The device development has been focused on four, highly interdependent, tasks: 1. Increase of breakdown voltage; 2. Threshold voltage control; 3. Reduction of leakage currents; and 4. Study of device reliability. In the subsections below, we describe the main innovations and efforts in each of these tasks.

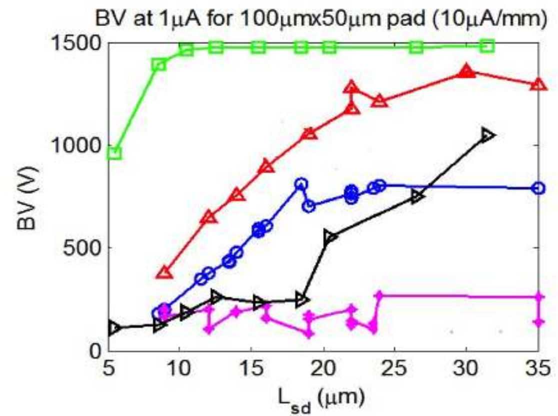


Fig. 25. Buffer breakdown vs length spacing of two isolated ohmic contacts for five GaN samples with different buffer structures. The total epitaxial thickness is 4 μm in all the cases.

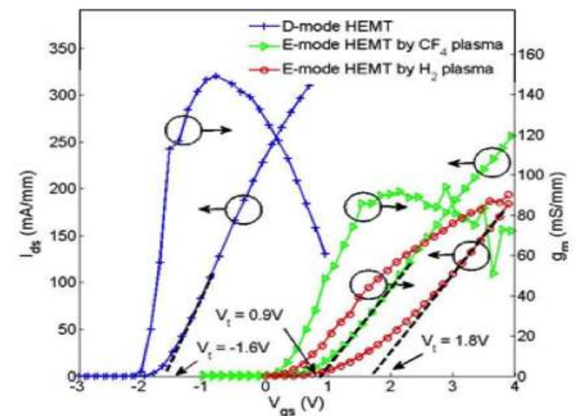


Fig. 26. Transfer characteristics at $V_{ds} = 5$ V of D-mode and E-mode HEMTs treated by H_2 and CF_4 plasma. For the same plasma power level, the shift in the threshold voltage is larger in the case of hydrogen than in fluorine plasma. This indicates that the hydrogen ions are more easily implanted than the fluorine ions, causing a larger change in the band diagram of the transistor

A. Increase of breakdown voltage

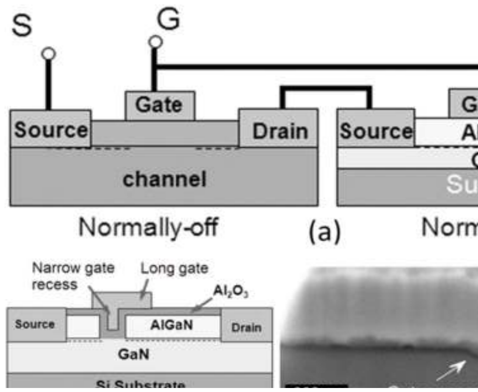
Although the use of Si substrates for GaN growth is preferred from an economic point of view, it also poses challenges in the device fabrication. On one hand, the large lattice mismatch between GaN and Si causes a very high dislocation density ($> 10^9$ cm^{-2}) which significantly increases the leakage current in these devices when compared to their GaN-on-SiC counterparts. This reduces the maximum operating voltage. In addition, because of the lower critical electric field of the Si substrate, there is a trade-off between the breakdown voltage of the transistors and the thickness of the GaN buffer layer. In this project, we have studied the impact of different GaN growth conditions on the total blocking voltage of fabricated transistors, for a given epitaxial thickness. As shown in Fig. 25, the exact buffer structure has a very important impact on the breakdown voltage of the devices. For a given breakdown voltage, it is desirable to have the thinnest possible buffer layer in order to reduce the growth time, wafer cost and bow.

B. Threshold voltage control

Standard AlGaN/GaN HEMTs have very low on-resistance, but also exhibit normally-on behavior (depletion, or D-mode), which is undesirable for power transistors for safety and circuit complexity reasons. Several approaches have been proposed in the past to fabricate more desirable normally-off (enhancement, or E-mode) nitride power transistors, but these methods have challenges such as irreproducibility, instability, gate leakage, and lack of performance data [87], [88], [89], [90], [91]. We have developed two new approaches to fabricate E-mode nitride transistors. Each one of them has the potential to allow high performance E-mode devices, but the combination of two of them in the same device will also improve the robustness of the devices. The two methods are i) Hydrogen-based surface treatment, and ii) dual-gate transistor technology.

1) Hydrogen-based surface treatment: Previous work has shown that enhancement mode operation can be induced in a GaN transistor by applying a F-based plasma to the gate region prior to gate metallization [88]. We found that hydrogen plasma is also able to induce E-mode operation, although the operating principle is different than in the D-mode devices. Hydrogen ions introduced by the H plasma are able to passivate the surface states in AlGaN/GaN structures, which depletes the channel underneath [90]. When the hydrogen plasma is applied in the gate region, prior to the gate metallization, the transistor becomes E-mode with a turn-on voltage of more than 1.8 V (Fig. 26) and more than two orders of magnitude lower gate leakage is observed in the H-treated HEMT with respect to the D-mode devices. These effects are thermally stable if the devices are properly passivated.

2) Dual-gate transistor technology: In parallel to H-plasma treatments, we have demonstrated a new technology that uses



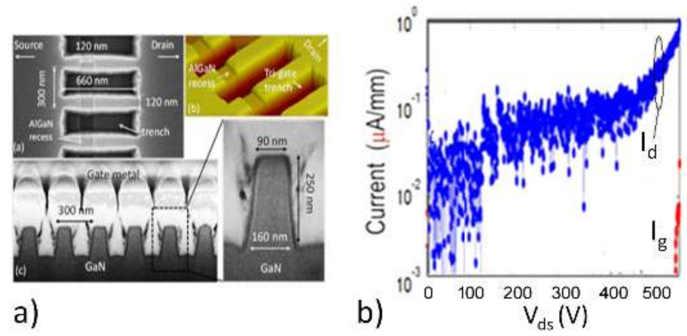


Fig. 29. a) Scanning electron microscope images of the top-view and cross-section of one of the fabricated tri-gate transistors. b) Drain leakage current of a 600-V E-mode tri-gate GaN power transistor [93].

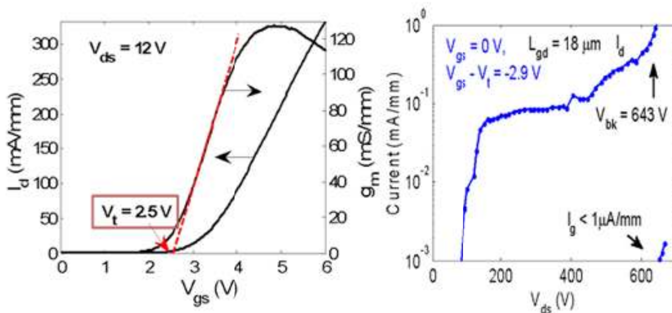


Fig. 28. Current-voltage characteristics of normally-off AlGaN/GaN transistors fabricated by dual-gate technology.

an integrated dual-gate structure to obtain better E-mode AlGaN/GaN transistors. The dual-gate allows the transistor to combine E-mode behavior with low on-resistance and very high breakdown voltage. As shown in Fig. 27, the device utilizes a short E-mode gate to control the threshold voltage and to limit the impact of the high-resistance normally-off region to the total resistance, while a D-mode long-gate structure stands off the high voltage from the drain. Therefore, AlGaN/GaN E-mode devices with high threshold voltage, high current and high breakdown voltage can be fabricated.

Fig. 28 shows the current-voltage characteristics of GaN transistors fabricated with a dual-gate technology [92]. The use of a very short E-mode gate minimizes the on-resistance penalty in these normally-off transistors. In this way, an excellent combination of on-resistance, breakdown voltage and threshold voltage is achieved. In spite of these results, this technology suffers from short channel effects in the E-mode gate, which significantly increases the leakage currents in the off-state as shown in Fig. 28 (right). To overcome this problem, a tri-gate technology was developed as described below.

C. Leakage current control

Traditionally, the breakdown voltage of many GaN-based power transistors has been measured at a drain leakage current of 1 mA/mm. Although this standard is good enough for RF power amplifiers, this current level is too high for power electronics where the devices can have several 100's of mm in total gate width. Approaches like the dual-gate technology introduced in the previous section further increase this problem due to short channel effects. To significantly reduce the leakage current in high voltage transistors it is important to have excellent electrostatic confinement of the channel electrons. For this, we have recently demonstrated a tri-gate technology that divides the transistor channel into thousands of parallel nanoribbons which are then wrapped by the gate electrode both on top and on the sidewalls [93]. This technology, when combined with the dual-gate E-mode technology, significantly reduces the drain leakage current of the transistors as shown in Fig. 29.

D. Device reliability

A key challenge in realizing the potential of GaN for power management applications is electrical reliability. Very little is known at this time about the dominant failure modes of GaN power transistors. Today, when comparing prototype GaN power devices with Si transistors at the same performance level, one finds that GaN exhibits a very significant advantage in terms of size and projected cost [94]. However, the comparison ought to be done also at the same reliability level. There is not enough understanding today to carry out this critical study. Nevertheless, the concern is frequently expressed that without significant reliability improvements, GaN power electronics might fail to reach the market-place [95].

In power switching applications, the switching transistors are designed to operate in two states: the off state (high voltage, very low current) and the on state (low voltage, high current). While the specifics depend on the application, the device is sometimes biased in the off state for relatively long times (order of μs–ms) while during other times it switches on and off rapidly, remaining in the on state for very short times (in the ns range). This brings several reliability concerns.

First, the high-voltage off state condition is known to result in the degradation of the drain and gate currents and an increase in the drain resistance of RF power GaN High-Electron Mobility Transistors (HEMTs) [96], [97]. A mechanism that has been postulated to explain this is defect formation as a result of excessive mechanical stress introduced by the piezoelectric effect [98]. The on condition by itself is not expected to result in significant device degradation. During the transient, however, there is the possibility of high current

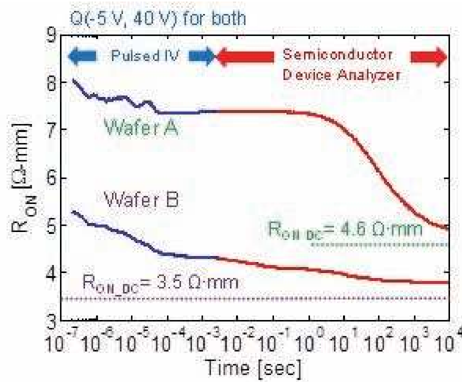


Fig. 30. R_{on} transients from 200 ns up to 10,000 s on GaN high voltage FETs grown on two nominally identical wafers grown by different epi suppliers and processed into devices at the same time in the same lot [101]. Dynamic R_{on} transients obtained after switching from $V_{GSQ} = -5$ V, $V_{DSQ} = 40$ V. The blue lines are obtained from a pulsed IV system and the red lines from a semiconductor device analyzer. Also shown are the DC values of R_{on} obtained after fully detrapping the device. Wafer A shows 73% higher R_{on} at 200 ns than in DC (marked as $R_{on,dc}$) and Wafer B shows a 52% increase.

and high voltage for short times in "hard switching." This will result in self-heating of the device and potentially hot-electron damage, only recently observed in a conclusive manner in GaN HEMTs [99].

The relatively high switching frequency gives rise to a condition known as "dynamic on resistance," or the observation of temporary high values of R_{on} as a result of prominent electron trapping that occurs during the off state [100], [101]. Strictly speaking, this is not a reliability concern, but it is an important device anomaly that gets exacerbated under prolonged off time and high-power electrical stress as a result of trap formation [102]. Our recent studies have shown that dynamic R_{on} in high-voltage GaN FETs can be very severe with short-time scale R_{on} values that are several times higher than $R_{on\text{-}dc}$ [101]. The high dynamic R_{on} values can take many hours to fully dissipate at room temperature (see Fig. 30). The problem also worsens as the off-state voltage increases. Dynamic R_{on} is also activated by hot-electron trapping under high-power conditions that might appear during hard switching. Understanding and solving this problem will require identifying the sources of the traps that are responsible and eliminating them.

While a great deal can be learned about the reliability of GaN power switching transistors from the better established RF-power GaN HEMTs [98], a number of unique issues are to be expected that arise from some significant differences between these two device technologies. A key one is the substrate which is large-area Si in the case of power switching applications while it is smaller diameter SiC in most RF-power-amplifier applications. The use of large area Si wafers brings in concerns related to defects, residual stress, and thermal resistance that are not present with SiC substrates. The increased defectivity of the GaN heterostructure when grown on Si substrates results in enhanced trapping [103]. A second important new issue is related to the presence of a gate dielectric which in power devices is necessary to limit gate leakage current. Since this is not present in standard RF devices, there is limited understanding about reliability issues associated with gate dielectrics on GaN [104]. A third issue is the voltage, which in the case of power switching applications can be large while for RF is typically limited to 100-200 V. High-voltage operation injects concerns about surface and substrate breakdown that are not present in SiC RF devices. These are all new factors about which there is little knowledge at this time and that we are investigating in this project.

VIII. Conclusion

The miniaturization and integration of low-power, high-voltage power electronics targeted in this project is a highly challenging goal. Achieving it requires substantial increases in converter switching frequency, supported by advances in each of three areas: power circuits, devices and passive components. We seek to attain this through coordinated developments in nitride-based power devices; nano-structured magnetic materials and microfabricated magnetic components; and high-frequency power circuits that leverage these elements. The technology approaches we have developed all enable batch fabrication and miniaturization of key components and high degrees of integration. Some of the technology variants further offer subsystem integration (e.g., magnetics embedded in the Si wafer, GaN power devices integrated with Si controls) and the possibility of complete monolithic system integration in the future. More immediately, however, we will construct powerchip systems that meet our performance targets (e.g., power density >100 W/in^3) with hybrid fabrication methods, using available technologies for system-in-package or system-on-package.

While this endeavor is still ongoing, there are a number of lessons that can be drawn from the work to date. It can be concluded that for the high frequencies considered (in the range of 3-30 MHz) there are several viable technology paths to integrated magnetic components that provide the necessary degree of performance, including both air-core and magnetic-core designs. With appropriate component designs, advanced high-frequency core materials can enable decisive advances in achievable efficiency and power density. At the same time, the availability of multiple viable approaches for miniaturized magnetics, including air-core designs that do not depend on core material characteristics, provides flexibility in selecting a fabrication method and the opportunity to take additional system factors into account.

Our success in miniaturizing magnetics has resulted not only from the work in magnetics technology, but also through the approach to the system design. In selecting a topology for the LED driver demonstrator system, we undertook an approach that limited the magnetics requirements, trading them against device component count and other factors. Based on our design results, it appears that designs placing more aggressive requirements on the integrated magnetics (e.g., providing greater voltage transformation and/or isolation) would be viable. Moreover, in seeking effective system designs, co-optimization of the circuit and magnetic component designs has been found to be extremely valuable, enabling us to identify the best

possible combinations of efficiency and power density within topology and fabrication constraints. It is anticipated that co-optimization with the semiconductor devices will likewise be valuable.

Nitride power device development in the PowerChip program also appears promising. Based on the work to date, there appear to be viable paths towards addressing three key device design considerations: enhancement-mode operation, increased breakdown voltage and off-state leakage. Reliability and degradation of nitride-on-silicon devices are much less well understood, but research in this area is a key aspect of our ongoing investigation.

The individual technologies under investigation each play an important role in achieving the sought-after goals, and — importantly — they are synergistic, yielding much more together than their parts. Consequently, is difficult to apportion how the elements contribute individually. Nonetheless, we can make some statements regarding how each technology supports our goals. It is clear that to achieve the desired level of miniaturization and integration, advances in magnetic components are crucial, which is why there is a heavy emphasis on this aspect. As part of this, components incorporating HF magnetic materials have the potential for the greatest degree of miniaturization, making these aspects of the work even more critical. While some program goals are achievable within the constraints of existing semiconductor device technology, this is only true within narrow constraints and with a much greater degree of circuit complexity than is otherwise desirable (e.g., to overcome the voltage and frequency limits of existing devices). The device advances we seek thus offer improvements in size, operating range and simplicity that could not otherwise be achieved. The architecture and circuit design efforts seek to best leverage the capabilities of the available devices and components; these aspects are important in making the targets achievable within present constraints. As the components improve, the circuit strategies are expected to evolve towards providing enhanced performance (e.g., higher efficiency and power factor, wider control ranges, etc.).

Lastly, it may be concluded that development of greatly miniaturized, integrated power electronics in this voltage and power space appears to be within reach, and that such power electronics would have a major impact on numerous applications.

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