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温度変動による利得変化を抑制したCMOS可変利得増幅器

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あらまし　携帯通信機器の中間周波数帯用の可変利得増幅器と直交復調器を 0.25-μm ルールの CMOS プロセスによって試作した．温度変動による利得の変化を避けるために MOS トランジスタの弱反転領域を利用したマスタースレーブ方式の指数変換回路を提案し，利得制御回路に適用した．また，可変利得増幅器には，MOS トランジスタを 2 乗領域にバイアスした増幅器と弱反転領域にバイアスした増幅器を組み合わせることによって，広範囲の可変利得特性を実現した．試作した回路は，電源電圧 2.5 V で，80 dB 分の線形可変利得範囲を達成した．

キーワード　可変利得増幅器，直交復調器，指数変換回路，弱反転領域，符号分割多元接続

A Temperature Stable CMOS Variable Gain Amplifier with 80-dB Linearly Controlled Gain Range

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Abstract　An IF variable gain amplifier (VGA) with a quadrature demodulator (QDEM) is fabricated in a 0.25-μm CMOS technology. In order to avoid the temperature dependence of the gain control characteristic, a master-slave control technique is adopted to the exponential voltage-to-current converters using MOS transistors biased in a subthreshold exponential region. Moreover, the VGA uses both a square-law region amplifier and an exponential region amplifier to obtain the wide gain control range. The experimental results show that the prototype chip achieves an 80-dB linearly controlled gain range with 2.5 V supply voltage.

Key words　VGA, Q-demo, exponential converter, weak-inversion region, CDMA

1 Introduction

A variable gain amplifier (VGA) is an indispensable function block for radio communication systems, and a linear-in-dB variable-gain characteristic is required for CDMA systems.

Prior to this work, a bipolar liner-in-dB VGA and its temperature stabilizing technique with additional temperature dependent current, were proposed [1]. However, the stabilizing technique is sensitive to the device parameters for temperature, and the reported results show that the variable-gain characteristic is still sensitive to the temperature.

In this paper, a temperature-stable, linear-in-dB CMOS VGA with a master-slave control technique is proposed. The master-slave control technique is a kind of feedback technique, and has the advantage of insensitivity to the temperature and device parameters. The experimental results indicate that the proposed technique is effective for a CMOS VGA.

2 Circuit Consideration

Figure 1 shows the block diagram of the test chip. The IF VGA consists of 4 cascoded amplifier stages. The first 2 stages consist of transistors which are biased in the square-law region. The following 2 stages and a mixer input stage of the quadrature demodulator (QDEM) contain subthreshold exponential region transistors as variable transconductance (gm) elements. The required dynamic range of the input stage is very wide, and the square-law region has advantage of a wider liner range. However, the gain control range is small, because the g_m of a square-law region transistor is proportional to the square root of the bias current.

On the other hand, the required dynamic range of the latter 2 stages is smaller than that of the input stage. This smaller dynamic range allows us to use exponential region transistors, which have a larger gain-control range, because g_m is proportional to the bias current.

Figure 2 shows our strategy for design of a gain control circuit, i.e. ,

1. To achieve a wide linear-in-dB control range, an MOS transistor biased in a subthreshold exponential region (M1 in Fig. 2) is used for exponential voltage-to-current conversion in the control and bias block shown in Fig. 1.

2. Temperature dependence of the gain-control characteristic is compensated for by the voltage converter which converts the gain control voltage (V_C) to the gate voltage of the transistor M1.

3. To achieve a temperature-stable gain at $V_C = V_{ref}$ and stable gain-control ratio (ΔdB/ΔV_C) simultaneously, a differential architecture is adopted for the voltage converter, and the common mode output voltage and differential mode gain are independently controlled.

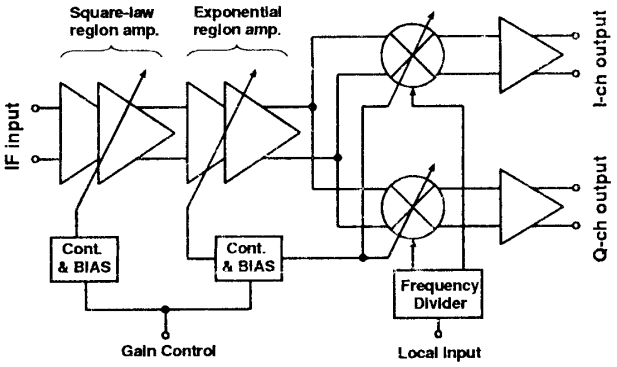

Figure 1: Block diagram of the test chip

2.1 Gain control ratio stabilizing technique:

A master-slave control technique is applied to our gain control circuit, as shown in Fig. 3. The master circuit generates bias voltage V_X, which controls the gain of the voltage converter in the slave circuit. Both voltage converters in the master and slave circuits have a common-mode feedback circuit, as shown in Fig. 4 but omitted in Fig. 3.

The output voltage of the master voltage converter is exponentially converted to an output current with the exponential region transistors M2 and M3. The drain currents of the M2 and the M3 are

$$I_{D2} = I_{ref} \exp\left(\frac{-A_M(V_{ref2} - V_{ref1})}{nV_T}\right)$$

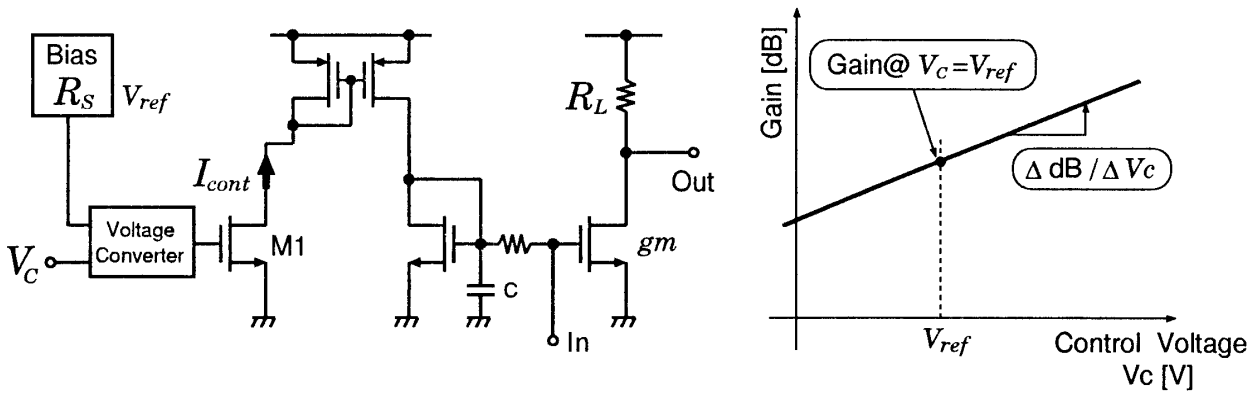

Figure 2: Design strategy of the VGA circuit

$$= \frac{I_{ref}}{\exp\left(\frac{A_M(V_{ref2}-V_{ref1})}{nV_T}\right)} \quad (1)$$

$$I_{D3} = I_{ref}\exp\left(\frac{A_M(V_{ref2}-V_{ref1})}{nV_T}\right), \quad (2)$$

where I_{ref} is the common-mode reference current, shown in Fig. 4, A_M is the differential voltage gain of the master voltage converter, and V_{ref1} and V_{ref2} are reference input voltages.

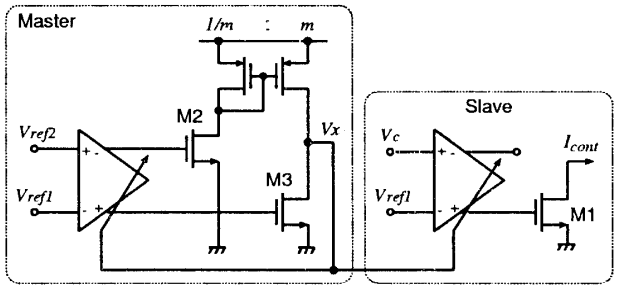

Figure 3: Gain control circuit with master-slave control

I_{D2} is input to the pMOS current mirror circuit and is multiplied by m^2. The output current of the pMOS current mirror circuit is compared and made equal to I_{D3} by a feedback loop. The output voltage V_X is generated and used as a gain control voltage of the voltage converter. The feedback loop sets the gain A_M at

$$\exp\left(\frac{A_M(V_{ref2}-V_{ref1})}{nV_T}\right) = m \quad (3)$$

$$A_M = \frac{nV_T}{V_{ref2}-V_{ref1}}\ln(m). \quad (4)$$

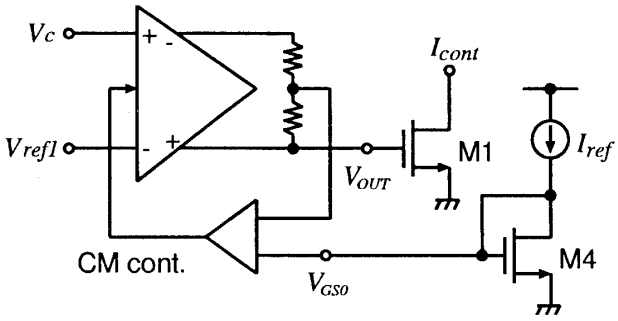

Figure 4: Common-mode feedback for stabilizing gain at V_c=V_{ref}

The slave voltage converter is controlled by V_X. Therefore, the gain is the same as the gain of the master converter. Consequently, The output current of the slave circuit is

$$I_{cont} = I_{ref}\exp\left(\frac{A_M(V_C-V_{ref1})}{nV_T}\right)$$

$$= I_{ref}\exp\left(\frac{V_C-V_{ref1}}{V_{ref2}-V_{ref1}}\ln(m)\right)$$

$$\ln(I_{cont}) = \ln(I_{ref}) + \frac{\ln(m)}{V_{ref2}-V_{ref1}}(V_C-V_{ref1}).$$

The coefficient $\ln(m)/(V_{ref2}-V_{ref1})$ depends on the gate width ratio of the current mirror circuit and the reference voltages. If the reference voltage is temperature insensitive, the coefficient is insensitive to the temperature. It means that the gain control ratio, $\Delta dB/\Delta V_C$, is insensitive to the temperature when the amplifier gain is proportional to the bias current.

Figure 5 is the voltage converter for the master and slave circuits. M5 and M6 are biased in the triode region, and the transconductances of M5 and M6 depend on the voltage between drain and source. This voltage converter has the advantage of a wide liner input range with variable gain [3, 4].

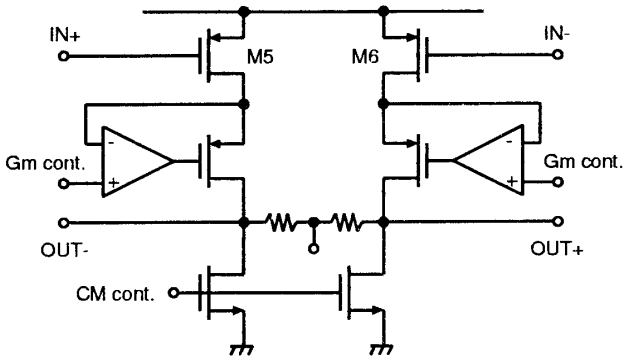

Figure 5: Schematic of the voltage converter used in the master-slave control circuit

2.2 Gain stabilizing technique:

Figure 6 shows a gain stabilizing technique which is applied to our VGA. To focus the principle, the schematic is simplified and a fixed-gain amplifier is indicated. This technique is applicable both to an amplifier using exponential transistors and to an amplifier using square-law transistors. When the transistors M7 and M8 are in an exponential region, the bias circuit operates as a V_T reference circuit. The drain current of M8 is

$$I_{D8} = \frac{nV_T \ln k}{R_S}, \tag{5}$$

where n is coefficient depending on the transistor fabrication, and k is the gate width ratio of M7 to M8. In this case, $k = 4$. The drain current of M10 is the same as that of M8. The transconductance of M10 is

$$g_{m10} = \frac{dI_{D10}}{dV_{GS10}} = \frac{I_{D10}}{nV_T} = \frac{\ln 4}{R_S}, \tag{6}$$

and the voltage gain of the amplifier, G, is

$$G = g_{m10}R_L = \frac{\ln 4}{R_S}R_L. \tag{7}$$

The gain G depends on the resistance ratio, and G is independent of temperature.

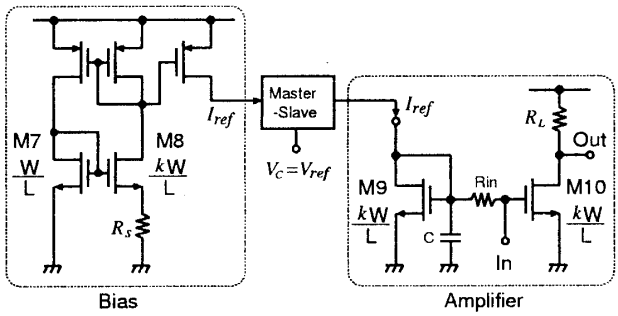

Figure 6: Bias circuit and amplifier for which gain is insensitive to temperature

A similar result is obtained in the case that M7 and M8 operate in a square-law region. Since the drain currents of M7 and M8 are the same,

$$\frac{W}{L}(V_{GS7} - V_{TH})^2 = \frac{4W}{L}(V_{GS8} - V_{TH})^2, \tag{8}$$

where V_{TH} is the threshold voltage. Equation (8) can be simplified as follows:

$$V_{GS7} = 2V_{GS8} - V_{TH}. \tag{9}$$

The drain current of M8 is derived:

$$I_{D8} = \frac{V_{GS7} - V_{GS8}}{R_S} = \frac{V_{GS8} - V_{TH}}{R_S}. \tag{10}$$

The drain current of M10 is the same as that of M8, and the transconductance of M10 is

$$\begin{aligned} g_{m10} &= \left.\frac{dI_{D10}}{dV_{GS10}}\right|_{V_{GS10}=V_{GS8}} \\ &= \left.\frac{d}{dV_{GS10}}\left(I_{D8}\frac{(V_{GS10} - V_{TH})^2}{(V_{GS8} - V_{TH})^2}\right)\right|_{V_{GS10}=V_{GS8}} \\ &= \frac{2}{R_S}. \end{aligned} \tag{11}$$

Consequently, the voltage gain of the amplifier, G, is

$$G = g_{m10}R_L = \frac{2R_L}{R_S}. \tag{12}$$

The gain, G, depends on the resistance ratio, and G is independent of temperature [2].

This temperature stabilizing technique is adopted in our VGA. The reference current is used in generating common-mode reference voltage of the voltage converter as shown in Fig. 4, and the gain at $V_C = V_{ref1}$ of our VGA is insensitive to the temperature.

2.3 Schematic of the amplifiers:

Figure 7 is the schematic of the IF amplifier. It consists of a variable gm input amplifier and a transimpedance output buffer. When the input transistors, M11 and M12, are in exponential region, gm is proportional to the bias current, I_{cont}. When the input transistors are in square-low region, gm is proportional to the square root of the I_{cont}. In both cases, $\log(gm)$ is proportional to $\log(I_{cont})$. The transimpedance output buffer has low input and output impedances, which make the frequency response of the IF amplifier wide and flat. The transresistance of this buffer is approximately the same as the feedback resistance, R_F. Consequently, the amplifier gain is gmR_F, which is the same as that of the amplifier shown in Fig. 6.

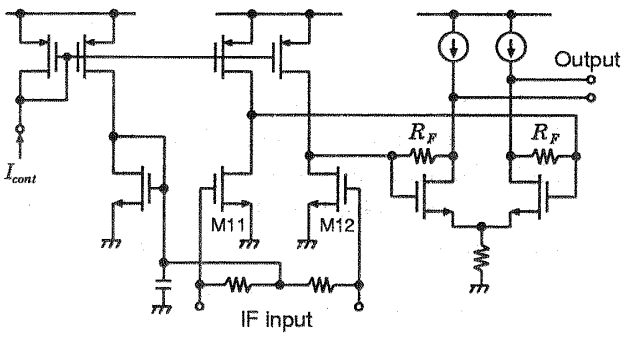

Figure 7: Schematic of the IF VGA unit amplifier

2.4 Schematic of the mixer:

Figure 8 is the schematic of the mixer block. Similar to the VGA circuit, the input transistors, M13 and M14, are in exponential region in order to control the gain. In Fig. 8, the local inputs are 4-phase non-overlapping waveforms. The output buffer circuits utlize a fully balanced circuit [5].

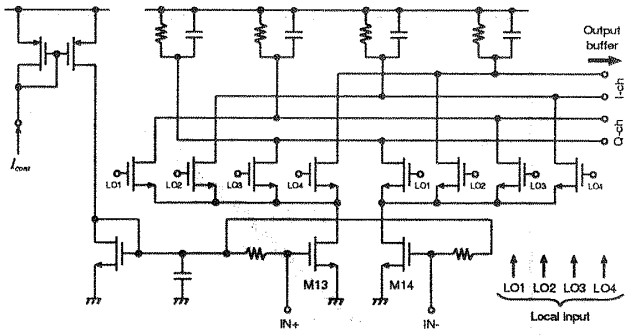

Figure 8: Schematic of the mixer

3 Experimental Results

Figure 9 is the die micrograph of our test chip. The active area occupies 0.7 mm × 0.7 mm.

Figure 10 shows the measured gain control characteristic at temperatures of −33°C, 26°C, and 83°C. As expected, a temperature stable gain and stable gain control ratio are obtained. The gain and the gain control ratio at V_c=1.5 V are 28.7±1.1 dB and 48.5±0.8 dB/V respectively. An 80-dB linearly controlled gain range within ±3 dB error is achieved at 26°C. Figure 11 is a frequency response of the VGA. The dc-decoupling capacitors between each stage limit the lower frequency, and the frequency divider used as a phase shifter in QDEM limits the upper frequency. Other measured results are summarized in Table 1.

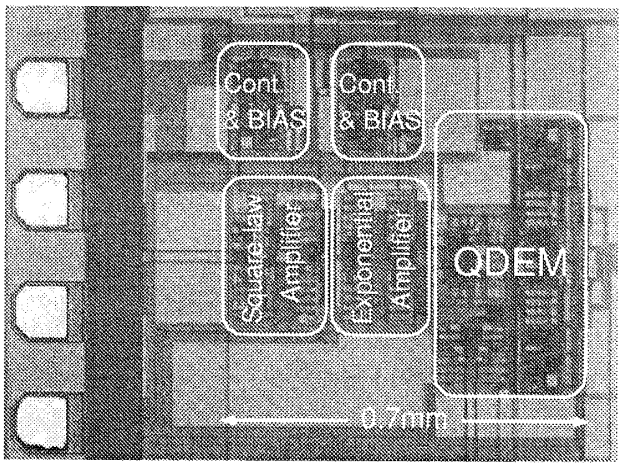

Figure 9: Die micrograph

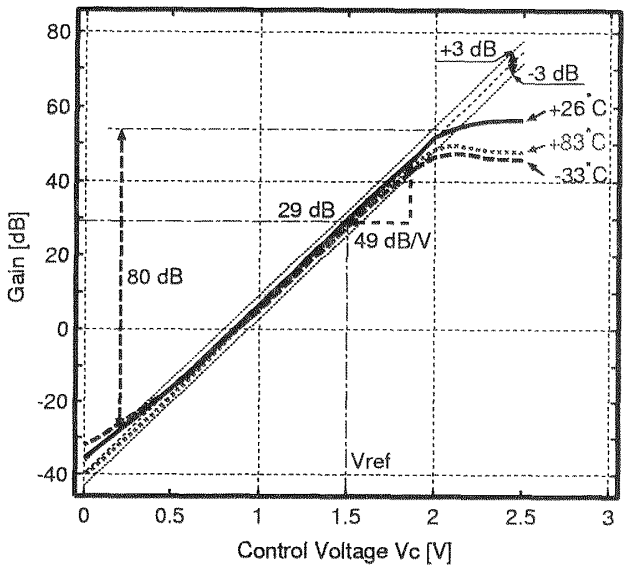

Figure 10: Gain control characteristics at −33°C, 26°C, and 83°C

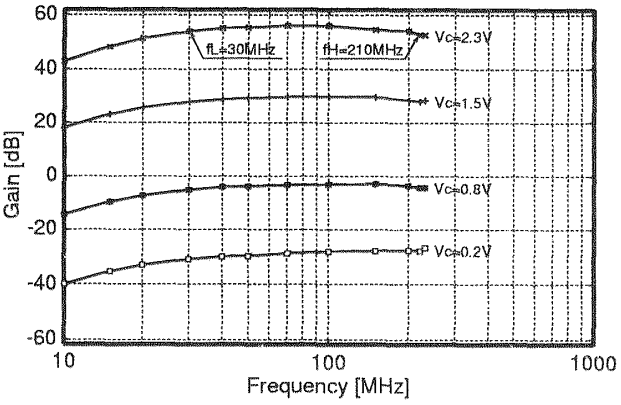

Figure 11: Frequency response of the VGA

Table 1: Performance summary

Power Supply Voltage	2.5 V
Current Consumption	11 mA
Input frequency range	30 ∼ 210 MHz
Gain range	−35 ∼ 55 dB
NF_{DSB} at G_{MAX}	7.6 dB
Input P1dB at G_{MAX}	−40 dBm
Input P1dB at G_{min}	−8 dBm
IIP3 at G_{MAX}	−28 dBm
IIP3 at G_{min}	7 dBm
I&Q Phase error	$< 2°$
I&Q Gain miss match	< 1.0 dB

4 Conclusions

An IF VGA with a master-slave temperature-stabilizing technique is proposed and temperature stability is confirmed from −33°C to 83°C with a test chip. An 80-dB linearly controlled gain range is achieved with exponential voltage-to-current converters using MOS transistors biased in a sub-threshold exponential region. This VGA is suitable for a highly integrated CMOS radio receiver.

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