

A Test Environment for Power Semiconductor Devices Using a Gate-Boosting Circuit

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Abstract—For semiconductor-based pulsed power generators, short turn-on and turn-off times of the employed switching elements are especially in hard switching condition of advantage. In order to enhance switching speeds for standard devices under hard switching conditions, we propose a capacitively coupled gate-boosting circuit with gate drive voltages of up to 80V. A low inductance test circuit has been set up to evaluate different switching elements under varying driving conditions. Beside single pulse operation, the setup allows for burst mode and continuous repetitive switching. The flexible design of the setup allows for testing MOSFETs as well as IGBTs. Exemplary, we show results for a SiC MOSFET and a standard IGBT. By applying 80 V gate drive voltage, the current rise rate of the SiC MOSFET could be increased by a factor of 3.5 up to 2.6 kA/ μ s. For standard IGBT devices we achieved an eight-fold increase in current rise rate to up to 4.2 kA/ μ s. We verified a reproducible pulse shape for over 10^8 pulses. Additionally, the gate drive circuit is able to drive the device in 3 MHz burst mode at 250 A peak collector current.

Index Terms—Pulse power systems, Pulse generation, Pulse circuits, Pulse power system switches, Power semiconductor devices, Insulated gate bipolar transistors, Power MOSFETs

I. INTRODUCTION

WHEN designing semiconductor-based pulsed power generators, the choice of the switching element is important. Whereas silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) are known for their fast switching speed [1], they suffer from increased on-state resistance with increased blocking voltage [2]. Using wide-bandgap semiconductors such as SiC, the on-state resistance can be lowered [3]. As economic alternative for reduced conduction losses, insulated-gate bipolar transistors (IGBTs) may be used [2]. Although their switching speed is lower when compared to MOSFETs, advanced gate drive circuits may reduce switching times [4].

Since datasheets contain experimental results for well defined test circuits only, evaluation tests for different devices specifically tailored to the intended application become necessary prior to circuit design. Especially when operating the devices near or beyond the specified limits, long term experiments can be used to detect slow device degradation [5] and hence to ensure reliable operation of the final generator. In this paper we present a gate drive circuit being able to speed up switching of both MOSFET and IGBT devices. In order to study the switching behavior of the devices under test, we

set up a low inductivity pulse circuit for studies in single pulse, burst and repetitive switching mode. With the obtained information, more precise predictions of the final generator behavior become feasible.

II. EXPERIMENTAL SETUP

A. Gate drive circuit

To achieve fast switching speeds, fast charging of the gate capacitance is important for both MOSFETs and IGBTs. Parasitic inductances in the gate drive circuit cause a time delay for turn-on and turn-off [6]. Additionally, they necessitate a damping resistor ("gate resistor") in series to the gate capacitance to prevent oscillations. The standard gate drive circuit consists of a push-pull stage charging the gate via a gate resistor with a voltage equal to the final gate voltage (for standard IGBTs +15 V to -15 V) [2]. The combination of gate resistor, gate capacitance and parasitic inductance, however, forms a RLC low-pass causing a low rise rate of the gate voltage. One approach for faster gate charging is the so called "gate boosting" [2]. A higher voltage than the final gate voltage is applied to the gate during the charging process for achieving higher gate charging currents. Some authors [2] use two different driving voltages during turn-on and steady-on (e.g. +24 V and +15 V), whereas others propose to discharge a capacitor (charged at +60 V) into the gate and clamp the gate voltage to less than 15 V using a Transient-Voltage-Suppression Diode [7]. These approaches work well, however, the circuit topology is complex and uses additional active elements as compared to a standard push-pull gate drive. The gate drive circuit under investigation in this paper is shown in fig. 1. Therein, the switching element T1 is considered to be an ideal semiconductor switch, whereas its internal components such as gate capacitance C2, parasitic device inductance L1 are drawn as discrete components. The outline of the device package with the external device leads (collector, gate and emitter) is indicated by dashed lines. The gate drive consists of a fast push-pull MOSFET stage (M1, M2; Fairchild FDT86102LZ [8]) receiving the gate signal. V1 represents the gate drive voltage and can be adjusted for experiments between 15 V and 80 V. Once M1 switches on, the gate drive voltage is divided by the damped capacitive divider C1 and the gate capacitance C2. The damping resistors R1, R2 and R3 are used to dampen oscillations that may arise from the combination of the before-mentioned capacitors and parasitic inductances. To compensate for charge loss during long pulses, additional charge is supplied via R5, whereas a maximum gate voltage of 15 V in steady on-state is ensured by the combination of

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D1 and R4. During turn-off, the capacitive divider enables fast discharging of the gate capacitance. In steady-off state, diode D2 prevents unintended gate charging. Therefore, a low resistance path to ground can be created by choosing R2 smaller in comparison to R1. As R1 and R2 also dampen oscillations between the output capacitances of M1 and M2, their lower limit is determined by the parasitic inductances in the layout.

Depending on the switching element under test, the coupling capacitor C1 which determines the final gate voltage V_G has to be adjusted to the driving voltage V_1 and the respective gate capacitance C_2 of the device. The final gate voltage V_G can be calculated according to eq. 1:

$$V_G = \frac{V_1 \cdot C_1}{C_1 + C_2} \quad (1)$$

The coupling capacitor may be adjusted to reach a gate-emitter voltage slightly above the recommended value in the datasheet without any collector-emitter voltage V_2 applied. Thereby, the additional charge required for charging the gate-collector capacitance with rising collector-emitter voltage ("Miller-capacitance") is accounted for. When choosing C1, the gate charge as given in the datasheet must not be exceeded. Otherwise, transient overvoltage may damage the device's gate structure. In the PCB layout of the circuit, special care has been taken with respect to low inductance connections in the gate path - allowing for the smallest damping resistors possible. In addition, a sufficient distance is to be kept from the gate connection to adjacent planes in order to minimize stray capacitances.

Due to the ease of adaptation to different switching elements and the adjustability of the driving voltage, this simple gate drive circuit allows us to study the influence of fast gate charging on different switching elements. To demonstrate the effect of a capacitively coupled gate drive, we chose a standard IGBT in a TO-247 housing with high pulse current handling capability (maximum rated pulse current 320 A - NGTB40N120IHLWG, ON Semiconductor [9]). As emerging technology [3], the second device under test was a fast SiC MOSFET with low conduction losses (C2M0080120D, Cree Inc. [10]) in the same package.

B. Pulse circuit

In some datasheets, values for current rise and fall times are given for an inductive load. We found that the measured switching times in hard switching conditions with a mainly ohmic load vary significantly from the given values. As for fast pulse generators low inductance setup is important, our test environment was designed for hard switching conditions. The setup of the pulse circuit is shown in fig. 2. Capacitor C3 (consisting of several pulse capacitors in parallel) is charged to voltage V_2 (up to 1 kV) via diode D3. Subsequently, switching element T1 is switched on and discharges the capacitor over load resistor R6 and shunt resistor R7. Hence, the measured current pulse is negative with respect to ground. For single pulse experiments, the load resistor consists of several ceramic pulse resistors connected in parallel. In case of repetitive

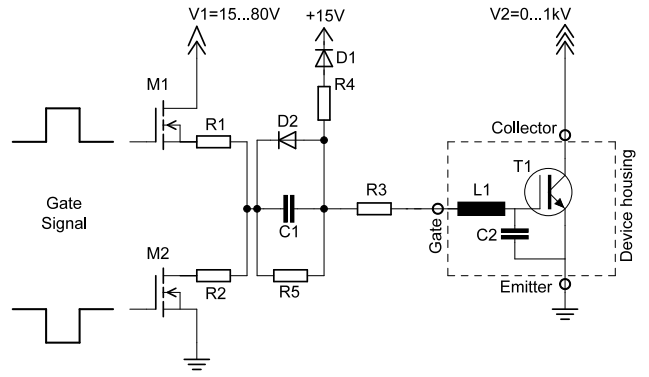


Fig. 1: The gate drive circuit under investigation. Here, the IGBT T1 is considered an ideal semiconductor switch, its internal components such as internal inductance L1 and gate capacitance C2 are shown as discrete components. The physical device housing with the collector, gate and emitter pins is indicated by dashed lines. On turn-on, the MOSFET half-bridge switches the gate drive voltage onto the capacitive divider comprising the coupling capacitor C1 and the gate capacitance C2.

experiments where power dissipation in the load is high, a coaxial water resistor has been used. For cooling, the switching element has been equipped with a water-cooled heatsink whereas the water resistor was immersed in cooling water. The used shunt resistor consists of 30 1Ω SMD resistors

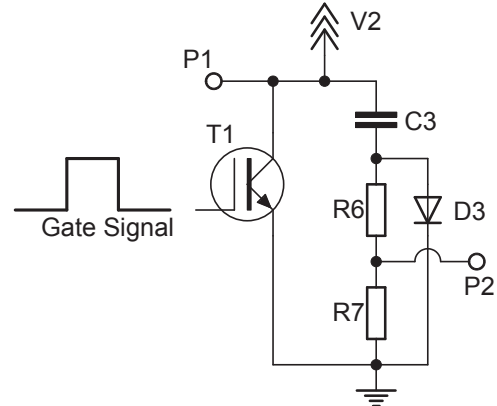


Fig. 2: Schematic of the designed pulse circuit. It is composed of the pulse capacitor C3 being charged to voltage V_2 via diode D3. When switching element T1 is switched on, the capacitor discharges over load resistor R6 and shunt resistor R7, resulting in a negative current peak with respect to ground. The collector-emitter voltage is measured at point P1, the current signal is measured at P2, both with respect to ground.

capable of pulsed overload connected in parallel in a coaxial configuration similar to a shunt resistor presented earlier [11]. Its frequency response is flat up to the measurement limit of 1 GHz. For the experiments with high repetition rate, the shunt resistor was replaced by a current monitor (Pearson type 110). All data was recorded using an oscilloscope with 2 GHz bandwidth (LeCroy WaveRunner 204MXi-A). Voltage has been decoupled by means of high voltage probes with a

rise time of 1.2 ns (Phillips PM8932). The cable propagation time difference between current and voltage measurement was measured to be 2 ns and hence negligible for the presented data. The measured inductance of the pulse circuit (excluding the switching element) was measured by means of a LCR bridge (Hameg HM8118) to be below 60 nH when using the ceramic resistors and below 80 nH when using the water resistor. For the load to be considered ohmic, the rise time of the switching element must be significantly larger than the maximum current rise time τ given as ratio of the circuit's inductance L over the circuit's resistance R (see eq. 2).

$$\tau = \frac{L}{R} \quad (2)$$

Fig. 3 shows collector current and collector-emitter voltage curves for a pulse with a rise and fall time in the order of 50 ns for a resistance of 3.75Ω in the 60 nH circuit (resulting maximum current rise time: 21 ns). As can be seen, both curves are identical and no significant phase lag between current and voltage is observable. Hence, the designed pulse circuit is suitable for experiments under hard switching conditions, if τ is kept sufficiently small.

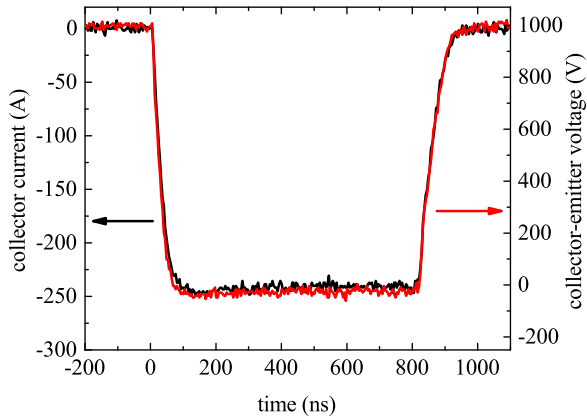


Fig. 3: The negligible phase lag between pulse current and voltage drop over the IGBT verifies the assumption of an ohmic load.

III. RESULTS AND DISCUSSION

A. Single Pulse Experiments

1) *SiC MOSFET*: The gate drive circuit has been adjusted to operate the MOSFET at a voltage across the gate capacitance between 0 V and 20 V. To study the influence of the load current magnitude on the pulse shape, the device was operated at 25 %, 50 % and 80 % of the maximum rated pulse current (80 A [10]). With a constant capacitor voltage of 1 kV, the load resistors were adjusted accordingly. For each current value, the gate drive voltage has been increased in steps of 20 V from 20 V to 80 V whereas the coupling capacitor has been adjusted to achieve 20 V across the gate capacitance. The measurement with 20 V gate drive voltage represents the standard gate drive. For this measurement, the coupling capacitor C_1 according

to fig. 1 has been shorted. In fig. 4 the resulting current measurements are shown for 80 % max. rated pulse current (i.e. 64 A) and varying gate drive voltage. As can be seen, the MOSFET turn-on and turn-off is nearly symmetric in all cases. The slow switching speed as achieved with the standard gate drive can be sped up to a great extent by applying an increased gate drive voltage.

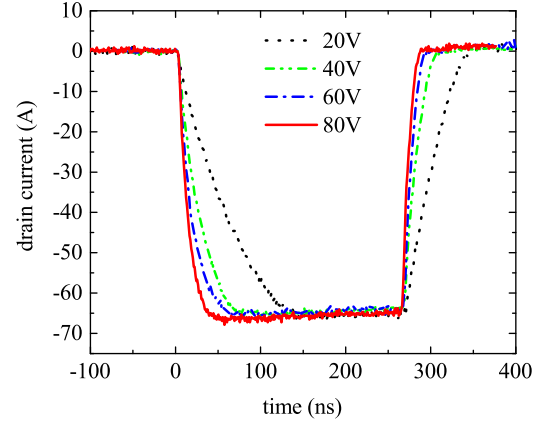


Fig. 4: Pulse shape of the drain current (C2M0080120D SiC MOSFET, 80 % max. rated pulse current) in dependence of the gate drive voltage. Rise and fall time may be decreased by increasing the driver voltage.

Figure 5 shows the dependence of the calculated current rise and fall (inset) times on the gate drive voltages for different currents. The values were obtained using a 90 % to 10 % threshold and averaging over 200 measurements. In comparison with the datasheet values for an inductive load (20 ns rise time, 19 ns fall time [10]) for 20 A (25 % max. current) the achieved 24 ns rise time and 36 ns fall time are significantly higher. For high currents, the switching times are even slower. With increasing gate drive voltage, however, a strong decrease in switching time is observable for all curves. Using 80 V driving voltage, it is possible to decrease the current rise time from 71 ns to 20 ns for 80 % maximum current. The accelerating effect of high driving voltages is more pronounced for high currents than it is for low currents. The achievable current rise rates for 65 A are increased from $0.7 \frac{\text{kA}}{\mu\text{s}}$ at 20 V to $2.6 \frac{\text{kA}}{\mu\text{s}}$ at 80 V during turn-on and from $-1.0 \frac{\text{kA}}{\mu\text{s}}$ at 20 V to $-3.5 \frac{\text{kA}}{\mu\text{s}}$ at 80 V during turn-off. Another beneficial effect of high gate drive voltages is that the rise time dependence on the current is lower, hence, the generated pulse shape has a well defined rise time regardless of the load.

2) *Si IGBT*: For the measurements concerning the IGBT, the gate drive circuit was adapted to achieve 17 V across the gate capacitance without any collector-emitter voltage applied. The resulting current pulse shapes for 250 A (80 % max. rated pulse current) are shown in fig. 6. Especially the current rise time is very susceptible to the gate drive voltage. The rise time is shown in fig. 7. Compared to the SiC MOSFET (fig. 5) which showed a linear decrease in current rise time with gate drive voltage, the IGBT may be sped up to a much greater

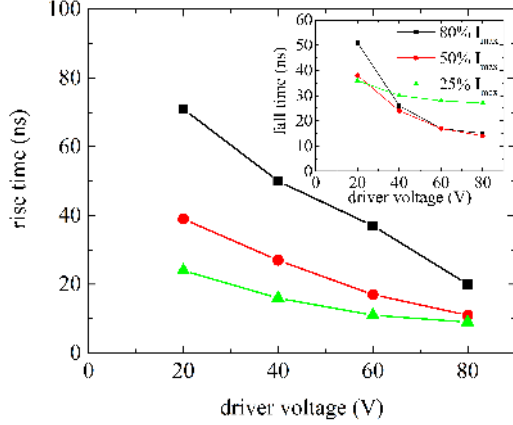


Fig. 5: Current rise times (Inset: fall times) of the SiC MOSFET C2M0080120D with varying driver voltage at 25 %, 50 % and 80 % maximum rated pulse current (i.e. 20 A, 40 A and 64 A) . Whereas the switching times are strongly dependent on the current, increasing the gate drive voltage decreases the switching time in all cases.

extend. For 250 A (80 % max. rated current) a reduction of current rise time from 400 ns to 49 ns and current fall time from 214 ns to 81 ns can be achieved using 80 V drive voltage. The corresponding current rise rates are increased from $0.5 \frac{\text{kA}}{\mu\text{s}}$ at 15 V to $4.2 \frac{\text{kA}}{\mu\text{s}}$ at 80 V during turn-on and from $-1.0 \frac{\text{kA}}{\mu\text{s}}$ at 15 V to $-2.6 \frac{\text{kA}}{\mu\text{s}}$ at 80 V during turn-off.

With the standard gate drive (i.e. "15 V"), the switching time is strongly depended on the current to be conducted. This dependency is significantly weakened for both rise and fall time by applying a high gate drive voltage. This allows for better defined rising and falling edges and, hence, better pulse shaping capabilities of the final generator when using a variable load.

For even faster switching, connecting several devices in parallel is an option. Both devices, MOSFET and IGBT, seem suitable for parallel operation with the proposed gate drive. As a device carrying a lower current switches on faster and off slower, this negative feedback is likely to counteract current sharing imbalances between parallel devices during switching operation.

B. Repetitive mode

For high speed pulse generators, a reliable pulse shape is important. Not only pulse-to-pulse variations have to be avoided, but also device degradation over the life time of the pulse generator is an issue. Comparing the device performance over many pulses, other authors could quantify the device degradation [5]. Whereas our gate drive circuit operates within the specified values (max. 25 V across the gate capacitance for the MOSFET [10], 20 V for the IGBT [9]), the stress on the gate leads is significantly higher due to the higher gate charging current. Therefore, our test setup includes the possibility to operate the device under test for extended periods of time in repetitive mode. To cope with the increased power

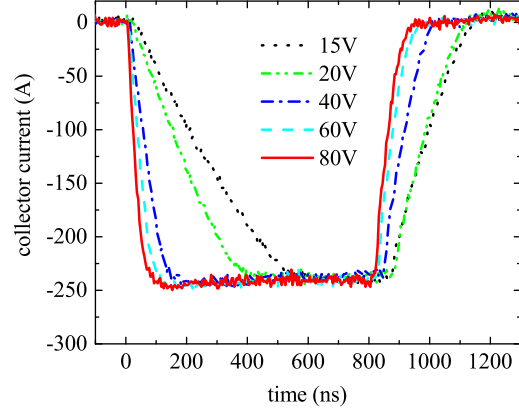


Fig. 6: Pulse shape of the collector current (NGTB40N120IHLW-D, 80 % max. rated pulse current) in dependence of the gate drive voltage. Especially the current rise time can be reduced significantly by applying a high gate drive voltage.

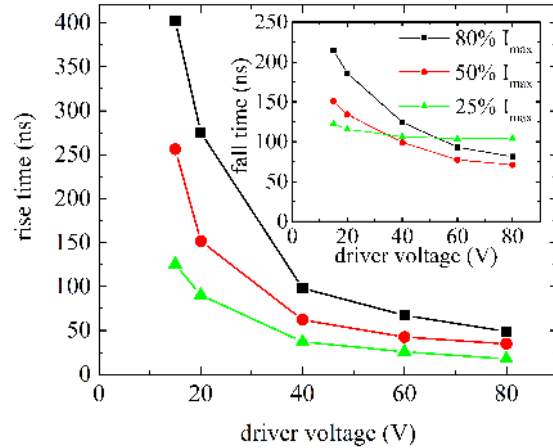


Fig. 7: Current rise times (Inset: fall times) of the IGBT NGTB40N120IHLW-D with varying driver voltage at 25 %, 50 % and 80 % maximum rated pulse current (i.e. 80 A, 160 A and 250 A). Compared to the results for the SiC MOSFET, the increase in switching speed is much more pronounced. In addition, the variation of the current rise and fall time with the conducted current becomes smaller.

dissipation at high repetition rates, a water-cooled heatsink has been used. Its thermal resistance has been measured to be $0.18 \frac{\text{K}}{\text{W}}$ (case-to-water).

The measurements for the IGBT have been conducted with a pulse length of 250 ns, a maximum current of 250 A at a repetition rate of 3 kHz. The gate drive voltage was set to maximum, i.e. 80 V. In order to demonstrate the stability of the pulse shape, 10^8 pulses were recorded, corresponding to 10 h of operation at 3 kHz.

The resulting graph is shown in fig. 8. Plotted is the current

pulse shape at the beginning of the measurement together with the pulse shape 10 h later. As can be seen, both traces are identical within the resolution of the measurement. Therefore, the excellent pulse reproducibility and device stability over 10^8 pulses is verified. A much longer operation time is necessary to exclude device degradation, however, the setup can now be used for long term experiments.

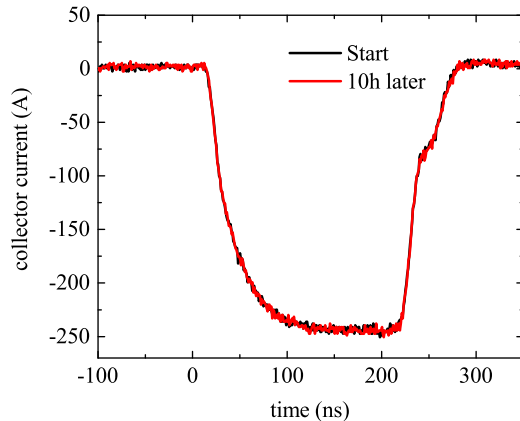


Fig. 8: Collector current pulse shape of the IGBT (NGTB40N120IHLW-D, 80 % maximum rated pulse current) before and after 10 h of continuous pulsing at 3 kHz switching frequency. The identical curves show pulse shape stability over 10^8 pulses.

The gate drive circuit is able to drive a device much higher frequency than the previously presented 3 kHz. Especially since many pulse generators are to perform fast pulse shaping [12], the maximum switching frequency in burst mode is important. With the IGBT under test we were able to achieve a maximum switching frequency of 3 MHz (50 % duty cycle) at a peak current of 250 A in a single device in burst mode. The resulting current trace is displayed in fig. 9.

IV. CONCLUSION

In this paper, our test setup for a capacitively coupled gate drive was presented. The first results have proven the flexibility of the gate drive to speed up both SiC MOSFETs as well as Si IGBTs as compared to the standard gate drive in hard switching conditions. In case of the IGBT an increase in current rise rate by a factor of 8 has been observed. The test environment thereby comprises possibilities for single pulse, burst and long term repetitive measurements. In the future, the setup will be used to benchmark new semiconductor devices for their usability in fast semiconductor-based pulse generators as well as to study the long term stability of those switching elements. Although we have not found any hints suggesting that device degradation or batch-to-batch variations influence the presented results of the tested devices, we now have the ability to identify potential problems prior to designing pulse generators.

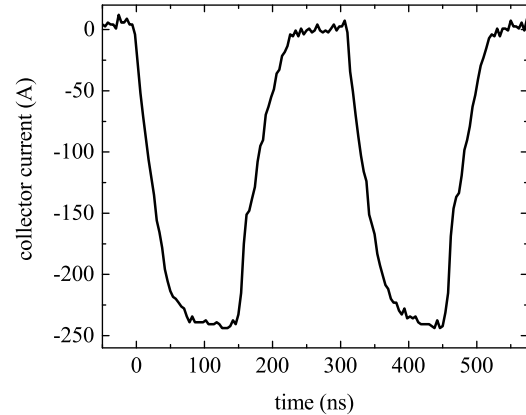


Fig. 9: Collector current of the IGBT (NGTB40N120IHLW-D, 80 % maximum rated pulse current) in 3 MHz burst mode. The device under investigation is, hence, suitable for reliable, fast repetitive switching when employing the proposed gate drive circuit.

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