A Test Time Theorem and Its Applications

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***Abstract*—We prove a theorem stating that the test time of digital test is obtained upon dividing the total energy dissipated during test by the average rate of consumption or power. As we try to reduce the test time, the critical path delay (structural constraint) and the peak power capability of the circuit (power constraint) limit our capability to increase the rate of energy consumption. The theorem leads to two modes of testing, namely, synchronous and asynchronous. Supply voltage plays a significant role in optimizing the test time.**

I. Introduction

Custom VLSI cores like microprocessors, digital signal processors and memories have long test sequences. Modern system-on-chip (SoC) devices containing many such cores are tested using scan and these tests run through a very large number of clock cycles. A long test time has a direct impact on the manufacturing cost [2].

Attempts at compacting tests usually result in non-functional tests, higher circuit activity and increased power consumption. If the power during test exceeds the power consumed during the normal functional operation for which the circuit was designed, then a good circuit can fail or even be damaged. Therefore, tests are often applied at a rate that is slower than the functional clock speed. This increases the test time.

Reducing test time and controlling test power are conflicting goals and therefore optimization of testing for both attributes is challenging. This topic has been addressed in the recent literature [3], [4], [5].

In this paper, we analyze a recently introduce idea of testing with a clock whose period is adjusted asynchronously to control power dissipation. Our objective is to minimize the test time. A theoretical analysis shows that the test time is minimized by a proper selection of the supply voltage that influences both the energy of test vectors and the critical path delay of the circuit.

II. Prior Work

Dynamic control of clock frequency for reducing the test time and power consumption for built-in self-test (BIST) and for externally applied test has been recently demonstrated [6], [7]. The idea of asynchronous testing was introduced at the LATW in 2012 [1]. Simulation results have shown the feasibility of this idea [9], [8]. Recent papers show that voltage reduction can increase the speed of power constrained synchronous testing [10], [11].

The research reported in this paper analyzes asynchronous testing, derives formulas and procedures for minimizing test time, shows voltage as a key parameter in the optimization process, and demonstrates the optimized synchronous testing to be a special case of the generalized asynchronous testing.

III. A Test Time Theorem

We consider a circuit under test (CUT) that may be designed for testing with or without scan. In either case it is synchronously tested with a single constant frequency clock. The test time is a product of the clock period and the total number of test cycles. For large circuits, the number of test cycles is large and test time is a cost concern. Hence, there is a great need to study and minimize the test time.

In the following discussion, we assume that dynamic energy and power that include the consumption due to transitions (function, glitch and short circuit) dominates and that due to leakage is negligible.

Theorem 1 – The test time (TT) for a synchronous test is given by,

$$TT = \frac{E_{TOTAL}}{P_{AV}} \tag{1}$$

where E_{TOTAL} is the total energy consumed and P_{AV} is the average power during the entire test. For technologies where leakage is significant, the leakage power is subtracted from the denominator.

Proof – The test time of a synchronous test is,

$$TT = N \times T_{test} \tag{2}$$

where N is the number of clock cycles required to run the test and T_{test} is the period of test clock. Suppose E_i is the energy consumption of ith test cycle, then

$$E_{TOTAL} = \sum_{1}^{N} E_i = \frac{TT}{N} \sum_{1}^{N} \frac{E_i}{T_{test}} = TT \times \frac{1}{N} \sum_{1}^{N} P_i \tag{3}$$

Proc. 14th IEEE Latin Aemrican Test Workshop, Cordoba, Argentina, April 2013 978-1-4799-0597-3/13/$31.00 ©2013 IEEE

because $E_i/T_{test} = P_i$, the power dissipation in ith cycle. But, the average power is,

$$P_{AV} = \frac{1}{N}\sum_{1}^{N} P_i \tag{4}$$

Therefore,

$$E_{TOTAL} = TT \times P_{AV} \tag{5}$$

which proves the statement of the theorem. ■

Theorem 1 points to the total energy as a fundamental characteristic or an "invariant" of the test. The test time then depends on the rate (or power) at which the energy is consumed. To minimize the test time, testing should dissipate the energy at the maximum average rate, i.e., use as small a clock period as possible. However, the test clock is constrained by the circuit structure (critical path delay) and the circuit's ability to consume power:

1) Structural constraint: The period of a structurally constrained clock must not be shorter than the critical path delay of the circuit. The fastest operation occurs when the clock period equals or barely exceeds the critical path delay. We define the fastest structurally constrained clock as $f_{structure} = 1/T_{structure}$, where $T_{structure}$ is the critical path delay.
2) Power constraint: The physical design of a VLSI chip is carried out to support the power dissipation during the functional operation. Tests that are often nonfunctional are found to consume more than the functional power. Even though the functional operation uses the fastest structurally constrained clock, the test clock may have to be slower to limit the power dissipation during test. We define the fastest power constrained clock frequency as $f_{power} = 1/T_{power} = P_{PEAKfunc}/E_{MAXtest}$, where $P_{PEAKfunc}$ is the peak power during a cycle consumed in functional operation and allowed by the physical design of CUT and $E_{MAXtest}$ is the maximum energy dissipated during any test cycle.

The critical path chosen can vary based on the operating mode. For instance, the test cycle can be either in scan shift mode where the critical path delay will be between two scan registers, or in capture mode where the delay is determined by the functional critical path, or in scan enable mode when the critical path will be the time taken for the rising/falling transition of scan enable signal to reach all the scan flip flops.

To minimize the test time, we find the shortest test clock period as,

$$T_{test} = \max\{T_{structure}, T_{power}\} \tag{6}$$

For power constrained testing, $T_{power} > T_{structure}$ and therefore,

$$T_{test} = T_{power} = \frac{E_{MAXtest}}{P_{PEAKfunc}} \tag{7}$$

The maximum energy (numerator) dissipated in a test cycle is a property of the test and the peak functional power (denominator) is a property of the circuit. For a given circuit, therefore, the test time is reduced by tests that do not necessarily consume less energy, but actually consume less maximum per cycle energy because from Equations (2) and (7),

$$TT = N \times \frac{E_{MAXtest}}{P_{PEAKfunc}} \tag{8}$$

Test vectors can be modified to reduce $E_{MAXtest}$ but that is often found to increase the number N of test vectors. In this paper, we address the question: Given a test characterized by N and $E_{MAXtest}$ and a circuit characterized by $T_{structure}$ and $P_{PEAKfunc}$ how can we minimize the test time? We consider two scenarios.

IV. Synchronous Test

The first scenario is *synchronous test*, where entire test is performed with a constant clock frequency $f_{test} = 1/T_{test}$. For a test of N clock cycles, we wish to minimize the test time (TT) as given by Equation (2).

The test clock period, T_{test}, is a controlling parameter of the test. It is given by Equations (6) and (7), and depends on three quantities:

1) $T_{structure}$, the critical path delay of the circuit.
2) $E_{MAXtest}$, the maximum energy consumed by any clock cycle of the entire test.
3) $P_{PEAKfunc}$, the peak power per cycle that the circuit is designed for.

According to the normal practice, testing is done at some specified nominal supply voltage. As discussed in Section III, the test clock is generally slowed down because testing is power constrained, i.e., $T_{power} > T_{structure}$. Suppose we reduce supply voltage at which the test is performed, causing a quadratic reduction in $E_{MAXtest}$ without changing $P_{PEAKfunc}$. According to Equation (7), T_{power} and hence T_{test} reduce. At the same time the reduced supply voltage slows down the critical path increasing $T_{structure}$. We can continue to reduce the voltage as long as the operation is power constrained. Once $T_{structure}$ exceeds T_{power}, the operation becomes structure constrained and according to Equation (6), T_{test} starts increasing. T_{test} attains its minimum value at supply voltage for which $T_{power} = T_{structure}$. Thus, for fastest testing supply voltage should be reduced such that maximum power consumption per cycle during test equals the specified functional power requirement $(P_{PEAKfunc})$ when test clock is fastest that the critical path would allow.

TABLE I
MINIMUM TEST TIME SYNCHRONOUS TEST OF ISCAS'89 CIRCUITS IN 180NM CMOS [11].

Circuit name	Total scan test cycles N	Peak per cycle power $P_{PEAKfunc}$ (W)	Nominal voltage test, $V_{nom} = 1.8$V		Optimum voltage synchronous test			Test time reduction
			Test frequency $f_{1.8V} = \frac{E_{MAXtest}}{P_{PEAKfunc}}$ (MHz)	Test time $N/f_{1.8V}$ (μs)	Supply V_{sync} (Volts)	Test frequency $1/T_{structure}$ (MHz)	TT_{sync} $N \times T_{structure}$ (μs)	(%)
s298	498	0.0012	187	2.66	1.072	511	0.971	63
s382	704	0.0029	300	2.34	1.34	500	1.41	40
s713	809	0.0027	136	5.89	1.38	227	3.56	40
s1423	4649	0.0045	141	33.00	1.72	155	29.89	10
s13207	41266	0.0213	110	375.00	1.44	170	242.00	35
s15850	67624	0.1781	182	371.56	1.68	174	388.00	12
s38417	181536	0.0737	122	1491.90	1.52	170	1064.00	29
s38584	186159	0.1106	129	1443.09	1.50	187	995.50	31

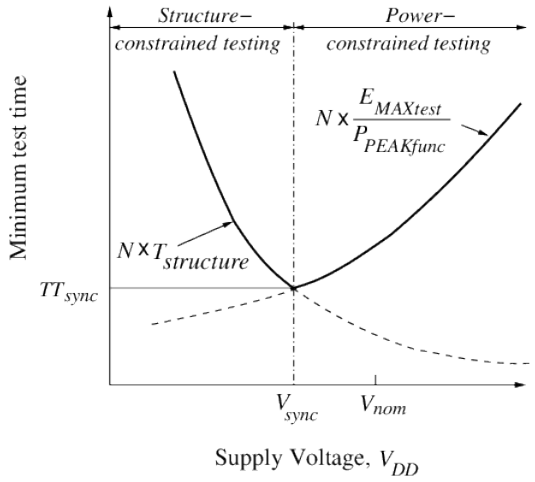

Fig. 1. Minimum test time as a function of supply voltage (V_{DD}) for N-cycle synchronous testing. For a minimum test time TT_{sync} supply voltage is V_{sync}, which is lower than the nominal voltage V_{nom}.

Thus, for synchronous testing at the optimum supply voltage for which,

$$\frac{E_{MAXtest}}{T_{structure}} = P_{PEAKfunc} \tag{9}$$

the minimum test time is given by,

$$TT_{sync} = N \times T_{structure} \tag{10}$$

This is illustrated in the sketch of Figure 1. It is assumed that at some nominal voltage (V_{nom}), e.g., 1.8V for 180nm CMOS technology, the testing is power constrained and the minimum test time is given by Equation (8). As voltage is reduced, $E_{MAXtest}$ drops but $T_{structure}$ increases until at some optimum voltage, shown as V_{sync} in Figure 1, the condition of Equation (9) is satisfied and testing just becomes structure constrained. For all lower voltages the minimum test time increases with $T_{structure}$.

Table I shows the results of optimized test obtained by an analytical procedure [11]. These results have been verified by Spice simulation [10].

Next, we ask can test time be further reduced? The following section discusses a possibility.

V. ASYNCHRONOUS TEST

In the synchronous test scenario of Equations (9) and (10), the test time of an N cycle test depends on the critical path delay. If we increase the supply voltage the circuit can speed up, thus reducing $T_{structure}$. However, then some high energy cycles will exceed the power budget $P_{PEAKfunc}$. Therefore, the synchronous testing cannot speed up any further.

From Theorem 1 of Section III, test time (TT) is minimum when P_{AV} is maximum. For any positive-valued function, the average value is maximum when the function holds a constant value. In that case, the constant value of the function is also the average. However, the specified maximum power $P_{PEAKfunc}$ should not be exceeded during test. Therefore, an optimum solution to the minimum test time problem would be to dissipate the test energy E_{TOTAL} at a constant rate $P_{PEAKfunc}$.

The above condition is achievable by asynchronous testing in which the clock period is customized for ith cycle as,

$$T_i = \max\{T_{structure},\ \frac{E_i}{P_{PEAKfunc}}\} \tag{11}$$

where E_i, $i = 1, 2, 3, \ldots, N$, is the energy consumption during ith clock cycle. Of course, T_i must not be shorter than $T_{structure}$ or the critical path delay.

Equation (11) classifies each cycle i as being either structure constrained ($E_i \leq T_{structure} \times P_{PEAKfunc}$) or power constrained ($E_i > T_{structure} \times P_{PEAKfunc}$). All structure constrained cycles are clocked synchronously with period $T_{structure}$ and periods of all power constrained cycles are

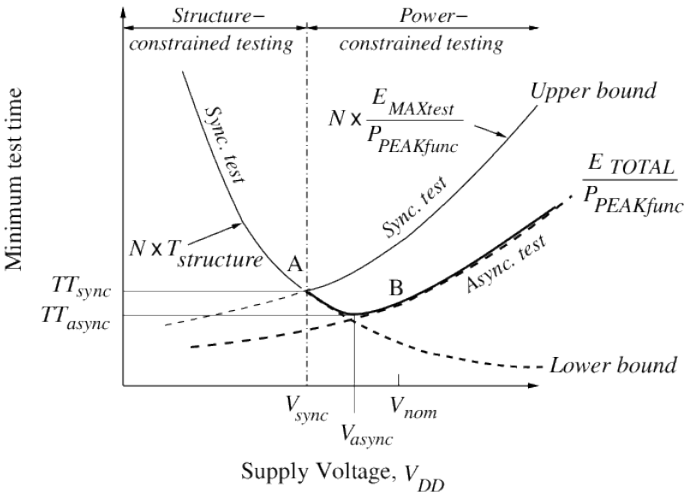

Fig. 2. Minimum test time as a function of supply voltage (V_{DD}) for N-cycle asynchronous testing. For minimum test time TT_{async}, supply voltage is V_{aync}. $TT_{async} \leq TTsync$ and $V_{sync} \leq V_{async} \leq V_{nom}$.

expanded asynchronously to stay within the power budget $P_{PEAKfunc}$. The test time (TT) is, therefore, bounded as

$$\max\{N \times T_{structure}, \frac{E_{TOTAL}}{P_{PEAKfunc}}\} \leq TT_{async} \tag{12}$$

$$TT_{async} \leq TT_{sync} = N \times \frac{E_{MAXtest}}{P_{PEAKfunc}} \tag{13}$$

The lower bound is the same as the best test time for synchronous testing (see Equation (9)) and will be achieved if all cycles consumed small amount of energy and therefore were structure constrained. The upper bound is due to Theorem 1 of Section III and becomes valid when all cycles consume high energy at the maximum allowable rate ($P_{PEAKfunc}$) achieved by appropriately stretching the clock periods (i.e., are power constrained). In this case, $P_{AV} = P_{PEAKfunc}$. Both limiting cases are according to Equation (11).

The minimum test time for an asynchronous test is sketched in Figure 2 for varying supply voltages. Here, point A indicates the optimum synchronous test. The bounds of Equations (12) and (13) are valid to the right of point A. Between A and B, the testing is mixed but many cycles are still structure constrained and, in general, a test would contain both types of cycles, namely, structure constrained and power constrained. As we move to to right of A, energies of all cycles increase. Still, the periods of low energy cycles shrink because they have not become power constrained. High energy cycles remain power constrained and their periods expand. On balance, the test time reduces if the test contains a majority of low energy cycles. As we further increase the supply voltage, cycles that were structure constrained start becoming power constrained. Hence, their periods no longer shrink but start expanding. Thus, an optimum voltage is found such that the test time of asynchronous testing is minimum. This voltage is shown as V_{async} in Figure 2 and can be, in general, above or below V_{nom} depending on the characteristics of test vectors and the circuit. However, $V_{async} \geq V_{sync}$ always.

As we move to the right of point B, testing tends to become fully asynchronous and the test time equals the lower bound of Equation (12).

Because synchronous testing is a special case of asynchronous testing, in general, the latter will provide a lower test time. This work is in progress and we should soon have the results.

Figure 3 shows the test time for the s298 benchmark included in Table I. The method used to find synchronous test times for the tests of Table I is described in a recent paper [11]. The method for calculating the asynchronous test time is based on the discussion of Section V and will be detailed in a forthcoming paper. For synchronous testing, the minimum test time is $TT_{sync} = 0.971\mu$s at $V_{sync} = 1.07$V. For asynchronous testing, $TT_{async} = 0.770\mu$s at $V_{async} = 1.25$V. For all $V_{DD} \geq V_{async}$, the asynchronous test time closely follows the lower bound of Equation (12) and is always lower than the synchronous test time, which equals the upper bound of Equation (13).

TABLE II
SYNCHRONOUS AND ASYNCHRONOUS TEST TIMES FOR S298 AT SELECTED VOLTAGES. TEST TIMES ARE NORMALIZED AS FRACTIONS OF 2.66μS, THE TEST TIME FOR THE CONVENTIONAL SYNCHRONOUS TEST AT NOMINAL VOLTAGE 1.8V.

Voltage	Synchronous test			Asynchronous test	
	Clock frequency	Test time		Test time	
		Actual	Normalized	Actual	Normalized
1.80V	187MHz	2.66μs	1.00	1.50μs	0.56
1.25V	404MHz	1.23μs	0.46	0.77μs	0.29
1.07V	511MHz	0.97μs	0.37	0.97μs	0.37

Test times for s298 are summarized in Table II. At the nominal voltage, 1.8V, some cycles are power constrained but still do not consume peak power. They can be speeded up and hence asynchronous test time is 56% that for synchronous test. As voltage is reduced, more cycles are speeded up and asynchronous test time further drops to 29% until, going below 1.25V, structure constrained cycles begin to dominate. The synchronous test time at 1.25V has reduced to 46% mainly because the peak power has reduced allowing the clock to be speeded up. At 1.07V all cycles become structure constrained and the two types of tests become identical, i.e., synchronous.

VI. CONCLUSION

The analysis in this paper examines the effect of supply voltage on test time when the circuit operation has a power limit. For synchronous testing, where the entire test runs at

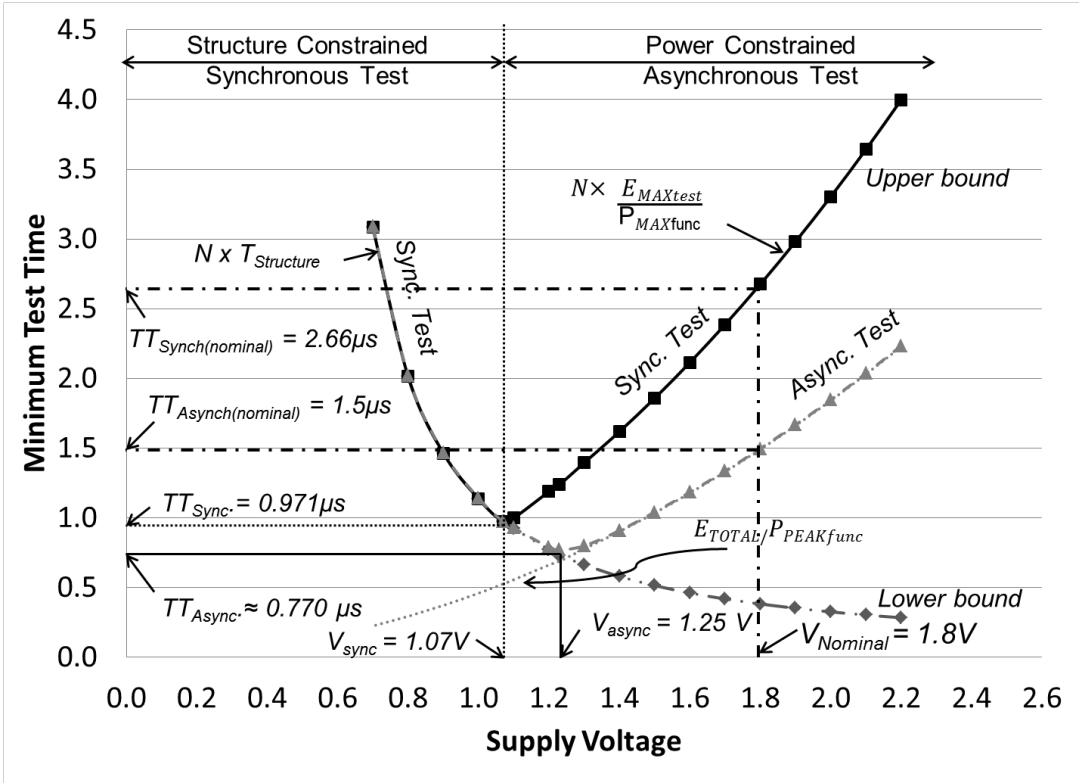

Fig. 3. Test time optimization for s298, 180nm CMOS, $P_{PEAKfunc} = 1.21$V, $N = 498$, $V_{nom} = 1.8$V. Optimum synchronous test: $V_{sync} = 1.07$V, $TT_{sync} = 0.971\mu$s. Optimum asynchronous test: $V_{sync} = 1.25$V, $TT_{async} = 0.770\mu$s.

a fixed maximum clock rate, the best voltage, to minimize the test time, is such that the power dissipation of maximum energy clock cycles remains under the power limit. This test time can be further reduced by asynchronous testing, which may run at an increased voltage.

In this work, once we find the optimum supply voltage, it remains fixed throughout the test while clock period dynamically varies according to the energy of the individual cycle. The voltage can also be customized for each cycle. For each cycle, given its energy consumption, we can find the voltage that minimizes the period under the specified power constraint. At the cost of some added complexity to the test set up the added degree of freedom will further reduce the test time. It is suggested that such a scheme be studied in the future.

ACKNOWLEDGMENT

This research is supported in part by the National Science Foundation Grants CNS-0708962, CCF-1116213 and IIP-0738088.

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