IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received July 20, 2019, accepted August 6, 2019, date of publication August 27, 2019, date of current version September 16, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2937922

A Thomas Algorithm-Based Generic Approach for Modeling of Power Supply Induced Jitter in CMOS Buffers

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ABSTRACT This paper presents an efficient and generic method for analysis of power supply induced jitter (PSIJ) in a chain of CMOS inverters as well as tapered buffers due to multiple deterministic noise sources. Generalised semi-analytical relations between noise and PSIJ are developed using Thomas algorithm. The proposed analysis can be used for both cases of same size of inverters as well as tapered buffers, and also for considering the effect of on-chip and off-chip interconnects. The validity and the efficiency of the proposed modeling is demonstrated for various applications of chain of inverters such as buffers in clock distribution, delay locked loops and I/Os, etc.

INDEX TERMS CMOS inverter, chain of inverters, clock-network, delay-line, I/O, jitter, power supply noise, power supply induced jitter, time interval error, tapered buffer.

I. INTRODUCTION

The demand for higher data rate in modern communication and computing systems has resulted in a sharp increase in the operating frequencies of digital circuits and systems. At higher operating frequencies, the design of integrated circuits is becoming more challenging due to the rigid timing and layout constraints as well as narrow timing margins. These challenges are further aggravated by the power supply noise (PSN) which is becoming one of the major performance limiting factors in high-speed low-power digital systems due to its impact on both amplitude and timing of the signal. PSN originates due to many factors, such as power fluctuations due to fast switching of heavy transient current demands, on-chip IR drop and inductive loss, etc. Resonance conditions due to plane or cavities formed on board, inductance of package, board and decoupling capacitors also lead to higher PSN. The overall impedance of the power delivery network (PDN) plays a vital role in delivering clean power supply to the circuits [1].

CMOS inverter is one of the basic building blocks in the design of high-speed systems. CMOS inverters are widely used due to their design simplicity and low static power consumption. Single inverter as well as chain-of-inverters are used in the form of delay-lines and I/O buffers. In a chain-of-inverters, multiple inverters are cascaded to get the required delay and to increase the slew-rate of output. In delay-lines, inverters of same size are used to make the chain. For driving higher capacitive loads, chain-of-inverters with inverter sizes increasing in geometric progression along the chain are often used, which are also known as tapered buffers.

A major drawback of a CMOS inverter is its sensitivity to PSN. Any noise from power supply, input data or ground will propagate to the output of inverter. The noise appearing at output also impacts the timing of the data. Signal transition time fluctuations are often measured in terms of time interval error (TIE) [2] which refers to the instantaneous jitter at the rising/falling edge in a cycle and also in terms of power supply induced jitter (PSIJ) which represents the peak-to-peak

The associate editor coordinating the review of this article and approving it for publication was Amedeo Andreotti.

value of the jitter over a large number of cycles. In the present SOCs, PSIJ is significantly impacting the timing budget [1].

In the literature, many studies can be found for the analysis of jitter in CMOS inverters, buffers and chain-of-inverters [3]–[21]. In [3], an analytical model of the PSIJ transfer function for inverter chains was described. Based on the PWL approximated MOSFET I-V characteristics, analytical expressions of PSIJ transfer functions at the output of each inverter in the chain was derived. The sensitivity functions of PSIJ based on the minimum and maximum propagation delay in the presence of supply noise was derived in [4]. The transfer functions relating supply voltage fluctuations to the jitter for a single-ended buffer are analytically derived in [9]. A slope based semi-analytical approach for the estimation of PSIJ in CMOS inverter chains is presented in [14].

In this paper, a generalized methodology is presented for estimation of power supply induced jitter (PSIJ) in a chain-of-inverters with the following contributions:

1) The proposed approach is generic and can be used for both cases, an inverter chain with same sizing of inverters as well as tapered buffers.
2) In order to overcome the difficulty associated with the previous approaches, the need for formulation and deriving the transfer function for each case of different noise sources, a generic approach resulting in a set of equations that are described by a tri-diagonal matrix is developed. Exploiting the resulting tri-diagonal form, Thomas algorithm [22] was used to develop semi-analytical relations for estimation of PSIJ.
3) The proposed method is extended to include the effects of both on-chip and off-chip interconnects.

The rest of the paper is organized as following. In Section II, the issue of PSIJ in inverters is discussed, followed by a semi-analytical method for the estimation of jitter. In Section III, analytical noise transfer functions for chain of inverters are derived using Thomas algorithm. In Section IV, noise transfer functions for a chain of inverters with on-chip interconnects are derived. Section V presents three practical validating examples and conclusions are presented in Section VI.

II. PROBLEM FORMULATION

In CMOS inverters, noise at the output causes the deviation of signal transition edge (rising/falling) from the nominal position and leads to time interval error (TIE) [23]. The TIE due to noise is proportional to the magnitude and phase of the resultant output noise from various paths. There are three main paths in an inverter through which noise propagates to the output: from power supply, ground and gate input, which are shown in FIGURE 1(a). The amplitude of noise appearing at the output of the inverter depends on the sizing of transistors and their threshold voltages, etc. [24].

It is to be noted that, an inverter acts as a *common-gate* amplifier for noise originating from power supply (V_{DD}) and ground. At the same time, it also acts as a *common-source*

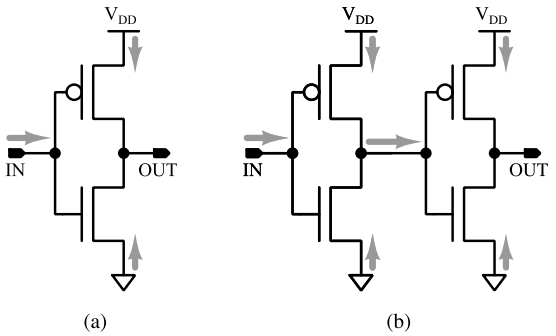

FIGURE 1. Noise paths in CMOS inverters: (a) Single inverter (b) Two cascaded inverters.

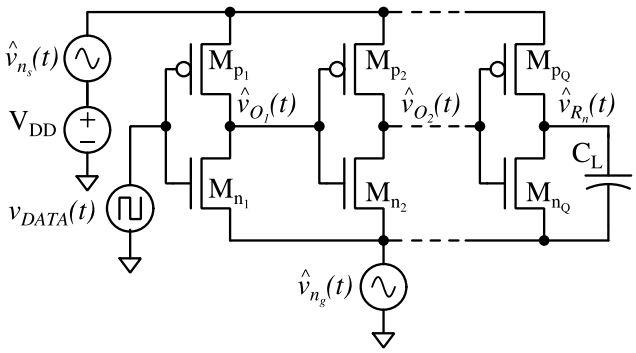

FIGURE 2. A chain-of-inverters with multiple noise sources.

amplifier for noise propagating through the input data [25]. The magnitude and phase response at the output due to the power supply noise, ground bounce and data noise can be obtained by deriving the transfer functions from respective inputs to the output [14].

In a chain-of-inverters or CMOS buffer circuits, noise from various paths propagate to the final output through cascaded inverters as shown in FIGURE 1(b). FIGURE 2 shows the schematic of a chain-of-inverters with noise sources from power supply and ground, represented by $\hat{v}_{n_s}(t)$ and $\hat{v}_{n_g}(t)$, respectively. Here C_L represents the external load capacitance. The output $v_{R_n}(t)$ represents the response at the output of the final stage inverter including the impact of all noise sources. In this case, the resultant noise at the output of a particular inverter acts as an input to the subsequent inverter. The TIE at the final stage output can be estimated from the noise response and the slope of signal rising/falling edge [26].

The timing analysis at the output of a delay-line or a tapered buffer in the presence of PSN can be performed using various methods [4], [6], [9]–[11], [14], [15]. In this paper, a simplified semi-analytical approach is developed for the analysis of TIE (as well as the jitter) at the output of a delay-line or tapered buffer that are designed using CMOS inverters. The proposed analysis is applicable for a chain-of-inverters with any number of stages, any stage ratio, and transistor sizing. The analysis is performed by representing the noise sources with sinusoidal signals.

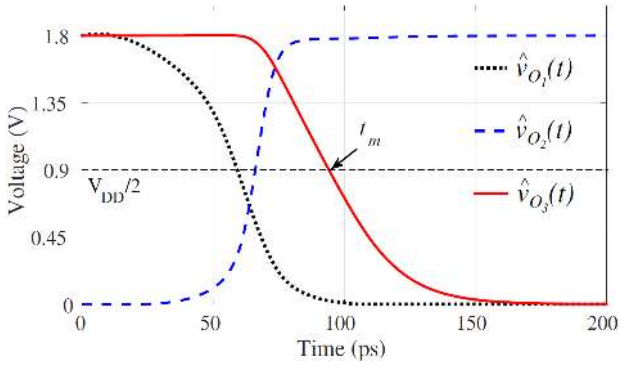

FIGURE 3. Transient waveforms at each stage output of a chain-of-inverters with three inverters (in this case, $\hat{v}_{R_n}(t) = \hat{v}_{O_3}(t)$).

III. DEVELOPMENT OF THE PROPOSED APPROACH

In the proposed approach, the noise due to deterministic sources, such as power supply noise ($\hat{v}_{n_s}(t)$) and ground bounce ($\hat{v}_{n_g}(t)$) are considered to be small-signal in nature. As a first step, a large signal analysis of the CMOS buffer circuit in FIGURE 2 is performed and using this information, its small-signal equivalent circuit is derived. A generic and analytical approach is developed to evaluate the total small-signal noise response ($\hat{v}_{r_n}(t)$) due to all deterministic noise inputs. Next, using the analytically computed $\hat{v}_{r_n}(t)$ and using the EMPSIJ method [26], TIE and PSIJ are evaluated. Note that, the proposed linearisation (small signal approximation) based approach is accurate only if the noise signals are of smaller magnitudes. For noise with larger variations, such as the scenario of Simultaneous Switching Output (SSO), a complete large signal analysis is required [27].

In the proposed approach, a given noise is decomposed into its harmonics and a closed-form response to each harmonic is obtained. The response due to the original noise is obtained as a sum of responses due to all the considered harmonics. The total small-signal noise output, $\hat{v}_{r_n}(t)$, is obtained using the superposition theorem,

$$\hat{v}_{r_n}(t) = \hat{v}_{r_s}(t) + \hat{v}_{r_g}(t) \tag{1}$$

where, $\hat{v}_{r_s}(t)$ and $\hat{v}_{r_g}(t)$ are the components of noise response (at the output) due to power supply and ground noise inputs, respectively. The noise responses in (1) are computed using the small-signal model at the mid-point of the output rising edge (t_m) by deriving the closed-form transfer functions based on the respective noise paths, which are presented in subsequent sections.

Since TIE (i.e., the timing error of a single rising/falling edge) is generally measured at the mid-point of the rising/falling edge of the signal, the quiescent point for the small-signal (noise) analysis is selected as the mid-point of the output signal transition edge. To obtain this information (nominal position of the output signal transition (rising/falling) edge), a simulation is performed for a duration of 1-bit without the input noise sources (i.e., $\hat{v}_{n_s}(t)$ and $\hat{v}_{n_g}(t)$). The mid-point (t_m) of the output rising/falling edge is noted (FIGURE 3). At this point, the node voltages define the operating region of all the transistors in the circuits. Voltages across and current through the transistors at the mid-point (t_m) define the small-signal parameters (g_m, g_{ds}) and the parasitic capacitances (C_{gs}, C_{gd} and C_{ds}) of the transistors. Here, g_m and g_{ds} are the transconductance and drain to source conductance of a transistor respectively. The values of g_m, g_{ds}, C_{gs}, C_{gd}, C_{ds} and the slope (α) of the output signal rising edge at t_m can be extracted from this one bit simulation. Correspondingly, the small-signal equivalent model of the CMOS buffer circuit (FIGURE 2 with 'Q' number of stages) can be constructed as shown in FIGURE 4. Here, for each stage, we have $C_{gd} = C_{gd_p} + C_{gd_n}$, where C_{gd_p} and C_{gd_n} are the gate to drain capacitance of pMOS and nMOS transistors, respectively. In the small-signal model, the current sources in an i^{th} inverter (FIGURE 4) can be expressed as follows:

$$i_{pi} = \begin{cases} g_{m_{pi}} \hat{v}_{n_s}(t); & i = 1; \\ g_{m_{pi}} (\hat{v}_{n_s}(t) - \hat{v}_{o_{(i-1)}}(t)); & i = 2, \ldots, Q \end{cases} \tag{2}$$

$$i_{ni} = \begin{cases} g_{m_{ni}} (-\hat{v}_{n_g}(t)); & i = 1 \\ g_{m_{ni}} (\hat{v}_{o_{(i-1)}}(t) - \hat{v}_{n_g}(t)); & i = 2, \ldots, Q \end{cases} \tag{3}$$

In the proposed approach, the PSIJ due to noise sources $\hat{v}_{n_s}(t)$ and $\hat{v}_{n_g}(t)$ is estimated by first analytically computing the individual noise response due to each of these sources. Since the noise from each path may be of different amplitudes, frequencies and phases, the transfer function is derived by considering only one noise at a time.

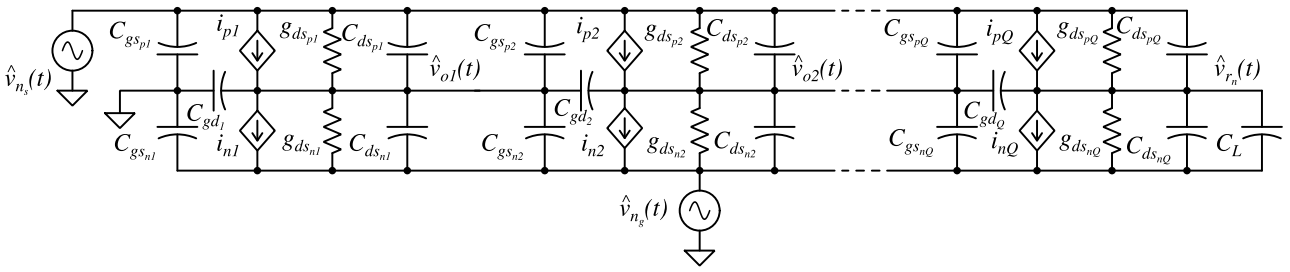

FIGURE 4. Small-signal model for a chain-of-inverters (in time domain).

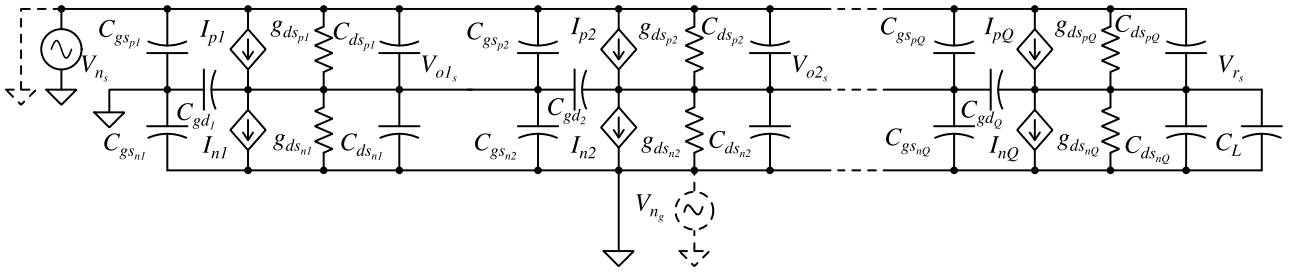

FIGURE 5. Small-signal model for the chain-of-inverters for a single harmonic of supply noise in frequency domain. The figure represents the case for single harmonic of power supply noise ($V_{n_s}(j\omega_s)$). In case of ground bounce ($V_{n_g}(j\omega_g)$), the components shown in dashed line are considered instead of the corresponding power supply noise components.

A. CLOSED-FORM TRANSFER FUNCTION FOR POWER SUPPLY NOISE RESPONSE

For the derivation of transfer function from supply noise to the final output, only supply noise ($\hat{v}_{n_s}(t)$) is considered (whereas $\hat{v}_{n_g}(t)$ is shorted to ground). For the purpose of development of the proposed method, without loss of generality, consider a single harmonic of $\hat{v}_{n_s}(t)$ in the form of a sine wave input noise with frequency f_s (i.e., $\omega_s = 2\pi f_s$) and amplitude M_s, represented by,

$$v_{n_s}(t) = M_s \sin(\omega_s t) \tag{4}$$

In the rest of this subsection, analysis with respect to a single harmonic is considered in frequency domain with variables represented by their respective frequency domain forms. For example, $v_{n_s}(t) \rightarrow V_{n_s}(j\omega_s)$, $v_{01}(t) \rightarrow V_{o1}(j\omega_s)$ and $v_{r_s}(t) \rightarrow V_{r_s}(j\omega_s)$, etc. For the simplicity of the presentation, and $j\omega$ is omitted in the equations and figures where appropriate. Correspondingly, the frequency-domain small-signal equivalent circuit for a single harmonic of the power supply noise ($V_{n_s}(j\omega_s)$) can be obtained as in FIGURE 5.

Applying the nodal analysis for the small-signal model by considering only the supply noise source $V_{n_s}(j\omega_s)$ and Q-stages of inverters, we have:

$$d_{1_s} V_{o1_s} + u_{1_s} V_{o2_s} = b_{1_s} V_{n_s} \tag{5}$$
$$l_{2_s} V_{o1_s} + d_{2_s} V_{o2_s} + u_{2_s} V_{o3_s} = b_{2_s} V_{n_s} \tag{6}$$
$$\vdots$$
$$l_{Q_s} V_{o(Q-1)_s} + d_{Q_s} V_{r_s} = b_{Q_s} V_{n_s} \tag{7}$$

The coefficients used in the above system of equations are the variables that are expressed in terms of small-signal parameters of the transistors, as follows:

$$d_{i_s} = d_i^r + j\omega_s d_i^i \tag{8}$$

where the superscripts *'r'* and *'i'* represent the *'real'* and *'imaginary'* quantities, with

$$d_i^r = g_{ds_i}; \quad i = 1, 2, \ldots, Q \tag{9}$$
$$d_i^i = \begin{cases} C_{L_i}; & i = 1, 2, \ldots, (Q-1) \\ C'_{L_i}; & i = Q \end{cases} \tag{10}$$

where

$$g_{ds_i} = g_{ds_{pi}} + g_{ds_{ni}} \tag{11}$$
$$C_{L_i} = C_{gd_i} + C_{ds_{pi}} + C_{ds_{ni}} + C_{gd_{i+1}} + C_{gs_{p(i+1)}} + C_{gs_{n(i+1)}} \tag{12}$$
$$C'_{L_i} = C_{gd_i} + C_{ds_{pi}} + C_{ds_{ni}} + C_L \tag{13}$$

and

$$l_{i_s} = l_i^r + j\omega_s l_i^i \tag{14}$$
$$l_i^r = \begin{cases} 0; & i = 1 \\ -g_{m_i}; & i = 2, 3, \ldots, Q \end{cases} \tag{15}$$
$$l_i^i = \begin{cases} 0; & i = 1 \\ C_{gd_i}; & i = 2, 3, \ldots, Q \end{cases} \tag{16}$$

where

$$g_{m_i} = g_{m_{pi}} + g_{m_{ni}} \tag{17}$$
$$u_{i_s} = \begin{cases} C_{gd_{i+1}}; & i = 1, 2, \ldots, (Q-1) \\ 0; & i = Q \end{cases} \tag{18}$$
$$b_{i_s} = \begin{cases} g_{m_{pi}} + g_{ds_{pi}} + j\omega_s C''_{L_i}; & i = 1, 2, \ldots, (Q-1) \\ g_{m_{pi}} + g_{ds_{pi}} + j\omega_s C_{ds_{pi}}; & i = Q \end{cases} \tag{19}$$
$$C''_{L_i} = C_{ds_{pi}} + C_{gs_{p(i+1)}} \tag{20}$$

The system of equations (5)-(7) can be written in the matrix form as follows:

$$\boldsymbol{A}_s(j\omega_s)\boldsymbol{X}_s(j\omega_s) = V_{n_s}(j\omega_s)\boldsymbol{B}_s(j\omega_s) \tag{21}$$

where

$$\boldsymbol{X}_s(j\omega_s) = \begin{bmatrix} V_{o1_s}(j\omega_s) \\ V_{o2_s}(j\omega_s) \\ \vdots \\ V_{o(Q-1)_s}(j\omega_s) \\ V_{r_s}(j\omega_s) \end{bmatrix}; \quad \boldsymbol{B}_s(j\omega_s) = \begin{bmatrix} b_{1_s}(j\omega_s) \\ b_{2_s}(j\omega_s) \\ \vdots \\ b_{(Q-1)_s}(j\omega_s) \\ b_{Q_s}(j\omega_s) \end{bmatrix} \tag{22}$$

$$\boldsymbol{A}_s(j\omega_s) = \boldsymbol{A}_1 + j\omega_s \boldsymbol{A}_2 \tag{23}$$

$$\boldsymbol{A}_1 = \begin{bmatrix} d_1^r & 0 & 0 & \dots & 0 & 0 \\ l_2^r & d_2^r & 0 & \dots & 0 & 0 \\ \vdots & \vdots & \vdots & \dots & \vdots & \vdots \\ 0 & 0 & 0 & \dots & d_{(Q-1)}^r & 0 \\ 0 & 0 & 0 & \dots & l_Q^r & d_Q^r \end{bmatrix} \tag{24}$$

$$\boldsymbol{A}_2 = \begin{bmatrix} d_1^i & u_1 & 0 & \dots & 0 & 0 \\ l_2^i & d_2^i & u_2 & \dots & 0 & 0 \\ \vdots & \vdots & \vdots & \dots & \vdots & \vdots \\ 0 & 0 & 0 & \dots & d_{(Q-1)}^i & u_{(Q-1)} \\ 0 & 0 & 0 & \dots & l_Q^i & d_Q^i \end{bmatrix} \tag{25}$$

The final form of $\boldsymbol{A}_s$ in (23) can be obtained as:

$$\boldsymbol{A}_s(j\omega_s) = \begin{bmatrix} d_{1_s} & u_{1_s} & 0 & \dots & 0 & 0 \\ l_{2_s} & d_{2_s} & u_{2_s} & \dots & 0 & 0 \\ \vdots & \vdots & \vdots & \dots & \vdots & \vdots \\ 0 & 0 & 0 & \dots & d_{(Q-1)_s} & u_{(Q-1)_s} \\ 0 & 0 & 0 & \dots & l_{Q_s} & d_{Q_s} \end{bmatrix} \tag{26}$$

B. THOMAS ALGORITHM AND CLOSED-FORM SOLUTION FOR NOISE RESPONSE DUE TO POWER SUPPLY NOISE

It can be noted that, the matrix obtained in (26) is a tri-diagonal matrix. Taking advantage of this form, (21) can be solved using '*Thomas algorithm*' [22] to analytically obtain the output noise response ($v_{r_s}(t)$) due to the supply noise input ($v_{n_s}(t)$). Using Thomas algorithm, the coeffcients of matrices $\boldsymbol{A}_s$ and $\boldsymbol{B}_s$ can be transformed as follows:

$$u'_{i_s} = \begin{cases} \dfrac{u_{i_s}}{d_{i_s}}; & i = 1 \\ \dfrac{u_{i_s}}{d_{i_s} - l_{i_s} u'_{(i-1)_s}}; & i = 2, 3, \dots, (Q-1) \end{cases} \tag{27}$$

$$b'_{i_s} = \begin{cases} \dfrac{b_{i_s}}{d_{i_s}}; & i = 1 \\ \dfrac{b_{i_s} - l_{i_s} b'_{(i-1)_s}}{d_{i_s} - l_{i_s} u'_{(i-1)_s}}; & i = 2, 3, \dots, Q \end{cases} \tag{28}$$

Correspondingly, (21) can be re-written as:

$$\boldsymbol{A}'_s(j\omega_s)\boldsymbol{X}_s(j\omega_s) = V_{n_s}(j\omega_s)\boldsymbol{B}'_s(j\omega_s) \tag{29}$$

$$\boldsymbol{A}'_s = \begin{bmatrix} 1 & u'_{1_s} & 0 & \dots & 0 & 0 \\ 0 & 1 & u'_{2_s} & \dots & 0 & 0 \\ \vdots & \vdots & \vdots & \dots & \vdots & \vdots \\ 0 & 0 & 0 & \dots & 1 & u'_{(Q-1)_s} \\ 0 & 0 & 0 & \dots & 0 & 1 \end{bmatrix};$$

$$\boldsymbol{B}'_s = \begin{bmatrix} b'_{1_s} \\ b'_{2_s} \\ \vdots \\ b'_{(Q-1)_s} \\ b'_{Q_s} \end{bmatrix} \tag{30}$$

It is obvious from (22), (29) and (30) that the noise response $V_{r_s}(j\omega_s)$ due to supply noise input $V_{n_s}(j\omega_s)$ can be obtained as a closed-form expression as:

$$V_{r_s}(j\omega_s) = b'_{Q_s}(j\omega_s) V_{n_s}(j\omega_s) \tag{31}$$

where, $b'_{Q_s}(j\omega_s)$ can be evaluated analytically using (27) and (28). Next, the time-domain noise response ($v_{r_s}(t)$) due to the harmonic under consideration can be analytically obtained from (31) as:

$$v_{r_s}(t) = |b'_{Q_s}(j\omega_s)| M_s \sin(\omega_s t + \angle b'_{Q_s}(j\omega_s)) \tag{32}$$

The form of (32) can be utilised to analytically compute the noise response due to any other harmonic of the noise input. Assuming H_s number of harmonics, the total noise output ($\hat{v_{r_s}}(t)$) can be obtained as a sum of noise response due to all its considered harmonics using (33), as

$$\hat{v}_{r_s}(t) = \sum_{i=1}^{H_s} (v_{r_s}(t))_i \tag{33}$$

It can be noted that the formulation leading to (21) is based on the nodal analysis, which can be easily adopted to SPICE like tool environment for systematic formulation. Also, the subsequent closed-form solution process using (27)-(31) can be easily adopted in them.

C. CLOSED-FORM TRANSFER FUNCTION FOR GROUND BOUNCE

The above formulation can be easily extended to include other types of noise sources, such as ground bounce. Consider the small-signal equivalent circuit in FIGURE 4 with just the ground bounce noise $\hat{v}_{n_g}(t)$. To obtain the corresponding noise response $\hat{v}_{r_g}(t)$, first, consider a single harmonic of the ground bounce with frequency f_g (i.e., $\omega_g = 2\pi f_g$) and amplitude M_g as:

$$v_{n_g}(t) = M_g \sin(\omega_g t) \tag{34}$$

Next, following the steps similar to the one developed in Section III.A, a frequency-domain small-signal equivalent circuit for a single harmonic of the ground bounce can be obtained similar to FIGURE 5 (with only V_{n_g} while V_{n_s} is shorted). Next, a set of equations in the matrix form to compute the ground bounce noise response V_{r_g} can be obtained as:

$$\boldsymbol{A}_g(j\omega_g)\boldsymbol{X}_g(j\omega_g) = V_{n_g}(j\omega_g)\boldsymbol{B}_g(j\omega_g) \tag{35}$$

where

$$\boldsymbol{A}_g(j\omega_g) = \boldsymbol{A}_1 + j\omega_g \boldsymbol{A}_2 \tag{36}$$

$\boldsymbol{X}_g(j\omega_g)$ corresponds to the nodal voltages due to ground bounce and $\boldsymbol{B}_g(j\omega_g)$ represents the source vector due to ground bounce, as

$$\boldsymbol{X}_g(j\omega_g) = \begin{bmatrix} V_{o1_g}(j\omega_g) \\ V_{o2_g}(j\omega_g) \\ \vdots \\ V_{o(Q-1)_g}(j\omega_g) \\ V_{r_g}(j\omega_g) \end{bmatrix}; \quad \boldsymbol{B}_g(j\omega_g) = \begin{bmatrix} b_{1_g}(j\omega_g) \\ b_{2_g}(j\omega_g) \\ \vdots \\ b_{(Q-1)_g}(j\omega_g) \\ b_{Q_g}(j\omega_g) \end{bmatrix} \tag{37}$$

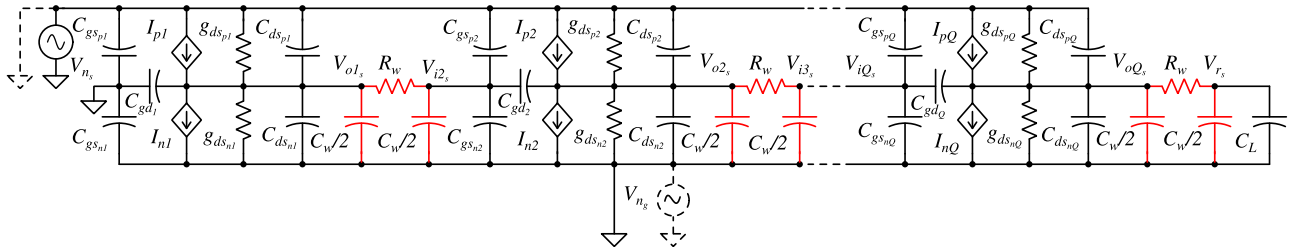

FIGURE 6. Small-signal model of the inverter chain including RC lumped π model on-chip interconnects. The figure represents the case for single harmonic of power supply noise ($V_{n_s}(j\omega_s)$). In case of ground bounce ($V_{n_g}(j\omega_g)$), the components shown in dashed line are considered instead of the corresponding power supply noise components.

where the coefficients b_{i_g} are obtained similar to (19) as:

$$b_{i_g} = \begin{cases} g_{m_{ni}} + g_{ds_{ni}} + j\omega_g C'''_{L_i}; & i = 1, 2, \ldots, (Q-1) \\ g_{m_{ni}} + g_{ds_{ni}} + j\omega_g C_{ds_{ni}}; & i = Q \end{cases} \tag{38}$$

$$C'''_{L_i} = C_{ds_{ni}} + C_{gs_{n(i+1)}} \tag{39}$$

A significant advantage of this formulation is that, $\boldsymbol{A}_g$ is evaluated in (36), by simply reusing the matrices that were obtained already in (24) and (25). It is also to be noted that $\boldsymbol{A}_g$ too retains the tri-diagonal form (similar to $\boldsymbol{A}_s$ in (26)). This facilitates using the closed-form solution process based on Thomas algorithm that is developed in Section III.B for evaluating the noise response ($V_{r_g}(j\omega_g)$) due to ground bounce ($V_{n_g}(j\omega_g)$) as:

$$V_{r_g}(j\omega_g) = b'_{Q_g}(j\omega_g) V_{n_g}(j\omega_g) \tag{40}$$

Next, using an analytical formulation similar to (32), the transient response due to a particular harmonic of ground bounce ($v_{r_g}(t)$) can be computed. Assuming H_g number of harmonics for the ground bounce, total noise response ($\hat{v}_{r_g}(t)$) due to all considered harmonics of ground bounce signal of any shape can be obtained as:

$$\hat{v}_{r_g}(t) = \sum_{i=1}^{H_g} (v_{r_g}(t))_i \tag{41}$$

A detailed derivation of the tri-diagonal form for the matrix (and re-use of $\boldsymbol{A}_1$ and $\boldsymbol{A}_2$ matrices) for computing the response due to ground bounce is given in Appendix-A.

D. EVALUATION OF PSIJ

In the proposed method, PSIJ is evaluated using the noise responses $\hat{v}_{r_s}(t)$ and $\hat{v}_{r_g}(t)$ that were analytically evaluated using (32), (33) and (41). The total small-signal noise response at the output ($v_{r_n}(t)$) due to both the noise sources can be obtained using the superposition theorem, as in (1).

Next, TIE can be estimated based on the slope of the rising/falling edge of the output signal [26]. In this method, TIE at the rising/falling edge of a bit is estimated from the noise voltage at the output $\hat{v}_{r_n}(t_m)$ by dividing it with the slope (α_{t_m}) of the output response at the mid-point (t_m).

$$\text{TIE} = J_r = \frac{\hat{v}_{r_n}(t_m)}{\alpha_{t_m}} \tag{42}$$

After calculating the instantaneous jitter for multiple bits (having different t_m values) using the expression (42), the peak-to-peak jitter which represents the PSIJ, can be estimated as:

$$\text{PSIJ} = J_{P-P} = \frac{\max(\hat{v}_{r_n}(t_m)) - \min(\hat{v}_{r_n}(t_m))}{\alpha_{t_m}} \tag{43}$$

IV. CMOS INVERTER CHAIN WITH ON-CHIP INTERCONNECTS

In some of the realistic environments, based on the frequency of operations and the device technology, on-chip interconnects can significantly influence jitter. The analytical relations based on Thomas algorithm presented in Section III, are extended in this section for the case of chain-of-inverters to include the effect of on-chip interconnects.

Fig. 6 shows the small-signal model including the on-chip interconnects. The interconnects between two consecutive stages of an inverter chain are modeled using lumped RC π-model [28] where R_w and C_w are the per unit length resistance and capacitance of the interconnect wire, respectively. Using steps similar to the previous case, the transfer function is derived by considering only one noise source at a time.

A. TRANSFER FUNCTION FOR POWER SUPPLY NOISE INCLUDING ON-CHIP INTERCONNECT EFFECTS

Consider the case of a buffer with 'Q' stages; as shown in FIGURE 6, there will be '$2Q$' nodes (hence '$2Q$' nodal equations). Corresponding nodal voltages can be written as follows,

$$\tilde{d}_{1_s} V_{o1_s} + \tilde{u}_{1_s} V_{i2_s} = \tilde{b}_{1_s} V_{n_s} \tag{44}$$

$$\tilde{l}_{2_s} V_{o1_s} + \tilde{d}_{2_s} V_{i2_s} + \tilde{u}_{2_s} V_{o2_s} = \tilde{b}_{2_s} V_{n_s} \tag{45}$$

$$\tilde{l}_{3_s} V_{i2_s} + \tilde{d}_{3_s} V_{o2_s} + \tilde{u}_{3_s} V_{i3_s} = \tilde{b}_{3_s} V_{n_s} \tag{46}$$

$$\vdots \tag{47}$$

$$\tilde{l}_{(2Q)_s} V_{(oQ)_s} + \tilde{d}_{(2Q)_s} V_{r_n} = \tilde{b}_{(2Q)_s} V_{n_s} \tag{48}$$

Similar to the case of inverter chain without on-chip interconnects, the coefficients in the system of equations (44)-(48) can also be represented as:

$$\tilde{d}_{i_s} = \tilde{d}^r_i + j\omega_s \tilde{d}^i_i \tag{49}$$

$$\tilde{d}^r_i = \begin{cases} G_w + g_{ds_{\frac{i+1}{2}}}; & i = 1, 3, \ldots, (2Q-1) \\ G_w; & i = 2, 4, \ldots, 2Q \end{cases} \tag{50}$$

$$\tilde{d}_i^i = \begin{cases} \tilde{C}'_{L_i}; & i = 1, 3, \ldots, (2Q-1) \\ \tilde{C}_{L_i}; & i = 2, 4, \ldots, (2Q-2) \\ \dfrac{C_w}{2} + C_L; & i = 2Q \end{cases} \quad (51)$$

$$g_{ds_{\frac{i+1}{2}}} = g_{ds_{p\frac{i+1}{2}}} + g_{ds_{n\frac{i+1}{2}}} \quad (52)$$

$$\tilde{C}'_{L_i} = C_{gd_{\frac{i+1}{2}}} + C_{ds_{p\frac{i+1}{2}}} + C_{ds_{n\frac{i+1}{2}}} + \frac{C_w}{2} \quad (53)$$

$$\tilde{C}_{L_i} = C_{gd_{\frac{i+2}{2}}} + C_{gs_{p\frac{i+2}{2}}} + C_{gs_{n\frac{i+2}{2}}} + \frac{C_w}{2} \quad (54)$$

$$\tilde{l}_{i_s} = \tilde{l}_i^r + j\omega_s \tilde{l}_i^i \quad (55)$$

$$\tilde{l}_i^r = \begin{cases} 0; & i = 1 \\ G_w; & i = 2, 4, \ldots, 2Q \\ -g_{m_{\frac{i+1}{2}}}; & i = 3, 5, \ldots, (2Q-1) \end{cases} \quad (56)$$

$$\tilde{l}_i^i = \begin{cases} 0; & i = 1 \\ 0; & i = 2, 4, \ldots, 2Q \\ C_{gd_{\frac{i+1}{2}}}; & i = 3, 5, \ldots, (2Q-1) \end{cases} \quad (57)$$

$$g_{m_{\frac{i+1}{2}}} = g_{m_{p\frac{i+1}{2}}} + g_{m_{n\frac{i+1}{2}}} \quad (58)$$

$$\tilde{u}_{i_s} = \tilde{u}_i^r + j\omega_s \tilde{u}_i^i \quad (59)$$

$$\tilde{u}_i^r = \begin{cases} G_w; & i = 1, 3, \ldots, 2Q-1 \\ 0; & i = 2, 4, \ldots, 2Q \end{cases} \quad (60)$$

$$\tilde{u}_i^i = \begin{cases} 0; & i = 1, 3, \ldots, (2Q-1) \\ C_{gd_{\frac{i+2}{2}}}; & i = 2, 4, \ldots, (2Q-2) \\ 0 & i = 2Q \end{cases} \quad (61)$$

$$\tilde{b}_{i_s} = \begin{cases} g_{i_p} + j\omega_s C_{ds_{p\frac{i+1}{2}}}; & i = 1, 3, \ldots, (2Q-1) \\ j\omega_s C_{gs_{p\frac{i+2}{2}}}; & i = 2, 4, \ldots, (2Q-2) \\ 0; & i = 2Q \end{cases} \quad (62)$$

$$g_{i_p} = g_{m_{p\frac{i+1}{2}}} + g_{ds_{p\frac{i+1}{2}}} \quad (63)$$

Next, the system of equations (44)-(48) can be written in the form of matrix as follows:

$$\tilde{\boldsymbol{A}}_s(j\omega_s)\tilde{\boldsymbol{X}}_s(j\omega_s) = V_{n_s}(j\omega_s)\tilde{\boldsymbol{B}}_s(j\omega_s) \quad (64)$$

where,

$$\tilde{\boldsymbol{X}}_s(j\omega_s) = \begin{bmatrix} V_{o1_s}(j\omega_s) \\ V_{i2_s}(j\omega_s) \\ \vdots \\ V_{oQ_s}(j\omega_s) \\ V_{r_s}(j\omega_s) \end{bmatrix}; \quad \tilde{\boldsymbol{B}}_s(j\omega_s) = \begin{bmatrix} \tilde{b}_{1_s}(j\omega_s) \\ \tilde{b}_{2_s}(j\omega_s) \\ \vdots \\ \tilde{b}_{(2Q-1)_s}(j\omega_s) \\ \tilde{b}_{2Q_s}(j\omega_s) \end{bmatrix} \quad (65)$$

$$\tilde{\boldsymbol{A}}_s(j\omega_s) = \tilde{\boldsymbol{A}}_1 + j\omega_s \tilde{\boldsymbol{A}}_2 \quad (66)$$

$$\tilde{\boldsymbol{A}}_1 = \begin{bmatrix} \tilde{d}_1^r & 0 & 0 & \ldots & 0 & 0 \\ \tilde{l}_2^r & \tilde{d}_2^r & 0 & \ldots & 0 & 0 \\ \vdots & \vdots & \vdots & \ldots & \vdots & \vdots \\ 0 & 0 & 0 & \ldots & \tilde{d}_{(2Q-1)}^r & 0 \\ 0 & 0 & 0 & \ldots & \tilde{l}_{2Q}^r & \tilde{d}_{2Q}^r \end{bmatrix} \quad (67)$$

$$\tilde{\boldsymbol{A}}_2 = \begin{bmatrix} \tilde{d}_1^i & \tilde{u}_1 & 0 & \ldots & 0 & 0 \\ \tilde{l}_2^i & \tilde{d}_2^i & \tilde{u}_2 & \ldots & 0 & 0 \\ \vdots & \vdots & \vdots & \ldots & \vdots & \vdots \\ 0 & 0 & 0 & \ldots & \tilde{d}_{(2Q-1)}^i & \tilde{u}_{(2Q-1)} \\ 0 & 0 & 0 & \ldots & \tilde{l}_{2Q}^i & \tilde{d}_{2Q}^i \end{bmatrix} \quad (68)$$

The final form of $\tilde{\boldsymbol{A}}_s$ in (66) can be obtained as:

$$\tilde{\boldsymbol{A}}_s(j\omega_s) = \begin{bmatrix} \tilde{d}_{1_s} & \tilde{u}_{1_s} & 0 & \ldots & 0 & 0 \\ \tilde{l}_{2_s} & \tilde{d}_{2_s} & \tilde{u}_{2_s} & \ldots & 0 & 0 \\ \vdots & \vdots & \vdots & \ldots & \vdots & \vdots \\ 0 & 0 & 0 & \ldots & \tilde{d}_{(2Q-1)_s} & \tilde{u}_{(2Q-1)_s} \\ 0 & 0 & 0 & \ldots & \tilde{l}_{2Q_s} & \tilde{d}_{2Q_s} \end{bmatrix} \quad (69)$$

B. TRANSFER FUNCTION FOR GROUND BOUNCE INCLUDING ON-CHIP INTERCONNECT EFFECTS

Referring to FIGURE 6, consider a single harmonic of the ground bounce (V_{n_g}). For computing the corresponding noise response (V_{r_g}), a system of equations similar to (64) can be derived as:

$$\tilde{\boldsymbol{A}}_g(j\omega_g)\tilde{\boldsymbol{X}}_g(j\omega_g) = V_{n_s}(j\omega_g)\tilde{\boldsymbol{B}}_g(j\omega_s) \quad (70)$$

where

$$\tilde{\boldsymbol{A}}_g(j\omega_g) = \tilde{\boldsymbol{A}}_1 + j\omega_g \tilde{\boldsymbol{A}}_2 \quad (71)$$

with $\omega_g = 2\pi f_g$; f_g represents the frequency of the ground bounce. $\tilde{\boldsymbol{X}}_g(j\omega_g)$ corresponds to the nodal voltages due to ground bounce and $\tilde{\boldsymbol{B}}_g(j\omega_g)$ represents the source vector due to ground bounce, as

$$\tilde{\boldsymbol{X}}_g(j\omega_g) = \begin{bmatrix} V_{o1_g}(j\omega_g) \\ V_{i2_g}(j\omega_g) \\ \vdots \\ V_{o(2Q-1)_g}(j\omega_g) \\ V_{r_g}(j\omega_g) \end{bmatrix};$$

$$\tilde{\boldsymbol{B}}_g(j\omega_g) = \begin{bmatrix} \tilde{b}_{1_g}(j\omega_g) \\ \tilde{b}_{2_g}(j\omega_g) \\ \vdots \\ \tilde{b}_{(2Q-1)_g}(j\omega_g)\tilde{b}_{(2Q)_g}(j\omega_g) \end{bmatrix} \quad (72)$$

where the coefficients b_{i_g} are obtained similar to (62) as:

$$\tilde{b}_{i_g} = \begin{cases} g_{i_n} + j\omega_g(C_{ds_{n\frac{i+1}{2}}} + \dfrac{C_w}{2}); & i = 1, 3, \ldots, (2Q-1) \\ j\omega_g(C_{gs_{n\frac{i+2}{2}}} + \dfrac{C_w}{2}); & i = 2, 4, \ldots, (2Q-2) \\ j\omega_g(\dfrac{C_w}{2} + C_L); & i = 2Q \end{cases} \quad (73)$$

where

$$g_{i_n} = g_{m_{n\frac{i+1}{2}}} + g_{ds_{n\frac{i+1}{2}}} \quad (74)$$

Similar to the case without on-chip interconnects, the noise components $v_{r_s}(t)$ and $v_{r_g}(t)$ can be calculated using Thomas

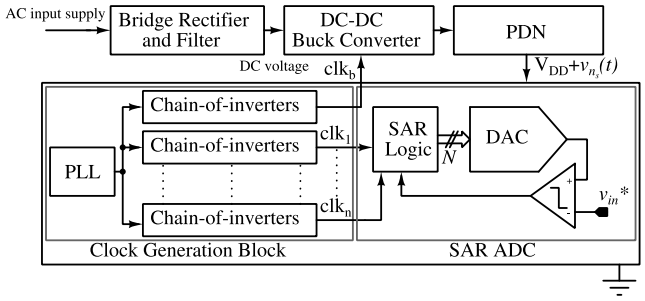

FIGURE 7. System block-diagram of SAR ADC with tapered buffer for Example-1.

algorithm by substituting the corresponding matrix coefficients in (27) and (28). The peak-to-peak jitter can be estimated using (43). The details are provided in Appendix-B.

V. RESULTS

The performance of the proposed semi-analytical approach is verified with SPICE based conventional simulation for three case studies. First example presents jitter at the output of a tapered buffer used in the clock distribution network. Second example presents PSIJ at the output of a delay-line including the effect of on-chip interconnects. Third example presents estimation of PSIJ at the output of buffer with off-chip load including the effect of package. In all the examples, an input signal with a data rate of 1 Gbps is used. All the experiments are done using the PDK of 55 nm triple-gate oxide BiCMOS technology of STMicroelectronics where the supply voltage (V_{DD}) is 1.8 V. The standard PDK based SPICE-simulation are reliable as they incorporate process related effects and are used for practical chip design in industry. Particularly, we have provided the validating comparisons for the results in terms of accuracy and speed of the proposed method against the leading SPICE-based commercial simulator, Spectre from Cadence.

A. EXAMPLE-1

In this example, the jitter estimation is done for a tapered buffer with four inverters and a *stage-ratio*, $\eta = 2$ (the ratio of transistor sizes between two consecutive inverters). The buffer is designed for an application of clock distribution network of a successive approximation register (SAR) analog-to-digital converter (ADC). FIGURE 7 shows the block diagram of a SAR ADC with the supporting circuitry (including phase locked loop (PLL), buffers and power delivery network). The on-chip supply voltage, $V_{\rm DD}$, is generated by an AC–DC rectifier, a DC–DC buck converter and a power delivery network (PDN). The 1.8 V DC signal is fed to the complete ADC as the supply voltage ($V_{\rm DD}$). This supply voltage is expected to be clean DC. However, the power supply has fluctuation due to the PDN. The block diagram includes a SAR loop which has three major design blocks; comparator, SAR logic, and DAC. The SAR logic is an implementation of a digital logic circuitry (shift-registers). The shift-register is implemented using D-flip-flops and is driven by various clocks with different phases of sampling rates ($clk_1, clk_2, \ldots, clk_n$). The input capacitance of shift-registers and output capacitance of PLL play a vital role in driving the SAR logic without losing logic information. For digital buffers, the chain is implemented with odd/even number of stages, depending on the required phase of the clock and the logical-effort [29]. The transistor sizing used for the design of buffer is given in TABLE 1. The sampling frequency of the ADC is 1 GHz with 6 bits of resolution.

TABLE 1. Transistor sizing.

Example	pMOS	nMOS	Stage ratio
Example - 1	$2.7\mu m/0.06\mu m$	$1.35\mu m/0.06\mu m$	2
Example - 2	$2.7\mu m/0.06\mu m$	$1.35\mu m/0.06\mu m$	1
Example - 3	$2.7\mu m/0.06\mu m$	$1.35\mu m/0.06\mu m$	2

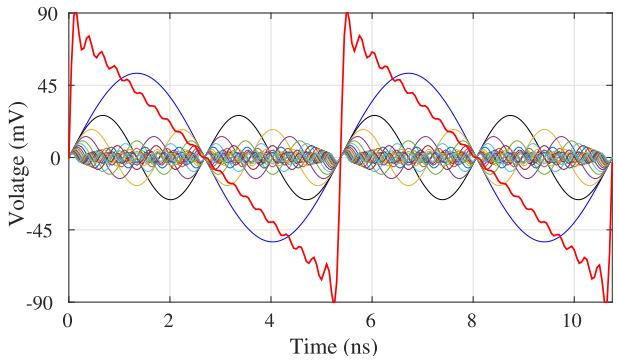

FIGURE 8. Generating sawtooth noise waveform using multiple sine waves (Example-1).

For estimation of jitter in the designed delay-line, two different sawtooth waves (with different time periods) are used as power supply and ground noise sources. The sawtooth waves are generated by superimposing multiple sine waves as shown in FIGURE 8. The peak-to-peak amplitudes of the noise sources are varied from 0 to 180 mV (10 % of V_{DD}). At various amplitude levels of input noise sources, jitter is estimated using both the proposed method and conventional simulation. The transfer function derived in (31) and (40) are used to calculate the output noise response. The TIE and PSIJ are estimated from the output noise response using the expressions (42) and (43), respectively. An accuracy comparison of conventional simulation (SPICE) results and the proposed semi-analytical approach is plotted in FIGURE 9. As seen, the results from both approaches are in good agreement.

B. EXAMPLE-2

In this example, the jitter estimation is performed for a delay-line with five inverters including the effect of on-chip interconnects. The delay-line is used for an application of a Delay Locked Loop (DLL) as shown in FIGURE 10. It also shows

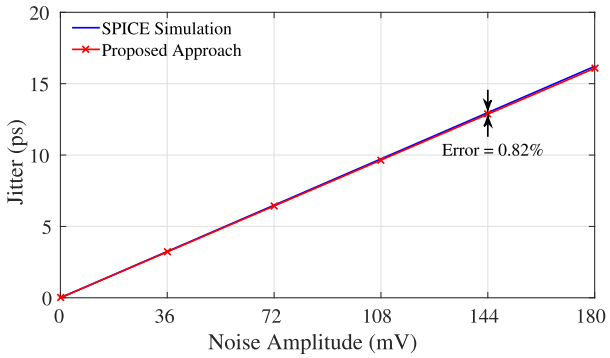

FIGURE 9. Comparison of jitter calculated using the conventional simulation and the proposed approach for a tapered buffer (Example-1).

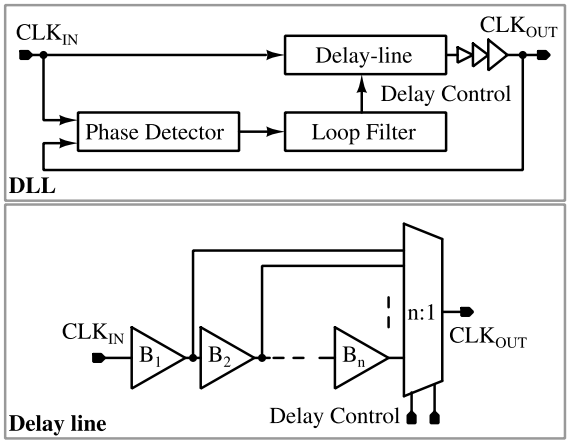

FIGURE 10. Block diagram of a delay-locked-loop (DLL) for Example-2.

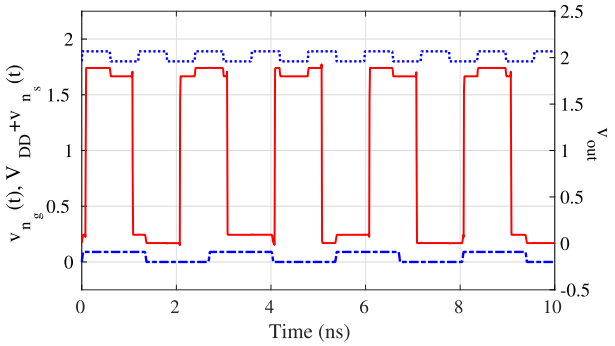

FIGURE 11. Distorted output waveform (right y-axis: Solid-line) in the presence of power supply noise (left y-axis: Top dotted-line) and ground noise (left y-axis: Bottom dashed-line) (Example-2).

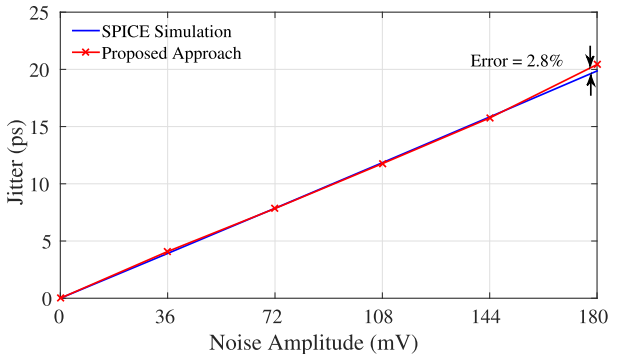

FIGURE 12. Comparison of jitter values calculated using the proposed approach and SPICE based simulation for a chain-of-inverters with five inverters (Example-2).

the implementation of variable delay-line using a chain-of-buffers, where each buffer is made up of two cascaded CMOS inverters. A wire length of 1 μm is used for modeling interconnects. An interconnect resistance of 1 $\Omega/\mu m$ and capacitance of 0.15 $fF/\mu m$ are used as R_w and C_w. The transistor sizes (W/L) used in the design of the chain-of-inverters are given in TABLE 1. Two different pulse trains (with different time periods) are used as power supply and ground noise sources, as shown in FIGURE 11. In FIGURE 11, both the power supply and ground noise are shown as well as their combined impact on the output response. Similar to the saw-tooth wave, the pulse train can also be reconstructed using superposition of multiple sine waves. The peak-to-peak input noise amplitudes are varied from 0 to 180 mV. At various amplitude levels of input noise sources, jitter is estimated by both the proposed method and conventional simulation. Here, for calculating the output noise response, the transfer functions derived in Section IV are used. The results obtained from both simulation and proposed approach including the impact of on-chip interconnects are compared in FIGURE 12.

C. EXAMPLE-3

This example shows a case study where a tapered buffer is driving an off-chip load (FIGURE 13). The optimal sizing for driver stages is chosen accordingly so that it can drive the load. The number of inverter stages required to drive the given 10 pF off-chip capacitive load with minimum delay can be calculated using the logical effort theory [29] as below,

$$\eta^N = \frac{C_L}{C_{in}} \tag{75}$$

where, η is the size ratio of transistors between two consecutive stages, C_L is the external load to be driven and C_{in} is the sum of gate capacitance of first inverter and output capacitance of the previous circuit. The stage ratio (η) is set as 2. The input gate capacitance is 17.3 fF. Substituting the values in (75), the number of stages (N) obtained is 9. The transistor sizes (W/L) used in the design of the I/O buffer are given in TABLE 1.

FIGURE 14 shows the physical layout of the package net used for this example. There is a connection from a bump of the die at the top layer to the ball at the package (bottom layer). The package has 8 layers and in FIGURE 14, only the top layer is shown. The parasitic components associated with this net are modeled using RLC model as shown in FIGURE 13. FIGURE 15 shows accuracy comparison of the S_{21} parameter of the package net using both the 3D EM tool as well as the lumped model. As can be seen, the lumped model accuracy is reasonable in the frequency range of interest.

Two noise sources generated by superimposing multiple sine waves are applied at the power supply and

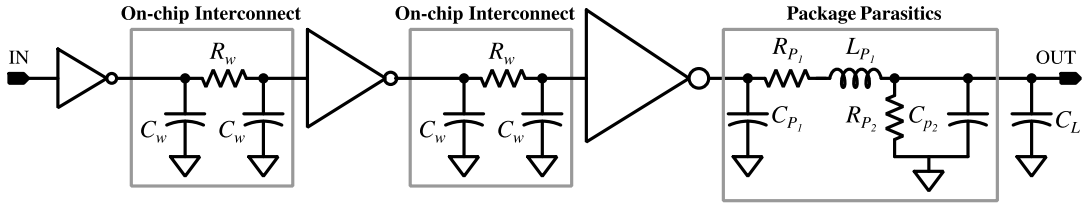

FIGURE 13. A tapered buffer with off-chip load (Example-3).

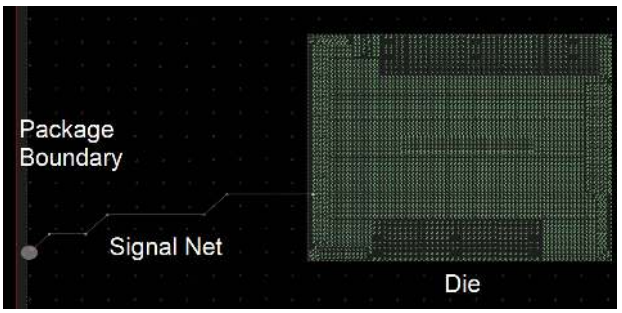

FIGURE 14. Physical layout of the package net (Example-3).

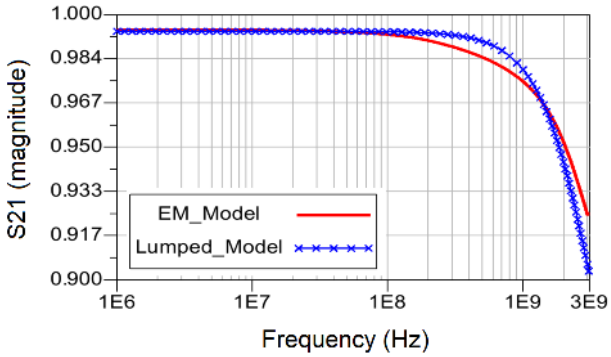

FIGURE 15. Accuracy comparison of the S_{21} parameters of the package net using both the 3D EM tool as well as the lumped model (Example-3).

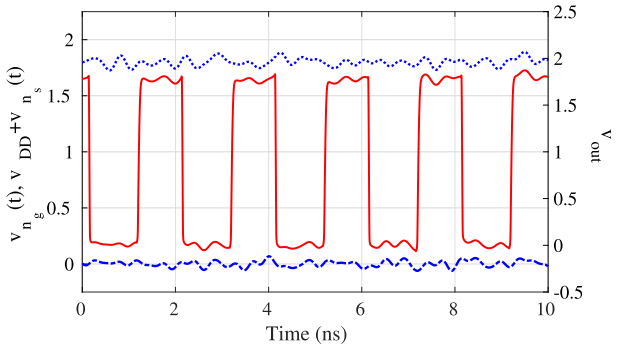

FIGURE 16. Distorted output waveform (right y-axis: Solid-line) in the presence of power supply noise (left y-axis: Top dotted-line) and ground noise (left y-axis: Bottom dashed-line) (Example-3).

ground terminals. The tri-diagonal matrix obtained for the buffer with off-chip load is given in Appendix-C. FIGURE 16 shows both the power supply and ground noise as well as their

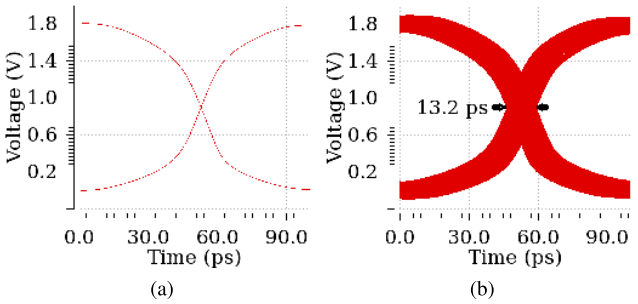

FIGURE 17. Eye crossing at the output of tapered buffer: (a) Without power supply and ground noise (b) With noise at power supply and ground (Example-3).

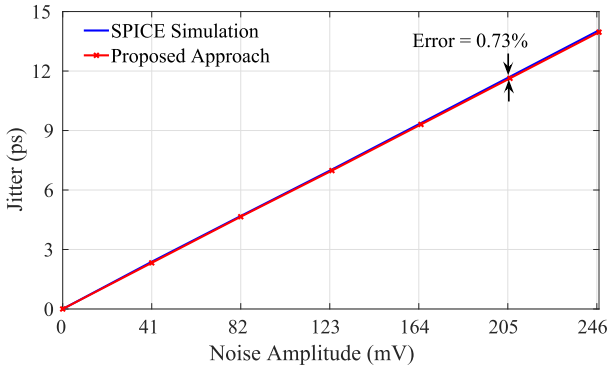

FIGURE 18. Comparison of jitter values calculated using the proposed approach and SPICE based simulation for a chain-of-inverters with nine inverters (Example-3).

TABLE 2. Performance comparison.

Example	Conventional Simulation (SPICE) (sec.)	Proposed Approach (sec.)	Speed up
Example - 1	514	4.17	123.26
Example - 2	672	4.18	160.76
Example - 3	934	4.16	224.51

combined impact on the output response. FIGURE 17 shows the eye-crossings at the output of the buffer when there is no noise present and in the presence of noise at the power supply and ground. The peak-to-peak jitter at the output of buffer is calculated using both the conventional (SPICE) simulation and the proposed approach for various noise amplitudes.

The jitter values obtained using both methods are compared in FIGURE 18.

Table 2 shows the CPU speed-up achieved using the proposed approach (1 bit simulation and analytical relations for 1000 bits) compared to the conventional simulation.

VI. CONCLUSION

A generic and efficient methodology for estimation of power supply induced jitter in a chain of CMOS inverters due to both power supply noise and ground bounce is presented in this paper. The new method can be used for tapered buffers as well as buffers with on-chip interconnects and off-chip loads. A tri-diagonal matrix based algorithm (Thomas algorithm) is developed for closed-form evaluation of transfer functions. Significant speed-up using the proposed method is achieved while providing reasonable accuracy in comparison with conventional simulation.

APPENDIX A
DERIVATION OF GROUND NOISE TRANSFER FUNCTION FOR BUFFERS (WITHOUT ON-CHIP INTERCONNECTS)

Writing the nodal equations for the small-signal circuit in FIGURE 5, by considering only ground noise source V_{n_g},

$$d_{1_g}V_{o1_g} + u_{1_g}V_{o2_g} = b_{1_g}V_{n_g} \tag{76}$$
$$l_{2_g}V_{o1_g} + d_{2_g}V_{o2_g} + u_{2_g}v_{o3_g} = b_{2_g}V_{n_g} \tag{77}$$
$$\vdots$$
$$l_{Q_g}V_{o(Q-1)_g} + d_{Q_g}V_{r_g} = b_{Q_g}V_{n_g} \tag{78}$$

The coefficients used in the above system of equations can be modeled similar to the coefficients in the supply noise transfer function as follows:

$$d_{i_g} = d_i^r + j\omega_g d_i^i \tag{79}$$
$$l_{i_g} = l_i^r + j\omega_g l_i^i \tag{80}$$
$$u_{i_g} = u_i \tag{81}$$

These system of equations can be written in terms of matrix form as given in (35)-(37), where $\boldsymbol{A}_g(j\omega_g)$ has similar form as that in (26) and $\boldsymbol{A}_1$ & $\boldsymbol{A}_2$ can be re-used from (24) and (25).

APPENDIX B
DERIVATION OF GROUND NOISE TRANSFER FUNCTION FOR BUFFERS WITH ON-CHIP INTERCONNECTS

Writing the nodal equations for the small-signal circuit in FIGURE 6, by considering only ground noise source V_{n_g},

$$\tilde{d}_1V_{o1_g} + \tilde{u}_1V_{i2_g} = \tilde{b}_1V_{n_g} \tag{82}$$
$$\tilde{l}_2V_{o1_g} + \tilde{d}_2V_{i2_g} + \tilde{u}_2V_{o2_g} = \tilde{b}_2V_{n_g} \tag{83}$$
$$\tilde{l}_3V_{i2_g} + \tilde{d}_3V_{o2_g} + \tilde{u}_3V_{i3_g} = \tilde{b}_3V_{n_s} \tag{84}$$
$$\vdots$$
$$\tilde{l}_{2Q}V_{oQ_g} + \tilde{d}_{2Q}V_{r_n} = \tilde{b}_{2Q}V_{n_g} \tag{85}$$

The coefficients used in the above system of equations can be modeled similar to the coefficients in the supply noise transfer function for buffer with interconnects as follows:

$$\tilde{d}_{i_g} = \tilde{d}_i^r + j\omega_g\tilde{d}_i^i \tag{86}$$
$$\tilde{l}_{i_g} = \tilde{l}_i^r + j\omega_g\tilde{l}_i^i \tag{87}$$
$$\tilde{u}_{i_g} = \tilde{u}_i^r + j\omega_g\tilde{u}_i^i \tag{88}$$

These system of equations can be written in terms of matrix form as given in (70)-(72), where $\tilde{\boldsymbol{A}}_g(j\omega_g)$ has similar form as that in (69) and $\tilde{\boldsymbol{A}}_1$ & $\tilde{\boldsymbol{A}}_2$ can be re-used from (67) and (68).

APPENDIX C
FORMULATION OF TRI-DIAGONAL MATRIX FOR EXAMPLE-3

Note that, in Example-3, the coefficients of the matrix at the output node is different from previous cases. The modified coefficients are given below.

$$\tilde{d}_{i_s} = \begin{cases} G_w + g_{ds_{\frac{i+1}{2}}} + j\omega_s C'_{L_i}; \\ \qquad i = 1, 3, \ldots, (2Q-3) \\ G_w + j\omega_s C_{L_i}; \\ \qquad i = 2, 4, \ldots, (2Q-2) \\ G_{P_1} + g_{ds_{\frac{i+1}{2}}} + j\omega_s\chi_i; \\ \qquad i = (2Q-1) \\ \dfrac{1}{R_{P_1} + j\omega_s L_{P_1}} + j\omega_s(C_{P_2} + C_L); \\ \qquad i = 2Q \end{cases}$$

$$\chi_i = C_{gd_{\frac{i+1}{2}}} + C_{ds_{p\frac{i+1}{2}}} + C_{ds_{n\frac{i+1}{2}}} + \frac{C_{P_1}}{L_{P_1}} \tag{89}$$

$$\tilde{l}_{i_s} = \begin{cases} 0; & i = 1 \\ G_w; & i = 2, 4, \ldots, (2Q-2) \\ j\omega_s C_{gd_{\frac{i+1}{2}}} - g_{m_{\frac{i+1}{2}}}; & i = 3, 5, \ldots, (2Q-1) \\ \dfrac{1}{R_{P_1} + j\omega_s L_{P_1}}; & i = 2Q \end{cases}$$

$$g_{m_{\frac{i+1}{2}}} = g_{m_{p\frac{i+1}{2}}} + g_{m_{n\frac{i+1}{2}}} \tag{90}$$

$$\tilde{u}_{i_s} = \begin{cases} G_w; & i = 1, 3, \ldots, (2Q-3) \\ j\omega_s C_{gd_{\frac{i+2}{2}}}; & i = 2, 4, \ldots, (2Q-2) \\ \dfrac{1}{R_{P_1} + j\omega_s L_{P_1}}; & i = (2Q-1) \\ 0 & i = 2Q \end{cases} \tag{91}$$

$$\tilde{b}_{i_s} = \begin{cases} g_i + j\omega_s C_{ds_{p\frac{i+1}{2}}}; & i = 1, 3, \ldots, (2Q-1) \\ j\omega_s C_{gs_{p\frac{i+2}{2}}}; & i = 2, 4, \ldots, (2Q-2) \\ 0; & i = 2Q \end{cases}$$

$$g_{i_p} = g_{m_{p\frac{i+1}{2}}} + g_{ds_{p\frac{i+1}{2}}} \tag{92}$$

For the transfer function from ground bounce, the coefficients $\tilde{d}_{i_g}$, $\tilde{l}_{i_g}$ and $\tilde{u}_{i_g}$ can be obtained by replacing ω_s with ω_g in the

above expressions. The coefficient b_{i_g} is given below.

$$\tilde{b}_{i_g}=\begin{cases} g_i + j\omega_g(C_{ds_{n\frac{i+1}{2}}} + \dfrac{C_w}{2}); & i=1,3,\ldots,(2Q-3) \\ j\omega_g(C_{gs_{n\frac{i+2}{2}}} + \dfrac{C_w}{2}); & i=2,4,\ldots,(2Q-2) \\ g_i + j\omega_g(C_{ds_{n\frac{i+1}{2}}} + \dfrac{C_{P_1}}{L_{P_1}}); & i=(2Q-1) \\ G_{P_2} + j\omega_g C_{P_2} + C_L; & i=2Q \end{cases}$$

$$g_{i_n}=g_{m_{n\frac{i+1}{2}}} + g_{ds_{n\frac{i+1}{2}}} \tag{93}$$

REFERENCES

[1] K. S. D. Oh and X. C. C. Yuan, *High-Speed Signaling Jitter Modeling, Analysis, and Budgeting*. Upper Saddle River, NJ, USA: Prentice-Hall, 2012.

[2] M. P. Li, *Jitter, Noise, and Signal Integrity at High-Speed*. Upper Saddle River, NJ, USA: Prentice-Hall, 2007.

[3] H. Kim, J. Kim, J. Fan, and C. Hwang, "Precise analytical model of power supply induced jitter transfer function at inverter chains," *IEEE Trans. Electromagn. Compat.*, vol. 60, no. 5, pp. 1491–1499, Oct. 2018.

[4] X. J. Wang and T. Kwasniewski, "Propagation delay-based expression of power supply-induced jitter sensitivity for CMOS buffer chain," *IEEE Trans. Electromagn. Compat.*, vol. 58, no. 2, pp. 627–630, Apr. 2016.

[5] R. Schmitt, H. Lan, C. Madden, and C. Yuan, "Investigating the impact of supply noise on the jitter in gigabit I/O interfaces," in *Proc. IEEE Elect. Perform. Electron. Packag.*, Atlanta, GA, USA, Oct. 2007, pp. 189–192.

[6] J. Kim, J. Lee, S. Cho, C. Hwang, C. Yoon, and J. Fan, "Analytical probability density calculation for step pulse response of a single-ended buffer with arbitrary power-supply voltage fluctuations," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 7, pp. 2022–2033, Jul. 2014.

[7] J. N. Tripathi, R. Achar, and R. Malik, "Fast analysis of time interval error in current-mode drivers," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 2, pp. 367–377, Feb. 2018.

[8] X. Chu, C. Hwang, J. Fan, and Y. Li, "Analytic calculation of jitter induced by power and ground noise based on IBIS I/V curve," *IEEE Trans. Electromagn. Compat.*, vol. 60, no. 2, pp. 468–477, Apr. 2018.

[9] C. Hwang, J. Kim, B. Achkir, and J. Fan, "Analytical transfer functions relating power and ground voltage fluctuations to jitter at a single-ended full-swing buffer," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 1, pp. 113–125, Jan. 2013.

[10] L. H. Chen, M. Marek-Sadowska, and F. Brewer, "Buffer delay change in the presence of power and ground noise," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 11, no. 3, pp. 461–473, Jun. 2003.

[11] J. Kim, "Statistical analysis for pattern-dependent simultaneous switching outputs (SSO) of parallel single-ended buffers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 1, pp. 156–169, Jan. 2017.

[12] J. N. Tripathi and F. G. Canavero, "An efficient estimation of power supply-induced jitter by numerical method," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 12, pp. 1050–1052, Dec. 2017.

[13] H. Kim, J. Fan, and C. Hwang, "Modeling of power supply induced jitter (PSIJ) transfer function at inverter chains," in *Proc. IEEE Int. Symp. Electromagn. Compat. Signal/Power Integrity (EMCSI)*, Washington, DC, USA, Aug. 2017, pp. 591–596.

[14] J. N. Tripathi, P. Arora, H. Shrimali, and R. Achar, "Efficient jitter analysis for a chain of CMOS inverters," *IEEE Trans. Electromagn. Compat.*, to be published.

[15] E. Park, J. Kim, H. Kim, and K. Shon, "Analytical jitter estimation of two-stage output buffers with supply voltage fluctuations," in *Proc. IEEE Int. Symp. Electromagn. Compat. (EMC)*, Raleigh, NC, USA, Aug. 2014, pp. 69–74.

[16] J. N. Tripathi, V. K. Sharma, H. Advani, P. N. Singh, H. Shrimali, and R. Malik, "An analysis of power supply induced jitter for a voltage mode driver in high speed serial links," in *Proc. IEEE 20th Workshop Signal Power Integrity (SPI)*, Turin, Italy, May 2016, pp. 1–4.

[17] F. Firouzi, S. Kiamehr, and M. B. Tahoori, "Modeling and estimation of power supply noise using linear programming," in *Proc. Int. Conf. Comput.-Aided Design*, San Jose, CA, USA, Nov. 2011, pp. 537–542.

[18] D. Oh, "System level jitter characterization of high speed I/O systems," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, Pittsburgh, PA, USA, Aug. 2012, pp. 173–178.

[19] Y. Duan, H. Wu, M. Shimanouchi, M. P. Li, and D. Chen, "A low-cost comparator-based method for accurate decomposition of deterministic jitter in high-speed links," *IEEE Trans. Electromagn. Compat.*, vol. 61, no. 2, pp. 521–531, Apr. 2019.

[20] C. Sui, S. Bai, T. Zhu, C. Cheng, and D. G. Beetner, "New methods to characterize deterministic jitter and crosstalk-induced jitter from measurements," *IEEE Trans. Electromagn. Compat.*, vol. 57, no. 4, pp. 877–884, Aug. 2015.

[21] Y. Duan and D. Chen, "Fast and accurate decomposition of deterministic jitter components in high-speed links," *IEEE Trans. Electromagn. Compat.*, vol. 61, no. 1, pp. 217–225, Feb. 2019.

[22] L. H. Thomas, "Elliptic problems in linear difference equations over a network," Watson Sci. Comput. Lab. Rep., Columbia Univ., New York, NY, USA, 1949.

[23] M. S. Illikkal, J. N. Tripathi, and H. Shrimali, "Analysing the impact of various deterministic noise sources on jitter in a CMOS inverter," in *Proc. 6th Int. Conf. Signal Process. Integr. Netw. (SPIN)*, Noida, India, Mar. 2019, pp. 208–211.

[24] Y. Tsividis and C. McAndrew, *Operation and Modeling The MOS Transistor (The Oxford Series in Electrical and Computer Engineering)*. New York, NY, USA: Oxford Univ. Press, 2004.

[25] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed. New York, NY, USA: McGraw-Hill, 2001.

[26] J. N. Tripathi, R. Achar, and R. Malik, "Efficient modeling of power supply induced jitter in voltage-mode drivers (EMPSIJ)," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 7, no. 10, pp. 1691–1701, Oct. 2017.

[27] M. Souilem, J. N. Tripathi, W. Dghais, and H. Belgacem, "An IBIS-like modelling for power/ground noise induced jitter under simultaneous switching outputs (SSO)," in *Proc. IEEE 23rd Workshop Signal Power Integrity (SPI)*, Chambéry, France, Jun. 2019, pp. 1–4.

[28] A. Morgenshtein, E. G. Friedman, R. Ginosar, and A. Kolodny, "Unified logical effort—A method for delay evaluation and minimization in logic paths with *RC* interconnect," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 5, pp. 689–696, May 2010.

[29] I. Sutherland, R. F. Sproull, B. Sproull, and D. Harris, *Logical Effort Designing Fast CMOS Circuits*. San Mateo, CA, USA: Morgan Kaufman, 1999.

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