

# A Three-Level Common-Mode Voltage Eliminated Inverter With Single DC Supply Using Flying Capacitor Inverter and Cascaded H-Bridge

P. Roshan Kumar, P. P. Rajeevan, K. Mathew, *Member, IEEE*, K. Gopakumar, *Fellow, IEEE*, Jose I. Leon, *Member, IEEE*, and Leopoldo G. Franquelo, *Fellow, IEEE*

**Abstract**—A three-level common-mode voltage eliminated inverter with single dc supply using flying capacitor inverter and cascaded H-bridge has been proposed in this paper. The three phase space vector polygon formed by this configuration and the polygon formed by the common-mode eliminated states have been discussed. The entire system is simulated in Simulink and the results are experimentally verified. This system has an advantage that if one of devices in the H-bridge fails, the system can still be operated as a normal three-level inverter at full power. This inverter has many other advantages like use of single dc supply, making it possible for a back-to-back grid-tied converter application, improved reliability, etc.

**Index Terms**—Common-mode voltage elimination, hybrid multilevel inverter, multilevel inverter, three-level inverter.

## I. INTRODUCTION

MULTILEVEL inverters have improved the performance of medium- and high-voltage drives [1], [2]. The flying capacitor inverter proposed in [3], the cascaded-H-bridge inverter proposed in [4], and the neutral-point-clamped inverter proposed in [5] are the three basic topologies of a multilevel inverter. The cascaded H-bridge inverter with capacitor-cell and voltage balancing has been proposed in [6] and [7]. In recent times, many hybrid topologies, which are modification to these basic topologies, have been proposed and have their own advantages and disadvantages [8]–[12].

The outputs of these dc–ac converters contain common-mode voltage switched at high frequencies with voltage magnitudes that are comparable to the inverter pole voltages. High frequency switching of the common-mode voltage in the induction motor causes several issues like leakage currents through the stray capacitance between the winding and the body of the motor and create shaft voltages causing bearing currents resulting in bearing failures of the motors [13]–[16].

The effects of common-mode voltage are much more adverse in the case of medium- and high-voltage drives due to high frequency switching of common-mode voltage in the order of few kilovolts. High  $dV/dt$  switching in common-mode voltage causes breakdown of bearing lubricant insulation and causes pitting in the bearing surfaces. This leads to quick failure of bearings as discussed in [17].

Many inverter topologies have been proposed to eliminate the effects of common-mode voltage in induction motor drives. The work presented in [18] gives an idea to eliminate the common-mode voltage by connecting two 2-level inverters to the induction motor which is connected in an open-end winding configuration and switching them appropriately so as to remove the common-mode voltage.

A three-level inverter with common-mode voltage elimination for open-end connected induction motor was presented in [19]. Using a five level-inverter to eliminate common-mode voltage wherein the motor is connected in an open-end winding configuration has been presented in [20]. This configuration requires more number of isolated power supplies and diode bridge rectifiers. The work presented in [21] gives an interesting idea of using a single dc power supply for a three-level common mode voltage eliminated inverter. Many topologies have been presented for removing the common-mode voltage in inverter output when fed to an induction motor drive. However, these configuration need motor to be connected in open-end winding configuration or need multiple isolated power supplies.

In this study, we propose a new three-level common-mode voltage eliminated inverter configuration. In the proposed configuration the motor will be connected in Y configuration as opposed to open-ended configuration. Also, the proposed configuration uses single dc supply. This use of single link dc power supply enables the inverter to be connected in back-to-back configuration with a front end converter so that the power can be drawn from the grid during motoring operation and put back to grid during regeneration (all four quadrant operation) with specific power factor (unity power factor in most cases).

## II. TOPOLOGY

Each phase of the proposed topology consists of a floating capacitor H-bridge with voltage maintained at  $(0.25 V_{dc})$ . This H-bridge is cascaded to a three-level flying capacitor inverter which can generate voltage levels of  $(0.5 V_{dc})$ ,  $0$ ,  $(-0.5 V_{dc})$ . The three-phase power circuit for the proposed configuration is

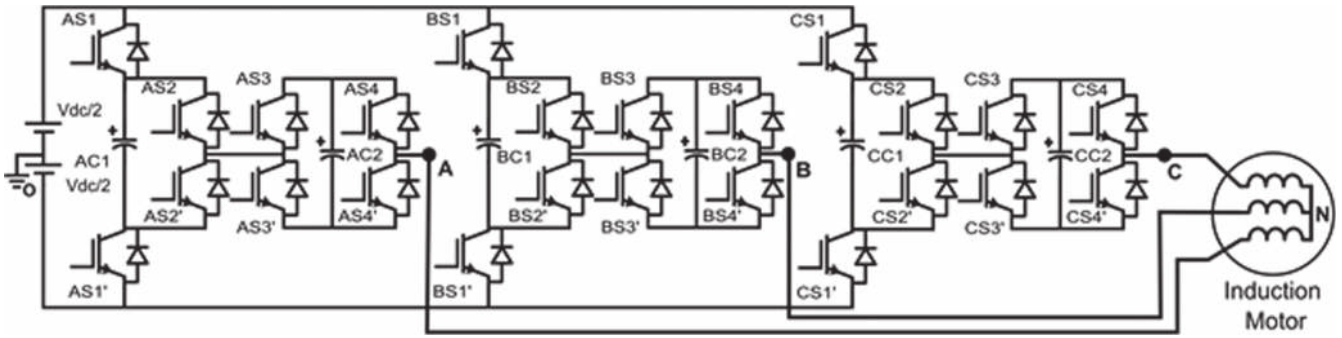


Fig. 1. Power circuit for the proposed three-level common mode voltage eliminated inverter.

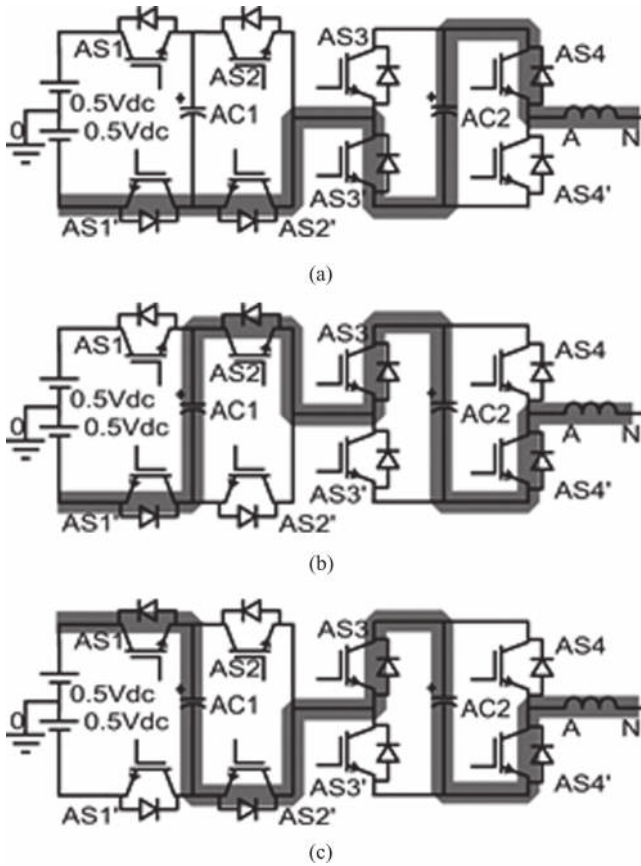


Fig. 2. Switching redundancies for pole voltage of  $-0.25 V_{dc}$ . (a) Path of current flow for switching state (0,0,0,1). (b) Path of current flow for switching state (0,1,1,0). (c) Path of current flow for switching state (1,0,1,0).

shown in Fig. 1. The voltage levels of capacitors AC1, BC1, and CC1 are maintained at  $(0.5 V_{dc})$  and that of AC2, BC2, and CC2 are maintained at  $(0.25 V_{dc})$ . Each pole of the inverter can generate voltage levels which are arithmetic combinations of the two cascaded structures. In the present power circuit, pole voltage levels of  $(-0.5 V_{dc})$ ,  $(-0.25 V_{dc})$ ,  $0$ ,  $(0.25 V_{dc})$ , and  $(0.5 V_{dc})$  can be generated with respect to dc-bus ground (node O in Fig. 1). The top and bottom devices are switched complementarily. Here, switching state of "1" represents the top device is switched ON and the bottom device is switched OFF and vice versa.

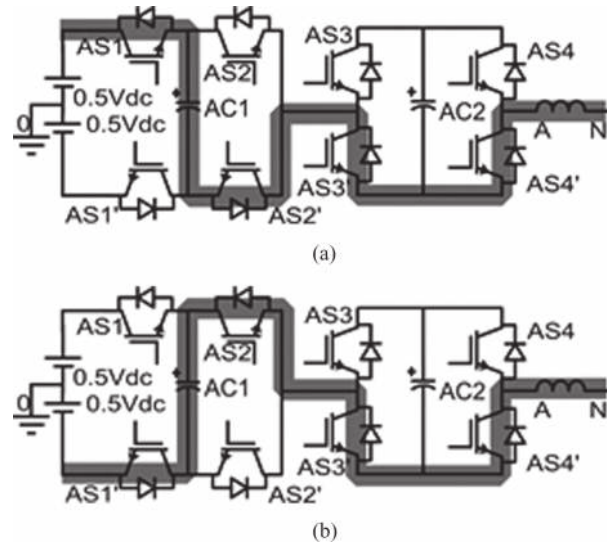


Fig. 3. Redundancies voltages of  $0.25 V_{dc}$ . (a) Path of current flow for switching state (1,0,0,0). (b) Path of current flow for switching state (0,1,0,0).

Fig. 2 depicts the redundant combinations for generating a pole voltage of  $-0.25 V_{dc}$  through various switching combinations. When the switching state of (0,0,0,1) is applied as shown in Fig. 2(a) and for positive direction of current, i.e., when the pole is sourcing current, capacitor AC2 gets discharged while applying the pole voltage of  $-0.25 V_{dc}$ . To charge capacitor AC2, redundant states of (0,1,1,0) and (1,0,1,0) are applied as shown in Fig. 2(b) and (c). In this process, capacitor AC1 gets discharged and charged when states shown in Fig. 2(b) and (c) are applied, respectively. Based on state of charge of capacitors and the direction of current, one of the switching states is applied for generating pole voltage of  $-0.25$ . By switching through all the three redundant states shown in Fig. 2, the voltages of the two capacitors can be maintained at their respective levels. The redundant switching states for pole voltage of  $0 V$  are depicted in Fig. 3. For positive direction of current, switching state (1,0,0,0) [see Fig. 3(a)] is applied to charge capacitor AC1 and state (0,1,0,0) [Fig. 3(b)] is applied to discharge the same, while voltage of AC2 is left unaffected, thereby maintaining the two capacitor voltages at their prescribed values. To generate the pole voltage of  $0.25 V_{dc}$ , switching state of (1,1,1,0) is applied which charges capacitor AC2 as shown in Fig. 4(a). To discharge the same, switching states of (0,1,0,1) and (1,0,0,1) are

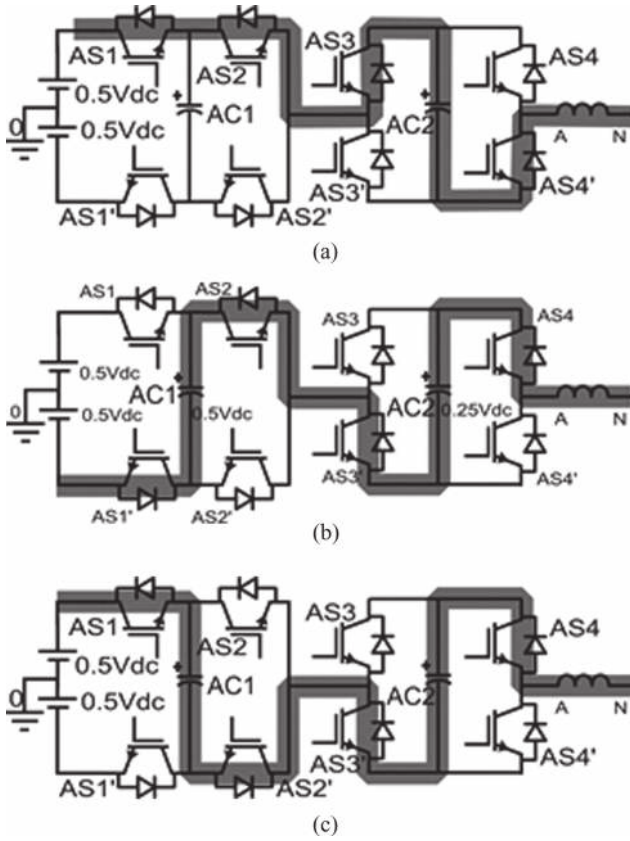


Fig. 4. Redundancies voltages of  $0.25 V_{dc}$ . (a) Path of current flow for switching state (1,1,1,0). (b) Path of current flow for switching state (0,1,0,1). (c) Path of current flow for switching state (1,0,0,1).

applied which discharges and charges capacitor AC1 as shown in Fig. 4(b) and (c), respectively. This helps in maintaining the two capacitor voltages at prescribed values. To generate pole voltage of  $0.5 V_{dc}$ , a switching state of (1,1,1,1) is applied and to generate  $-0.5 V_{dc}$ , a switching state of (0,0,0,0) is applied while the capacitor voltages are unaffected.

A detailed list of pole voltage redundancies and their effect on capacitor voltage for the positive direction of current has been presented in Table I. For the negative direction of current, the capacitor effects shown in the table are complemented. For any pole voltage, based on the state of charge of capacitor and the direction of current, a switching state is applied every switching cycle so as to maintain the capacitor voltage ripple within the prescribed values.

### III. COMMON-MODE VOLTAGE ELIMINATED STATES

There are total of 125 ( $5 \times 5 \times 5$ ) three-phase pole voltage combinations for the proposed inverter. The space vector structure for the voltage levels that are generated from the proposed circuit is as shown in Fig. 5 where the 125 voltage combinations are mapped to 61 locations of the space vector polygon. In-depth analysis of the algorithm for balancing the capacitor voltage at various voltage levels and other aspects of the configuration have been presented in [22]. The common-mode voltage of a Y-connected induction motor is given by (1) where

TABLE I  
CAPACITOR STATES FOR DIFFERENT POLE VOLTAGE REDUNDANCIES FOR POSITIVE CURRENT

Pole Voltage	Switching redundancy <sup>†</sup>	Cap AC1 (0.5Vdc)*	Cap AC2 (0.25Vdc)*
-0.5Vdc	(0,0,0,0)	No effect	No effect
-0.25Vdc	(0,0,0,1)	No effect	Discharge
-0.25Vdc	(0,1,1,0)	Discharge	Charge
-0.25Vdc	(1,0,1,0)	Charge	Charge
0	(0,1,0,0)	Discharge	No effect
0	(1,0,0,0)	Charge	No effect
0.25Vdc	(1,1,1,0)	No effect	Charge
0.25Vdc	(1,0,0,1)	Charge	Discharge
0.25Vdc	(0,1,0,1)	Discharge	Discharge
0.5Vdc	(1,1,1,1)	No effect	No effect

<sup>†</sup>1 indicates top device is ON and 0 indicates bottom device is ON.

\*The capacitor states are complemented for the negative direction of current.

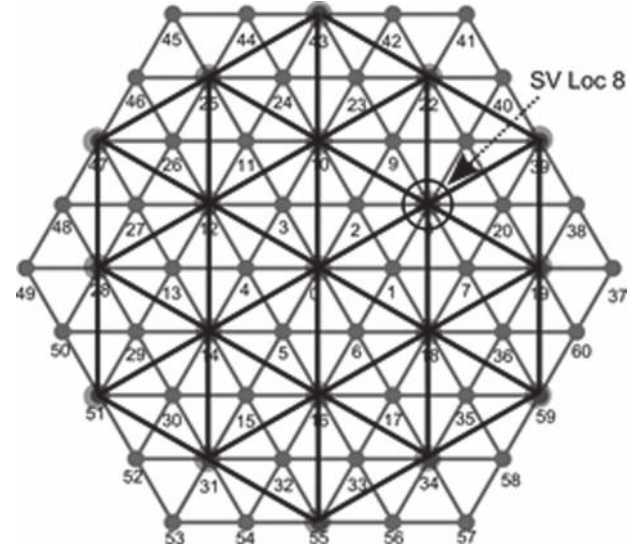


Fig. 5. SV-polygon of the five-level inverter and the locations with zero common-mode voltage locations.

$V_{AO}$ ,  $V_{BO}$ , and  $V_{CO}$  are the pole voltages of the inverter. Of all the 125 pole-voltage combinations formed by the proposed inverter configuration there are 19 combinations for which the common-mode voltage is zero

$$V_{CM} = (V_{AO} + V_{BO} + V_{CO})/3. \quad (1)$$

All the 19 space-vector locations and their pole-voltage combinations for zero common mode have been presented in Table II. The locations with zero common-mode voltage have been highlighted on the five-level space-vector diagram formed



TABLE II  
STATES WITH ZERO COMMON-MODE VOLTAGE

Space Vector Location	Combination of three phase Pole voltages <sup>a</sup>	Pole voltage Combination with zero common mode voltage <sup>a</sup>
0	(-2,-2,-2) (-1,-1,-1) (0,0,0) (1,1,1) (2,2,2)	(0,0,0)
8	(0,-1,-2) (1,0,-1) (2,1,0)	(1,0,-1)
10	(-1,0,-2) (0,1,-1) (1,2,0)	(0,1,-1)
12	(-2,0,-1) (-1,1,0) (0,2,1)	(-1,1,0)
14	(-2,-1,0) (-1,0,1) (0,1,2)	(-1,0,1)
16	(-1,-2,0) (0,-1,1) (1,0,2)	(0,-1,1)
18	(0,-2,-1) (1,-1,0) (2,0,1)	(1,-1,0)
19	(1,-2,-2) (2,-1,-1)	(2,-1,-1)
22	(1,1,-2) (2,2,-1)	(1,1,-2)
25	(-1,2,-1) (-2,1,-2)	(-1,2,-1)
28	(-2,1,1) (-1,2,2)	(-2,1,1)
31	(-1,-1,2) (-2,-2,1)	(-1,-1,2)
34	(1,-2,1) (2,-1,2)	(1,-2,1)
39	(2,0,-2)	(2,0,-2)
43	(0,2,-2)	(0,2,-2)
47	(-2,2,0)	(-2,2,0)
51	(-2,0,2)	(-2,0,2)
55	(0,-2,2)	(0,-2,2)
59	(2,-2,0)	(2,-2,0)

<sup>a</sup> 2, 1, 0, -1, -2 represents pole voltages of  $V_{dc}/2$ ,  $V_{dc}/4$ , 0,  $-V_{dc}/4$ ,  $-V_{dc}/2$ .

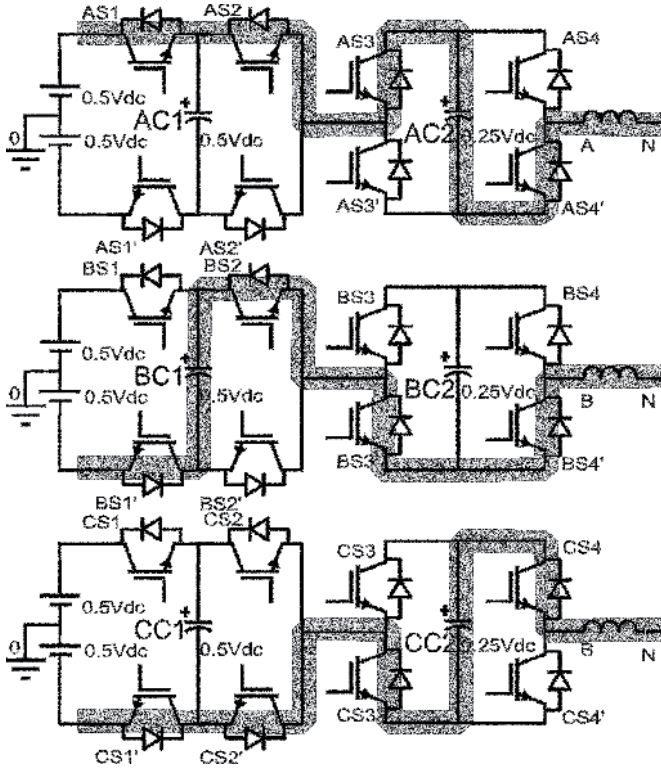


Fig. 6. Three-phase pole voltage combination for SV-location 8.

by the proposed inverter topology in Fig. 5. A three-level space-vector polygon rotated by  $30^\circ$  will be formed with all the zero common-mode voltage combinations for the proposed inverter structure.

Consider a case wherein the controller demands the inverter to generate SV-location 8. The pole voltages are  $(0.25 V_{dc})$ , 0 and  $(-0.25 V_{dc})$  for phases A, B, and C, respectively. One switching combination where poles A and B are sourcing current to the motor and pole C is sinking current is presented in

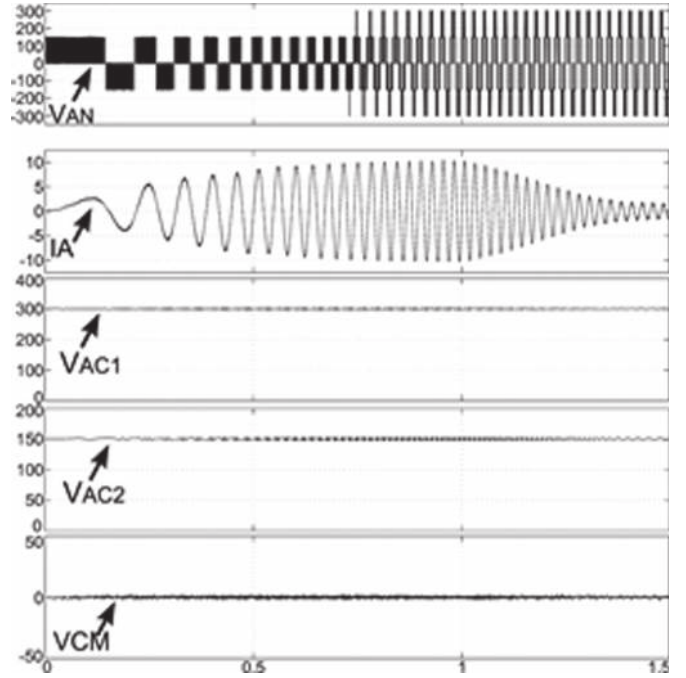


Fig. 7. Simulation result for accelerating the motor throughout the entire modulation range.  $V_{AO}$ : pole voltage (100 V/div),  $I_A$ : pole current (5 A/div),  $V_{AC1}$ : cap1-voltage (100 V/div),  $V_{AC2}$ : cap2-voltage (50 V/div),  $V_{CM}$ : common-mode voltage (50 V/div), time: 500 ms/div.

Fig. 6. Here, the capacitors AC2, CC2 charge, BC1 discharge, while the other capacitor voltages remain unchanged. To balance the capacitors, other redundant states can be applied for the same set of pole voltages as discussed in the previous section in detail.

#### IV. SIMULATION

For simulation, the proposed converter is used with a 3-kW, 400-V, 50-Hz Y-connected induction motor. The converter is run with open-loop V/f control algorithm at various modulation indices and frequencies. The switching frequency of the inverter is set at 1 kHz. The capacitors are sized so that the voltage ripple is 2 V at full load current. A level-shifted carrier-based space vector pulse width modulation (PWM) generation technique, which was presented in [23], was used to generate the gating signals for the switches. The performance of the capacitor-balancing algorithm was tested by accelerating the motor from zero to full speed at no load. The pole voltage, the pole current, the two capacitor voltages, and the common-mode voltage waveforms for the simulation are plotted in Fig. 7. To test the ruggedness of the capacitor balancing algorithm, the algorithm was disabled and re-enabled. The simulation results are presented in Fig. 8. It can be observed that the capacitor voltages deviate from their intended values and the common-mode voltage starts rising when the controller is disabled. Also, it can be observed that on re-enabling the controller, the capacitors are balanced back to their intended values bringing the common-mode voltage back to zero.

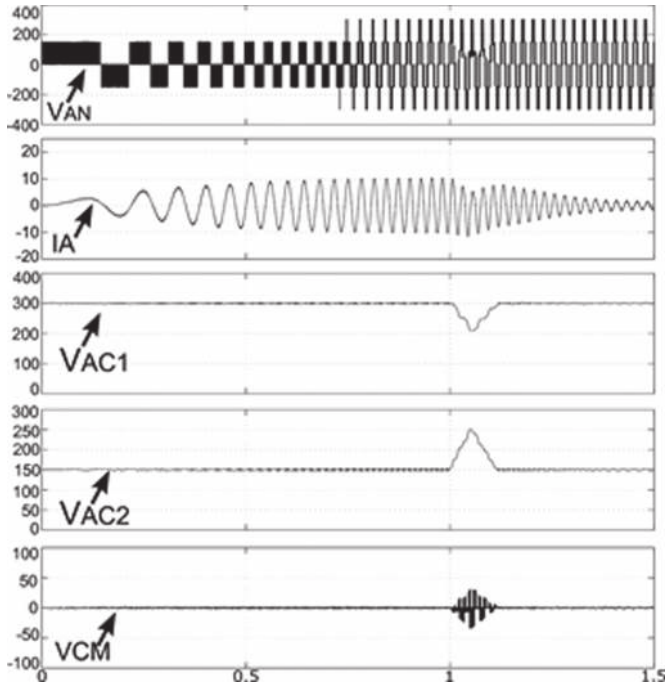


Fig. 8. Simulation result for testing the capacitor balancing algorithm.  $V_{AO}$ : pole voltage (100 V/div),  $I_A$ : pole current (5 A/div),  $V_{C1}$ : cap1-voltage (100 V/div),  $V_{C2}$ : cap2 voltage (50 V/div),  $V_{CM}$ : common-mode voltage (50 V/div), time: 500 ms/div.

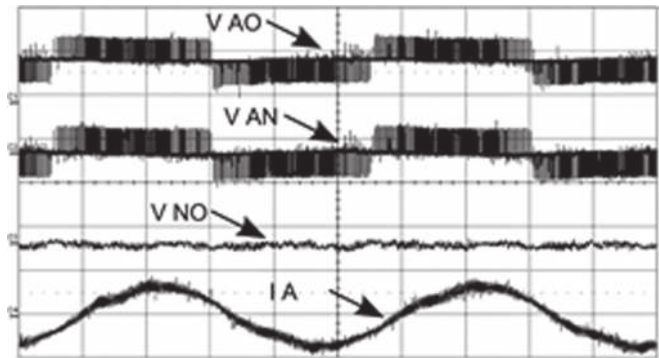


Fig. 9. Steady-state performance at 10 Hz.  $V_{AO}$ : pole voltage (100 V/div),  $V_{AN}$ : phase voltage (100 V/div),  $V_{NO}$ : neutral point voltage (20 V/div),  $I_A$ : phase current (2 A/div), time: 20 ms/div.

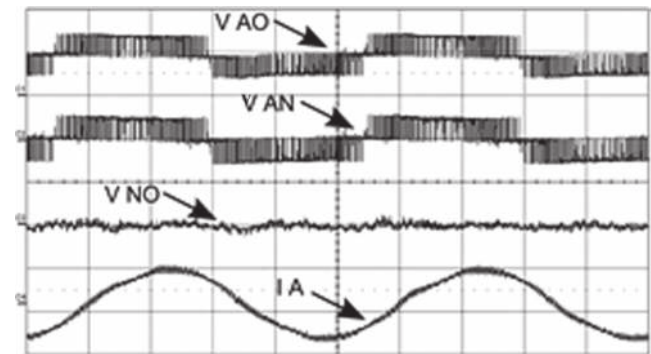


Fig. 10. Steady-state performance at 20 Hz.  $V_{AO}$ : pole voltage (100 V/div),  $V_{AN}$ : phase voltage (100 V/div),  $V_{NO}$ : neutral point voltage (20 V/div),  $I_A$ : phase current (2 A/div), time: 10 ms/div.

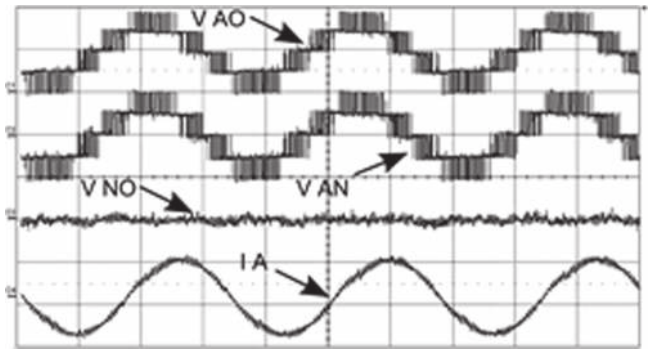


Fig. 11. Steady-state performance at 30 Hz.  $V_{AO}$ : pole voltage (100 V/div),  $V_{AN}$ : phase voltage (100 V/div),  $V_{NO}$ : neutral point voltage (20 V/div),  $I_A$ : phase current (2 A/div), time: 10 ms/div.

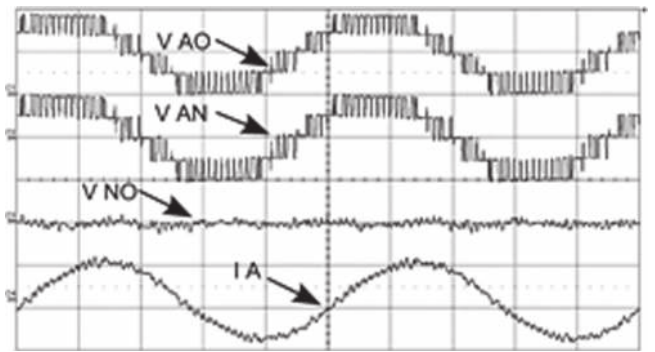


Fig. 12. Steady-state performance at 40 Hz.  $V_{AO}$ : pole voltage (100 V/div),  $V_{AN}$ : phase voltage (100 V/div),  $V_{NO}$ : neutral point voltage (20 V/div),  $I_A$ : phase current (2 A/div).

## V. IMPLEMENTATION

The proposed three-level inverter with common-mode voltage elimination was tested on a 50-Hz, three-phase, Y-connected, 3-kW induction motor. The controller is realized using a TMS320F2812 DSP platform and a Xilinx Spartan-3 XC3200 field-programmable gate array (FPGA) kit. The inverter was constructed using Semikron SK80GM123D insulated gate bipolar transistor (IGBT) modules driven by M56972L hybrid drivers. The capacitor voltages for all the three phases were sampled every switching cycle and are compared with reference value of  $(V_{dc}/2)$  for  $C1$  and  $(V_{dc}/4)$  for  $C2$ . These comparator outputs are fed to the FPGA along with the level data and PWM signals of all three phases from DSP. Based on the comparator output, direction of current, level data, and the PWM signals, one of the redundant pole voltage states is applied to balance the capacitors back to their intended values by changing the direction of current flowing through them. The total dc-bus voltage was chosen as 200 V ( $\pm 100$  V) for verifying the overall system.

The motor was run at frequencies of 10, 20, 30, 40, and 50 Hz, at modulation indices of 0.2, 0.4, 0.6, 0.8, and 0.9 (overmodulation), respectively, at no load. The pole voltage, phase voltage, common-mode voltage, and phase current for 10, 20, 30, 40, and 50 Hz for one of phases are shown in Figs. 9–13, respectively. The pole voltage along with the two capacitor voltages and the phase current for one phase are plotted in Figs. 14–18.



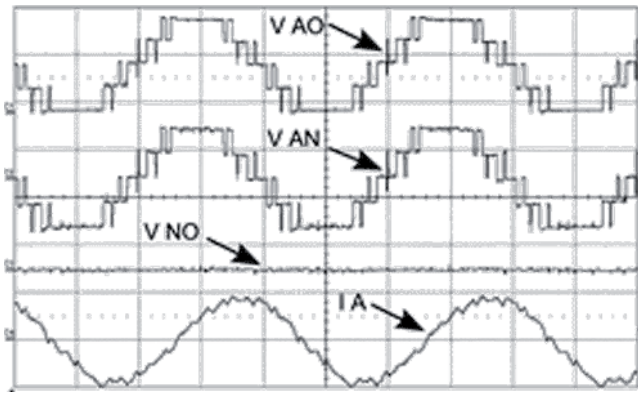


Fig. 13. Steady-state performance at 50 Hz.  $V_{AO}$ : pole voltage (100 V/div),  $V_{AN}$ : phase voltage (100 V/div),  $V_{NO}$ : neutral point voltage (200 V/div),  $I_A$ : phase current (2 A/div), time: 5 ms/div.

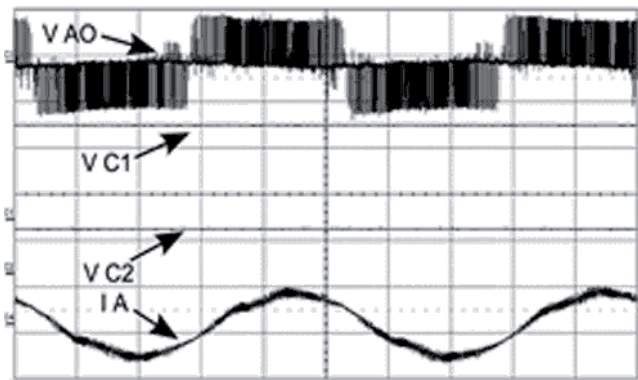


Fig. 14. Steady-state performance at 10 Hz.  $V_{AO}$ : pole voltage (50 V/div),  $V_{C1}$ :  $C1$  ( $V_{dc}/2$ ) cap voltage (50 V/div),  $V_{C2}$ :  $C2$  cap voltage (50 V/div),  $I_A$ : phase current (2 A/div), time: 10 ms/div.

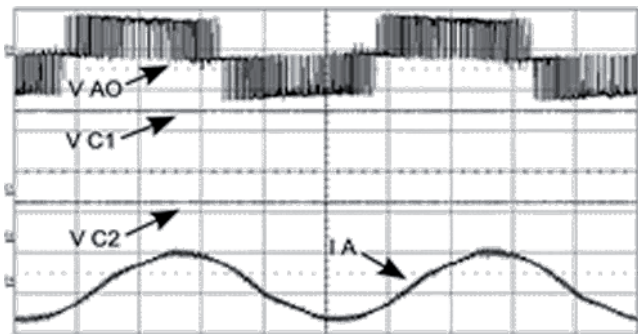


Fig. 15. Steady-state performance at 20 Hz.  $V_{AO}$ : pole voltage (50 V/div),  $V_{C1}$ :  $C1$  cap voltage (50 V/div),  $V_{C2}$ :  $C2$  cap voltage (50 V/div),  $I_A$ : phase current (2 A/div), time: 10 ms/div.

It may be observed from the aforementioned results that the common-mode voltage ripple is negligible compared to the dc-bus voltage at all modulation indices and frequencies. Thus, effects of common-mode voltage that lead to mechanical failure of the machines are mitigated.

The motor was suddenly accelerated at no load, during which the stability of the capacitor balancing algorithm was proven and zero common mode was observed throughout the entire range of modulation indices. The phase voltage, capacitor voltage ripple, and the common-mode voltage waveforms along with the phase

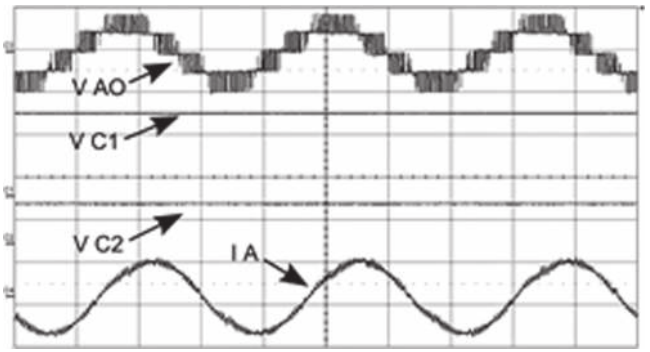


Fig. 16. Steady-state performance at 30 Hz.  $V_{AO}$ : pole voltage (100 V/div),  $V_{C1}$ :  $C1$  cap voltage (50 V/div),  $V_{C2}$ :  $C2$  cap voltage (50 V/div),  $I_A$ : phase current (2 A/div), time: 10 ms/div.

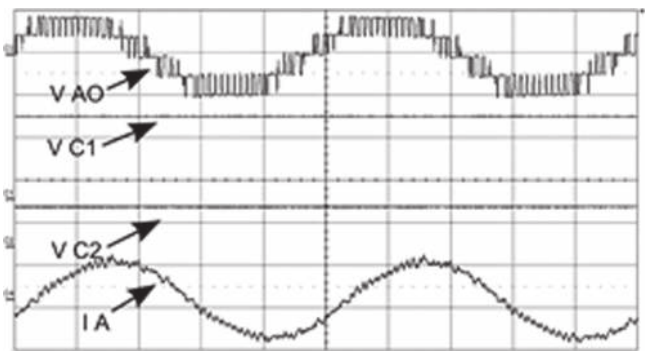


Fig. 17. Steady-state performance at 40 Hz.  $V_{AO}$ : pole voltage (100 V/div),  $V_{C1}$ :  $C1$  cap voltage (50 V/div),  $V_{C2}$ :  $C2$  cap voltage (50 V/div),  $I_A$ : phase current (2 A/div).

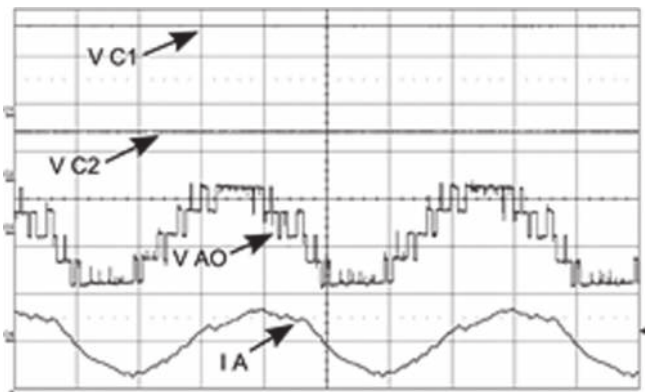


Fig. 18. Steady-state performance at 50 Hz.  $V_{AO}$ : pole voltage (100 V/div),  $V_{C1}$ :  $C1$  cap voltage (50 V/div),  $V_{C2}$ :  $C2$  cap voltage (50 V/div),  $I_A$ : phase current (2 A/div), time: 10 ms/div.

current during the sudden acceleration process are presented in Fig. 19. It can be observed that the capacitor voltage ripple is less than 2 V even when the motor is drawing huge current during the acceleration period.

The stability of the capacitor balancing algorithm was also tested by disabling and re-enabling the same, as shown in Fig. 20. It may be observed that within few cycles after the controller was enabled, the capacitor voltages were restored back to their intended values and the common-mode voltage was brought back to zero. This feature helps in performing the

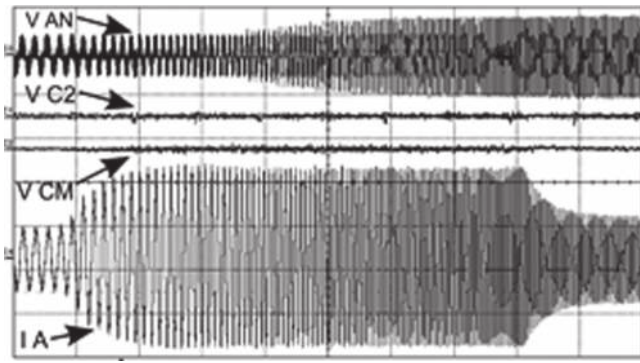


Fig. 19. Acceleration performance.  $V_{AN}$ : phase voltage (100 V/div),  $V_{C2}$ :  $C2$  cap voltage ripple (2 V/div),  $V_{CM}$ : neutral point voltage (10 V/div),  $I_A$ : phase current (2 A/div), time: 500 ms/div.

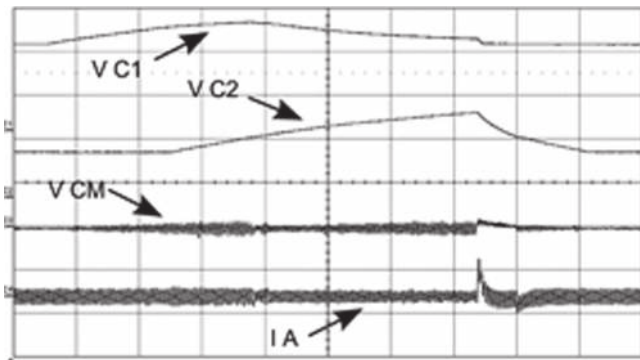


Fig. 20. Capacitor balancing algorithm test,  $V_{C1}$ :  $C1$  ( $V_{dc}/2$ ) cap voltage,  $V_{C2}$ :  $C2$  ( $V_{dc}/4$ ) cap voltage,  $V_{CM}$ : common-mode voltage (10 V/div),  $I_A$ : phase current (10 A/div), time: 500 ms/div.

“start-on-the-fly” operation when the capacitor voltages are not at their intended values. Also, if the capacitor voltages were to momentarily deviate from the desired values, the controller would ensure that the voltages are brought back to their designed values within few fundamental cycles.

## VI. CONCLUSION

In this paper, a three-level common-mode voltage eliminated inverter with single dc supply using flyin capacitor inverter and cascaded H-bridge was proposed and studied. The operation and performance of the proposed inverter is simulated in Simulink with induction motor load. Various aspects of the inverter configuration such as the transients and the performance of the capacitor balancing algorithm, have been studied. The proposed inverter is implemented in hardware using IGBT-based inverters. A three-phase Y-connected induction motor is run with the proposed inverter and the performance of the drive is analyzed for both steady-state operation and transient operation during sudden acceleration. In all the cases, the inverter was able to give faithful reproduction of intended voltage levels with negligible capacitor voltage ripple and common mode, thereby improving the life of bearings. This configuration has various advantages like motor being connected in single-ended configuration use of reduced number of switches, use of single dc supply, etc. Also, this configuration has improved reliability.

In case of failure of one of the devices in the H-bridge, the inverter can still be operated as a normal three-level inverter at full power or a two-level common-mode voltage eliminated inverter at full power rating by bypassing the H-bridges, thereby improving the overall reliability of the system greatly.

## REFERENCES

- [1] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, “The age of multilevel converters arrives,” *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.
- [2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, “Recent advances and industrial applications of multilevel converters,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
- [3] T. A. Meynard and H. Foch, “Multi-level conversion: High voltage choppers and voltage-source inverters,” in *Proc. IEEE 23rd Annu. Power Electron. Spec. Conf.*, Jun. 29–Jul. 3, 1992, vol. 1, pp. 397–403.
- [4] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, “A non-conventional power converter for plasma stabilization,” in *Proc. IEEE 19th Annu. Power Electron. Spec. Conf. Rec.*, Apr. 11–14, 1988, vol. 1, pp. 122–129.
- [5] A. Nabae, I. Takahashi, and H. Akagi, “A new neutral-point-clamped PWM inverter,” *IEEE Trans. Ind. Appl.*, vol. 1A-17, no. 5, pp. 518–523, Sep. 1981.
- [6] J. N. Chiasson, B. Ozpineci, and L. M. Tolbert, “A five-level three-phase hybrid cascade multilevel inverter using a single-dc source for a PM synchronous motor drive,” in *Proc. 22nd Annu. IEEE Appl. Power Electron. Conf.*, Feb. 25–Mar. 1, 2007, pp. 1504–1507.
- [7] Z. Du, L. M. Tolbert, J. N. Chiasson, B. Ozpineci, H. Li, and A. Q. Huang, “Hybrid cascaded H-bridges multilevel motor drive control for electric vehicles,” in *Proc. IEEE 37th Power Electron. Spec. Conf.*, Jun. 18–22, 2006, pp. 1–6.
- [8] A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, “A hybrid cascaded converter topology with series-connected symmetrical and asymmetrical diode-clamped H-bridge cells,” *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 51–65, Jan. 2011.
- [9] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, “A new topology of cascaded multilevel converters with reduced number of components for high-voltage applications,” *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3109–3118, Nov. 2011.
- [10] D. Pefitis, G. Tolstoy, A. Antonopoulos, J. Rabkowski, J. Lim, M. Bakowski, L. Ångquist, and H. Nee, “High-power modular multilevel converters with SiC JFETs,” *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 28–36, Jan. 2012.
- [11] P. P. Rodriguez, M. M. D. Bellar, R. R. S. Muñoz-Aguilar, S. S. Busquets-Monge, and F. F. Blaabjerg, “Multilevel-clamped multilevel converters (MLC),” *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1055–1060, Mar. 2012.
- [12] M. F. Kangarlu and E. Babaei, “A generalized cascaded multilevel inverter using series connection of submultilevel inverters,” *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 625–636, Feb. 2013.
- [13] S. Chen, T. A. Lipo, and D. Fitzgerald, “Source of induction motor bearing currents caused by PWM inverters,” *IEEE Trans. Energy Convers.*, vol. 11, no. 1, pp. 25–32, Mar. 1996.
- [14] D. Macdonald and W. Gray, “PWM drive related bearing failures,” *IEEE Ind. Appl. Mag.*, vol. 5, no. 4, pp. 41–47, Jul.–Aug. 1999.
- [15] D. Busse, J. Erdman, R. J. Kerkman, D. Schlegel, and G. Skibinski, “Bearing currents and their relationship to PWM drives,” *IEEE Trans. Power Electron.*, vol. 12, no. 2, pp. 243–252, Mar. 1997.
- [16] M. J. Costello, “Shaft voltages and rotating machinery,” *IEEE Trans. Ind. Appl.*, vol. 29, no. 2, pp. 419–426, Mar.–Apr. 1993.
- [17] J. Adabi, F. Zare, G. Ledwich, and A. Ghosh, “Leakage current and common mode voltage issues in modern AC drive systems,” in *Proc. Australasian Univ. Power Eng. Conf.*, Dec. 9–12, 2007, pp. 1–6.
- [18] M. R. Baiju, K. K. Mohapatra, R. S. Kanchan, and K. Gopakumar, “A dual two-level inverter scheme with common mode voltage elimination for an induction motor drive,” *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 794–805, May 2004.
- [19] R. S. Kanchan, P. N. Tekwani, M. R. Baiju, K. Gopakumar, and A. Pittet, “Three-level inverter configuration with common-mode voltage elimination for induction motor drive,” *IEE Proc. Electr. Power Appl.*, vol. 152, no. 2, pp. 261–270, Mar. 4, 2005.

- [20] P. N. Tekwani, R. S. Kanchan, and K. Gopakumar, "Five-level inverter scheme for an induction motor drive with simultaneous elimination of common-mode voltage and DC-link capacitor voltage imbalance," *IEEE Proc. Electr. Power Appl.*, vol. 152, no. 6, pp. 1539–1555, Nov. 4, 2005.
- [21] R. S. Kanchan, P. N. Tekwani, and K. Gopakumar, "Three-level inverter scheme with common mode voltage elimination and DC link capacitor voltage balancing for an open-end winding induction motor drive," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1676–1683, Nov. 2006.
- [22] P. Roshankumar, P. P. Rajeevan, K. Mathew, K. Gopakumar, J. I. Leon, and L. G. Franquelo, "A five-level inverter topology with single-dc supply by cascading a flyin capacitor inverter and an H-bridge," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3505–3512, Aug. 2012.
- [23] R. S. Kanchan, M. R. Baiju, K. K. Mohapatra, P. P. Ouseph, and K. Gopakumar, "Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages," *IEEE Proc. Electr. Power Appl.*, vol. 152, no. 2, pp. 297–309, Mar. 2005.



**P. Roshan Kumar** received the B.E. degree in electrical and electronics engineering from Acharya Nagarjuna University, Guntur, India, in 2006, and the M.Tech. degree in electronic design from the Centre for Electronics Design and Technology, Indian Institute of Science, Bengaluru, India, in 2010, where he is currently working toward the Ph.D. degree.

His research interests include renewable energy systems, power electronics, and electro mechanic systems.



**P. P. Rajeevan** received the B.Tech. degree in electrical engineering from the University of Calicut, Kozhikode, India, and the M.E. degree in power electronics from Bangalore University, Bengaluru, India. He is currently working toward the Ph.D. degree at the Centre for Electronics Design and Technology, Indian Institute of Science, Bengaluru.

His research interests include multilevel power converters, drives, PWM techniques and power quality



**K. Mathew** (M'84) received the B.E. degree in electronics and communication engineering from KVG Engineering College, Mangalore, India, in 1994, and the M.Tech. degree in electronic design from the Centre for Electronics Design and Technology, Indian Institute of Science, Bangalore, India, in 2006, where he is currently working toward the Ph.D. degree.

He is a faculty member in the Department of Electronics Engineering, Mar Athanasius College of Engineering, Kothamangalam, India. His research interests include embedded systems, power electronics,

and electro mechanic systems.



**K. Gopakumar** (M'94–SM'96–F'11) received the B.E., M.Sc. (Eng.), and Ph.D. degrees from the Indian Institute of Science, Bengaluru, India, in 1980, 1984, and 1994, respectively.

From 1984 to 1987, he was with the Indian Space Research Organization, Bengaluru. He is currently the Chairman and Professor at the Center for Electronics Design and Technology, Indian Institute of Science. His research interests include pulse width modulation converters and high power drives.

Dr. Gopakumar is a Fellow of Institution of Electrical and Telecommunication Engineers, India, and the Indian National Academy of Engineers. He is currently an Associate Editor of the *IEEE TRANSACTION ON INDUSTRIAL ELECTRONICS*.



**Jose I. Leon** (S'04–M'07) was born in Cádiz, Spain, in 1976. He received the B.S., M.S., and Ph.D. degrees in telecommunications engineering from the University of Seville (US), Seville, Spain, in 1999, 2001, and 2006, respectively.

He is currently an Associate Professor with the Department of Electronic Engineering, US. His research interests include electronic power systems, modulation and control of power converters, and industrial drives.

Dr. Leon was recipient as coauthor of the 2008 Best Paper Award of the *IEEE Industrial Electronics Magazine*.



**Leopoldo G. Franquelo** (M'84–SM'96–F'05) received the M.Sc. and Ph.D. degrees in electrical engineering from the University of Seville, Seville, Spain, in 1977 and 1980, respectively.

From 1998 to 2005, he was the Head of the Department of Electronics Engineering, University of Seville, where he is currently a Full Professor and the Head of the Power Electronics Group. He is author of more than 60 publications in international journals and 180 papers in international conference proceedings. He is the holder of ten patents and participated

in 96 R&D projects. His current research interests include modulation techniques for multilevel inverters and its application to power electronic systems for renewable energy systems.

Dr. Franquelo was the Vice President of the Industrial Electronics Society (IES) Spanish Chapter during 2002–2003 and a member at large of the IES Administrative Committee during 2002–2003. He was the Vice President for conferences during 2004–2007, in which he has also been a Distinguished Lecturer since 2006. Since 2007, he has been an Associate Editor for the *IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS*. He was the President of IES during 2010–2011.