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A Novel Three-Level Isolated AC-DC PFC Power Converter Topology with Reduced Number of Switches

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A Novel Three-Level Isolated AC-DC PFC Power Converter Topology with Reduced Number of Switches

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by

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ABSTRACT

The three-level isolated AC-DC power factor corrected (PFC) converter provides safe and more efficient power conversion. In comparison with two-level, three-level PFC converter has the advantages of low total harmonic distortion, low device voltage rating, low d_i/d_t, better output performance, high power factor, and low switching losses at higher switching frequencies. The high frequency transformer (HFT) grants galvanic isolation, steps up or down secondary voltage, and limits damage in case of a fault current.

The existing three-level converter based on solid-state transformer (SST) topologies convert ac power from the electrical grid to a dc load while maintaining at least the minimum requirements set by the international standards (i.e., high power factor and low total harmonic distortion). The SST topologies with the capability of controlling intermediate dc-bus and output voltage simultaneously require two full bridges at the primary and secondary side of the HFT. As the power level increases, the number of cascaded bridges increases accordingly, and the price associated with these semiconductor devices becomes highly expensive. As result, the demand of converting high power level led to emphasis on high performance and cost-effective power conversion topology.

The aim of this dissertation is to develop a new low-cost and high-performance three-level isolated AC-DC (PFC) converter topology. The proposed topology replaces the conventional three-level inverter in the secondary side of the HFT by only two switches and four diodes while still maintaining the basic functionality of a three-level converter (i.e., regulating the output voltage, controlling the dc-bus voltage to be within desired limits). The advantages of this new topology are: (1) low conduction losses; (2) low-cost; (3) no need to consider the issue of the

power backflow; (4) zero-voltage switching (ZVS) and zero-current switching (ZCS) at turn ON are inherently guaranteed without any extra control effort.

Two isolated three-level AC-DC power converter topologies are developed and investigated through the dissertation. First topology is based on the neutral point clamping (NPC) converter, and the second topology composed of the T-type converter. Two scale-down prototypes rated at 900-W and 1kW, 200 V are built to test the overall performance of the proposed topologies. The first and second topologies exhibit 94.5 % and 95.8 % efficiency scaled at a nominal power, respectively. The secondary bridge (novel circuit) in both topologies, which consists of two switches and four diodes, has 99.34 % practical efficiency.

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DEDICATION

This dissertation is dedicated to my parents, Martha Aldosari and Haia Aldosari. You have been with me in every step of the way, through good and bad ones. Thank you for the unconditional love, guidance, and support you have given me.

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[3.1] O. Aldosari, L. A. Garcia Rodriguez, G. G. Oggier and J. C. Balda, "A Three-Level Isolated AC-DC PFC Power Converter Topology with Reduced Number of Switches," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*. doi: 10.1109/JESTPE.2019.2962704. Published.

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INTRODUCTION AND BACKGROUND

1.1 Solid-State Transformer Converter Background

The solid state transformer (SST) technology has gained much attention in the field of power distribution systems [1.1] since its early-developed concept in the 1970s [1.2]. In the last decades, the number of renewable energy resources connected to the electrical networks has increased [1.3]. The SST converters play significant role of interfacing these renewable resources with numerous industrial applications [1.4]. The need to offer high-power quality to customers encourage utilities to employ the SST topologies in their power networks. A review of SST technologies and their applications in power distribution system is presented in [1.5]. The SST converter has three main functionalities: 1) galvanic isolation between the main source and the load; 2) ability to step up or down the voltage to meet specific application requirements; and 3) controlling the power flow and fault current limitation [1.1].

Nowadays, the advancement in reliable wide bandgap semiconductor devices technology increases the demand for more efficient SST converter topologies to replace the large volume and bulky conventional transformer [1.6]. The latest developments in semiconductor technology (i.e., 10 kV SiC MOSFET) promotes SST converters to be used in high-voltage applications; i.e., 7 kV/400 V DC data center [1.7]. However, the devices ratings are still the limitation for employing such converters in high-voltage levels. Hence, multi-level converters, for example, three-level converters (i.e., neutral point clamped (NPC)), are preferred over the two-level ones especially for high-power applications.

As the rated power of an application increases, the price associated with the SST topology increases as well. That is because, active switches do not support a high-voltage or current and

there is a need to connect the switches in parallel or in series to sustain the application current and voltage ratings. In high-power applications where modular multilevel AC-DC converters are required, the issue of unbalancing power in each module presents instability problem [1.8].

The basic structure of a single-phase isolated ac-dc converter is composed of ac-dc rectifier and SST dc-dc converter that includes a high frequency transformer (HFT) and power electronic converters as shown in Fig. 1.1. The operating frequency of the HFT is one of the parameters that defines the size of the magnetic cores [1.9]. For that reason, the primary and secondary converters operate at higher frequency resulting in much compact sizes when compared to the conventional 60/50 Hz transformer.

The remainder of this chapter is organized as follows: Section 1.2 provides an overview of the existing single-phase isolated AC-DC power factor corrected (PFC) converters including two- and three-level topologies; Section 1.3 presents the research focus and objectives; Section 1.4 gives a brief description of the proposed two topologies; Section 1.5 shows the conventional and the proposed design steps of HFT; and Section 1.6 describes how this dissertation is organized.

1.2 Existing Isolated Single-Phase AC-DC (PFC) Topologies

The isolated AC-DC PFC converters operate at high power factors (PF) to comply with international standards, such as IEC 1000-3-2 [1.10].

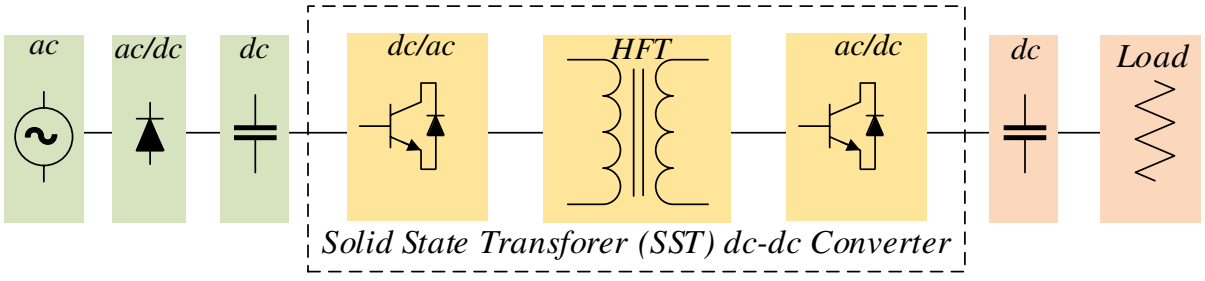

Figure 1.1: Solid-State Transformer (SST) configuration.

One method to guarantee a high PF is to connect passive filter components (inductor and capacitors) at the input terminals to shape the input current to a sine waveform and in phase with the input voltage [1.11]. However, the overall system becomes bulky and difficult to handle due to the size of the passive elements. Another method is to insert a boost inductor between the input and the front end rectifier to boost the intermediate dc-bus voltage to a high level (i.e., [$V_{dc} > 2V_{in(pk)}$]) [1.12].

Isolated single-phase AC-DC PFC topologies can be characterized into two categories: mainly, two- and three-level isolated AC-DC PFC converters. Developed two-level topologies are constructed from buck, boost and buck-boost converters. These types of converters are suitable for low-power applications (i.e., few Watts to several kW) [1.13]. The three-level topologies based on the neutral-point-clamped (NPC) converter [1.14] and the three-level T-type converter ($3LT^2C$) are used for higher power applications.

1.2.A Two-Level Topologies

The two-level topologies are classified into three major circuit structures (i.e., buck, boost, and buck-boost). These types of converters are suitable for low-power applications such as medical equipment, small rating ASDs in fans, and telecommunication applications. Fig. 1.2 shows the classification of the two-level converter family [1.15] that depends on the circuit topology. Some of these converters are used for low-power applications; and other can be used for higher power applications. For instance, isolated buck forward AC-DC converter shown in Fig. 1.3 is appropriate for low-power application i.e., 1-kW, 48-V isolated battery charger. At the front end, the AC-DC stage rectifies the AC source to an uncontrolled dc-bus voltage.

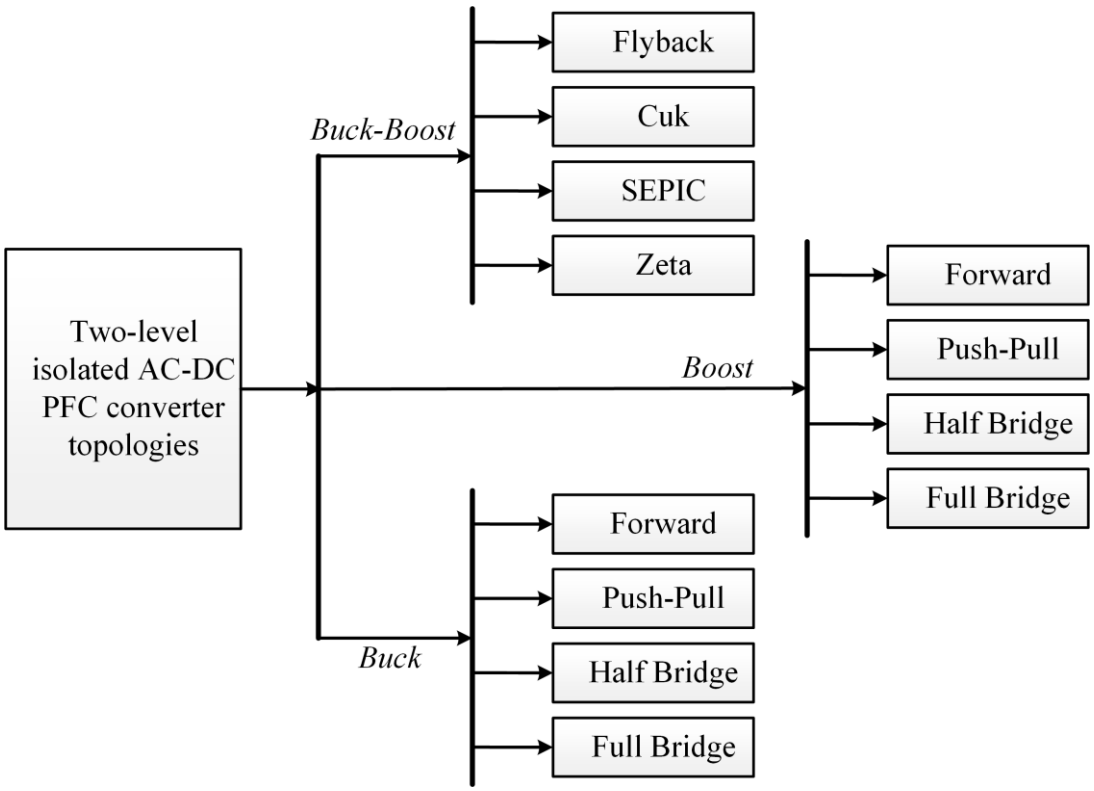

Figure 1.2: Classification of two-level isolated AC-DC PFC converter family.

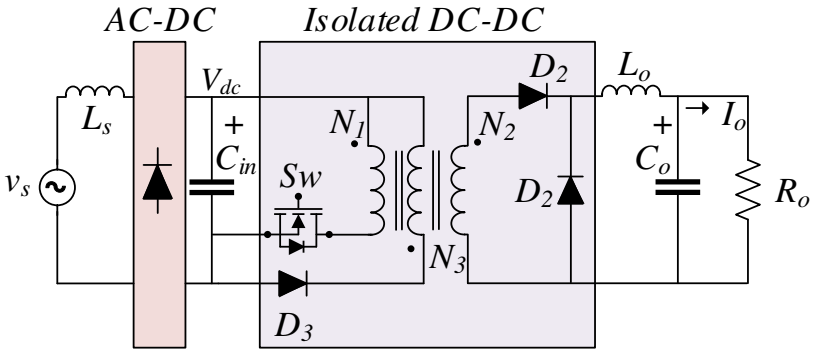

Figure 1.3: Isolated buck forward AC-DC converter.

The intermediate dc-capacitance C_{in} supplies the output through an isolated forward dc-dc converter. During the ON state, primary current makes the secondary current to flow through D_2 and energy is transferred directly to the output load. Unlike the flyback converter which stores the energy in the primary windings during the ON state and then transfers the power to the load during the OFF time [1.16]. The parameters needed to control the output voltage of the isolated buck

forward converter are the switch duty cycle, transformer turn ratio, and input voltage. Usually, the output voltage of the isolated buck forward, push-pull, half-bridge, and full-bridge AC-DC converters is controlled by adjusting the duty cycle of the primary switch [1.15]. Previous researchers provided many different control strategies to operate this type of converters [1.17][1.19].

The main advantages of utilizing the two-level converters are as follows:

1. Cost-effective (few devices).
2. Less control effort.
3. Small size.

The drawbacks of two-level converters are:

1. Higher switching losses at higher switching frequencies (poor efficiency) [1.20].
2. Adverse acoustic noise [1.20].
3. Unable to regulate dc-bus while controlling the output voltage.

1.2.B Three-Level Topologies

The isolated three-level AC-DC power converters are extensively used in many high-power applications; for example, uninterrupted power supplies (UPS), battery charging systems, induction heater, hybrid (AC-DC) microgrids or offshore wind farms, etc. [1.21]-[1.24]. It converts the alternating current (AC) from the utility grid or renewable source (i.e., wind turbine) to a direct current (DC) to supply a dc-load through a HFT. Fig. 1.4 shows an illustration of the overall network structure of these types of converters.

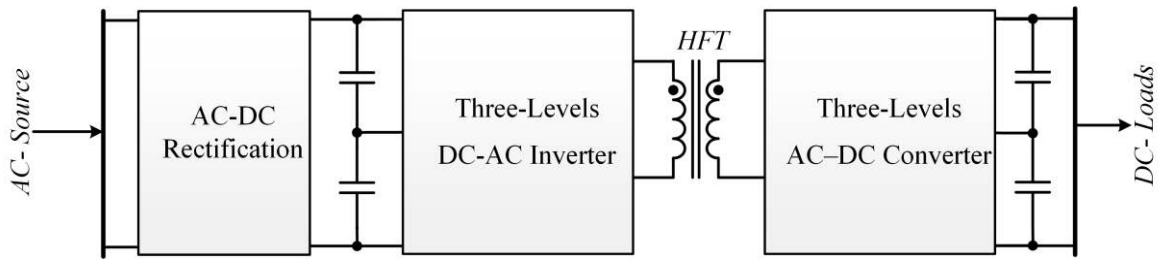

Figure 1.4: Network representation of isolated three-level AC-DC power converter.

These converters must operate while complying with international standard requirements [1.25], [1.26] to improve the power quality at the grid (i.e., the AC source) and deliver reliable energy to the costumers. The AC-DC rectification consists of a full or half diode bridge rectifier and/or controlled rectifier to convert the ac input to a dc voltage. The three-level DC-AC inverter (i.e., NPC, T-type, and H-bridge) lies between the intermediate dc-bus capacitor and the primary terminals of the HFT and inverts the dc-current to ac-current at high frequency. The last stage (i.e., three-level AC-DC converter) rectifies the secondary AC-current of the transformer to a DC-current to supply the output capacitors.

For high-power applications in the range of megawatt levels, the inverter at the primary side of the HFT must be cascaded in a series configuration (multilevel converter) to reduce the voltage stress on the semiconductor devices. At the secondary side for low output voltage applications, the converters are connected in parallel to share current between switches. A comprehensive study on multilevel inverters, a survey of topologies, control strategy, and applications are presented in many previous publications [1.27], [1.28], and [1.29]. The NPC converter is the most wildly used multilevel converter since its invention in 1981 [1.30].

The existing three-level isolated AC-DC converter topologies capable of controlling dc-bus and output voltages consist of at least eight active switches to deliver power at high input PF. The most well-known topology is the H-bridge circuit in each stage, as presented in [1.31]. The main

advantages of this topology are bidirectional power-flow capability and full control of the dc-bus and output voltages. However, even this topology has three voltage-levels at the primary terminals ($+V_{dc}$, 0, $-V_{dc}$) and at the secondary terminals ($+V_o$, 0, $-V_o$), the switches sustain the full dc-bus and output voltage which is a major drawback when compared to NPC converter that sustain only half of the dc-bus and output voltages. Another disadvantage is the price associated with the multiple number of switches within this topology especially at high-power levels, which requires cascading multiple converters in parallel or in series. More details regarding this topology will be provided in Chapter 2, section 2.3.1.

Another topology is a unidirectional three-level isolated single-stage PFC converter presented in [1.11]. The advantages of this topology are: 1) low-cost because there are only four active switches; 2) the switches sustain half of the dc-bus voltage; 3) high PF. The main disadvantage is that there is no way to control the dc-bus and output voltages, simultaneously. The pros and cons of this topology will be presented in more detail in Chapter 2, section 2.3.2.

To reduce the number of the devices further, the full diode rectifier is replaced by a half-bridge diode rectifier, as presented in [1.32] and shown in Fig. 1.5.

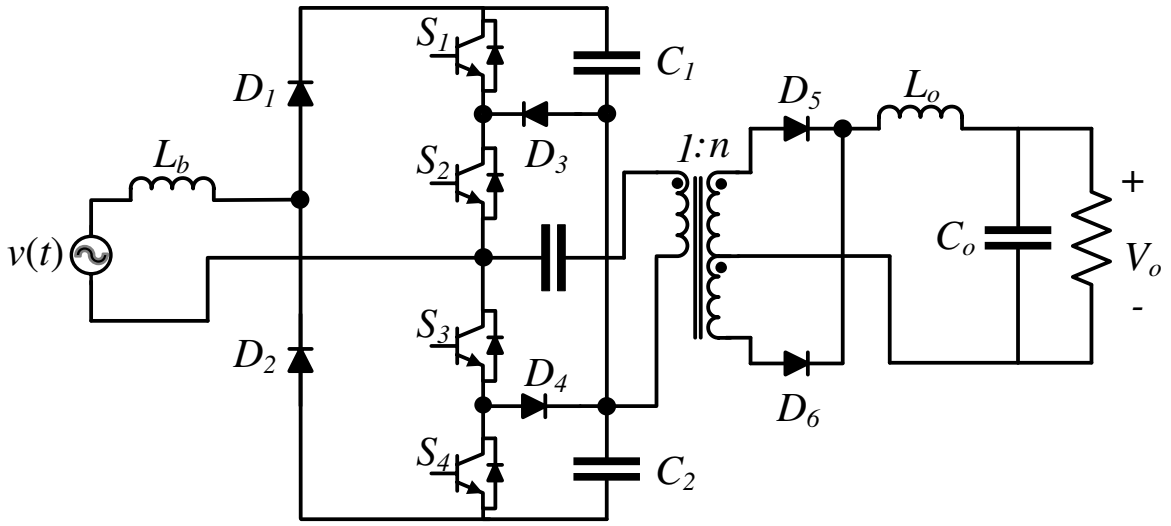

Figure 1.5: Isolated three-level AC-DC power converter with minimum power devices [1.32].

Essentially, this is another version of the NPC converter with a different connection of the dc-bus capacitors. Furthermore, this topology is not capable of regulating the dc-bus voltage and controlling the output voltage at the same time.

To overcome the issue of controlling the dc-bus and output voltages simultaneously, a new solid-state transformer (SST) three-level isolated AC-DC converter was proposed in [1.33] and shown in Fig. 1.6. The benefits of adopting this topology are few power conversions stages, lower voltage stresses on the primary switches and lower currents through the secondary switches. However, the secondary side switches sustain a full output voltage, which is a major drawback of this topology.

Furthermore, the soft-switching region is depending on the mode of operation; that is, the primary duty cycle D_p and the secondary duty cycle D_s may overlap, or partially overlaps, and or fully overlap. For example, at partial overlap, the phase shift D_φ between the primary and secondary voltages should be less than $[(D_p + D_s)/2]$, D_s should be larger than or equal to $[2(1-D_p/2)- D_\varphi]$, and D_s should be larger or equal to $[1-D_p]$.

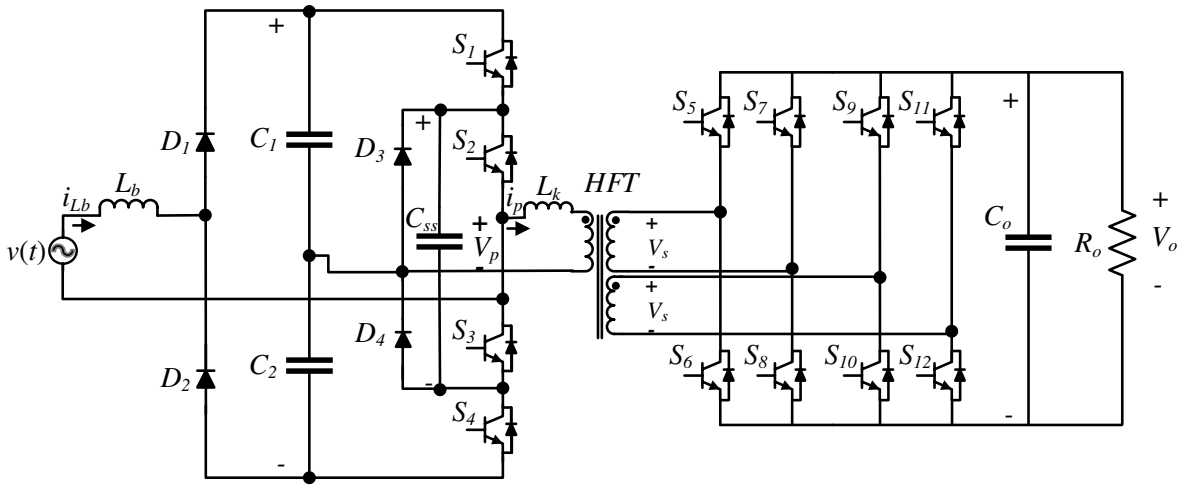

Figure 1.6: Boost-based three-level SST topology [1.33].

These restrictions add more complicity to the control technique and limit the control functionality when the load suddenly increases or decreases. Another disadvantage is the issue of power back-flow between the primary and secondary bridges adding more restrictions and more control effort. Power back-flow happens when current and voltage have different polarities at the same time [1.34]. The source of all the mentioned issues is the secondary-side bridge that needs to be replaced with a new cost-effective and reliable circuit.

1.3 Research Focus and Objectives

This research work focus on developing two novel unidirectional isolated three-level AC-DC PFC topologies. The first topology is based on NPC inverter and the second topology is based on T-type inverter. With only six active switches, both topologies must achieve the following objectives:

1) Shaping the input current to be a sine waveform and in phase with the input voltage to obtain a high PF.
2) Regulating the dc-bus voltage while controlling the output voltage.
3) Operating the converter under soft-switching within a wide range of operation.
4) Achieving all the above objectives with a minimum number of active switches.

This dissertation will focus on defining the steady-state analysis, obtaining the design equations for all the passive components (inductors, capacitors, and HFT), realizing the soft-switching, and recognizing the full characteristic of the propose converters. As a part of this research work, a control strategy of the proposed topology should be introduced. In addition, this dissertation should cover the trade-offs when designing a high-frequency transformer for a specific power converter. The main objective of designing a HFT is to obtain a high efficient HFT and optimize the selection of its magnetic material.

1.4 Proposed Isolated Single-Phase AC-DC PFC Topologies

From the above, it can be concluded that there is a need for a power converter topology that has the following capabilities:

1) Regulating the dc-bus and output voltages at the same time.
2) Controlling the power flowing from the source to the dc-load.
3) Correcting the input PF.

In addition, the operation of the system is nonlinear due to the presence of the semiconductor devices, and converters inject harmonics back into the grid. For that reason, the total harmonics distortion (THD) should be less than a specific value set by international standards. Furthermore, the proposed topologies should achieve the above listed requirements with only six active switches, which is a great contribution work adding to the state of art.

The research motivation is to fill the gap between existing topologies that have a complete functionality of a three-level AC-DC converter, which may be expensive, and those ones that may be cost-effective but not satisfying the above listed capabilities. The above topics are addressed by the following new topologies.

1.4.A Proposed Topology Based on NPC Inverter

The first proposed three-level unidirectional isolated AC-DC PFC converter topology is based on the NPC inverter as shown in Fig. 1.7. The secondary switches (S_5, S_6) and series diodes (D_5, D_6) sustain half of the output voltage, which makes a difference in terms of the cost and the freedom of having a high output voltage without adding series devices. The main function of (S_5, S_6) is to control the phase shift between the primary and secondary voltages.

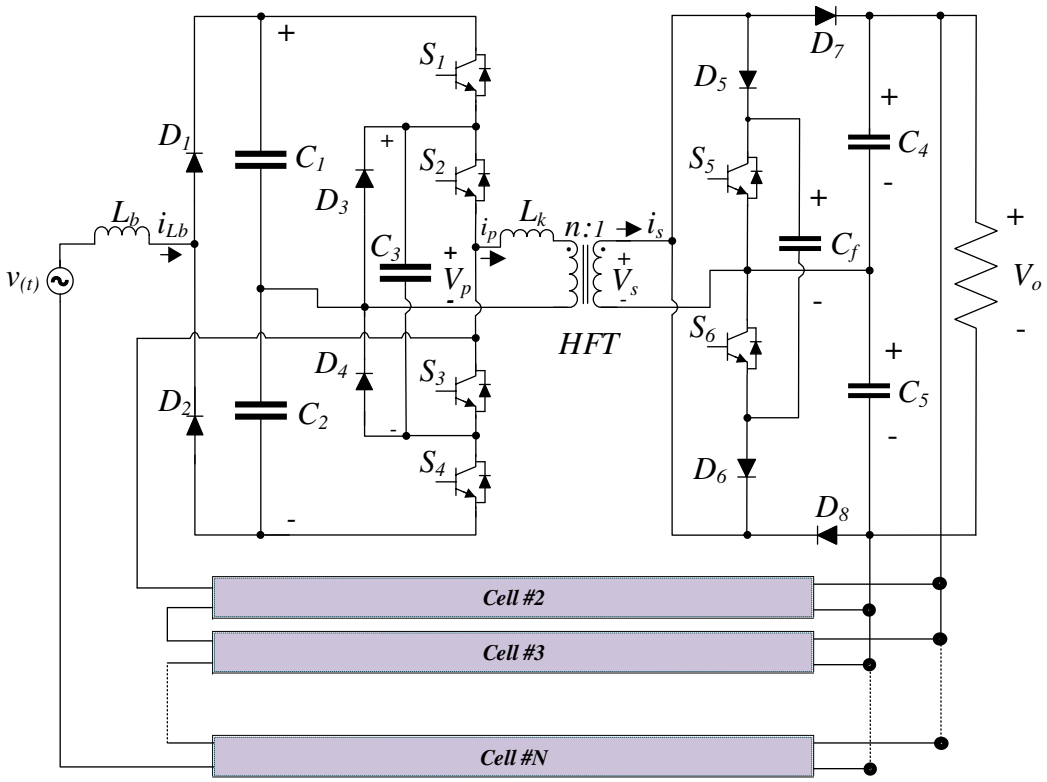

Figure 1.7: Proposed three-level isolated AC-DC PFC topology based on NPC inverter.

The diode (D_5, D_6) is connected in series with the switch (S_5, S_6) to block the secondary current when one of the anti-parallel diodes of (S_5, S_6) is forward bias. The diode (D_7, D_8) prevents shorting the output capacitors (C_4, C_5).

During the (positive or negative) half cycle of the secondary voltage, only one diode (D_7 or D_8) conducts, which reduces the conduction losses and improves the overall efficiency. The flying capacitor C_f connected between the nodes of (D_5, S_5) and (S_6, D_6) acts as a charging and discharging bank of the parasitic capacitances (C_{S5}, C_{S6}) to allow soft-switching action at turning ON. More details about the soft-switching technique of the secondary switches will be given in Chapter 3. This topology is suitable for high-power high-voltage applications because all the primary and secondary switches sustain half of the dc-bus and output voltages.

1.4.B Proposed Topology Based on T-type Inverter

The second topology is a modification of the first topology where the NPC circuit is replaced with a T-type inverter as shown in Fig. 1.8.

The main advantages of T-type topology when compared to the NPC topology are listed below:

- Cost-effective.
- Low conduction losses at higher primary and phase shift duty cycles, only one switch (S_1 or S_4) conducts the primary and boost currents.
- Possibility of generating PWM singles based on the proposed modulation scheme to conduct primary and boost currents through S_2 and S_3 instead of body diodes.
- Compact size.

However, there are disadvantages associated with T-type topology when compared to NPC topology.

- S_1 and S_4 block the full dc-bus voltage V_{dc} where in the NPC converter same switches block half of V_{dc}.

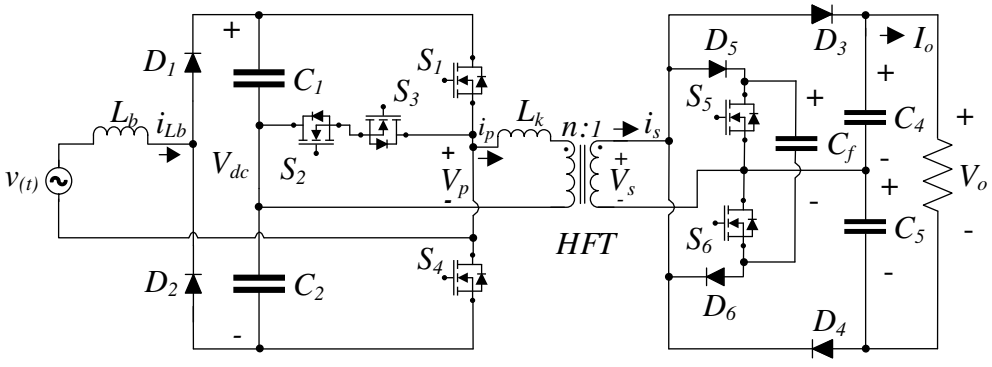

Figure 1.8: Proposed three-level isolated AC-DC PFC topology based on T-type inverter.

- During the circulation of the primary current through the HFT winding, S_2 and S_3 conduct the primary and boost inductor currents. However, the NPC switches S_2, S_3 conduct the primary current only.
- Suitable for high-power and low-voltage applications.

The T-type based topology shows a higher efficiency when compared to the NPC based topology. In both topologies, most of the converter losses are associated with the magnetic components which makes the design of a HFT is an essential part to complete this dissertation. The next section will present the conventional and the proposed steps for designing HFT.

1.5 High Frequency Transformer Design

The basic structure of an ideal transformer consists of a core and two independent windings (primary, secondary) which transfer energy between two isolated circuits by means of electromagnetic induction process as shown in Fig. 1.9 [1.35], [1.36]. Once an alternative current flow through a coil (primary), it produces a magnetic flux, which in return induces an electromotive force across the other coil (secondary).

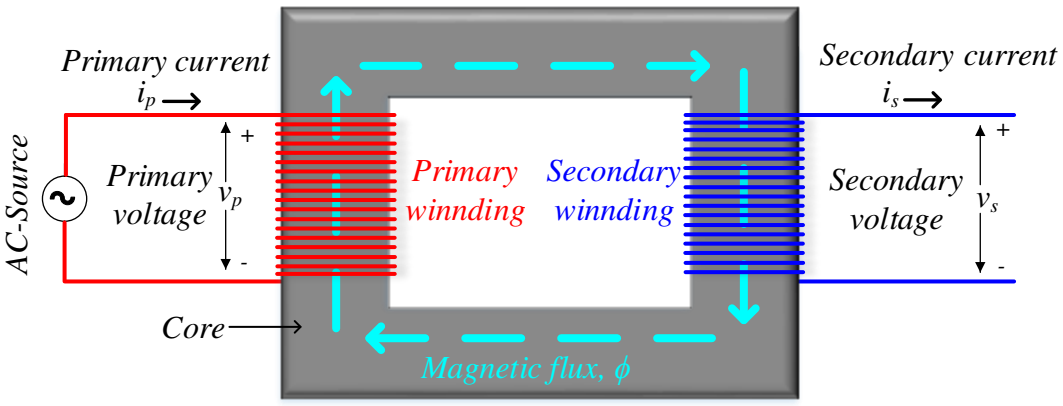

Figure 1.9: Ideal electrical transformer and induction law representation.

For an ideal electrical transformer, Faraday's induction law states that, since the same magnetic flux ϕ flows through primary and secondary windings, it induces voltages proportional to the number of turns.

1.5.A Conventional Design

The main concept and designing steps of HFT have been detailed in many previous publications; e.g., [1.37], [1.38]. These steps are:

1. Specifications of the application: output power, desired efficiency, primary and secondary voltages, primary and secondary currents, required leakage inductance, duty cycle, operating frequency of the converter, expecting temperature rise, and isolation level.
2. Material selection: Steinmetz coefficients, flux saturation density, and isolation material properties including, safety margin and dielectric strength.
3. Optimized flux density calculation: the optimized flux depends on:
   - The typical values of the dimensionless coefficient k_a =40, k_c=5.6, and k_w=10 [1.39].
   - The type of cooling, i.e., the heat transfer h_c=10W/m^2 for natural convection.
   - The window utilization factor which depends on winding tightness.
   - The stacking factor that relates the effective cross section area to the physical core area.
   - The waveform factor i.e., k_v=4.44 for a sinusoidal and k_v=4 for a square waveform [1.40].
4. Physical core dimensions which can be calculated as in [1.37].
5. Wire selection based on the current density.
6. Required isolation distance.
7. Leakage inductance calculation. If the calculated leakage is not met, then designer should either go back to step 5 and changes the selected wire or modifies the isolation distance.

8. Volume calculation.
9. Total loss calculation.
10. Efficiency and temperature rise calculations.

As the operating frequency increases, the loss density increases as well, making the selection of soft-magnetic material a critical step when designing HFT. At medium frequency operation, the nanocrystalline and amorphous materials show high efficiency due to reduced eddy current losses [1.41].

1.5.B Proposed Design

The new power electronic converter topologies and different applications' requirements have an impact upon the design steps of the HFT. For instant, the dual active bridge (DAB) requires specific leakage inductance and very large magnetizing inductance where a topology based on the flyback converter working principle requires very low leakage inductance and specific value of magnetizing inductance. The new proposed design counts for these two specifications and include them in the first step of designing the HFT. More explanation regarding how to take into consideration these two parameters will be provided in section 5.3A.

In addition, the proposed design includes finite-element analysis (FEA) using ANSYS^{TM} in the design steps to measure and visualize the distribution of magnetic flux inside the core. If the core is saturated, then the designer should stop and go back to choose different core size or change the way the windings are arranged around the core. Furthermore, the proposed design will present a new method which estimates the losses of different magmatic materials as a function of the output power.

1.6 Organization of This Dissertation

This dissertation is organized as follows:

- Chapter 2 introduces the first proposed topology including circuit configuration, steady-state analysis (waveforms and operational principle), a comparison between existing topologies and the proposed topology, a simulation case study on a 87.5-kW, as well as a 250-W experimental prototype. All the results of this chapter were obtained under open-loop conditions (that is, there is no closed loop applied). In this chapter, the drain-source capacitances C_{ds} of secondary switches charge up to half of the output voltage and do not discharge during the OFF time, which drives the secondary switches to operate under hard-switching. Therefore, Chapter 3 proposes a new technique to overcomes the hard-switching issue.
- Chapter 3 continues with the investigation into the proposed topology. The new study includes modifying the secondary-side circuit by adding a flying capacitor to achieve soft-switching, steady-state analysis, soft-switching analysis (primary and secondary switching), and proposed converter design procedure (boost inductor, dc-bus capacitor selection, HFT design, and output capacitor selection). As a proof of concept, the theoretical analysis was evaluated through a 25-kW case study simulation as well as a 900-W experimental prototype. Furthermore, three closed-loop PI controllers were applied to the proposed topology to investigate how the converter response to a load change.
- Chapter 4 is a modification of the previously proposed topology where the primary side NPC bridge is replaced with a T-type three-level inverter. In contrast to NPC based topology (Chapter 3), T-type based topology (Chapter 4) has less devices (cost-

effective) and low conduction losses (high efficiency). Chapter 4 includes steady-state analysis (circuit configuration, steady-state waveforms with a new pulse-width modulation scheme, and operational principles), soft-switching analysis for primary and secondary switches, and experimental results. Mainly, chapter 4 focus on the full-characterizations of ac-dc converter based on T-type topology.

- Chapter 5 addresses for completeness the design procedures of a HFT including magnetic material selection, in particular, nanocrystalline, amorphous, and ferrite. In addition, it includes temperature rise consideration, design methodology (e.g., magnetizing and leakage inductances, design steps), simulation of a 120-kVA case study obtained using finite-element analysis (FEA), and demonstrating the feasibility of the ideas by building a scale-down 1-kW prototype.
- Chapter 6 provides the conclusions and contributions of this doctoral work. In addition, possible future works that can be done on this topology to improve the overall efficiency.

1.7 References

[1.1] X. She, A. Q. Huang and R. Burgos, "Review of Solid-State Transformer Technologies and Their Application in Power Distribution Systems," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 186-198, Sept. 2013.

[1.2] W. McMurray, "Power converter circuits having a high-frequency link," U.S. Patent 3 517 300, Jun. 23, 1970.

[1.3] X. She, X. Yu, F. Wang, and A. Q. Huang, "Design and demonstration of a 3.6-kV-120-V/10-kVA solid-state transformer for smart grid application," *IEEE Trans. Power Electron*., vol. 29, no. 8, pp. 3982–3996, Aug. 2014.

[1.4] E. R. Ronan, S. D. Sudhoff, S. F. Glover and D. L. Galloway, "A power electronic-based distribution transformer," in *IEEE Trans. on Power Delivery*, vol. 17, no. 2, pp. 537-543, April 2002.

[1.5] X. She, A. Q. Huang and R. Burgos, "Review of Solid-State Transformer Technologies and Their Application in Power Distribution Systems," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 186-198, Sept. 2013.

[1.6] D. G. Shah and M. L. Crow, "Stability design criteria for distribution systems with solid-state transformers," *IEEE Trans. Power Del.*, vol. 29, no. 6, pp. 2588–2595, Dec. 2014.

[1.7] D. Rothmund, T. Guillod, D. Bortis and J. W. Kolar, "99% Efficient 10 kV SiC-Based 7 kV/400 V DC Transformer for Future Data Centers," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 753-767, June 2019.

[1.8] J. Shi, W. Gou, H. Yuan, T. Zhao and A. Q. Huang, "Research on voltage and power balance control for cascaded modular solid-state transformer," in *IEEE Trans. on Power Electronics*, vol. 26, no. 4, pp. 1154-1166, April 2011.

[1.9] L. Keke and L. Lin, "Analysis of favored design frequency of high-frequency transformer with different power capacities," *2014 International Conference on Power System Technology*, Chengdu, 2014, pp. 2272-2278.

[1.10] D. D. C. Lu, D. K. W. Cheng, and Y. S. Lee, "Single-stage AC–DC power-factor-corrected voltage regulator with reduced intermediate bus voltage stress," *Proc. Inst. Elect. Eng.—Elect. Power Appl.*, vol. 150, no. 5, pp. 506–514, Sep. 2003.

[1.11] S. Dusmez, X. Li and B. Akin, "A Fully Integra ted Three-Level Isolated Single-Stage PFC Converter," in IEEE *Trans. on Power Electronics*, vol. 30, no. 4, pp. 2050- 2062, April 2015.

[1.12] P. M. Barbosa, F. Canales, J. M. Burdio and F. C. Lee, "A three-level converter and its applicationto power factor correction," in *IEEE Trans. on Power Electronics*, vol. 20, no. 6, pp. 1319-1327, Nov. 2005.

[1.13] B. Singh, S. Singh, A. Chandra and K. Al-Haddad, "Comprehensive Study of Single-Phase AC-DC Power Factor Corrected Converters With High-Frequency Isolation," in *IEEE Trans. on Industrial Informatics*, vol. 7, no. 4, pp. 540-556, Nov. 201

[1.14] A. Nabae, I. Takahashi, and H. Akagi, "A neutral-point clamped PWM inverter," *IEEE Trans. Ind. Appl.,* vol. 1A-17, no. 5, pp. 518–523, Sep. 1981.

[1.15] B. Singh, S. Singh, A. Chandra and K. Al-Haddad, "Comprehensive Study of Single-Phase AC-DC Power Factor Corrected Converters With High-Frequency Isolation," in *IEEE Trans. on Industrial Informatics*, vol. 7, no. 4, pp. 540-556, Nov. 2011.

[1.16] N. Coruh, S. Urgun and T. Erfidan, "Design and implementation of flyback converters," *2010 5th IEEE Conference on Industrial Electronics and Applications*, Taichung, 2010, pp. 1189-1193.

[1.17] N. Mohan, T. Udeland, and W. Robbins, *Power Electronics: Converters, Applications and Design,* 3rd ed. New York: Wiley, 2002.

[1.18] J. C. Bennett, *Practical Computer Analysis of Switched Mode Power Supplies*. New York: CRC Press, 2006.

[1.19] Yen-Wu Lo and R. J. King, "High performance ripple feedback for the buck unity-power-factor rectifier," in *IEEE Trans. on Power Electronics*, vol. 10, no. 2, pp. 158-163, March 1995.

[1.20] A. Choudhury, P. Pillay and S. S. Williamson, "Comparative Analysis Between Two-Level and Three-Level DC/AC Electric Vehicle Traction Inverters Using a Novel DC-Link Voltage Balancing Algorithm," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 529-540, Sept. 2014.

[1.21] S. Jeong, J. Kwon and B. Kwon, "High-Efficiency Bridgeless Single-Power-Conversion Battery Charger for Light Electric Vehicles," *IEEE Trans. on Industrial Electronics*, vol. 66, no. 1, pp. 215-222, Jan. 2019.

[1.22] B. Whitaker et al., "A High-Density, High-Efficiency, Isolated On-Board Vehicle Battery Charger Utilizing Silicon Carbide Power Devices," *IEEE Trans. on Power Electronics*, vol. 29, no. 5, pp. 2606-2617, May 2014.

[1.23] M. de Prada, L. Igualada, C. Corchero, O. Gomis-Bellmunt, A. Sumper, "Hybrid AC-DC Offshore Wind Power Plant Topology: Optimal Design," *IEEE Trans. on Power Systems*, Vol. 30, No. 4, July 2015, pp. 1868-1876.

[1.24] C. Li and D. Xu, "Family of Enhanced ZCS Single-Stage Single-Phase Isolated AC–DC Converter for High-Power High-Voltage DC Supply," *IEEE Trans. on Industrial Electronics*, vol. 64, no. 5, pp. 3629-3639, May 2017.

[1.25] *IEEE Recommended Practices and Requirements for Harmonics Control in Electric Power Systems,* IEEE Standard 519, 1992.

[1.26] *Electromagnetic Compatibility (EMC) – Part 3: Limits- Section 2: Limits for Harmonic Current Emissions (equipment input current 16 A per phase),* IEC1000-3-2 Document, 1st ed., 1995.

[1.27] J. Rodriguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," in *IEEE Trans. on Industrial Electronics*, vol. 49, no. 4, pp. 724-738, Aug. 2002.

[1.28] S. Kouro *et al*., "Recent Advances and Industrial Applications of Multilevel Converters," in *IEEE Trans. on Industrial Electronics*, vol. 57, no. 8, pp. 2553-2580, Aug. 2010.

[1.29] Jih-Sheng Lai and Fang Zheng Peng, "Multilevel converters-a new breed of power converters," in *IEEE Trans. on Industry Applications*, vol. 32, no. 3, pp. 509-517, May-June 1996.

[1.30] Y. Jiao and F. C. Lee, "New Modulation Scheme for Three-Level Active Neutral-Point-Clamped Converter With Loss and Stress Reduction," in *IEEE Transa. on Industrial Electronics*, vol. 62, no. 9, pp. 5468-5479, Sept. 2015.

[1.31] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen and J. W. Kolar, "Optimal ZVS Modulation of Single-Phase Single-Stage Bidirectional DAB AC–DC Converters," in *IEEE Trans. on Power Electronics*, vol. 29, no. 8, pp. 3954-3970, Aug. 2014.

[1.32] W. Choi, J. Choi and J. Yoo, "Single-stage bridgeless three-level AC/DC converter with current doubler rectifier," *8th International Conference on Power Electronics - ECCE Asia*, Jeju, 2011, pp. 2704-2708.

[1.33] L. A. Garcia Rodriguez, V. Jones, A. R. Oliva, A. Escobar-Mejía and J. C. Balda, "A New SST Topology Comprising Boost Three-Level AC/DC Converters for Applications in Electric Power Distribution Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 2, pp. 735-746, June 2017

[1.34] B. Zhao, Q. Yu and W. Sun, "Extended-Phase-Shift Control of Isolated Bidirectional DC–DC Converter for Power Distribution in Microgrid," in *IEEE Trans. on Power Electronics*, vol. 27, no. 11, pp. 4667-4680, Nov. 2012.

[1.35] L. M. Faulkenberry and W. Coffer, Electrical Power Distribution and Transmission Englewood Cliffs, NJ: Prentince Hall, 1996.

[1.36] T. Gonen, Electric Power Distribution System Engineering, Second Edition. Boca Raton, FL: CRC Press Taylor & Taylor Group, 2008.

[1.37] W. G. Hurley, W.H. Wölfle, Transformers and Inductors for Power Electronics: Theory, Design and Applications, 1st ed., Wiley, 2013.

[1.38] C. William, T. McLyman, Transformer and Inductor Design Handbook, 4th ed., Taylor & Francis Group, 2011.

[1.39] W.G. Hurley, W. H. Wöfle, J. G. Breslin, "Optimized transformer design: Inclusive of highfrequency effects," in *IEEE Trans. on Power Electronics,* vol. 13, no. 4, pp. 651-659, July 1998

[1.40] G. Ortiz, J. Biela, J. W. Kolar, "Optimized design of medium frequency transformers with high isolation requirements," in *Proceeding of the 36th IEEE Industrial Electronics Society Conference*, IECON 2010, pp. 631-638, Nov. 2010.

[1.41] T. Kauder and K. Hameyer, "Performance Factor Comparison of Nanocrystalline, Amorphous, and Crystalline Soft Magnetic Materials for Medium-Frequency Applications," in *IEEE Trans. on Magnetics*, vol. 53, no. 11, pp. 1-4, Nov. 2017.

NEW ISOLATED AC-DC POWER CONVERTER TOPOLOGY WITH REDUCED NUMBER OF SWITCHES FOR HIGH-INPUT VOLTAGE AND HIGH-OUTPUT CURRENT APPLICATIONS

O. Aldosari, L. A. Garcia Rodriguez, D. C. Rojas and J. C. Balda, "A New Isolated AC-DC Power Converter Topology with Reduced Number of Switches for High-Input Voltage and High-Output Current Applications," *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, Busan, Korea (South), 2019, pp. 1-8.

Abstract

The main objective of this research work is to develop a new low-cost isolated three-level ac-dc power converter topology that is suitable for applications having high input ac voltages and high output currents; for example, hybrid (ac-dc) microgrids or offshore wind farms. Existing three-level converter topologies convert ac power to dc power while maintaining requirements set by international standards for power conversion. These types of converters have significant conduction losses due to high currents in the low-voltage side and high costs, particularly when using several devices in series or in parallel to achieve high-voltage and high-power levels. The proposed topology replaces the conventional three-level converters in the low-voltage side by only two controlled devices and four diodes while still maintaining the basic functionality of a three-level converter. Simulation results for a 87.5-kW case study and experimental results on a 250-W scale-down prototype demonstrate the feasibility of the proposed ideas.

2.1 Introduction

Isolated ac-dc unidirectional power converters are commonly used to convert distribution-level ac currents and voltages to supply dc loads such as electric vehicle battery charger systems [2.1],

hybrid ac-dc wind farms [2.2], telecommunication systems [2.3], dc-powered datacenters, and uninterrupted power supply (UPS). Unidirectional and bidirectional power converters are widely used in hybrid microgrid, where the input sources of these converters are usually interfaced with ac/dc loads through high frequency transformer [2.4]. Input power factor correction (PFC), low total harmonic distortion (THD) and output voltage regulations are usually the minimum requirements for isolated ac-dc power converters [2.3]. The international standard IEC 61000-3-2:2018 [2.5] requires that the harmonic contents of the input current should be reduced to specified levels; these are normally achieved by implementing the so-called PFC techniques [2.5],[2.6].

Preferred features are also symmetrical voltage distribution across semiconductors devices on the high-voltage side, and current sharing between devices on the low-voltage side to minimize power conduction losses and reduce current and voltage ratings [2.7]. However, preserving high efficiency and high power density along with the previous requirements continues to be a top challenge among the scientific community [2.7].

Converter applications with high-voltage ac inputs and low-voltage dc outputs (load side), such as chargers for electrical vehicles [2.8], requires multiple converters connected in series at the high-voltage side and in parallel at the low-voltage side. The controlled switches in the high- and low-voltage sides are used to maintain the primary dc-bus voltage within a certain tolerance, regulate the output voltage and control the delivered output power [2.9].

However, the cost and conduction losses are significant for high-power applications where multiple H-bridges are connected in parallel in the low-voltage side. Furthermore, the power backflow is another issue for some isolated dc-dc converters requiring an additional control effort to eliminate having different polarities of currents and voltages at the same time [2.10].

The new topology presented can overcome the above issues while still preserving the fundamental working principles of three-level isolated ac-dc converters (i.e., regulating the output voltage, and controlling the dc-bus voltage to be within the desired levels determined by the load specification). The proposed topology can be employed to convert energy generated by a wind turbine (WT) to a high-voltage dc-bus distribution line, especially when a permanent magnet synchronous generator (PMSG) is used as shown in Fig. 2.1 [2.11].

The paper is organized as follows: the proposed topology including circuit configuration, steady-state waveforms, and operational principles are described in Section II. A *qualitative* comparison between a bidirectional isolated ac-dc converter and a unidirectional one against the proposed topology is presented in Section III. Simulation results on a 87.5-kW case study for interfacing a wind turbine generator with a dc-load and experimental results on a 250-W scaled-down prototype are given in Section IV. The conclusions about the findings of this research are given in Section V.

2.2 Proposed Topology

2.2.A Circuit Configuration

The proposed topology shown in Fig. 2.2 is composed of a neutral-point clamped (NPC) converter connected to the primary side of a high-frequency transformer (HFT) [2.8] and the proposed new three-level secondary circuit. The rated voltage of the two switches of the new circuit is half of the output voltage. The front end of the proposed topology is connected to a half-bridge diode rectifier. The analysis of the proposed topology throughout the paper will only focus on the new secondary circuit since the primary-side circuit was already described in [2.9].

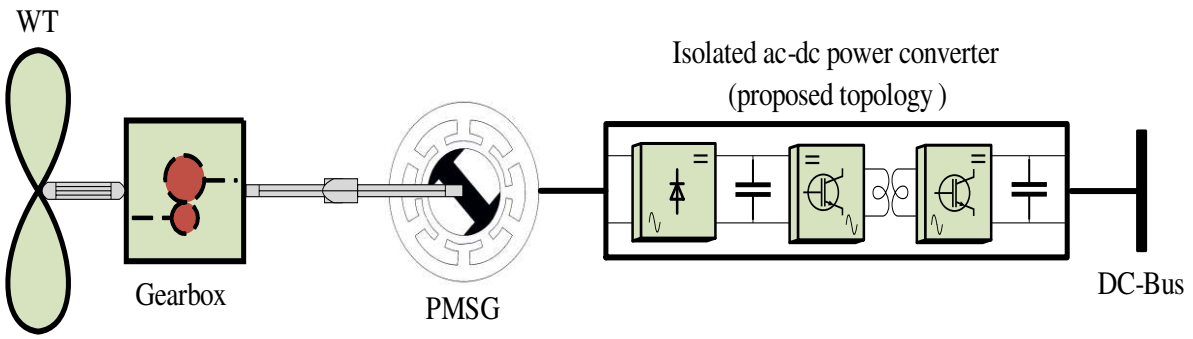

Figure 2.1: Type 4 wind turbine configuration, wind turbine blades, gearbox, PMSG, ac-dc power converter, and DC-bus.

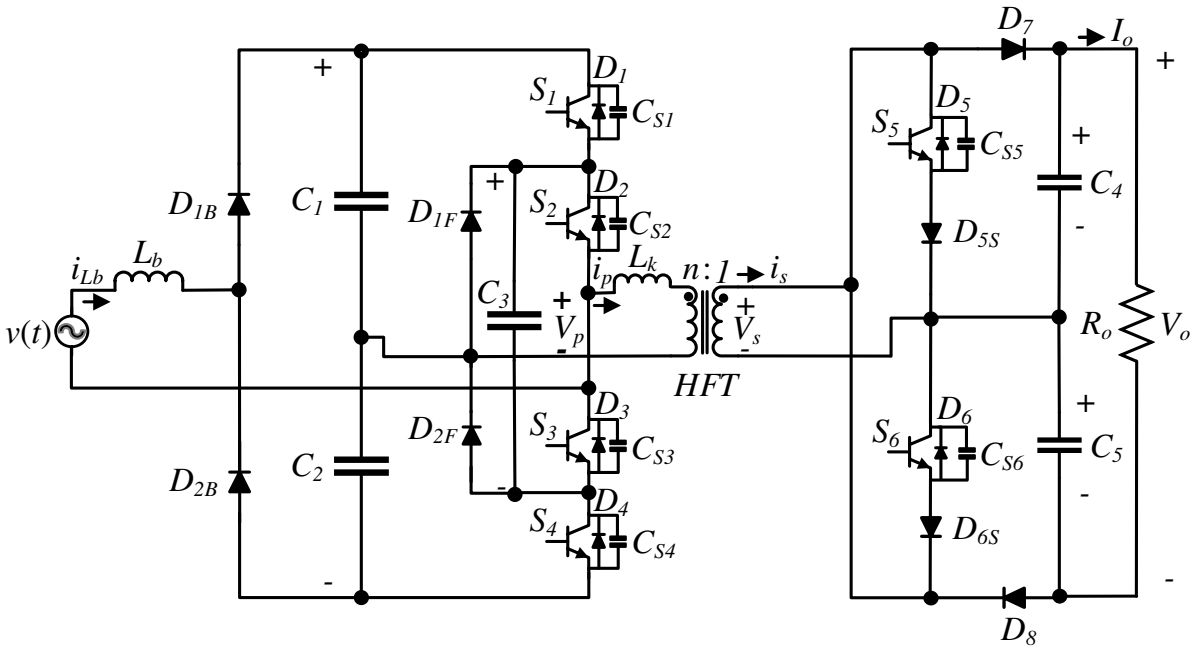

Figure 2.2: Proposed isolated ac-dc power converter topology.

2.2.B Steady-State Waveforms

The theoretical waveforms were first established to present the steady-state modulation scheme of the proposed topology as shown in Fig. 2.3. Due to the symmetry between top and bottom parts of the proposed secondary side, only the main waveforms at the top (V_{S5}, V_{D7},

I_{S5} and I_{D7}) are depicted. The intervals with the corresponding conducting devices are shown at the bottom of Fig. 2.3.

When the secondary current flows out of the positive terminal of the HFT, it either flows through S_5 and D_{5S}, or flows through D_7 to charge C_4, and then returns to the negative terminal of the HFT. For the positive half cycle of the secondary current, diode D_7 is allowing the current to charge the capacitor C_4 as well as preventing C_4 from shorting its terminals when S_5 is turned ON.

Switch S_5 (S_6) is placed across the HFT terminals to circulate the current when the output voltage is above the desired value. When switch S_5 (S_6) is OFF, the voltage across it will increase until becoming larger than the output capacitor voltage C_4 (C_5), which will forward bias the diode D_7 (D_8). In case of using a semiconductor device that has an antiparallel body diode (e.g., a SiC MOSFET), another diode D_{5S} (D_{6S}) must be connected in series with the switch S_5 (S_6) to block any negative (positive) current from returning to the HFT positive (negative) terminal. During the negative cycle of the secondary current, switch S_5 can be turned ON at zero current and zero voltage. Also, during the positive cycle of the secondary current, switch S_6 can also be turned ON at zero current and zero voltage as shown in Fig. 2.3. The primary duty cycle D_p is used to control the primary dc-bus voltage. The secondary duty cycle D_s and the phase shift between primary and secondary voltages D_ϕ are used to control the output voltage and delivered power. The HFT turns ratio is noted as n, and ϕ is the fundamental phase shift that depends on the primary and secondary voltages and duty cycles.

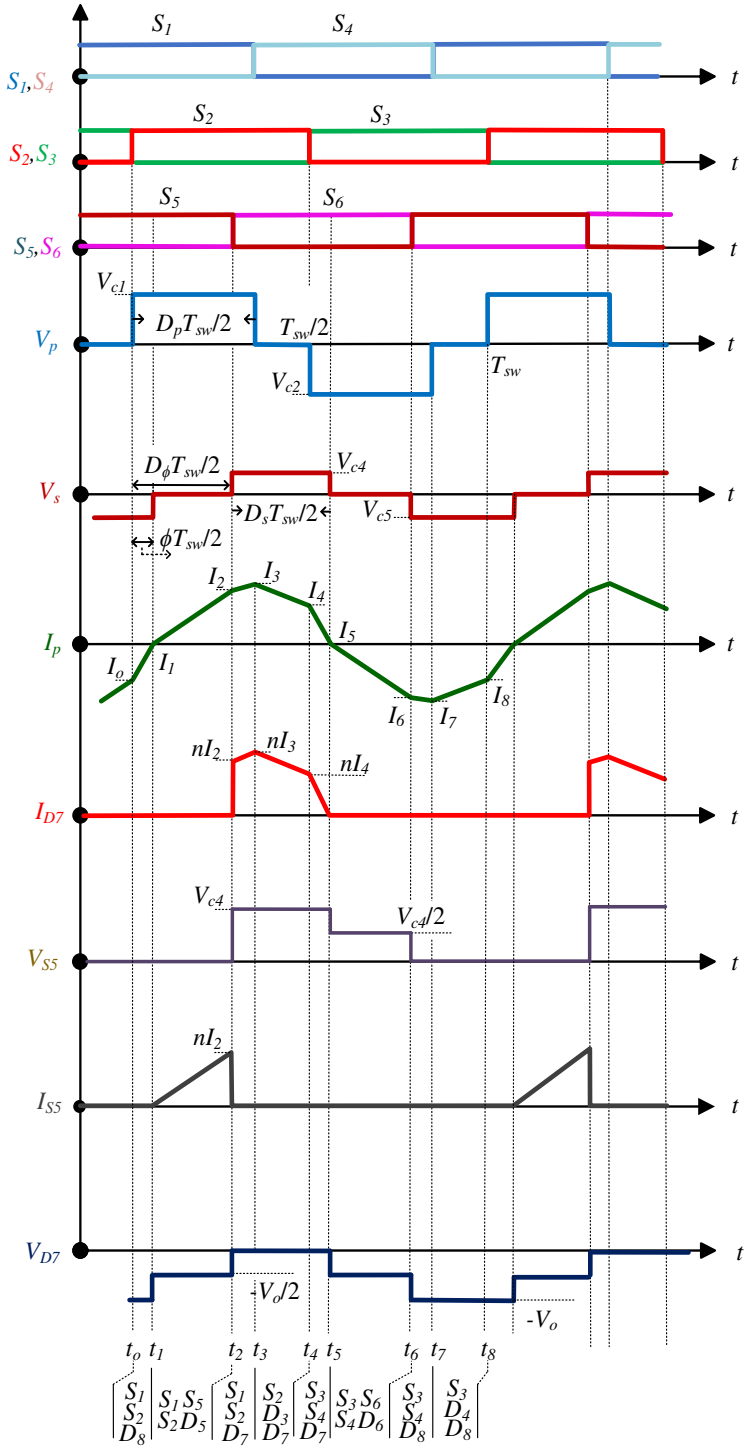

Figure 2.3: Steady-state waveforms of the proposed topology.

2.2.C Operational Principles

[t_o – t_1] *Interval*: the primary current i_p is initially negative and conducting through the antiparallel diodes of switches S_1 and S_2, as well as capacitor C_1. The secondary current is flows

through capacitor C_5 and diode D_8 as shown in Fig. 2.4(a). The primary voltage v_p is equal to the voltage of capacitor C_1 whereas the secondary voltage v_s is equal to the voltage of capacitor [C_5 = -V_o/2]. The primary current has a positive slope and continues increasing at a rate of [(V_{C1} + nV_o/2)/L_k]. At the instant when switches S_1 and S_2 are ON, the boost inductor starts charging at a rate of [$v(t)/L_b$].The time duration of this stage is [($D_\varphi + D_s$ - 1)T_{sw}/2], and the primary current i_p of the HFT is given by:

$$i_p(t) = \frac{1}{L_k}\left(V_{C1} + \frac{nV_o}{2}\right)(t - t_0) + I_0 \cdot \tag{2. 1}$$

At the end of this interval, the primary current i_p is zero. Thus, the initial condition I_o of the primary current i_p can be calculated as follows:

$$I_0 = -\frac{1}{2f_{sw}L_k}\left(\frac{nV_o}{2} + V_{C1}\right)\left(D_\varphi + D_s - 1\right) \cdot \tag{2. 2}$$

[$t_1 - t_2$] *Interval*: the primary current i_p flows in the same direction as the leakage inductor current i_{Lk}. The secondary current i_s flows through switch S_5, the series diode D_{S5}, and the secondary winding of the HFT. Fig. 2.4(b) shows the current conduction path during this interval. The primary voltage v_p is equal to the voltage of capacitor C_1 while the secondary voltage v_s is equal to zero. Primary and secondary currents, i_p and i_s, increase at a rate of [V_{C1}/L_k]. The time duration of this stage is equal to [(1 - D_s)T_{sw}/2], and the primary current i_p is calculated as follows:

$$i_p(t) = \frac{V_{C1}}{L_k}(t - t_1) + I_1 . \tag{2. 3}$$

Due to the circuit configuration, [$I_1 = 0$] and [$i_p(t_2) = I_2$] can be calculated as follows:

$$I_2 = \frac{V_{C1}}{2f_{sw}L_k}\left(1 - D_s\right). \tag{2. 4}$$

[$t_2 - t_3$] *Interval*: The primary current i_p continues to increase through C_1, S_1 and C_2 at a rate of [$(V_{C1} - nV_o/2)/L_k$]. Before the beginning of this interval, switch S_5 turns OFF, and the secondary current i_s continuously increases flowing through D_7 and C_4. While the primary voltage v_p is equal to the voltage of capacitor C_1, the secondary voltage v_s is equal to the voltage of capacitor C_4. Fig. 2.4(c) presents the equivalent circuit of this interval. Primary current i_p increases at a rate of [$(V_{C1} - nV_o/2)/L_k$] for the interval time duration of [$(D_p - D_\varphi)T_{sw}/2$]. Primary current i_p is given by:

$$i_p(t) = \frac{1}{L_k}\left(V_{C1} - \frac{nV_o}{2}\right)(t - t_2) + I_2 \cdot \tag{2. 5}$$

The peak current happens during [$t_2 - t_3$] *Interval* and it can be calculated as:

$$I_3 = \frac{1}{2f_{sw}L_k}\left(V_{C1} - \frac{nV_o}{2}\right)\left(D_p - D_\varphi\right) + I_2 \cdot \tag{2. 6}$$

[$t_3 - t_4$] *Interval*: Switch S_1 is turned OFF while switch S_2 is kept ON, then the primary current i_p starts flowing through D_3 and S_2, and decreasing at a rate of [$-nV_o/(2L_k)$], while the secondary current i_s continues flowing through D_7 and C_4. The primary voltage v_p is equal to zero and the secondary voltage v_s is equal to the voltage of capacitor C_4, which is equal to [$V_o/2$] as shown in Fig. 2.4(d). The time duration of this interval is [$(1 - D_p)T_{sw}/2$] and the primary current i_p is determined by:

$$i_p(t) = -\frac{nV_o}{2L_k}(t - t_3) + I_3 \cdot \tag{2. 7}$$

The current at the end of [$t_3 - t_4$] *Interval* is calculated from (7) as follows:

$$I_4 = -\frac{1}{2f_{sw}L_k}\frac{nV_o}{2}\left(1 - D_p\right) + I_3 \cdot \tag{2. 8}$$

[$t_4 - t_5$] *Interval*: Switch S_2 turns OFF, while the secondary current i_s keeps flowing through D_7 and C_4, and the primary current i_p conducts through C_2, D_4 and D_3; and decreasing at a rate of [-

(V_{C2} + nV_o/2)/L_k]. During this interval, the primary voltage v_p is negative and equal to the voltage of capacitor C_2 whereas the secondary voltage v_s is still positive as in the previous interval as depicted in Fig. 2.4(e). The interval time duration is the same as that of [t_o – t_1] *Interval* and the primary current is calculated by:

$$i_p(t) = -\frac{1}{L_k}\left(V_{C2} + \frac{nV_o}{2}\right)(t - t_4) + I_4 . \qquad (2.9)$$

At the end of the interval, the primary current i_p is equal to zero which makes $I_5 = 0$.

[t_5 - t_6] *Interval*: The primary current i_p changes direction from positive to negative and flows through S_3, S_4 and C_2 as presented in Fig. 2.4(f). Switch S_6 turns ON before the primary current i_p becomes negative to achieve soft-switching at turn ON. The secondary current i_s now flows through S_6 and D_{6S} which generates a zero-voltage level across the secondary winding of the HTF. The primary voltage v_p is equal to the voltage of capacitor C_2, and the voltage of the secondary side v_s is equal to zero. The interval time duration is the same as that of [t_1 – t_2] *Interval*. The primary current can be described by:

$$i_p(t) = -\frac{V_{C2}}{L_k}(t - t_5) + I_5 . \qquad (2.10)$$

In this stage, the initial condition of the primary current i_p is [$I_5 = I_1 = 0$], where $I_6 = -I_2$.

[t_6 - t_7] *Interval*: The primary current i_p flows through S_3, S_4 and C_2 and continues to decrease at a rate of [(nV_o/2 – V_{C2})/L_k]. At the beginning of this interval, switch S_6 turns OFF, and the secondary current i_s flows through C_5 and D_8. At the end of this interval, i_p is at its maximum negative peak value as indicated in Fig. 2.4(g). The primary voltage v_p is equal to the voltage of capacitor C_2 while the voltage of the secondary v_s is equal to the voltage of capacitor C_5. The time

duration of this interval is the same as that of [$t_2 - t_3$] *Interval* and the primary current i_p can be calculated as:

$$i_p(t) = \frac{1}{L_k}\left(\frac{nV_o}{2} - V_{C2}\right)(t - t_6) + I_6 \cdot \qquad (2.\ 11)$$

The initial current is [$I_6 = -I_2$] and [$I_7 = -I_3$].

[t_7 - t_8] *Interval*: Switch S_4 turns OFF, and the primary current i_p flows through S_3 and D_{2F} with a positive slope of [$nV_o/(2L_{lk})$]. The secondary current i_s continues to flow through C_5 and D_8 as shown in Fig. 2.4(h). The primary voltage v_p is equal to zero, and the secondary voltage v_s is equal to the voltage of capacitor C_5, (- V_o/2). The time duration of this interval is the same as that of [$t_3 - t_4$] *Interval* and the primary current i_p is given by:

$$i_p(t) = \frac{nV_o}{2L_k}(t - t_7) + I_7 \,. \qquad (2.\ 12)$$

The initial current is [$I_7 = -I_3$] and [$I_8 = I_o$].

The fundamental phase shift φ between primary and secondary voltages can be obtained from the steady-state analysis as follows:

$$\varphi = \frac{D_p}{2} - \frac{nV_o}{2V_{dc}} D_s \,, \qquad (2.\ 13)$$

where V_{dc} is the primary-side dc-link voltage. The total phase shift D_φ between primary and secondary voltages can be expressed in terms of the primary duty cycle D_p, and the secondary duty cycle D_s as follows:

$$D_\varphi = 1 + \frac{D_p}{2} - \left(\frac{nV_o}{2V_{dc}} + 1\right) D_s \,. \qquad (2.\ 14)$$

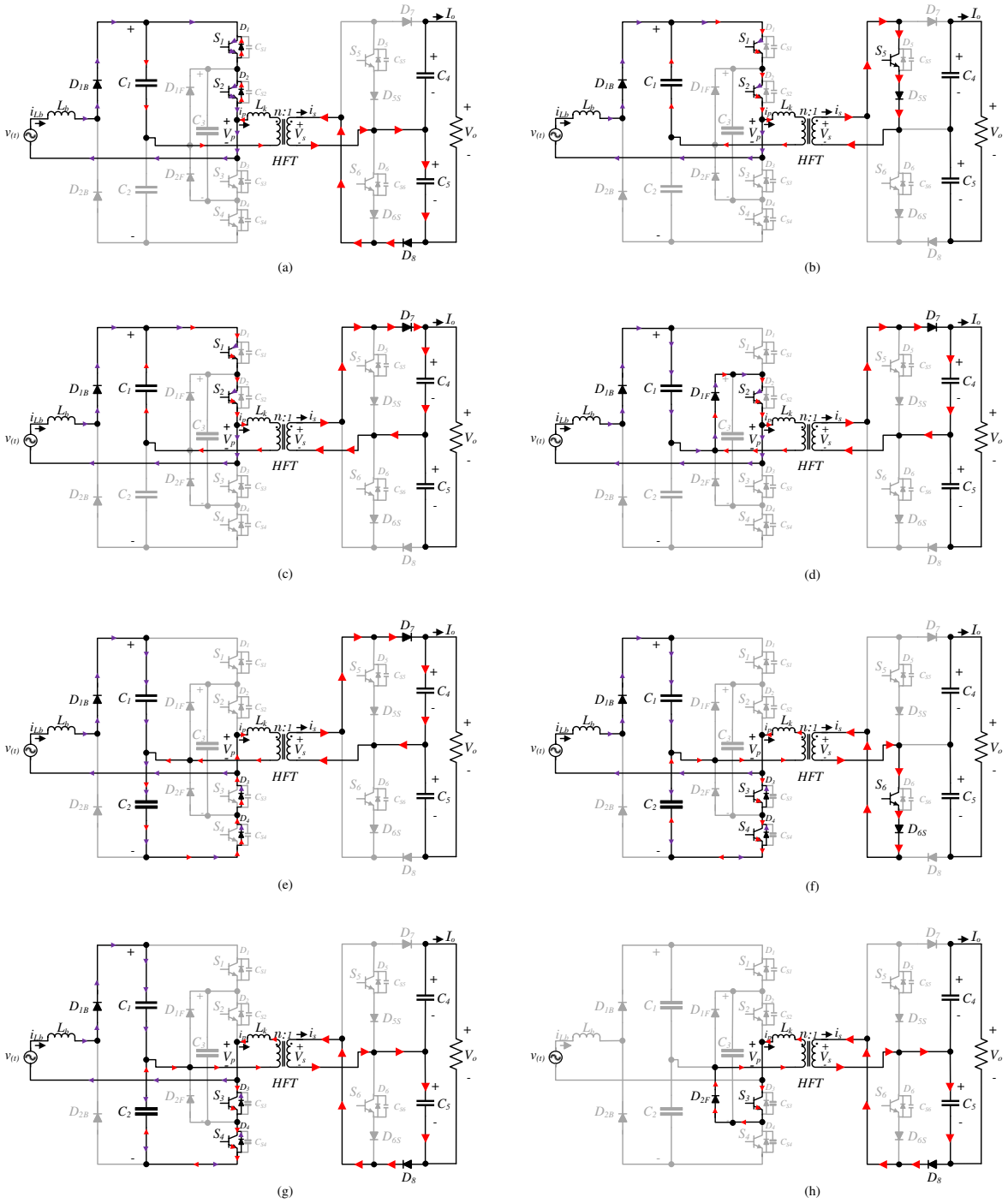

Figure 2.4: Steady-state equivalent operating circuits of the proposed topology, (a) [t_0-t_1] *Interval*, (b) [t_1-t_2] *Interval*, (c) [t_2-t_3] *Interval*, (d) [t_3-t_4] *Interval*, (e) [t_4-t_5] *Interval*, (f) [t_5-t_6] *Interval*, (g) [t_6-t_7] *Interval*, and (h) [t_7-t_8] *Interval*.

2.3 Existing AC-DC Converters vs Proposed Topology Comparison

In this section, the proposed topology will be *qualitatively* compared with two different ones: (1) a bidirectional isolated ac-dc converter, and (2) a unidirectional isolated ac-dc converter.

2.3.A Topology #1

The single-phase, single-stage, bidirectional and isolated dual active bridge (DAB) ac-dc converter is the conventional ac-dc power conversion as presented in [2.12] and shown in Fig. 2.5.

The topology front end is composed of a full bridge rectifier to allow power flow in both directions. All the semiconductor switches sustain the full dc-bus voltages in the high- and low-voltage sides. The aim of a bidirectional converter is to interface ac grids with a network having energy storage systems, solar energy farms, and other ac or dc sources. It can also work as a unidirectional power flow to supply from the utility source dc loads such as battery storage, dc-powered datacenters, electrical battery chargers, etc.

2.3.B Topology #2

The unidirectional three-level isolated single-stage PFC converter depicted in Fig. 2.6 is another topology with reduced number of controlled switches proposed in [2.12], [2.13].

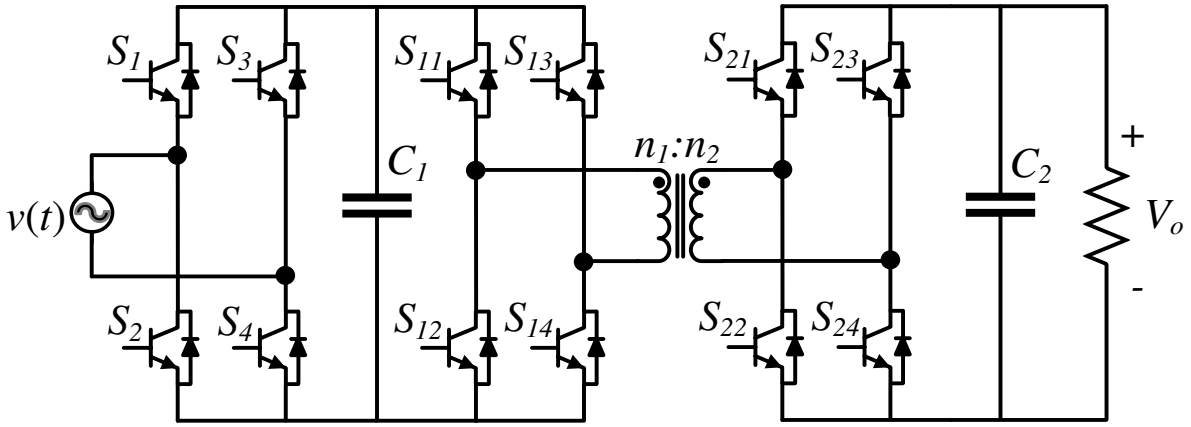

Figure 2.5: Topology #1 bidirectional ac-dc power converter.

This topology has an ac-dc conversion stage at the front end and a three-level isolated dc-dc converter. Compared to topology #1, it does not have the capability of controlling the voltage of each capacitor in the primary side of the HFT while at the same time controlling the output voltage.

The voltage of the capacitors C_1 and C_2 depend on the load conditions. Therefore, in case of light-load conditions, the capacitor voltages increase with respect to the rated power level. The later means that transistors at the transformer primary side must be overrated.

This topology finds its application when the output load is constant and does not change due to any outside disturbance. The only advantages of topology #2 over topology #1 are the low total cost since it is only composed of four controlled switches and the rated voltage of the switches is half of the dc-bus voltage.

2.3.C Proposed Topology

The proposed topology has the basic functionality of topology #1 controlling the dc-bus and output voltages simultaneously, yet it has only six controlled switches (low-cost) and can operate under soft-switching conditions (high-efficiency).

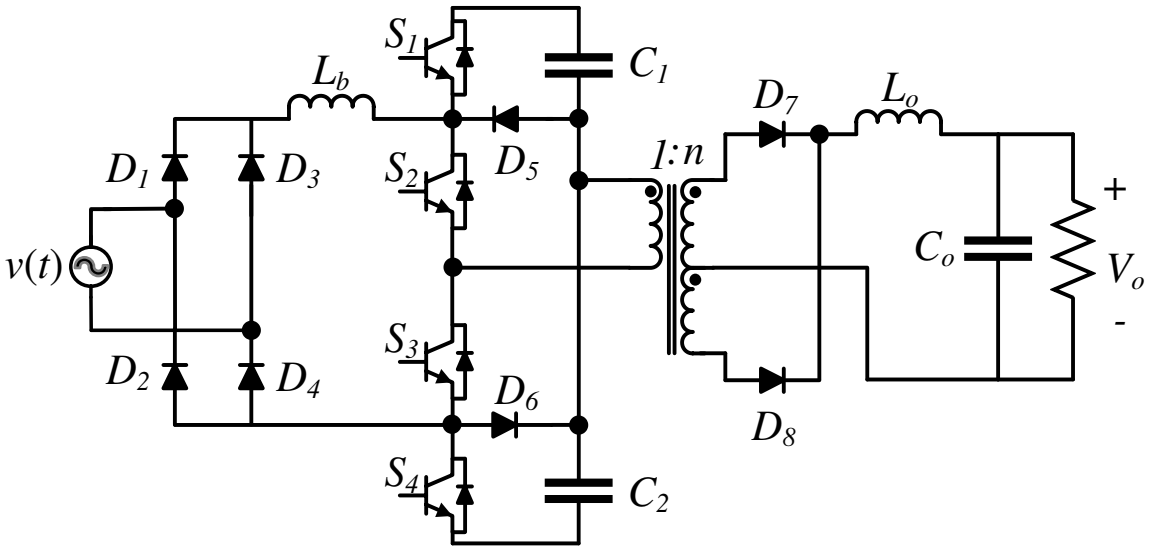

Figure 2.6: Topology #2 unidirectional ac-dc power converter.

For high power applications, the proposed topology can be connected in series at the high-voltage side to reduce the required breakdown voltage of the semiconductor switches. Also, it can be connected in parallel at the low-voltage side to use switches with lower current ratings as shown in Fig. 2.7.

However, the proposed topology does not support bidirectional power flow and has high secondary current, which requires large output capacitors. This topology can be employed in hybrid microgrids, hybrid wind farms [2.2], dc-powered datacenters, and electric vehicle chargers [2.14], [2.15]. At the load side of topology #1, the power is delivered to the load through two semiconductor switches, whereas in the proposed topology, it is delivered through only one diode, which reduces conduction losses.

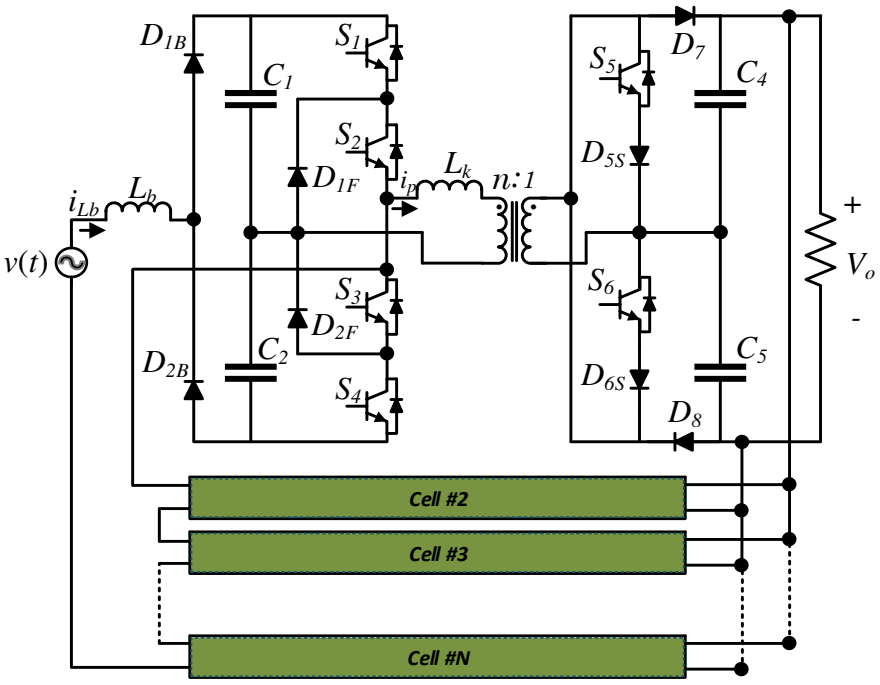

Figure 2.7: Proposed topology connected in series (high side) and in parallel (low side) for high power applications.

In such an application when power is required to flow in one direction, power backflow could be an issue for topology #1 unless designer employs a control algorithm to avoid having at the same time different polarities of voltage and current at the transformer terminals [2.10]. However, it is impossible to encounter this problem when the proposed topology and topology #2 are adapted due to the connection of the diodes on both sides of the HFT.

At the load side, the proposed topology does not require a dead time between the complementary switches due to the connection of the diodes D_7 and D_8. Table 2-I presents a general comparison between these three topologies.

2.4 Simulation and Experimental Results

2.4.A Simulation Results for a Case-Study

A microgrid provides more advantages to the utilities and users in term of power quality and power management [2.16]. A typical microgrid includes renewable energy resources (e.g., wind turbines, photovoltaic arrays, etc.), distributed grid lines (ac grid, dc grid), power conversions (power converters, transformers) and loads (ac-load, dc-load) [16].

Table 2-I: Qualitative Topology Comparison

Parameters	***Topology #1***	***Topology #2***	***Proposed Topology***
Bidirectional power flow capability	Yes	No	No
Total cost	High	Low	Fair
Switch blocking voltage	Full	Half	Half
Number of switches	12	4	6
Number of diodes	0	6	6
Controlling dc-bus and output voltage	Yes	No	Yes
Capacitors size	Small	Large	Medium

A type-4 wind turbine connected to the dc main bus of a hybrid microgrid using the proposed topology is considered here; please, refer to Fig. 2.1 [2.11].

The specifications of this case study are shown in Table 2-II. The RMS input current displayed in Fig. 2.8 is in phase with the input voltage. The boost inductor current and voltage, the transformer primary current and dc bus voltage are plotted in Fig. 2.9. The transformer primary and secondary voltages, and primary current are shown in Fig. 2.10. These waveforms are identical to the theoretical steady-state waveforms in Fig. 2.3. The output voltage V_o, output current I_o, and the output capacitors voltages V_{c4} and V_{c5}, are shown in Fig. 2.11. The two capacitors have the same voltage because they have the same duty cycle.

As the input ac voltage of the converter increases, the number of modules connected in series (high-voltage side) and in parallel (low-voltage side) increases in order to achieve a specific device voltage level and or current level as shown in Fig. 2.7. For instance, the required number of the 87.5-kW modules for a 3.0-MW, 2.4-kV three-phase ac source is 12 per phase with the assumption of utilizing 1.7 kV SiC MOSFETs at the high voltage [1.28].

Table 2-II: Simulation Parameters

Specifications	
Parameters	***Values***
Output power P_o (kW)	87.5
Switching frequency f_{sw} (kHz)	20
Input voltage v_{in} (V_{rms})	600
High side dc-bus voltage $V_{dc} > 2V_{inpk}$ (kV)	1.7
Low side capacitors voltages $V_{c4} = V_{c5}$ (V)	200
Output voltage V_o (V)	400
Output current I_o (A)	219

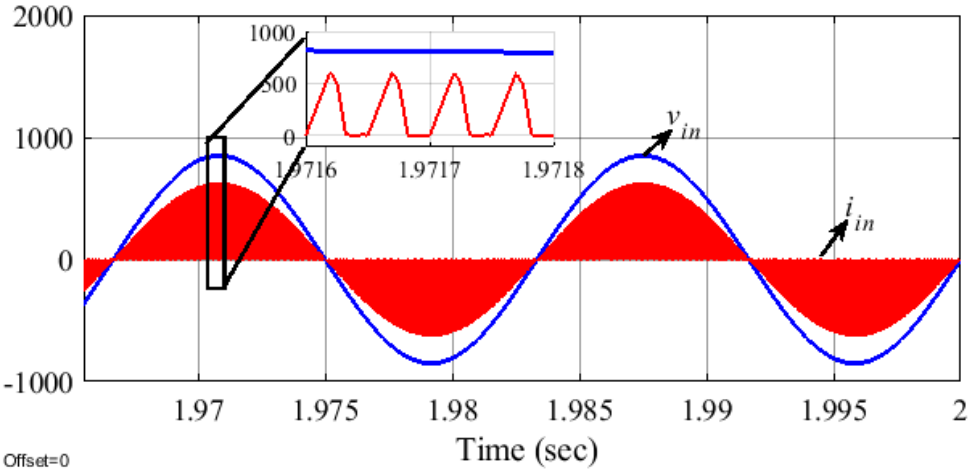

Figure 2.8: Input voltage and current from the wind turbine.

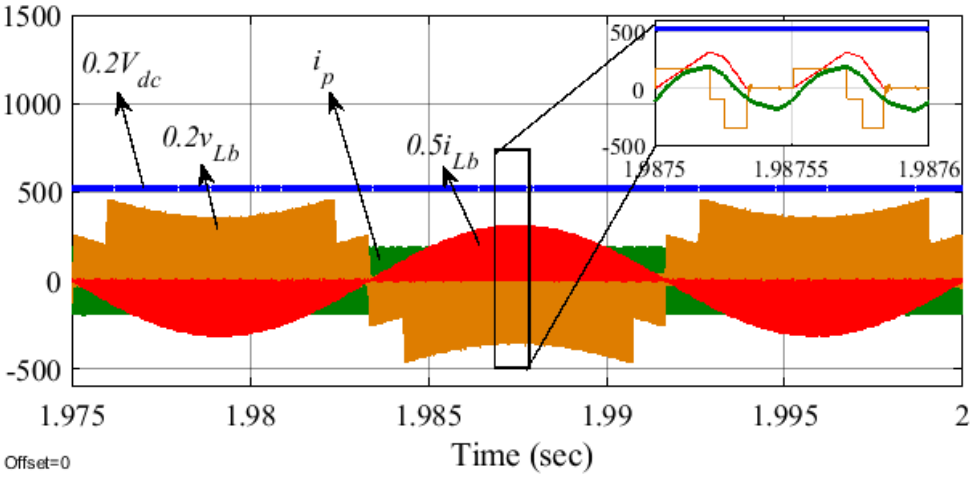

Figure 2.9: Simulations waveforms of the dc-bus voltage V_{dc}, boost inductor (voltage v_{Lb}, current i_{Lb}) primary current i_p.

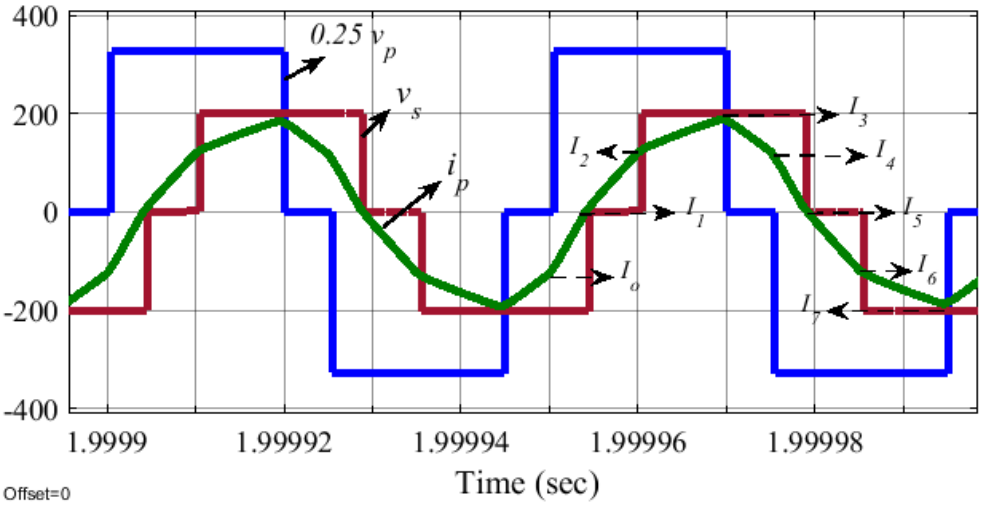

Figure 2.10: Simulated waveforms of the transformer primary-side voltage v_p, secondary-side voltage v_s, and primary current i_p.

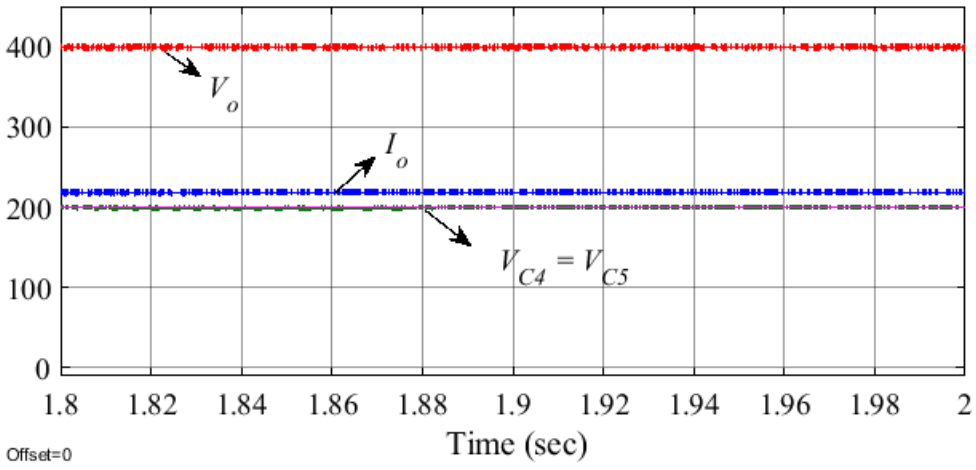

Figure 2.11: Output voltage V_o, output current I_o, capacitors voltages V_{c4}, and V_{c5}.

2.4.B Scaled-Down Prototype

A 250-W scaled-down prototype is implemented to validate the proposed topology performance. The main specifications of the prototype are shown in Table 2-III.

The input voltage of the system is a 110-V_{rms}, 60 Hz sinusoidal ac source that is rectified to a dc voltage using a half-bridge diode rectifier. The boost inductor of the proposed topology is sized to operate under the discontinuous condition mode (DCM) as shown in Fig. 2.12 (brown). As a result, the inductor peak current follows the input sinusoidal voltage.

Table 2-III: Experimental Parameters

Specifications	
Parameters	***Values***
Output power P_o (W)	250
Switching frequency (kHz)	20
Input voltage v_{in} (V_{rms})	110
High side dc-bus voltage $V_{dc} > 2V_{inpk}$ (V)	320
Low side capacitors voltages $V_{c4} = V_{c5}$ (V)	24
Output voltage V_o (V)	48
Resistive load R_o (Ω)	9

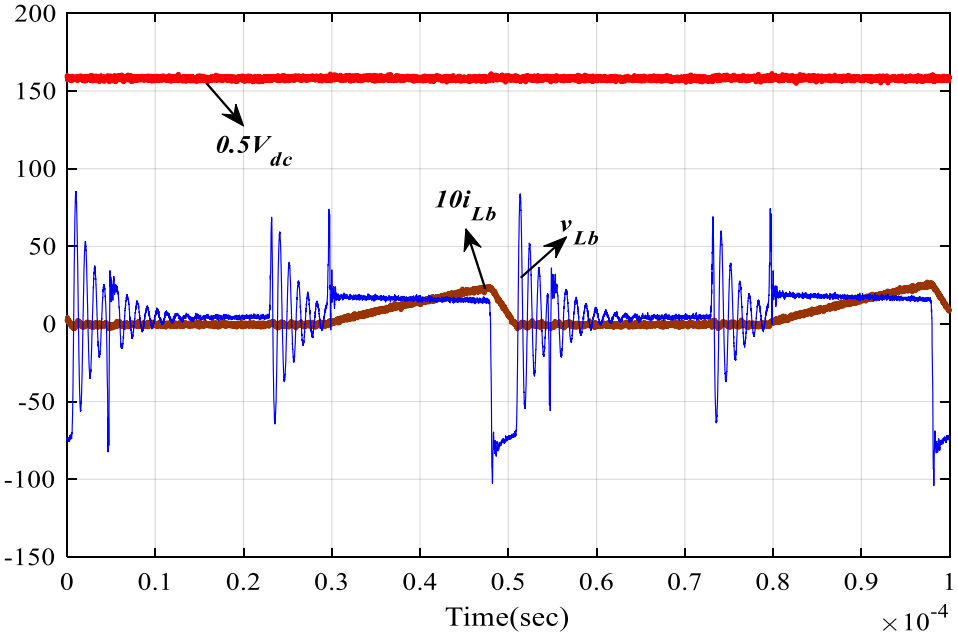

Figure 2.12: Topology high-side dc-bus voltage (red), boost inductor current (brown), and boost inductor voltage (blue).

The input current is the same as the boost inductor current, which is in phase with the input voltage. Consequently, the power factor at the input of the system is close to unity under the condition of having a dc-bus voltage of at least twice the peak of the input voltage; the condition that keeps the converter under DCM operation. The boost inductor voltage (blue) and current are shown in Fig. 2.12 as well as the dc-bus voltage (red). The oscillations that appears in the inductor voltage occurs when the boost inductor current is zero due to an oscillation between the diode parasitic capacitance and the boost inductor.

The transformer primary-side voltage (blue) and current (green), and the transformer secondary-side voltage (brown) are displayed in Fig. 2.13. For that particular condition, both primary and secondary voltages have three levels.

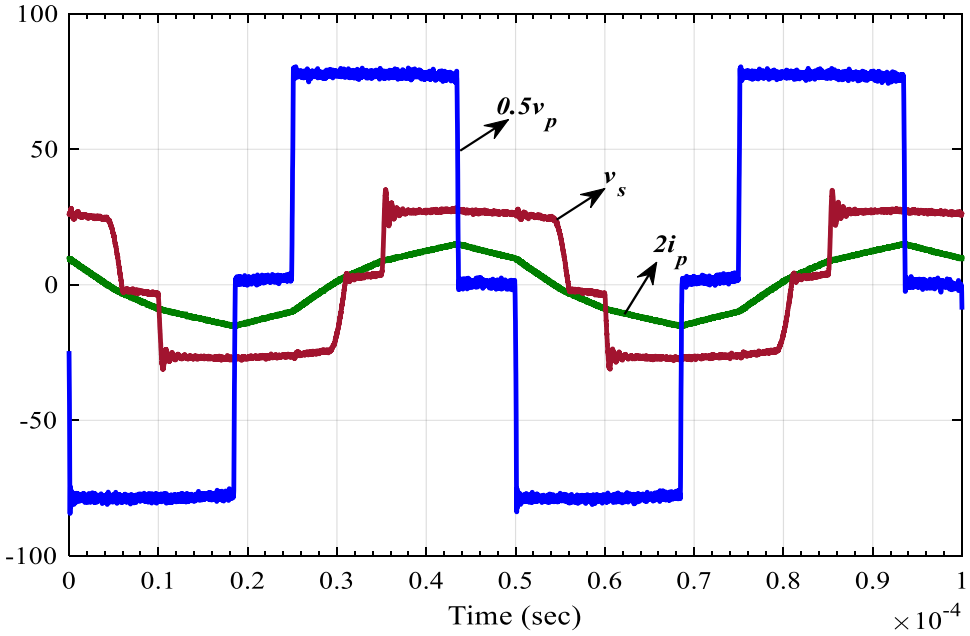

Figure 2.13: Primary voltage (blue), secondary voltage (brown), and primary current (green).

The zero-voltage level in the primary side controls the input power drawn from the source. When either S_5 and D_{5S}, or S_6 and D_{6s} conduct, a zero voltage appears at the secondary side which controls the output voltage. Transistor S_5 turns ON at zero voltage and zero current because its antiparallel diode D_5 is forward biased before the transition due to the transformer secondary voltage at that time is equal to $[-V_{C5}]$. Similarly, S_6 turns ON at zero current and zero voltage conditions when the secondary voltage equals to V_{C4}.

Fig. 2.14 presents the output voltage V_o, and output current I_o. When one of the capacitors discharges through the load, the other one is charged from the source, which in return, it smooths the output voltage. The voltage of the capacitors C_4 and C_5 is half of the output voltage.

2.5 Conclustions

A new topology for isolated unidirectional ac-dc power converter was presented and analyzed. The steady-state analysis illustrated achieving a three-level voltage waveform using only two controlled switches at the low-voltage side.

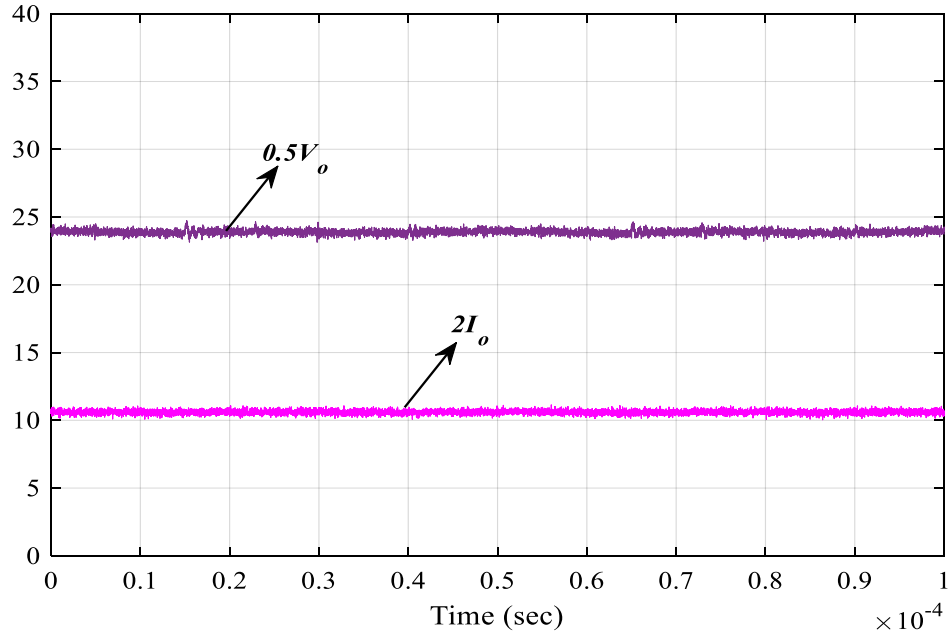

Figure 2.14: Output voltage (purple), and output current (pink).

It was also shown that this new (low-voltage) secondary circuit together with the NPC converter (high-voltage side) was able to control the primary dc-bus voltage and output voltage. The simulation and experimental results for this new topology agreed reasonably well with the theoretical equations and steady-state waveforms. Furthermore, a general comparison between two different isolated ac-dc converters and the proposed topology was carried out. The findings showed that the new topology has multiple advantages in terms of low losses, cost effectiveness, preventing power backflow, and allowing ZCS and ZVS at turn ON without any additional control effort.

2.6 References

[2.1] T. Soeiro, T. Friedli and J. W. Kolar, "Three-phase high power factor mains interface concepts for Electric Vehicle battery charging systems," *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, " Orlando, FL, 2012, pp. 2603-2610.

[2.2] M. de Prada, L. Igualada, C. Corchero, O. Gomis-Bellmunt, A. Sumper, “Hybrid AC-DC Offshore Wind Power Plant Topology: Optimal Design,” *IEEE Transactions on Power Systems*, Vol. 30, No. 4, July 2015, pp. 1868-1876.

[2.3] C. Li and D. Xu, "Family of Enhanced ZCS Single-Stage Single-Phase Isolated AC–DC Converter for High-Power High-Voltage DC Supply," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 5, pp. 3629-3639, May 2017.

[2.4] F. Nejabatkhah and Y. W. Li, "Overview of Power Management Strategies of Hybrid AC/DC Microgrid," in *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 7072-7089, Dec. 2015.

[2.5] EN61000-3-2 Edition 2.2: Limits for Harmonic Current Emissions (equipment input current ≤ 16 A per phase), 2004.

[2.6] B. Singh, S. Singh, A. Chandra and K. Al-Haddad, "Comprehensive Study of Single-Phase AC-DC Power Factor Corrected Converters With High-Frequency Isolation," in *IEEE Transactions on Industrial Informatics*, vol. 7, no. 4, pp. 540-556, Nov. 2011.

[2.7] J. A. L. Barboza, O. C. S. Filho, L. C. S. Mazza and R. P. T. Bascopé, "Five-level T-type NPC PFC rectifier based on multistate switching cell," *2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC)*, Fortaleza, 2015, pp. 1-6.

[2.8] D. Sha, G. Xu and Y. Xu, "Utility Direct Interfaced Charger/Discharger Employing Unified Voltage Balance Control for Cascaded H-Bridge Units and Decentralized Control for CF-DAB Modules," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 7831-7841, Oct. 2017.

[2.9] L. A. Garcia Rodriguez, V. Jones, A. R. Oliva, A. Escobar-Mejía and J. C. Balda, "A New SST Topology Comprising Boost Three-Level AC/DC Converters for Applications in Electric Power Distribution Systems," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 2, pp. 735-746, June 2017.

[2.10] B. Zhao, Q. Yu and W. Sun, "Extended-Phase-Shift Control of Isolated Bidirectional DC–DC Converter for Power Distribution in Microgrid," in *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4667-4680, Nov. 2012.

[2.11] Venkata Yaramasu; Bin Wu, "Basics of Wind Energy Conversion Systems (Wecs)," in *Model Predictive Control of Wind Energy Conversion Systems*, IEEE, 2017

[2.12] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen and J. W. Kolar, "Optimal ZVS Modulation of Single-Phase Single-Stage Bidirectional DAB AC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 3954-3970, Aug. 2014.

[2.13] S. Dusmez, X. Li and B. Akin, "A Fully Integra ted Three-Level Isolated Single-Stage PFC Converter," in IEEE *Transactions on Power Electronics*, vol. 30, no. 4, pp. 2050- 2062, April 2015.

[2.14] F. Musavi, W. Eberle and W. G. Dunford, "A High-Performance Single-Phase Bridgeless Interleaved PFC Converter for Plug-in Hybrid Electric Vehicle Battery Chargers," in *IEEE Transactions on Industry Applications*, vol. 47, no. 4, pp. 1833-1843, July-Aug. 2011.

[2.15] B. Whitaker *et al*., "A High-Density, High-Efficiency, Isolated On-Board Vehicle Battery Charger Utilizing Silicon Carbide Power Devices," in *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2606-2617, May 2014.

[2.16] B. S. Hartono, Budiyanto and R. Setiabudy, "Review of microgrid technology," *2013 International Conference on QiR*, Yogyakarta, 2013, pp. 127-132.

[2.17] V. Yaramasu, B. Wu, P.C. Sen, S. Kouro, M. Narimani, “High-Power Wind Energy Conversion Systems: State-of-the-Art and Emerging Technologies,” .*Proceedings of the IEEE*, Vol. 103, No. 5, May 2015, pp. 740-788.

APPENDIX 2.A

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November 13, 2019

To whom it may concern,

This letter is to verify that Mr. Obaid Martha Aldosari, ID 010768784, is the first author and did at least 51% of the work for the paper titled "A New Isolated AC-DC Power Converter Topology with Reduced Number of Switches for High-Input Voltage and High-Output Current Applications".

Kind Regards,

Dr. Juan Carlos Balda

University Professor, Department Head and Major Advisor to Mr. Obaid Martha Aldosari

A THREE-LEVEL ISOLATED AC-DC PFC POWER CONVERTER TOPOLOGY WITH REDUCED NUMBER OF SWITCHES

O. Aldosari, L. A. G. Rodriguez, G. G. Oggier and J. C. Balda, "A Three-Level Isolated AC-DC PFC Power Converter Topology with Reduced Number of Switches," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*. doi: 10.1109/JESTPE.2019.2962704

Abstract

The main objective of this research work is to develop a new low-cost isolated three-level ac-dc power converter topology with a reduced number of switches. Existing three-level converter topologies change ac power to dc power while maintaining requirements set by international standards for power conversion. These types of converters have significant conduction losses due to high currents in the low-voltage side and high costs, particularly when using several active devices in series or in parallel to achieve high-voltage and high-power levels. The proposed topology replaces the conventional three-level converters in the secondary side by only two controlled devices and four diodes while still maintaining the basic functionality of a three-level converter. Furthermore, simulation results for a 25 kW case study and experimental results on a 900 W scale-down prototype demonstrate the feasibility of the proposed ideas.

3.1 Introduction

Distribution–level ac currents and voltages are usually adapted to supply dc loads such as electric-vehicle battery charger systems [3.1], [3.2], hybrid ac-dc wind farms [3.3], telecommunication systems [3.4], dc-powered datacenters, and uninterrupted power supplies (UPS), through isolated ac-dc unidirectional power converters. A bidirectional converter finds its applications when power required to flow in both directions, i.e., controlling power flow between

electrical vehicles (EV) charger and the grid [3.5]. Recent developments of the 10 kV SiC-MOSFET enables a reliable two-stage solid-state transformer (SST) topology to convert from a medium ac voltage to a low dc voltage to power dc loads (e.g., data centers) [3.6]. Many isolated ac-dc SST converters topologies use 10 kV SiC-MOSFET (e.g., LLC Series Resonant Converter) and show high efficiency for converting from a 7 kV ac-line to a 400 V dc-bus [3.7]. Unidirectional and bidirectional power converters are widely used in hybrid microgrids to support and provide reliable power management strategies [3.8]. As the power level increases, the number of cascaded cells increases to form a multilevel voltage suitable for the device rating [3.9]. Input power factor correction (PFC), low total harmonic distortion (THD) and output voltage regulations are usually the minimum requirements for isolated ac-dc power converters [2.3][3.3], [3.4]. The international standard IEC 61000-3-2:2018 [3.10] requires that the harmonic content of the input current is limited to specified levels; these are normally achieved by implementing the so-called PFC techniques [3.11].

Preferred features for this type of converters are also symmetrical voltage distribution across the semiconductors devices on the high-voltage side, and current sharing between devices on the low-voltage side to minimize power conduction losses and reduce current and voltage ratings [3.12]. However, preserving high efficiency and high-power density along with the previous requirements continues to be a top challenge among the scientific community [3.12].

One of the most used solid-state isolated AC-DC converters is the single-phase, single-stage, bidirectional dual active bridge (DAB) converter as presented in [3.13]. The benefit of using a synchronous rectifier (SR) at the front end is to shape the ac-current close to a sinusoidal waveform and to be in phase with the input voltage, which in return improves the power factor (PF) and reduces the THD level. Furthermore, the primary and secondary bridges generate three-level

voltages, i.e., $+v$, 0, $-v$ which provide full control of the dc-bus voltage, output power, and output voltage. The drawbacks of utilizing this converter especially when power is flowing in one direction are the usage of twelve active switches with full dc-bus voltage rating (high-cost), as well as dealing with the issue of power back-flow (extra control effort) [3.14].

Another alternative cost-effective topology is a three-level unidirectional isolated single-stage PFC converter with fewer switches presented in [3.15]. At the primary side, a boost inductor and a full-wave diode bridge rectifier are connected to a three-level neutral point clamping (NPC) converter, and the secondary side is connected to a half-bridge diode rectifier and output inductor. The main advantages of adopting this topology are: (1) minimum number of devices, (2) high PF when the dc bus voltage is much higher than the peak input voltage, (3) active switches sustain half of the dc-bus voltage. However, it is not possible to regulate the dc-bus and output voltages simultaneously; a significant disadvantage of having active switches only on the primary side. Then, at light-load conditions, the dc-bus voltage increases cumulatively to the point where switches sustain high voltage stresses.

The proposal given in [3.16] is a boost-based topology, and it controls both dc-bus and output voltage levels. The secondary side is composed of two H-bridges connected to two transformer secondary windings to reduce the current stress on the secondary side switches. For high output voltage applications, this topology is not desirable since it requires eight switches that sustain the full output voltage. Besides, secondary side switches lose soft-switching at low-power operation.

This article presents a new topology shown in Fig. 3.1 that allow overcomes the issues mentioned above while preserving the fundamental working principles of three-level isolated ac-dc converters, like regulation of the output voltage and controlling the dc-bus voltage within desired levels determined by the load specifications. By controlling the dc-bus voltage at an

adequate level, the current through the boost inductor is discontinuous, which enables a high PF.

The main contribution of the proposed topology is the new secondary side circuit, which consists of only two active switches and four diodes. In comparison with [3.16], the secondary side bridge operates at ZVS and ZCS at turn ON at all modes of operation and power levels, while in the other case, soft-switching is guaranteed only at a specific region determined by the power level. Besides, the switches on the primary and secondary sides sustain only half of the dc-bus voltage and half output voltage, respectively. In contrast, in [3.16], the voltage rating of the eight active devices of the secondary side corresponds to the full output voltage level. Furthermore, during a half switching period, power is delivered from the secondary terminals to the load through only one device. In contrast, in a conventional H-bridge, the current circulates through two active devices.

The article is organized as follows: the proposed topology including the circuit configuration, steady-state waveforms, and operating principles are described in Section II. Soft-switching analysis regarding to the proposed topology is explained in Section III. The design procedure of the converter is presented in Section IV.

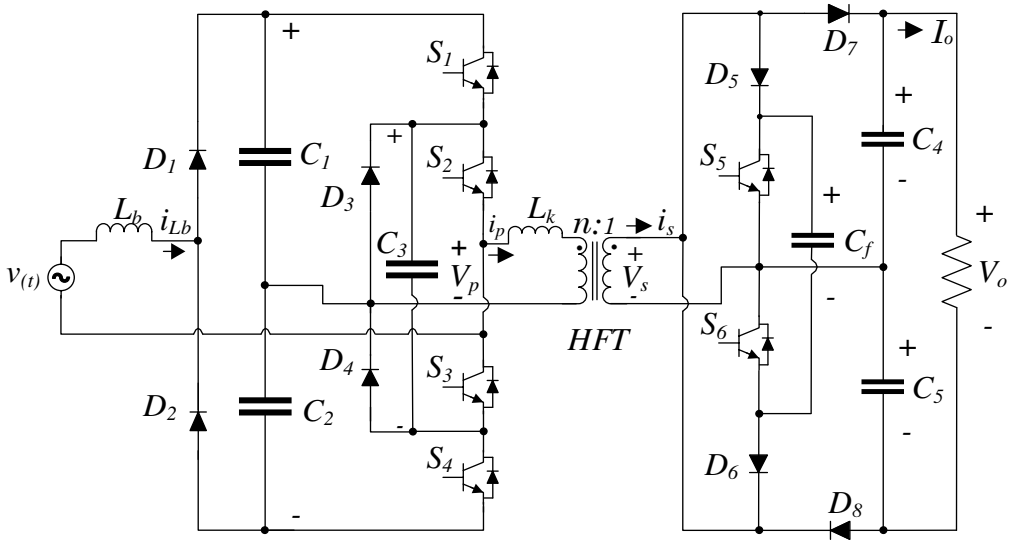

Figure 3.1: Proposed isolated ac-dc power converter topology.

Simulation results on a 25-kW case study for interfacing a small wind turbine generator with a dc load and experimental results on a 900 W scaled-down prototype are given in Section V. The conclusions about the findings of this research are provided in Section VI.

3.2 Proposed Isolated AC-DC Topology

The proposed ac-dc topology consists of a boost-based front-end diode-rectifier, which allows the need of an active rectifier to be eliminated, at the expense of losing the directional power conversion capability [3.16]. Then, NPC connects to the dc-link capacitors, and the high-frequency transformer. The NPC has a dual function; first, it behaves as the active switch of the boost based front-end rectifier. On the other hand, the NPC is the primary-side bridge of a DAB-type topology form by the NPC, the high-frequency transformer, and the new secondary side active bridge with the minimum number of active switches. The following section details the new secondary-side bridge topology.

3.2.A Circuit Configuration

With reference to Fig. 3.1, the rated voltage of the two switches of the new secondary side circuit is half of the output voltage level. The flying capacitor C_f is placed across the two switches (S_5, S_6) to facilitate the charging and discharging action of the parasitic capacitances. The soft transitions between modes will be explained with great detail in the soft-switching section. At the front end, the boost inductor is connected to a half-bridge diode rectifier. The analysis of the proposed topology throughout the paper will focus on the new secondary side circuit since the primary-side circuit was already described in a previous publication [1.20][3.16].

3.2.B Steady-State Waveforms

The theoretical waveforms shown in Fig. 3.2 illustrates the steady-state modulation scheme of the proposed topology. Due to the symmetry between the top and bottom parts of the proposed

secondary side, only the main waveforms for the top side (V_{S5}, V_{D7}, I_{S5} and I_{D7}) are depicted. The voltage of the primary and secondary capacitors (C_1, C_2, C_4, C_5) are indicated in the primary and the secondary voltages (V_p, V_s) waveforms, as shown in Fig. 3.2.

When the secondary current flows out of the positive terminal of the high-frequency transformer (HFT), it either flows through S_5 and D_5, or flows through D_7 to charge C_4, and then returns to the HFT negative terminal. For the positive half cycle of the secondary current, diode D_7 is allowing the current to charge C_4 as well as preventing C_4 from shorting its terminals when S_5 turns ON.

Switch S_5 (S_6) is placed across the HFT terminals to circulate the current when the output voltage is above the desired level. When switch S_5 (S_6) is OFF, the voltage across it increases until becoming larger than the output capacitor voltage C_4 (C_5), which will forward bias the diode D_7 (D_8). In case of using a semiconductor device with bidirectional current capability (e.g., a Si or SiC MOSFETs), a diode D_5 (D_6) must be connected in series with the switch S_5 (S_6) to block any negative (positive) current from returning to the HFT positive (negative) terminal. During the negative cycle of the secondary current, switch S_5 can be turned ON at ZVS and ZCS. In addition, switch S_6 can also be turned ON at ZVS and ZCS during the positive cycle of the secondary current as shown in Fig. 3.2. The primary duty cycle D_p is used to control the primary dc-bus voltage. The secondary duty cycle D_s and the phase shift between primary and secondary voltages D_ϕ are used to control the output voltage and delivered power. The HFT turns ratio is noted as n, and ϕ is the fundamental phase shift that depends on the primary and secondary voltages and duty cycles.

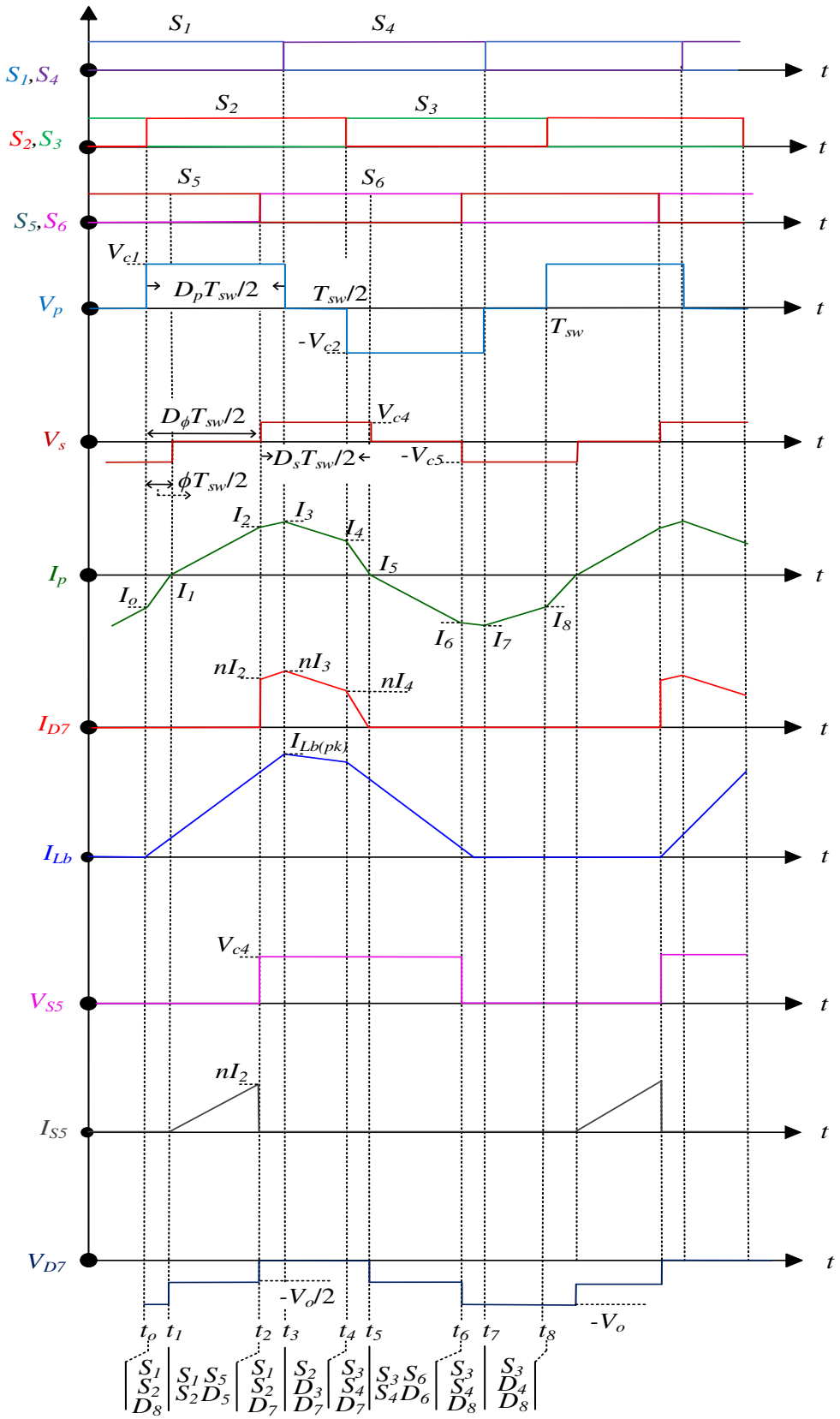

Figure 3.2: Steady-state waveforms of the proposed topology.

3.2.C Operational Principles

Fig. 3.3 shows the equivalent circuit for each interval. The green arrows represent the input current i_{in}, which is the same as the boost inductor current i_{Lb}, and the pink arrows represent the primary and secondary currents of the HFT.

3.2.C. i $[t_o - t_1]$ *Interval*: the primary current i_p is initially negative and conducting through the antiparallel diodes of switches S_1 and S_2, as well as the capacitor C_1. The secondary current i_s flows through capacitor C_5 and diode D_8 as shown in Fig. 3.3. The primary voltage v_p is equal to the voltage of capacitor C_1 whereas the secondary voltage v_s is equal to the voltage of capacitor $[C_5 = -V_o/2]$. The primary current has a positive slope and continues increasing at a rate of $[(V_{C1} + nV_o/2)/L_k]$. At the instant when switches S_1 and S_2 are ON, the boost inductor starts charging at a rate of $[v(t)/L_b]$. The time duration of this stage is $[(D_\varphi + D_s - 1)T_{sw}/2]$, and the HFT primary current i_p is given by:

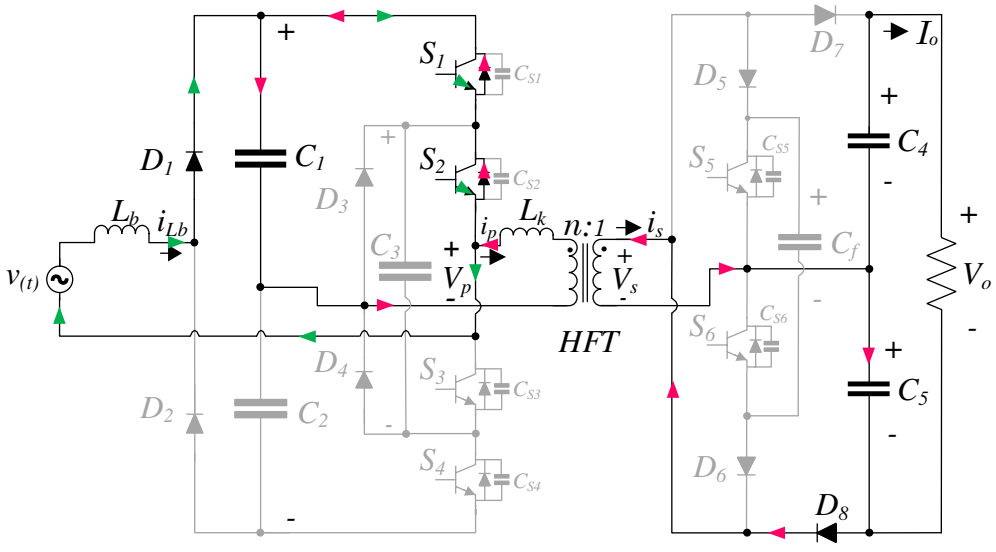

Figure 3.3: $[t_0\text{-}t_1]$ Interval, steady-state equivalent operating circuits of the proposed topology.

$$i_p(t) = \frac{1}{L_k}\left(V_{C1} + \frac{nV_o}{2}\right)(t - t_0) + I_0 \,. \tag{3. 1}$$

At the end of this interval, the primary current i_p is zero. Thus, the initial condition I_o of the primary current i_p can be calculated as follows:

$$I_0 = -\frac{1}{2f_{sw}L_k}\left(\frac{nV_o}{2} + V_{C1}\right)\left(D_\varphi + D_s - 1\right). \tag{3. 2}$$

3.2.C. ii $[t_1 - t_2]$ *Interval*: the primary current i_p becomes positive and flows through S_1 and S_2. The secondary current i_s flows through the series diode D_5, and switch S_5. Fig. 3.4 shows the current conduction path during this interval. The primary voltage v_p is equal to the voltage of capacitor C_1 while the secondary voltage v_s is equal to zero. The primary current i_p increases at a rate of $[V_{C1}/L_k]$. The time duration of this stage is equal to $[(1 - D_s)T_{sw}/2]$, and the primary current i_p is calculated as follows:

$$i_p(t) = \frac{V_{C1}}{L_k}(t - t_1) + I_1 \,. \tag{3. 3}$$

Due to the circuit configuration, $[I_1 = 0]$, and $[i_p(t_2) = I_2]$ that can be calculated as follows:

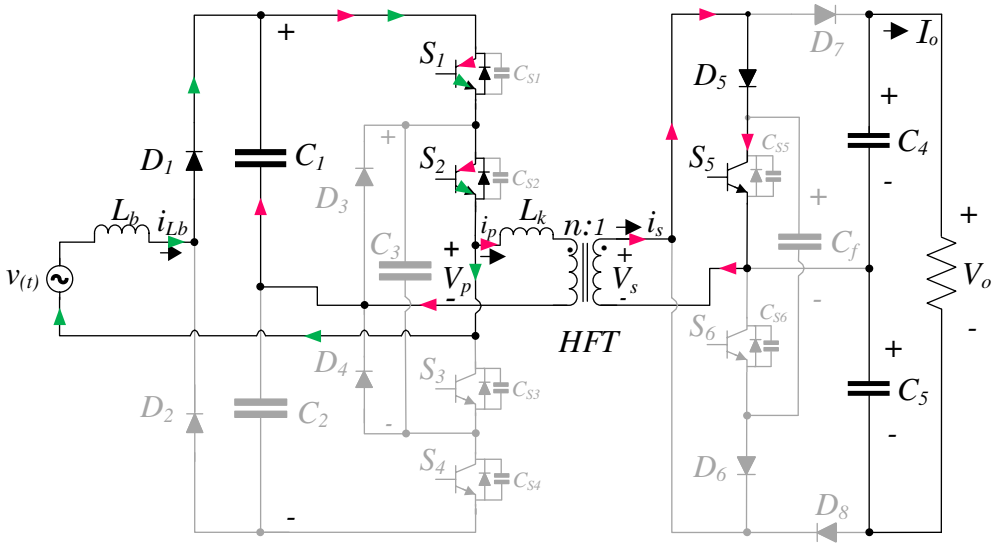

Figure 3.4: $[t_1$-$t_2]$ Interval, steady-state equivalent operating circuit of the proposed topology.

$$I_2 = \frac{V_{C1}}{2 f_{sw} L_k}\left(1 - D_s\right). \tag{3. 4}$$

3.2.C. iii $[t_2 - t_3]$ *Interval*: switch S_5 turns OFF and the secondary current i_s flows through D_7 and C_4. While the primary voltage v_p is equal to the voltage of capacitor C_1, the secondary voltage v_s is equal to the voltage of capacitor C_4. Fig. 3.5 presents the equivalent circuit of this interval which has a time length of $[(D_p - D_\varphi)T_{sw}/2]$. The primary current i_p continues to flow through C_1, S_1, and S_2 at a rate given by $[(V_{C1} - nV_o/2)/L_k]$. The slope of i_p depends on the voltage across the leakage inductance. In the particular case of Fig. 3.2, V_{C1} is larger than $[nV_o/2]$, so the slope of i_p is positive and can be calculated as:

$$i_p(t) = \frac{1}{L_k}\left(V_{C1} - \frac{nV_o}{2}\right)(t - t_2) + I_2\,. \tag{3. 5}$$

At the end of this interval, primary current reaches its peak and it calculated as:

$$I_3 = \frac{1}{2 f_{sw} L_k}\left(V_{C1} - \frac{nV_o}{2}\right)\left(D_p - D_\varphi\right) + I_2. \tag{3. 6}$$

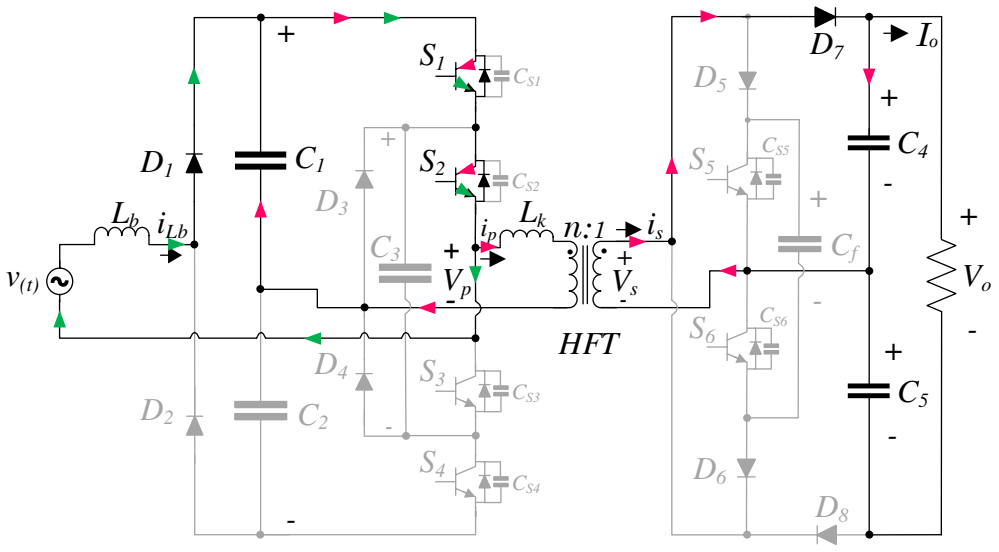

Figure 3.5: $[t_2\text{-}t_3]$ Interval, steady-state equivalent operating circuits of the proposed topology.

3.2.C. iv [$t_3 - t_4$] *Interval*: Switch S_1 is turned OFF while switch S_2 is kept ON, then the primary current i_p starts to flow through D_3 and S_2, and decrease at a rate of [$-nV_o/(2L_k)$], while the secondary current i_s continues flowing through D_7 and C_4. The primary voltage v_p is equal to zero and the secondary voltage v_s is equal to the voltage of capacitor C_4, which is equal to [$V_o/2$] as shown in Fig. 3.6. The time duration of this interval is [$(1 - D_p)T_{sw}/2$], and the primary current i_p is determined by:

$$i_p(t) = -\frac{nV_o}{2L_k}(t - t_3) + I_3 . \tag{3. 7}$$

The current at the end of this interval is calculated from (3.7) as follows:

$$I_4 = -\frac{1}{2f_{sw}L_k}\frac{nV_o}{2}\left(1 - D_p\right) + I_3 . \tag{3. 8}$$

3.2.C. v [$t_4 - t_5$] *Interval*: After S_2 turns OFF, the primary current conducts through C_2 and the antiparallel diodes of S_4 and S_3, while the secondary current i_s continues flowing through D_7. Since the voltage across the L_k is negative, i_p decreases at a rate of [$-(V_{C2} + nV_o/2)/L_k$]. During

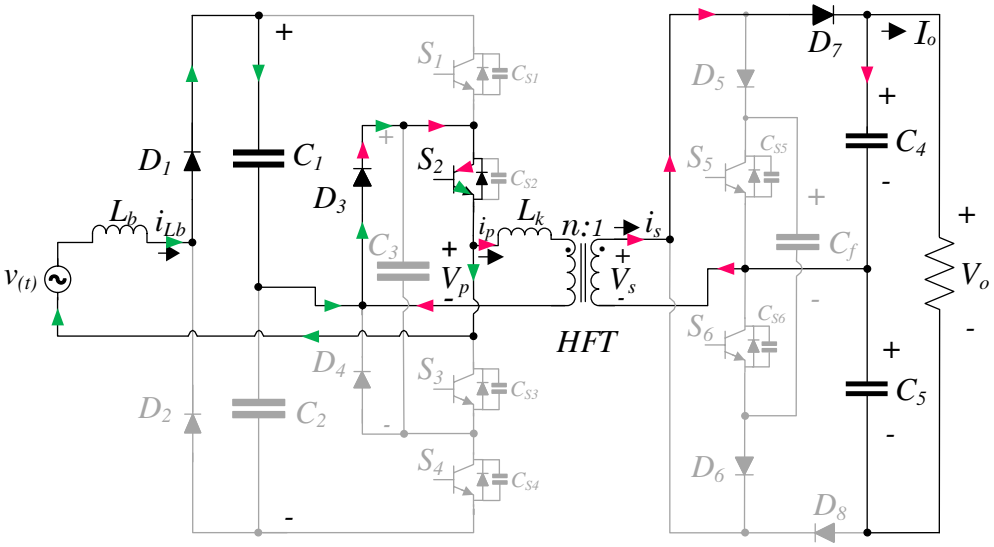

Figure 3.6: [t_3-t_4] Interval, steady-state equivalent operating circuits of the proposed topology.

this interval, the primary voltage v_p is negative and equal to the voltage of capacitor C_2 whereas the secondary voltage v_s is still positive as in the previous interval as depicted in Fig. 3.7. The interval time duration is the same as that of $[t_o - t_1]$ *Interval* and the primary current is calculated by:

$$i_p(t) = -\frac{1}{L_k}\left(V_{C2} + \frac{nV_o}{2}\right)(t - t_4) + I_4 . \qquad (3.9)$$

At the end of this interval, the primary current i_p is equal to zero which makes $[I_5 = 0]$.

3.2.C. vi $[t_5 - t_6]$ *Interval*: The primary current i_p changes polarity and flows through S_3, S_4, and C_2 as presented in Fig. 3.8. Switch S_6 turns ON before the primary current i_p becomes negative to achieve soft-switching at turn ON. The secondary current i_s now flows through S_6 and D_6 which generates a zero-voltage level across the HFT secondary winding. The primary voltage v_p is equal to the negative voltage of capacitor C_2, and the voltage of the secondary side v_s is equal to zero. The interval time duration is the same as that of $[t_1 - t_2]$ *Interval*. The primary current can be described by:

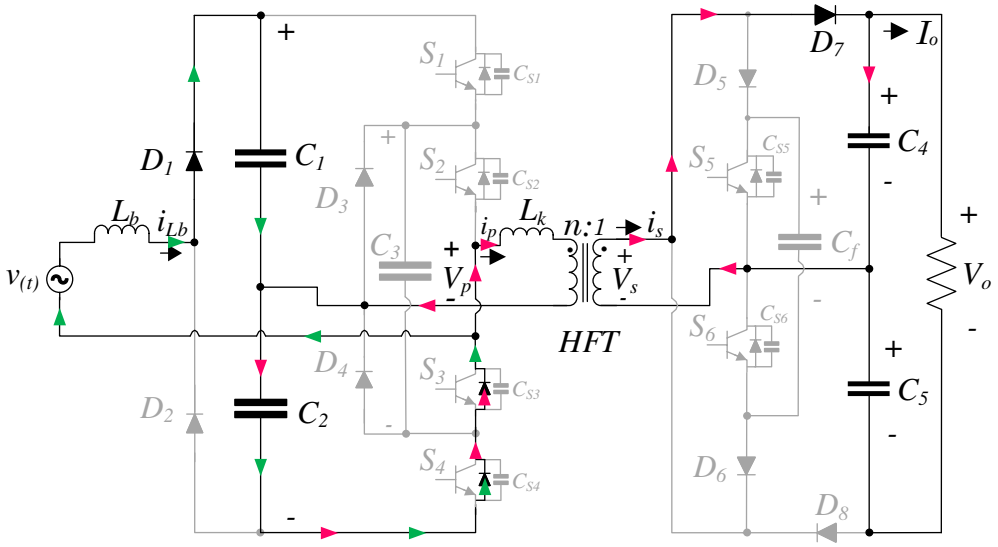

Figure 3.7: $[t_4\text{-}t_5]$ Interval, steady-state equivalent operating circuits of the proposed topology.

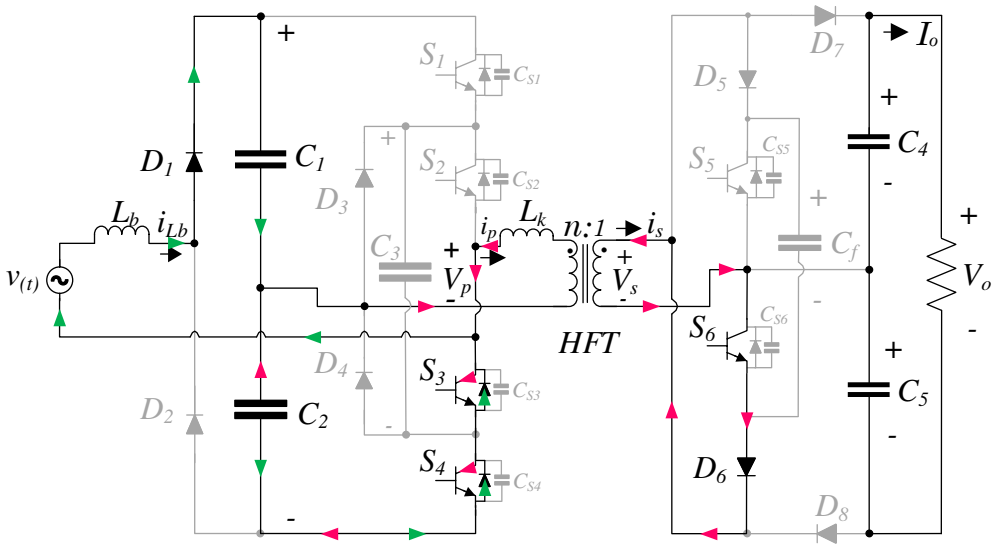

Figure 3.8: [t_5-t_6] Interval, steady-state equivalent operating circuits of the proposed topology.

$$i_p(t) = -\frac{V_{C2}}{L_k}(t - t_5) + I_5 . \qquad (3.\ 10)$$

In this stage, the initial condition of the primary current i_p is $I_5 = I_1 = 0$. By evaluating (3.10) at [$t = t_6$], the peak of the primary current at the end of the interval is I_6 which in steady-state equals [$-I_2$].

3.2.C. vii [$t_6 - t_7$] *Interval*: At the beginning of this interval, switch S_6 turns OFF, and the secondary current i_s flows through C_5 and D_8. The primary current i_p flows through S_3, S_4 and C_2 and continues to decrease at a rate of [$(nV_o/2 - V_{C2})/L_k$]. For the particular case shown in Fig. 3.9, at the end of this interval, i_p is at its maximum negative peak value. The primary voltage v_p is equal to the negative voltage of capacitor C_2 while the voltage of the secondary side v_s is equal to the negative voltage of capacitor C_5. The time duration of this interval is the same as that of [$t_2 - t_3$] *Interval*, and the primary current i_p can be calculated as:

$$i_p(t) = \frac{1}{L_k}\left(\frac{nV_o}{2} - V_{C2}\right)(t - t_6) + I_6 . \qquad (3.\ 11)$$

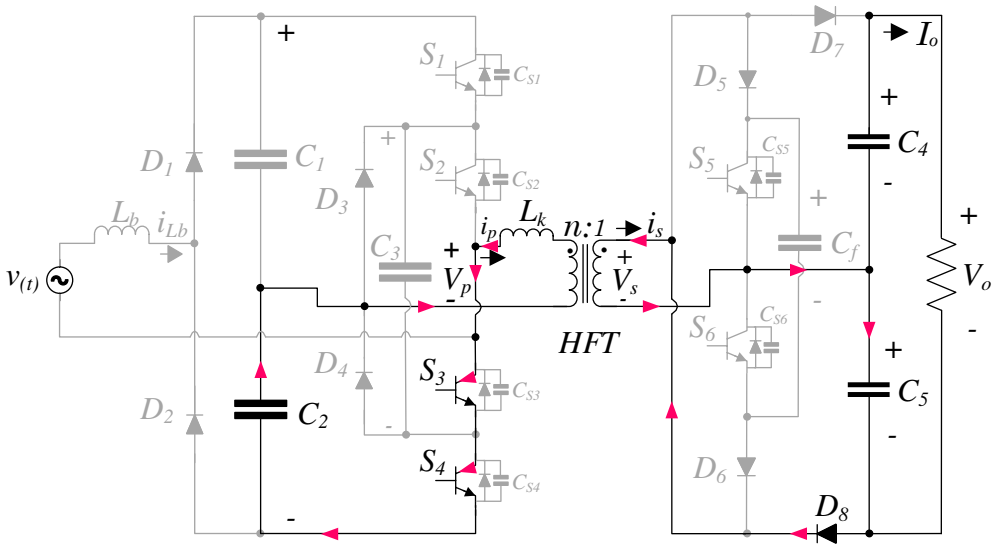

Figure 3.9: [t_6-t_7] Interval, steady-state equivalent operating circuits of the proposed topology.

3.2.C. viii [$t_7 - t_8$] *Interval*: Switch S_4 turns OFF, and the primary current i_p flows through S_3 and D_4 with a positive slope of [$nV_o/(2L_{lk})$]. The secondary current i_s continues to flow through C_5 and D_8 as shown in Fig. 3.10. The primary voltage v_p is equal to zero, and the secondary voltage v_s is equal to the negative voltage of capacitor C_5, [$-V_o/2$]. The time duration of this interval is the same as that of [$t_3 - t_4$] *Interval* and the primary current i_p is given by:

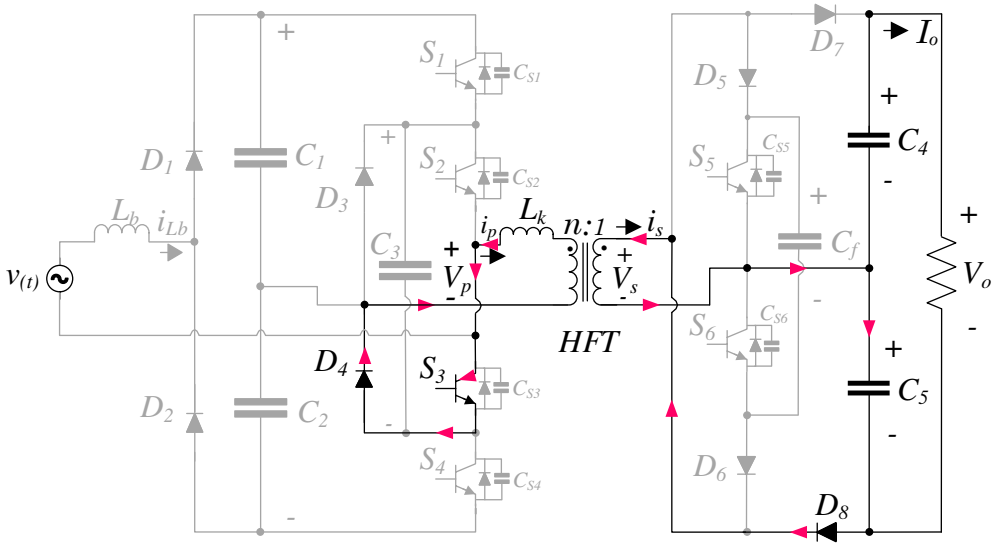

Figure 3.10: [t_7-t_8] Interval, steady-state equivalent operating circuits of the proposed topology.

$$i_p(t) = \frac{nV_o}{2L_k}(t - t_7) + I_7 \,. \tag{3. 12}$$

The initial current is [$I_7 = -I_3$].

The fundamental phase shift φ between primary and secondary voltages can be obtained from the steady-state analysis as follows:

$$\varphi = \frac{D_p}{2} - \frac{nV_o}{2V_{dc}} D_s \,, \tag{3. 13}$$

where V_{dc} is the primary-side dc-link voltage. The total phase shift D_φ between primary and secondary voltages can be expressed in terms of the primary duty cycle D_p, and the secondary duty cycle D_s as follows:

$$D_\varphi = 1 + \frac{D_p}{2} - \left(\frac{nV_o}{2V_{dc}} + 1 \right) D_s \,. \tag{3. 14}$$

3.3 Soft-Switching Analysis

The analysis for realizing soft switching at turn ON in this section concentrates only on switch S_1 (primary side) and switches S_5 and S_6 (secondary side). Due to the symmetry of the primary and secondary currents, i_p and i_s, the rest of the switches have the same operating principles and analytical processes. All devices in both transformer sides turn OFF at ZVS.

3.3.A Primary-Side Switches

The capacitance of the dc-bus capacitors (C_1, C_2) is equal and relatively large in contrast to the flying capacitor C_3. Furthermore, the capacitance of C_3 is much larger than the parasitic capacitance of the switches (C_{S1}, C_{S2}, C_{S3}, and C_{S4}). For the sake of simplicity, the voltages of (C_1, C_2, and C_3) are assumed constant, and the voltage drops across each semiconductor device are neglected.

Initially, S_3 and S_4 are ON, and S_1 and S_2 are OFF as indicated in Fig. 3.9. The primary current flows through the primary coil, S_3, S_4, and C_2 as shown in Fig. 3.9 (pink arrows). C_{S1} is connected in series to the parallel combination of C_3 and C_{S2}. As a result, the voltage of the dc-bus capacitors must be distributed equally between C_{S1} [$V_{CS1} = V_{C1} = V_{C2}$] and the parallel combination of C_3 and C_{S2} [$V_{CS2}||V_{C3} = V_{C1} = V_{C2}$].

As soon as S_4 turns OFF while S_3 still ON, if [$I_7 < 0$] the parasitic capacitance C_{S4} charges up to V_{C1} and C_{S1} discharges up to zero while the voltage across C_3 and C_{S2} remains constant. During [t_6-t_7] *Interval* which represented in Fig. 3.9, S_1 can be turned ON at ZVS. The next stage is to turn S_3 OFF at ZVS, which forces C_{S3} to charge up to V_{C1}, and discharge C_{S2} up to zero. The primary current is now flowing through the anti-parallel diodes of S_1 and S_2, C_1, and the leakage inductance L_k, which defines the condition of turning S_1 and S_2 at ZVS (Fig. 3.3). The condition that guarantees I_o is negative by the beginning of [t_0-t_1] *Interval* is given by:

$$D_{\varphi} + D_s \geq 1. \tag{3. 15}$$

The flying capacitor C_3 increases the range of soft switching for S_1 and S_4 whereas the energy stored in L_k enables discharging and charging actions for C_{S2} and C_{S3}, respectively.

3.3.B Secondary-Side Switches

Fig. 3.11(a) shows the equivalent secondary-side circuit of the transition between [t_1-t_2] *Interval* and [t_2-t_3] *Interval* that was presented in Fig. 3.3. The flying capacitor C_f is connected to the nodes between D_5 and S_5, and D_6 and S_6. The significance of C_f is it allows drain-source capacitance of the S_5 and S_6 to be discharged to achieve ZVS at turn ON. Once S_5 turns OFF, the secondary current charges C_{S5} up to V_{C4} and discharge C_{S6} up to zero as indicated in Fig. 3.11(a). Since the capacitance value of C_f is large compared to the parasitic capacitances of the switches and diodes, its voltage is almost constant at all operating modes. At the instant when S_5 is turned

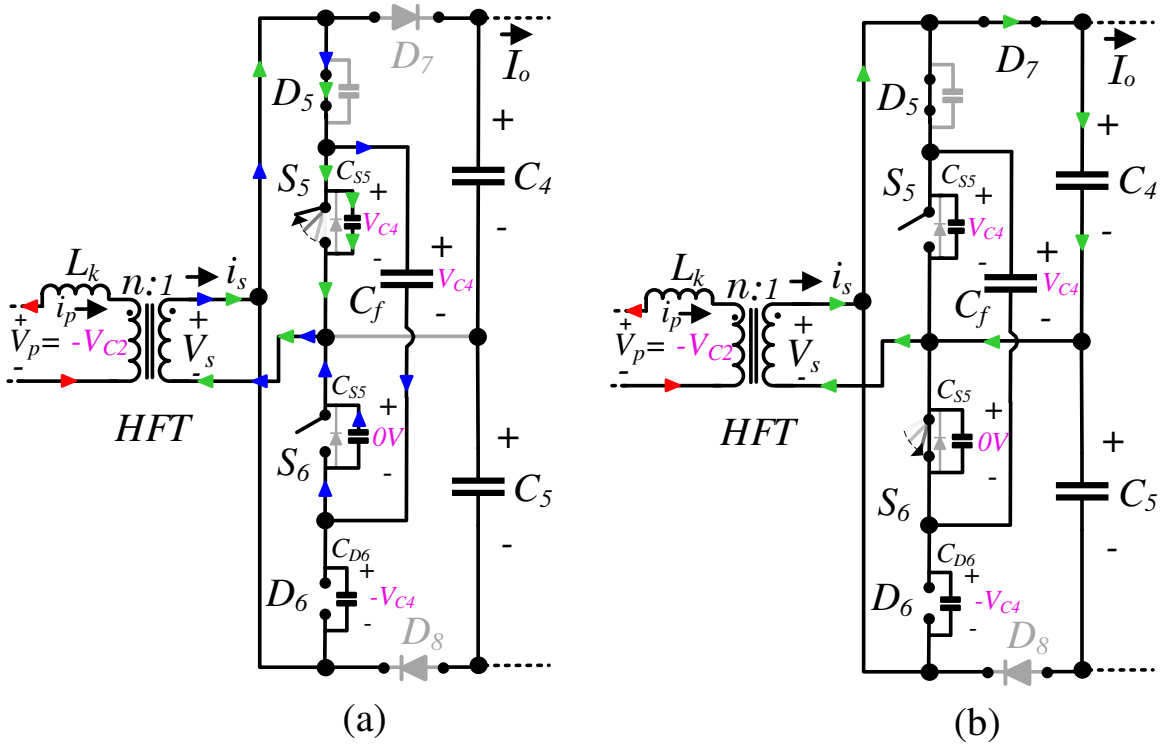

Figure 3.11: Equivalent secondary side circuit showing charging and discharging C_{S5} and C_{S6}. (a) At turning S_5 OFF, (b) at turning S_6 ON.

OFF, [$i_s = nI_2$] is assumed to be constant. By assuming that [$C_{S5} = C_{S6} = C_S$], the following expression is obtained:

$$nI_2 = C_S \frac{dV_{S5}}{dt} + C_S \frac{dV_{S6}}{dt}. \qquad (3.16)$$

By integrating (3.16) in both sides, the maximum time that takes to charge C_{S5} up to V_{C4}, and discharge C_{S6} up to zero can be found as:

$$t_{\max} = \frac{4C_S f_{sw} L_k V_{C4}}{nV_{C1}(1-D_s)}, \qquad (3.17)$$

where D_s is the secondary-side duty cycle, which is limited by [$0 < D_s < 1$]. The inequality that defines D_s boundaries is due to the fact that [$D_s = 0$] means S_5 is ON during the entire positive half cycle, and $D_s = 1$ means S_5 is OFF during the complete positive half cycle. As soon as D_7 becomes forward biased, the output capacitor C_4 is charged by the secondary current as shown in Fig.

3.11(b) (green arrows). Now, S_6 can be turned ON at ZVS and ZCS, as long as [i_s > 0] and conducting through D_7.

The analysis of charging C_{S6} and discharging C_{S5} is similar to the previous approach. Once S_6 turns OFF, C_{S6} is charged up to V_{C4} and C_{S5} is discharged up to zero, which represents the transition between Fig. 3.8 and Fig. 3.9. The drain-source voltage of S_5 starts to decrease at a rate of [$-C_{s5}dV_{S5}/dt$] until it reaches zero, and the drain-source voltage of S_6 starts at the same time to increase at a rate of [$C_{s6}dV_{S6}/dt$] until it reaches V_{C4}. At that moment, D_8 starts to conduct and S_5 can be turned ON at ZVS and ZCS as long as [i_s < 0], and flowing through D_8.

Fig. 3.12 shows the Matlab™ simulations of the gate-source signals V_{gs}, drain-source voltages V_{ds}, and drain currents i_d of S_5 and S_6. The zero voltage and zero current switching transitions, and the times where the parasitic capacitances C_{S5} and C_{S6} are discharging are marked in the figure as *ZVS*, *ZCS*, and discharge respectively.

3.4 Converter Design Procedure

The design guidelines of the proposed topology are presented by considering the following converter specifications: sinusoidal ac input voltage [$v\ (t) = 110\ V_{RMS}$] operating at 60 Hz, output power [P_o = 900-W], output voltage [V_o = 200-V] and switching frequency [f_{sw} = 20-kHz].

The dc voltage V_{dc} of the primary side is selected to be larger than twice of the peak input voltage V_{pk} to insure a high PF.

$$V_{dc} > 2\sqrt{2}v_{pk} \cong 312\ V\ . \qquad (3.\ 18)$$

Then, 450-V is selected as the dc-bus voltage in the primary side. Therefore, capacitors C_1 and C_2 should be rated higher than 200-V.

3.4.A Boost Inductor Design

The boost inductor of the proposed topology is sized to operate under DCM that is insured by

satisfying the following inequality:

$$\frac{1}{2}\Delta i_{Lb} \geq i_{Lb}\,, \tag{3. 19}$$

where Δi_{Lb} is the inductor peak ripple current and can be calculated as:

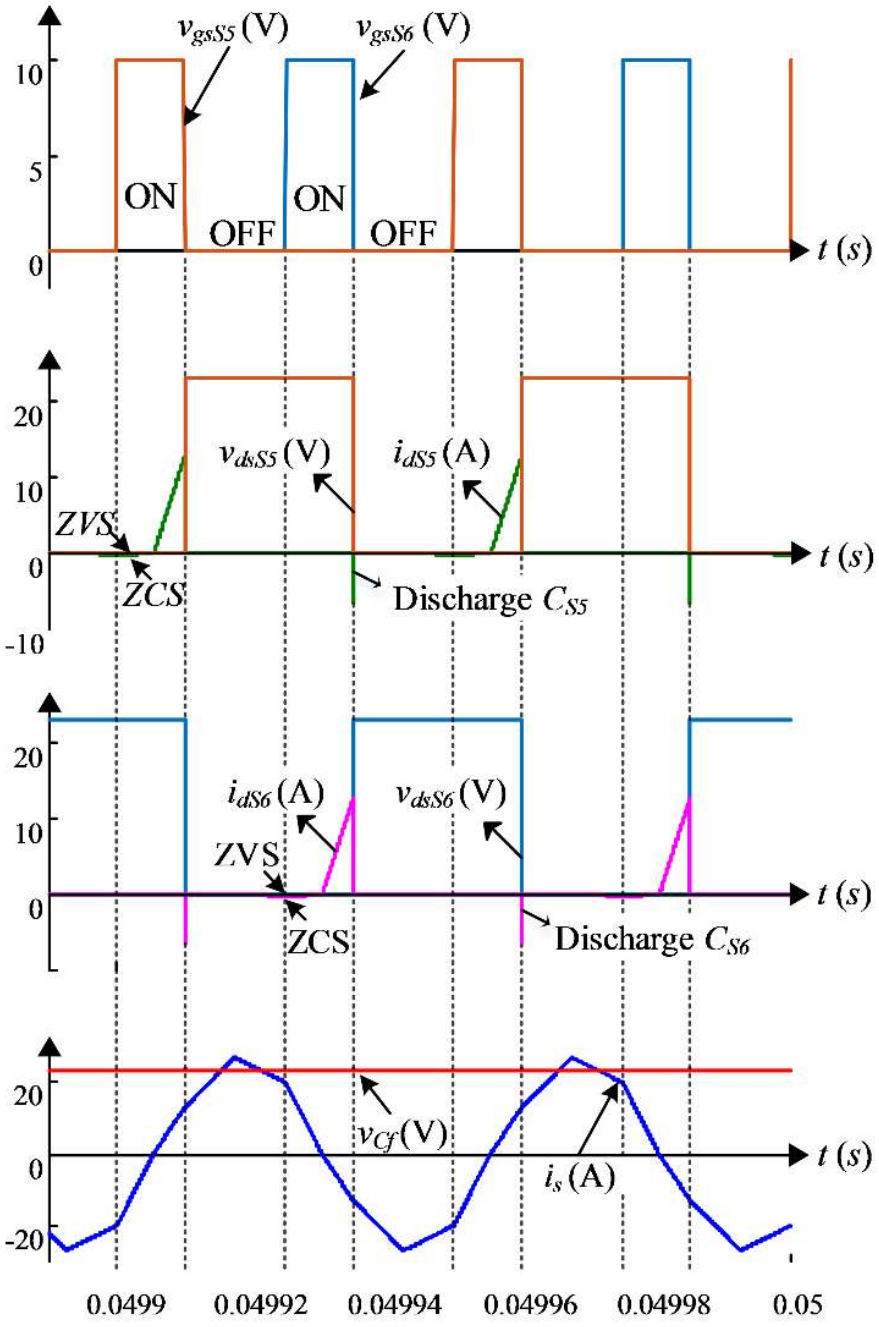

Figure 3.12: Simulation waveforms of the soft-switched proposed topology (secondary side).

$$\Delta i_{Lb} = \frac{V_{dc} D_p T_{sw}}{2L_b}, \tag{3. 20}$$

and

$$i_{Lb} = \frac{P_{\max}}{V_{in(pk)} D_p}. \tag{3. 21}$$

By combining (3.19), (3.20), and (3.21), the critical value of the boost inductor to operate at DCM is determined as follows:

$$L_b \le \frac{V_{in(pk)}^2 D_p^2}{8 f_{sw} P_{\max}}. \tag{3. 22}$$

For 900-W and [$D_p = 1$], then L_b should be equal or less than 160 μH. The lower limit for L_b should be selected to avoid exceeding the rating current of the NPC devices. The boost inductor current is obtained as:

$$i_{Lb(pk)} = \frac{V_{in(pk)}}{2 f_{sw} L_b}. \tag{3. 23}$$

3.4.B DC-Bus Capacitor Selection

The dc-bus capacitors C_1 and C_2 are designed based on the allowed peak-to-peak voltage ripple [$\Delta V_{C1} = \Delta V_{C2} < 0.05*250$]. Because the peak current of the boost inductor $i_{L(pk)}$ flows through the dc-bus capacitors, C_1 and C_2 are calculated as:

$$C_1 = C_2 = \frac{P_{\max}}{2 V_{in(pk)} f_F \Delta v_{C1}}, \tag{3. 24}$$

where f_F is the fundamental frequency of the ac source. The two capacitors calculated using (3.24) are [$C_1 = C_2 > 4300\mu F$].

3.4.C High-Frequency Transformer Design

The design of a high/medium-frequency transformer has been presented in many publications including, design steps [3.17], design trade-offs [3.18], and practical solutions of HFT [3.19]. The

most important parameters to consider are the required leakage inductance, turns ratio [$n = v_p / v_s$], and magnetizing inductance L_m. The value of L_m depends on the geometry of the cores and the number of turns. In this topology, L_m is assumed to be considerably large, so it can be eliminated from the analysis. The proposed topology can operate as a buck or boost converter based on the selection of n. If the secondary voltage v_s referred to the primary side is larger than primary voltage v_p, then the converter operates in boost mode; otherwise it operates in buck mode. For the given [$v_p = 200\ V$] and [$v_s = 100\ V$], n should be less than 2 to operate in buck mode. In this paper, the buck mode is of interest. Following the procedure design given in [3.18] and the specifications of the proposed topology, the optimal flux B_{opt} for the S8020E-026 ferrite material is 0.0536 T, and the required number of primary turns N_p is calculated as:

$$N_p = \frac{V_p}{k_v B_{opt} A_c f_{sw}}, \tag{3. 25}$$

where [$k_v = 4$] is the waveform factor, and [$A_c = 7.78\ cm^2$] is the core cross sectional area. Using (3.25), [$N_p = 50$], so the number of secondary turns should be [$N_s \geq N_p v_s / v_p$]. Therefore, n should be selected as:

$$n_c < n \leq \frac{v_p}{v_s} = 2, \tag{3. 26}$$

where n_c is the turns ratio limit for which the converter is not able anymore to regulate the output voltage v_o to the required level. The selection of n is a function of the rating of the semiconductor devices. However, selecting n close to 1 is the best choice in terms of transformer efficiency [3.18].

The output power delivered from the ac-source to the load during the positive half-switching cycle is given by:

$$P_o = \frac{2}{T_{sw}} \int_{t_o}^{T_{sw}/2} v_p i_{Lk}(t) dt \,. \tag{3. 27}$$

By solving the integral term of (3.27), the following expression is obtained:

$$P_o = \frac{v_p^2}{4 f_{sw} L_k} \left(\frac{n V_o}{v_p} A + B \right). \tag{3. 28}$$

where

$$A = -\frac{D_p^2}{2} - \frac{D_s^2}{2} - D_\varphi^2 + D_s + D_\varphi \left(D_p - D_s + 1 \right) - \frac{1}{2}, \tag{3. 29}$$

and

$$B = D_p^2 + 2 D_p \left(1 - D_s - D_\varphi \right). \tag{3. 30}$$

The maximum output power $P_{o(max)}$ is obtained when the phase shift between the primary and secondary voltages D_φ equals 0.5 and the primary side duty D_p equals one. The needed value of D_s for maximum power can be obtained from (3.14) as [D_s = 0.83]. Then, the required leakage inductance L_k can be calculated from (3.28) as 146 µH.

3.4.D Output Capacitor Selection

When S_5 turns OFF, D_7 is forward biased and the secondary current i_s is equal to:

$$i_s(t) = n i_p(t) = C_4 \frac{\Delta V_{C4}}{\Delta t} + \frac{V_o}{R_o} \,. \tag{3. 31}$$

C_4 charges as long as i_s is larger than the output current I_o, and C_4 discharges when i_s is smaller than I_o. During the time duration of this interval [$\Delta t = (1 - D_s) T_{sw}/2$], i_s has three different slopes described by (3.5), (3.7), and (3.9). Rearranging (3.31) and integrating both sides, C_4 can be calculated as:

$$C_4 = \frac{n^2 V_o}{16 f_{sw}^2 L_k \Delta V_{C4}} \left[A_1 + \frac{2 V_{C1}}{n V_o} B_1 - \frac{4 L_k f_{sw} D_s}{n^2 R_o} \right], \tag{3. 32}$$

where

$$A_1 = -\frac{D_p^{\,2}}{2} - \frac{D_\varphi^{\,2}}{2} - \frac{D_s^{\,2}}{2} + D_p D_\varphi \,, \tag{3. 33}$$

and

$$B_1 = -\frac{D_\varphi^{\,2}}{2} - \frac{3D_s^{\,2}}{2} + 2D_s + D_\varphi + D_p D_s - 2D_\varphi D_s - \frac{1}{2}. \tag{3. 34}$$

for [ΔV_{C4} < 0.05*100] , [D_p = 1], [D_φ = 0.5], and [D_s = 0.84] the minimum value of the output capacitors can be found using (3.32) as [$C_4 = C_5$ > 20 μF].

3.5 Simulation and Experimental Results

3.5.A Simulation Results for Case Study

A microgrid provides advantages to utilities and users in terms of power quality and power management [3.20]. A typical microgrid includes renewable energy resources (e.g., wind turbines, photovoltaic arrays, etc.), distributed grid lines (ac grid, dc grid), power conversion units (power converters, transformers) and loads (ac load, dc load) [3.21]. Recent research proposed a new topology that connects wind and photovoltaic (PV) systems to ac-grid [3.22]. The proposed topology is analyzed to connect a type-4 wind turbine to a dc main bus of a hybrid microgrid as shown in Fig. 3.13 and the specifications of this case study are shown in Table 3-I.

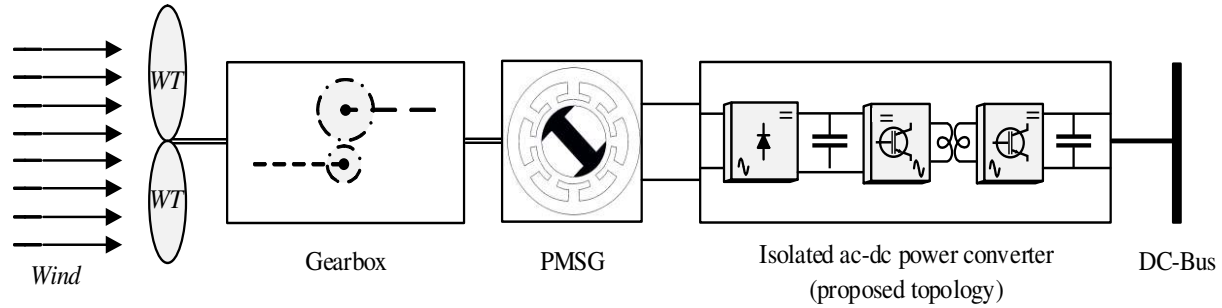

Figure 3.13: Type-4 wind turbine configuration, wind turbine blades, gearbox, PMSG, ac-dc power converter, and DC-bus.

Table 3-I: Simulation Specifications

Parameters	Values
Output power P_o (kW)	25
Switching frequency f_{sw} (kHz)	20
Input voltage $v(t)$ (V_{RMS})	690
High-side dc-bus voltage $V_{dc} > 2V_{inpk}$ (kV)	2
Low-side capacitors voltages $V_{c4} = V_{c5}$ (kV)	1
Output voltage V_o (kV)	2
Output current I_o (A)	12.5

Steady-state simulations are shown in Figs. 3.14 thought Fig. 3.16. The input current displayed in Fig. 3.14 is in phase with the input voltage. The boost inductor voltage and current, and the dc-bus voltage are plotted in Fig. 3.15. The oscillations that appears in the inductor voltage occurs when the boost inductor current is zero due to a resonance between D_1, S_1, and S_2 parasitic capacitances and the boost inductor. The transformer primary and secondary voltages, and primary current are shown in Fig. 3.16.

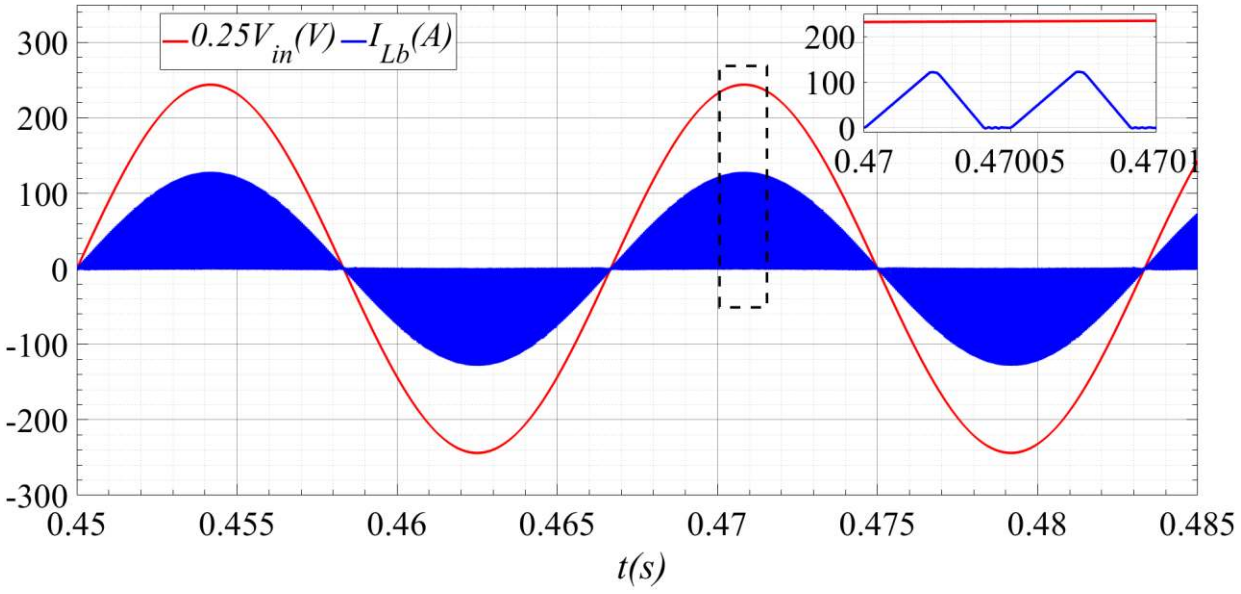

Figure 3.14: Simulation waveforms of the input voltage and current.

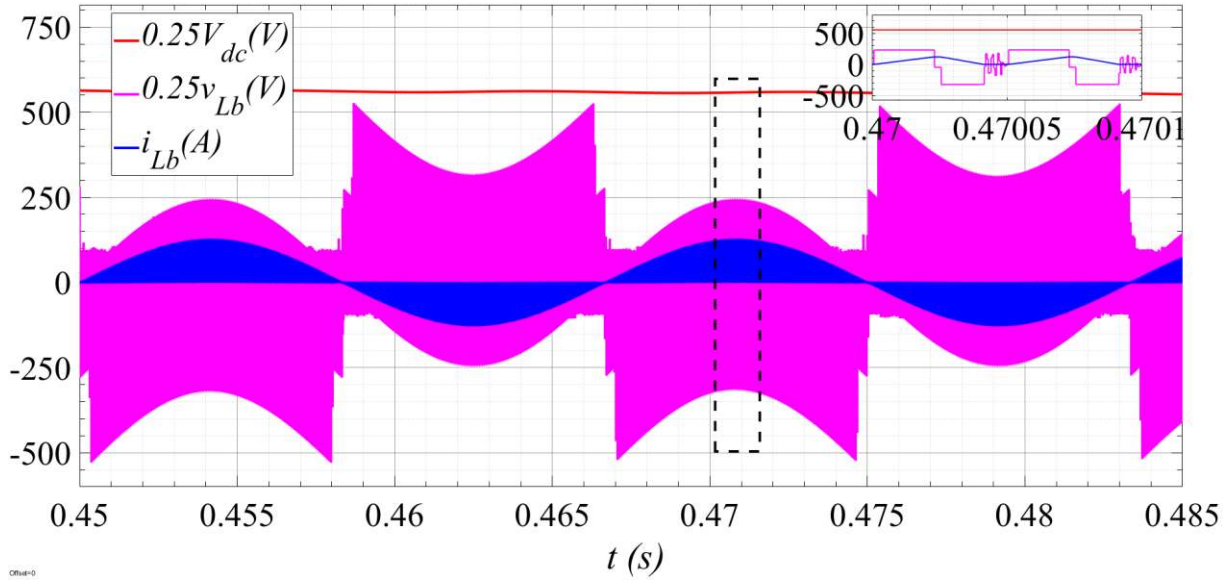

Figure 3.15: Simulation waveforms of the dc-bus voltage V_{dc}, boost inductor (voltage v_{Lb}, current i_{Lb}).

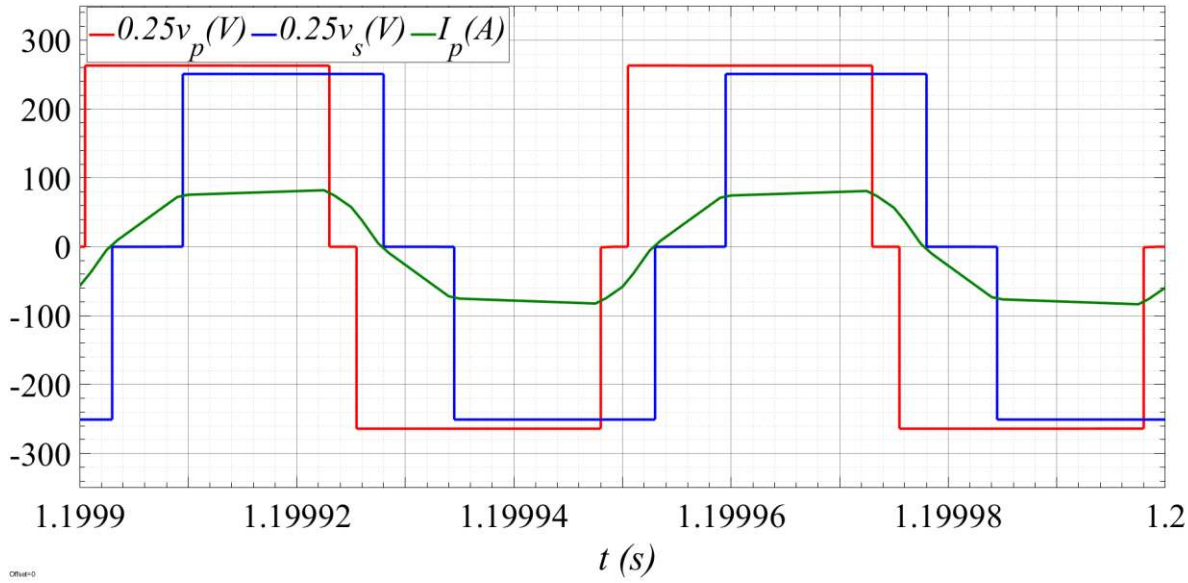

Figure 3.16: Simulation waveforms of the transformer primary-side voltage v_p, secondary-side voltage v_s, and primary current i_p.

Fig. 3.17 shows the output power P_o, dc bus voltage V_{dc}, and secondary duty cycle D_s, as a function of primary duty cycle D_p with D_ϕ as a parameter, using the converter specifications given in Table 3-I.

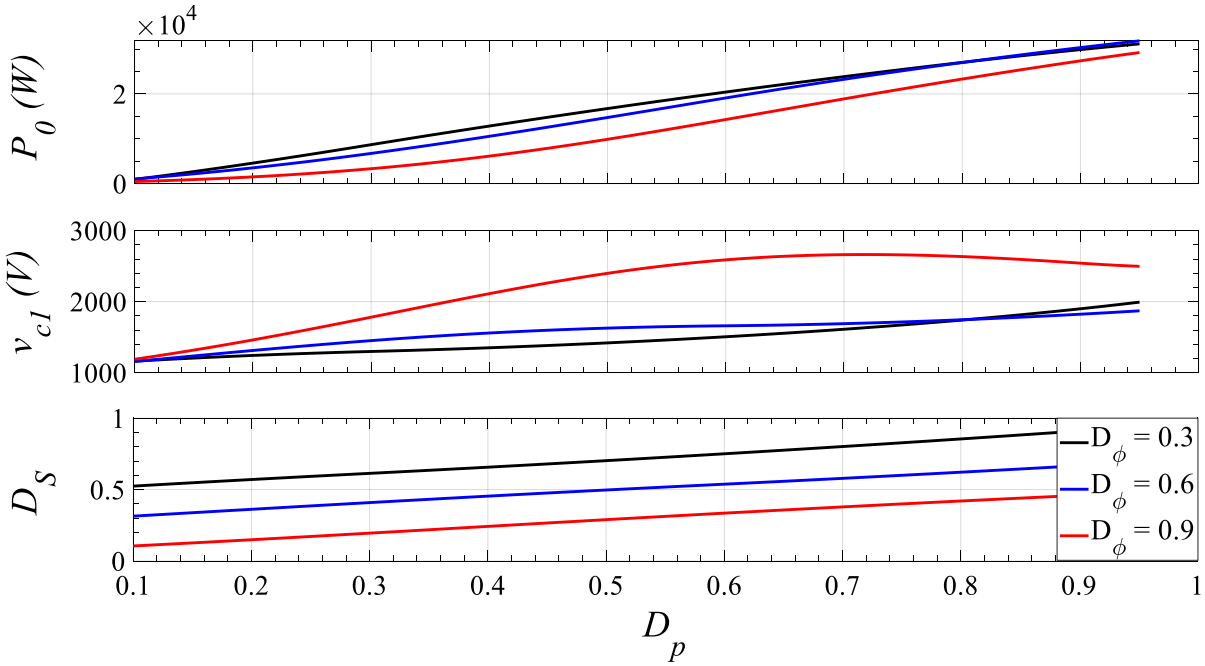

Figure 3.17: Output power P_o, dc bus voltage v_{C1} and secondary duty cycle D_s as a function of the primary duty cycle D_p with D_ϕ as a parameter.

The output voltage is constant and equal to 2000 V. These results correspond to the evaluation of the steady-state expressions given in *Section II*. According to these results, this paper proposes the use of D_p to control P_o, and D_ϕ to control V_{dc}. Also, Fig. 3.17 shows that D_s is a function of the converter operating point, which makes the dynamic of the system highly nonlinear. However, since the objective of this paper is to propose a new low-cost isolated three-level ac-dc topology, the authors do not consider it necessary to include this information in this paper because of the space that would be required to do so. Fig. 3.18 shows the block diagram of the prototype implemented in this work using three control loops:

1) An outer voltage loop to regulate the output voltage, adjusting D_p.

2) A transformer current controller to avoid saturation and to balance the voltage across the capacitors, adjusting the positive or negative half-cycle of D_p (D_{aux}).

3) A dc-bus voltage controller to regulate its value as a function of load specifications, adjusting D_ϕ.

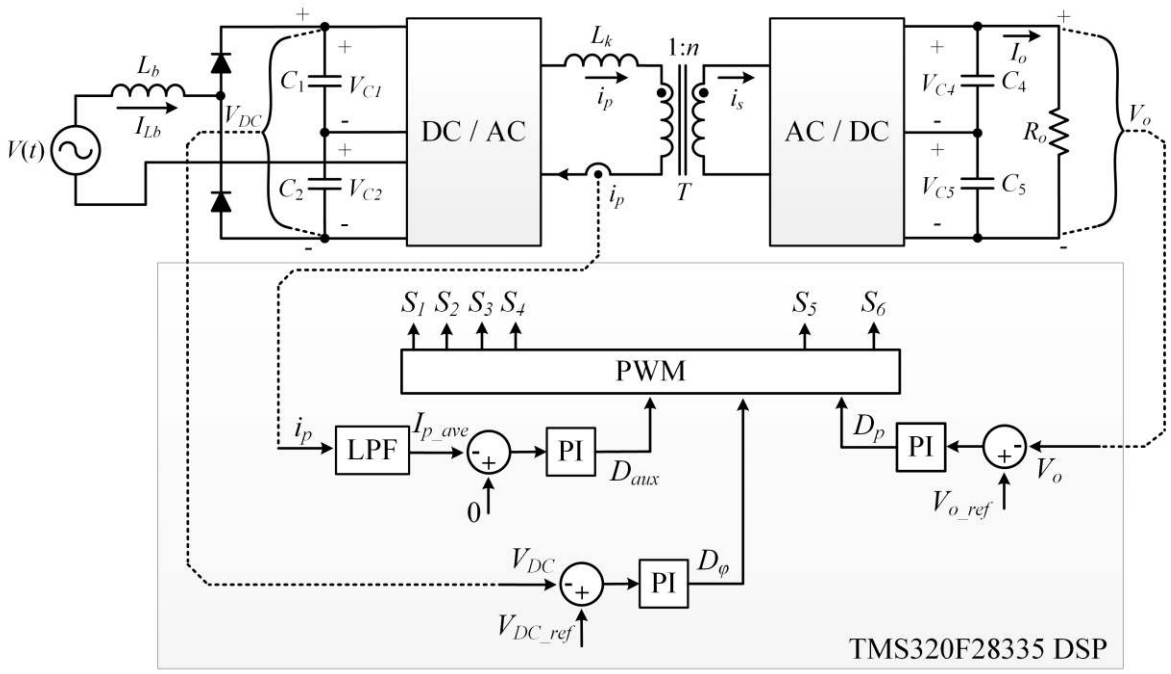

Figure 3.18: Block diagram of the implemented hardware and close-loop control setup.

All these controllers were implemented using proportional-integral (PI) algorithms. The criteria adopted to adjust the controllers is that the loop of the output voltage is the fastest, followed by the control of the transformer current, and the dc bus controller is the slowest.

Figs. 3.19 through 3.20 show the simulated dynamic response of the converter for sudden resistive load change, from 6.5 to 11.5 A, reaching the target operating point in 5 msec. Fig. 3.19 shows input current (boost current) and the grid voltage. The response of the system under the sudden load change remains stable and with a high power factor.

Fig. 3.20 shows the evolution of the input and output capacitor voltages. Independently of the load condition, the voltage across these capacitors is balanced, which can be explained by the fact that the transformer current control ensures a zero-average current. Finally, Fig. 3.21 displays the output voltage, the voltage error signal fed to the controller input, and the PI controller action when the load changes.

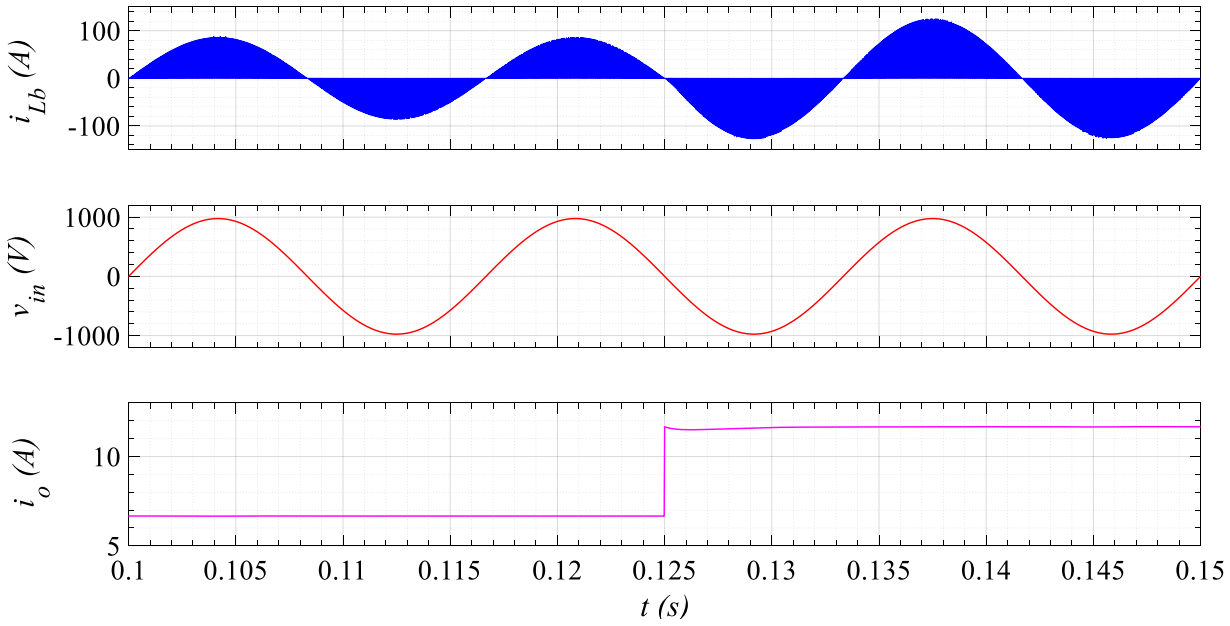

Figure 3.19: Boost inductor current i_{Lb} and input voltage v_{in} response to a load change.

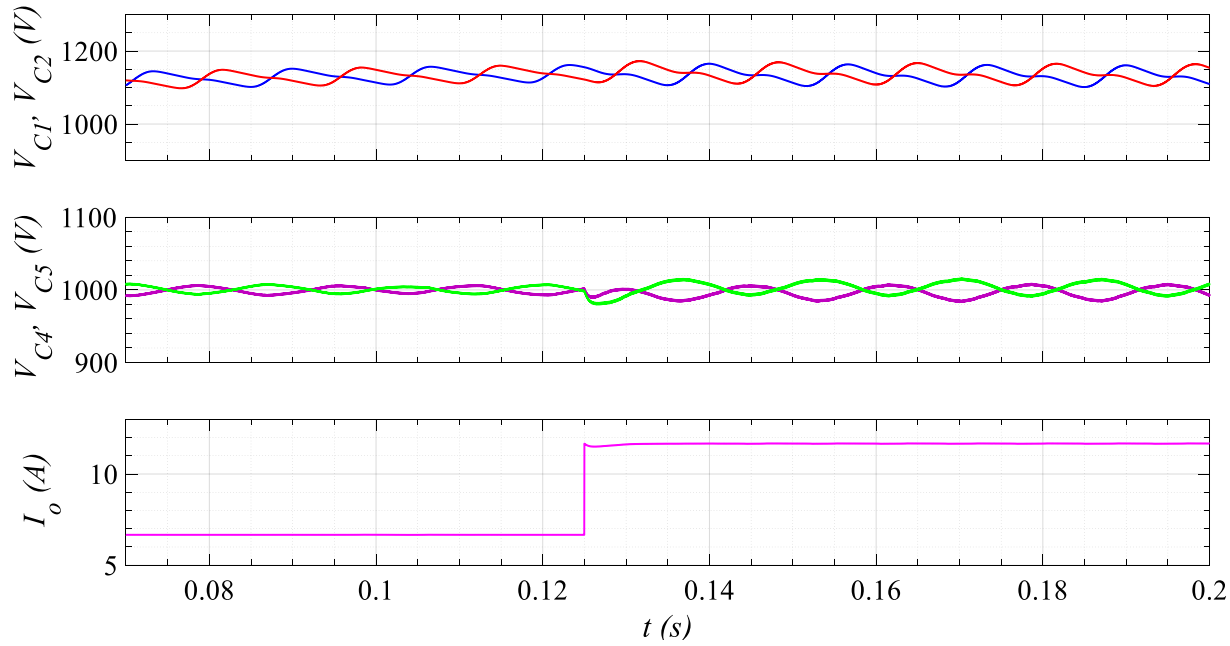

Figure 3.20: Primary capacitor (V_{C1}, V_{C2}) and output capacitor (V_{C4}, V_{C5}) voltages when load change.

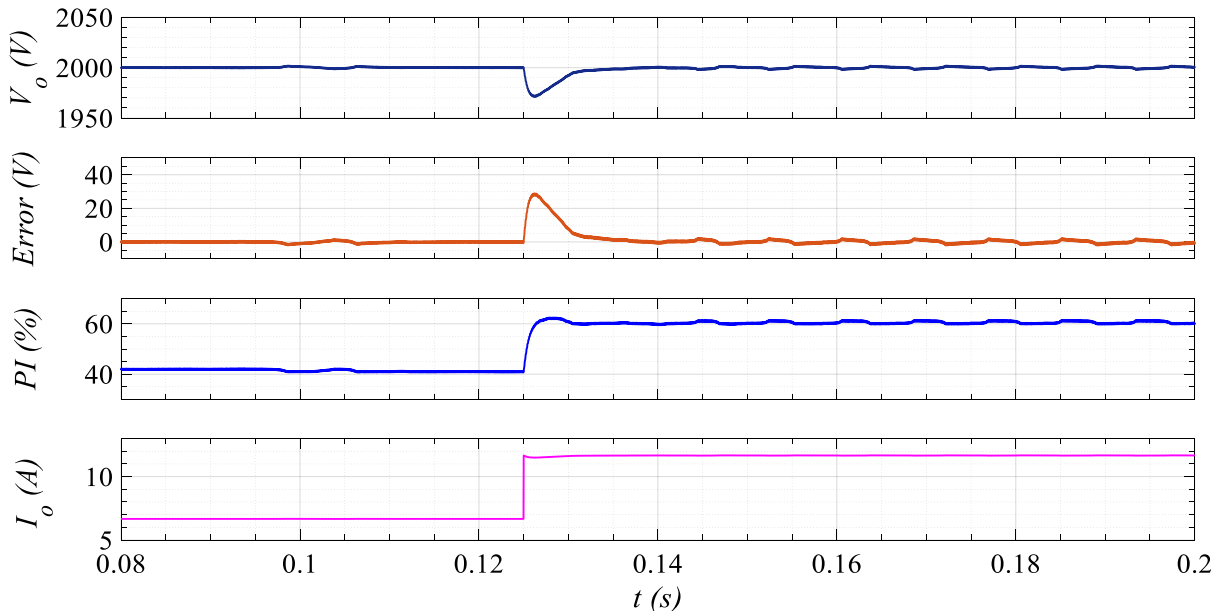

Figure 3.21: Representation of output voltage (*Vo*), PI control signal (*PI*), control error (*Error*) at a load change.

3.5.B Scaled-Down Prototype

A 900-W scaled-down prototype is implemented to validate the proposed topology performance. The main specifications of the prototype are shown in Table 3-II, and the devices selected for this experiment are presented in Table 3-III. The proposed topology setup is shown in Fig. 3.22.

The boost inductor of the proposed topology is sized to operate under DCM and follow the sine wave as shown in Fig. 3.23. As a result, the proposed topology draws power at unity power factor under the condition of having a dc-bus voltage of at least twice the peak of the input voltage; the condition that keeps the converter under DCM operation.

Table 3-II: Experimental Parameters

Parameters	Values
Output power P_o (W)	900
Switching frequency (kHz)	20
Input voltage v_{in} (V_{rms})	110
High-side dc-bus voltage $V_{dc} > 2V_{inpk}$ (V)	450
Low-side capacitors voltages $V_{c4} = V_{c5}$ (V)	100
Output voltage V_o (V)	200
Rated power resistive load R_o (Ω)	73

Table 3-III: Experimental Prototype Devices Selection

Device	Part #/Rated Values
Front-end diodes	RURG5060_F085/600V, 50A
NPC switches	AOK60N30L/300V, 40A
NPC diodes	GP2D020A060B/600V, 31A
Secodary-circuit switches	IPP075N15N3 G/150V, 100A
Secodary-circuit diodes	GP2D020A060B/600V, 31A

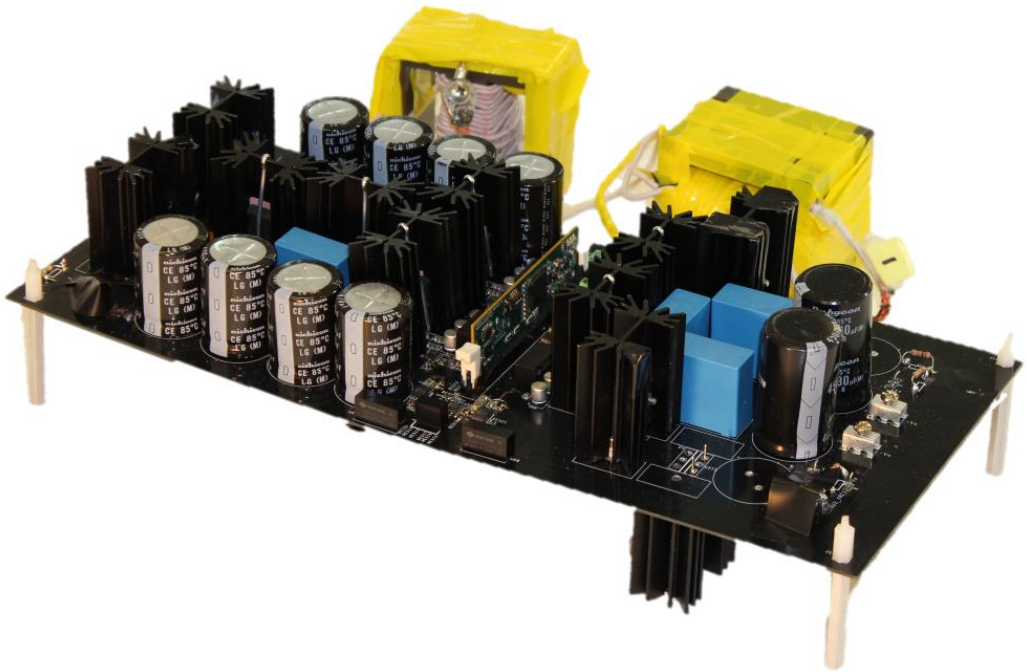

Figure 3.22: Proposed scaled-down prototype topology including AC-DC converter, DSP card, sensors, leakage inductance, and high frequency transformer (PCB dimensions 380mm x 170mm) "Photo by author".

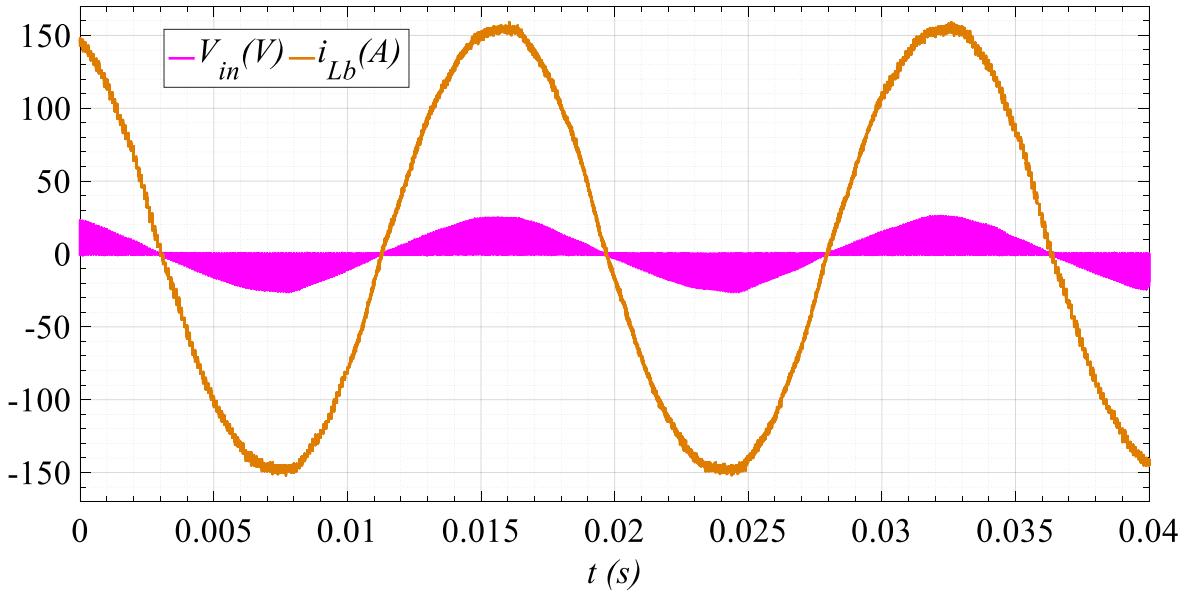

Figure 3.23: Experimental waveform of input voltage v_{in}, and boost inductor current i_{Lb}.

The transformer primary-side voltage v_p and current i_p, the transformer secondary-side voltage v_s, and the boost inductor current i_{Lb} are displayed in Fig. 3.24. For that particular condition, both primary and secondary voltages have three levels. The primary side duty cycle, which limits the input power drawn from the ac source, is used to control the output voltage.

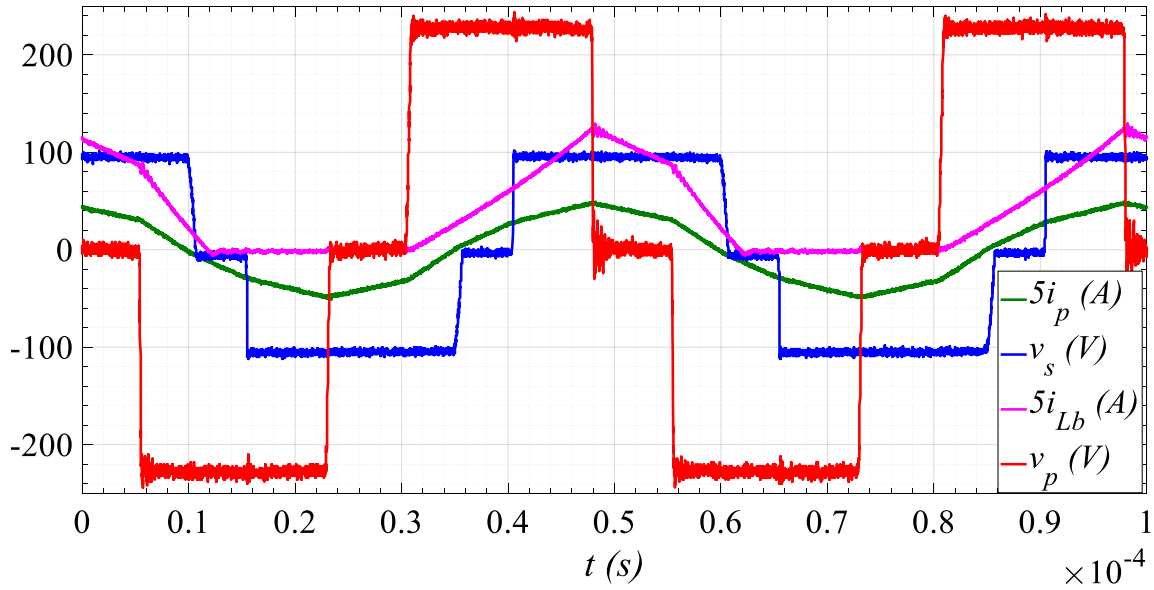

Figure 3.24: Experimental waveforms of the primary voltage (v_p), secondary voltage (v_s), boost inductor current (i_{Lb}) and primary current (i_p).

When S_5 and D_5, or S_6 and D_6, conduct, the voltage across the secondary windings is zero, which defines the duty cycle at the secondary side D_s. D_s is a function of the primary side duty cycle (D_p), the phase shift between v_p and v_s (D_ϕ), and the dynamic voltage level of the converter.

Fig. 3.25 presents the output capacitors voltages (V_{C4}, V_{C5}) and output current I_o. When one of the capacitors discharges through the load, the other one is charged from the dc bus capacitors through the transformer, which in return, smooths the output voltage. As shown in Fig. 3.25, the voltage across each capacitor is balanced and equal to a half of the output voltage.

Fig. 3.26 shows the gate-source and drains-source voltage waveforms of S_5 as well as the secondary side current i_s. It can be seen that S_5 turns ON at ZVS [V_{dsS5} = 0 V] and ZCS [I_{S5} = 0 A] during [t_0-t_1] *Interval* while the secondary current [i_s < 0] and conducts through D_8. Also, S_5 turns OFF at ZVS as shown in the zoomed box at the top corner of Fig. 3.25.

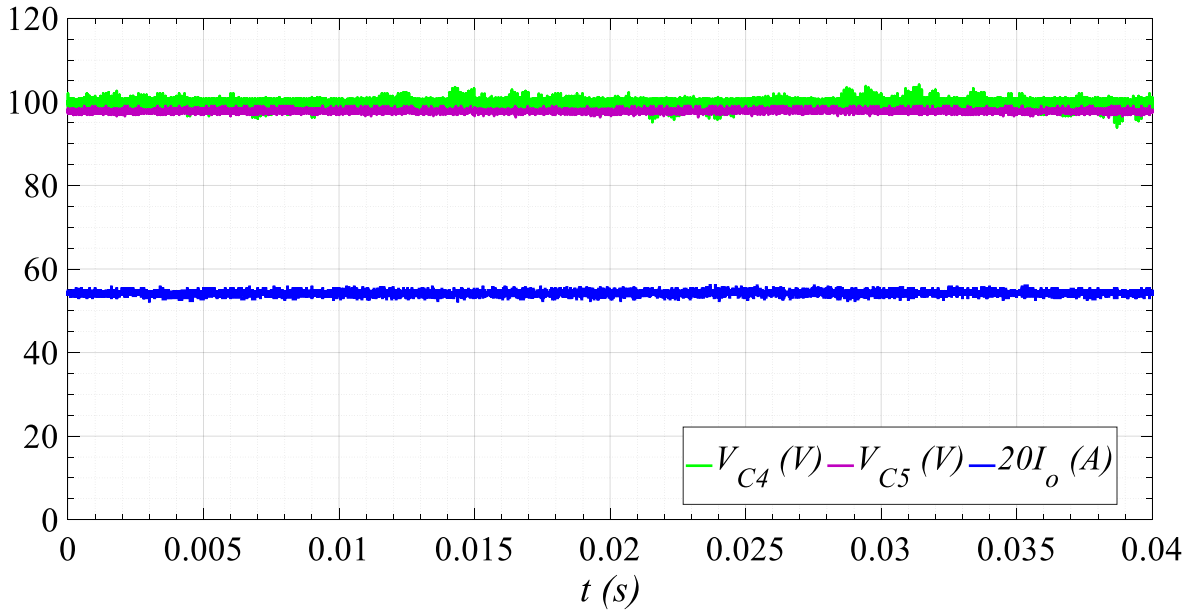

Figure 3.25: Experimental waveforms of the output capacitors voltages (V_{C4}, V_{C5}), and output current (I_o).

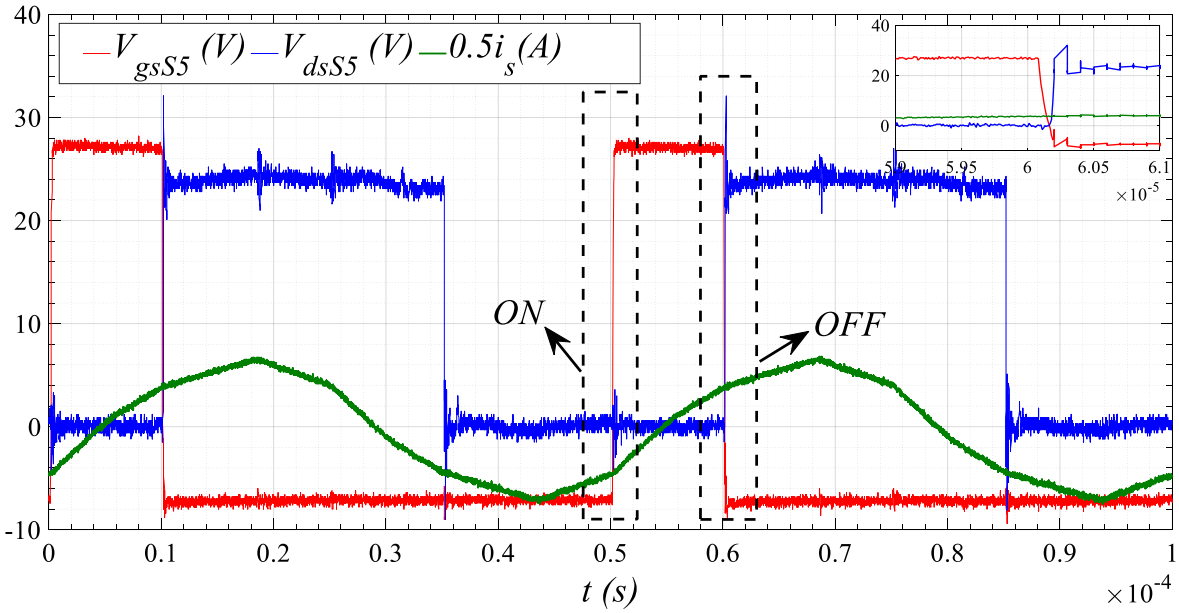

Figure 3.26: Experimental waveforms representing the soft switching transitions of S_5 (ZCS, ZVS) at turning ON and (ZVS) at turning OFF.

Similarly, S_6 turns ON at ZVS and ZCS while the secondary current $i_s > 0$ and conducting through D_7 as explained in *Section III (B)*.

Fig. 3.27 shows the closed-loop response of the converter at the time when a sudden increase in the load occurs. The controller satisfactorily reacts to compensate for the output voltage drop due to the extreme load increase. Also, the controller successfully keeps a stable and even voltage across each dc-link and output capacitors, providing safe operation.

Fig. 3.28 shows the overall efficiency of the proposed topology, where it is remarkable that only 12 % of the total converter losses are due to the proposed secondary side bridge. The latter is due to the soft-switching operation for the entire power range that this converter has, and the fewer devices required to conduct the output current. Table 3-IV presents a comparison among the proposed new topology with other existing ones. The main advantage of using the proposed topology is the capability of controlling the dc bus and output voltage with a minimum number of switches. Furthermore, the total price of the proposed converter is minimum owing to the reduced

number of components. Also, operation under soft-switching mode is possible in the full power operating range. The disadvantage is that this topology is only suitable for unidirectional power applications.

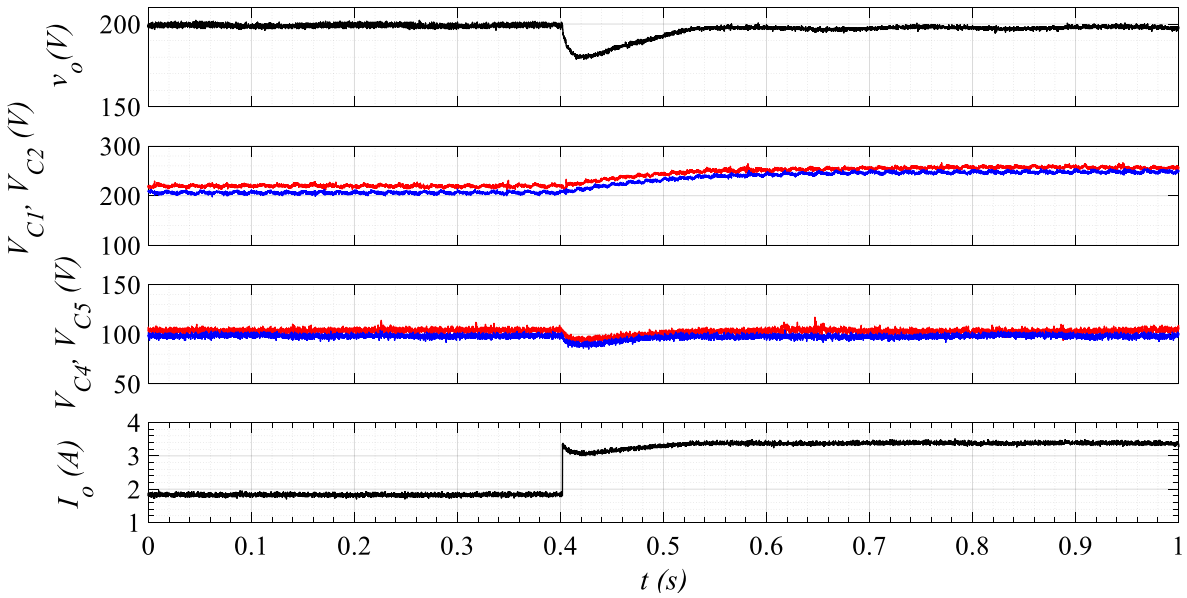

Figure 3.27: Converter transient closed-loop response: Output voltage V_o, dc bus capacitor voltages V_{C1} and V_{C2}, and output capacitor voltages V_{C4} and V_{C5} when a sudden load increase occurs.

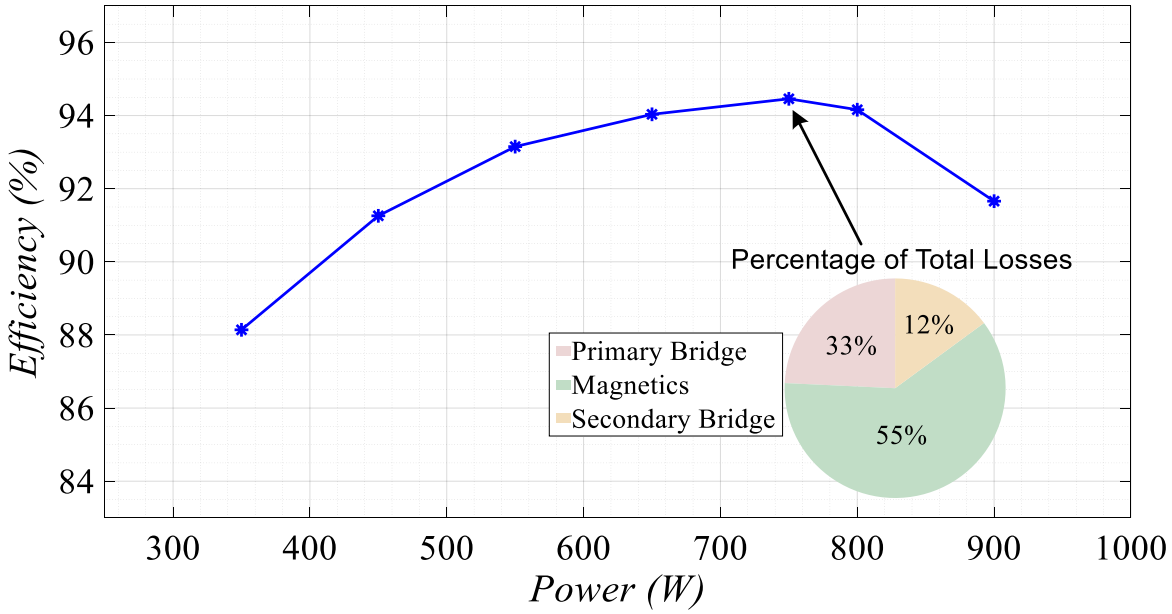

Figure 3.28: Efficiency representation of the proposed ac-dc converter over a wide range of output power.

Table 3-IV: Qualitative Topology Comparison.

Parameters	***Topology #1*** [13]	***Topology #2***[15]	***Topology #3***[16]	***Proposed Topology***
Bidirectional power flow capability	Yes	No	No	No
Total cost	High	Low	High	Fair
Switch blocking voltage	Full	Half	Full	Half
Number of switches	12	4	12	6
Number of diodes	0	6	4	6
Controlling dc-bus and output voltage	Yes	No	Yes	Yes
Capacitors size	Small	Large	Medium	Medium

The remarkable features of the proposed topology over other existing ones are as follows:

1. Been able to control dc-bus and output voltage using only six switches, other similar topologies require more than six switches[3.16],[3.23].
2. Secondary active devices switch at ZVS and ZCS over the full range of power where it is impossible to achieve the same advantage with other existing topologies [3.16].
3. In comparison with the topology presented in [3.16], which claims a maximum efficiency of 93%, the proposed topology exhibits a higher efficiency of 94.5%.

3.6 Conclusions

A new topology for an isolated three-level unidirectional ac-dc power converter was presented and analyzed. The proposed secondary side circuit generates a three level voltage waveform across the secondary side transformer terminals using only two active switches and four diodes. The proposed topology is capable of controlling the input power, dc-bus voltage and output voltage with minimum number of active devices.

Furthermore, the new topology has multiple advantages in terms of cost-effectiveness, preventing power back-flow, and allowing ZCS and ZVS at turn ON without any additional control

effort. The simulation and experimental results for this new topology agreed very well with the theoretical equations, steady-state analysis, and closed-loop control performance.

3.7 References

[3.1] S. Jeong, J. Kwon and B. Kwon, "High-Efficiency Bridgeless Single-Power-Conversion Battery Charger for Light Electric Vehicles," IEEE Trans. on Industrial Electronics, vol. 66, no. 1, pp. 215-222, Jan. 2019.

[3.2] B. Whitaker et al., "A High-Density, High-Efficiency, Isolated On-Board Vehicle Battery Charger Utilizing Silicon Carbide Power Devices," *IEEE Trans. on Power Electronics*, vol. 29, no. 5, pp. 2606-2617, May 2014.

[3.3] M. de Prada, L. Igualada, C. Corchero, O. Gomis-Bellmunt, A. Sumper, "Hybrid AC-DC Offshore Wind Power Plant Topology: Optimal Design," *IEEE Trans. on Power Systems*, vol. 30, no. 4, pp. 1868-1876, July 2015.

[3.4] C. Li and D. Xu, "Family of Enhanced ZCS Single-Stage Single-Phase Iso lated AC–DC Converter for High-Power High-Voltage DC Supply," *IEEE Trans. on Industrial Electronics*, vol. 64, no. 5, pp. 3629-3639, May 2017.

[3.5] T. He, J. Zhu, D. D. Lu and L. Zheng, "Modified Model Predictive Control for Bidirectional Four-Quadrant EV Chargers With Extended Set of Voltage Vectors," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 7, no. 1, pp. 274-281, March 2019.

[3.6] D. Rothmund, T. Guillod, D. Bortis and J. W. Kolar, "99% Efficient 10 kV SiC-Based 7 kV/400 V DC Transformer for Future Data Centers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 753-767, June 2019.

[3.7] T. Guillod, D. Rothmund and J. W. Kolar, "Active Magnetizing Current Splitting ZVS Modulation of a 7kV/400V DC Transformer," *IEEE Trans. on Power Electronics*. doi: 10.1109/TPEL.2019.2918622.

[3.8] F. Nejabatkhah and Y. W. Li, "Overview of Power Management Strategies of Hybrid AC/DC Microgrid," *IEEE Trans. on Power Electronics*, vol. 30, no. 12, pp. 7072-7089, Dec. 2015.

[3.9] J. P. R. A. Méllo and C. B. Jacobina, "Asymmetrical Cascaded Three-Phase AC–DC Converters With Injection Transformers," *IEEE Trans on Industry Applications*, vol. 55, no. 3, pp. 2800-2812, May-June 2019.

[3.10] EN61000-3-2 Edition 2.2: Limits for Harmonic Current Emissions (equipment input current ≤ 16 A per phase), 2004.

[3.11] B. Singh, S. Singh, A. Chandra, K. Al-Haddad, "Comprehensive Study of Single-Phase AC-DC Power Factor Corrected Converters With High-Frequency Isolation," *IEEE Trans. on Industrial Informatics*, vol. 7, no. 4, pp. 540-556, Nov. 2011.

[3.12] J. A. L. Barboza, O. C. S. Filho, L. C. S. Mazza and R. P. T. Bascopé, "Five-level T-type NPC PFC rectifier based on multistate switching cell," *2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC)*, Fortaleza, 2015, pp. 1-6.

[3.13] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen and J. W. Kolar, "Optimal ZVS Modulation of Single-Phase Single-Stage Bidirectional DAB AC–DC Converters," *IEEE Trans. on Power Electronics*, vol. 29, no. 8, pp. 3954-3970, Aug. 2014.

[3.14] B. Zhao, Q. Yu and W. Sun, "Extended-Phase-Shift Control of Isolated Bdirectional DC–DC Converter for Power Distribution in Microgrid," *IEEE Trans. on Power Electronics*, vol. 27, no. 11, pp. 4667-4680, Nov. 2012.

[3.15] S. Dusmez, X. Li and B. Akin, "A Fully Integrated Three-Level Isolated Sngle-Stage PFC Converter," *IEEE Trans. on Power Elctronics*, vol. 30, no. 4, pp. 2050- 2062, April 2015.

[3.16] L. A. Garcia Rodriguez, V. Jones, A. R. Oliva, A. Escobar-Mejía and J. C. Balda, "A New SST Topology Comprising Boost Three-Level AC/DC Converters for Applications in Electric Power Distribution Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 2, pp. 735-746, June 2017.

[3.17] R. J. G. Montoya, A. Mallela and J. C. Balda, "An evaluation of selected solid-state transformer topologies for electric distribution systems," *2015 IEEE Applied Power Electronics Conference and Exposition*, Charlotte, NC, 2015, pp. 1022-1029.

[3.18] O. Aldosari, L. A. Garcia Rodriguez, J. C. Balda and S. K. Mazumder, "Design Trade-Offs for Medium- and High-Frequency Transformers for Isolated Power Converters in Distribution System Applications," *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Charlotte, NC, 2018, pp. 1-7.

[3.19] B. Zhao, Q. Song, W. Liu, "A Practical Solution of High-Frequency-Link Bidirectional Solid-State Transformer Based on Advanced Components in Hybrid Microgrid," *IEEE Trans. on Industrial Electronics*, vol. 62, no. 7, pp. 4587-4597, July 2015.

[3.20] B. S. Hartono, Budiyanto and R. Setiabudy, "Review of microgrid technology," *2013 International Conference on QiR*, Yogyakarta, 2013, pp. 127-132.

[3.21] J. M. Guerrero, P. C. Loh, T. Lee, M. Chandorkar, "Advanced Control Architectures for Intelligent Microgrids—Part II: Power Quality, Energy Storage, and AC/DC Microgrids," *IEEE Trans. on Industrial Electronics*, vol. 60, no. 4, pp. 1263-1270, April 2013.

[3.22] A. Radwan and Y. Mohamed, "Grid-Connected Wind-Solar Cogeneration Using Back-to-Back Voltage Source Converters," *IEEE Trans. on Sustainable Energy.* doi: 10.1109/TSTE.2019.2890828.

[3.23] H. Kim, M. Ryu, J. Baek and J. Jung, “High-Efficiency Isolated Bidirectional AC–DC Converter for a DC Distribution System,” in *IEEE Trans. on Power Electronics*, vol. 28, no. 4, pp. 1642-1654, April 2013.

APPENDIX 3.A

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November 13, 2019

To whom it may concern,

This letter is to verify that Mr. Obaid Martha Aldosari, ID 010768784, is the first author and did at least 51% of the work for the paper titled "A Three-Level Isolated AC-DC PFC Power Converter Topology with Reduced Number of Switches".

Kind Regards,

Dr. Juan Carlos Balda

University Professor, Department Head and Major Advisor to Mr. Obaid Martha Aldosari

A BOOST-BASED T-TYPE PFC UNIDIRECTIONAL SOLID-STATE TRANSFORMER FOR MEDIUM-LEVEL POWER APPLICATIONS

O. Aldosari, L. A. G. Rodriguez, G. G. Oggier and J. C. Balda, "A Three-Level Isolated AC-DC PFC Power Converter Topology with Reduced Number of Switches," in *IEEE Trans. on Industrial Electronics*, Submitted in (04-25-2020).

Abstract

A new three-level isolated ac-dc power factor correction (PFC) topology with a minimum number of semiconductor devices is the main focus of this paper. The proposed topology provides high input power factor (PF), soft-switching, and full control of the primary and secondary side bridges to regulate the intermediate dc-bus and output voltages. Comparing to existing PFC topologies, the proposed configuration has lower voltage rating requirements, which lead to lowering the total cost, minimizing power losses and increasing the converter rated power while using similar rated devices than in other topologies. A theoretical analysis describes the full characterization of the proposed converter. Experimental results on a 1-kW prototype show high PF and efficiency in the whole operating range of the converter.

Index Terms—AC-DC converters, conduction losses, power factor correction, soft-switching, solid-state transformer.

4.1 Introduction

Public concerns about the environmental impact of fossil-based energy sources have increased the demand for renewables such as photovoltaic (PV) modules and wind turbines, as well as the use of electric vehicles and more efficient lighting systems, such as LED technology [4.1]. Power

electronic interfaces are necessary to adapt the characteristics of the non-conventional energy sources to the type of the electric power grid [4.2].

DC loads such as data centers, telecommunication systems and electric vehicle charging stations require ac-dc converters with high-efficiency and high-power density [4.3]-[4.4]. Solid-state transformer (SST) topologies with unidirectional power flow have been proposed for dc loads to eliminate the use of low-frequency transformers [4.3]. The unidirectional SST retains most of the features of the conventional bidirectional SST such as a power-factor correction (PFC), total harmonic distortion control, fault current limiting, isolated dc-bus voltage availability, etc. [4.3], [4.5]-[4.6].

SSTs for ac-dc applications usually consist of two stages: a controlled ac-dc front-end stage, and a dual active bridge converter (DAB) as a second stage [4.7]-[4.9]. The front-end rectifier is realized by a single- or three-phase half-bridge, full-bridge or multi-level converter that controls the shape of the input current and the level of the high-voltage dc bus [4.4], [4.10]-[4.12]. The DAB consists of a primary-side bridge, a high-frequency transformer and a secondary-side bridge [4.13]. Depending on the application, the bridges of the DAB are implemented using half-bridge converters, full-bridge converters, or multilevel converters [4.8]-[4.9], [4.14]-[4.16]. For high power applications, the system is connected to the distribution system (from 2.4 to 34 kVac three-phase feeders), and multiple SSTs are connected in series at the high-voltage side, and in parallel at the low-voltage side establishing a modular multilevel configuration [4.5], [4.8], [4.17]. This solution requires a large number of semiconductor devices, which, in addition to representing a high cost, increases its probability of failure.

In order to reduce the required number of semiconductor devices, boost-based topologies were proposed which combine the SST rectifier stage with the primary-side bridge of the DAB [4.18]-

[4.21]. In [4.18]-[4.19], the DAB secondary-side active bridge was replaced by diodes at the expense of losing control of the high-voltage side dc bus. A three-level boost based unidirectional SST topology was proposed in [4.20] where two full bridges were implemented as the secondary side bridge of the DAB which provides full control of the high-voltage dc bus, and high current output capability. The three-level configuration allows the voltage rating of the semiconductor devices to be reduced, making the topologies suitable for high-voltage applications. Another three-level boost-based configuration with a new secondary side was presented in [4.21] where only two transistors are required to produce a positive, negative, or zero voltage across the secondary side of the transformer, which allows the full control of the high-voltage dc-bus.

For medium power applications [< 20-kW] where the ac voltage is at the residential level [120 – 240 Vac] as in the case of vehicle charging applications [4.4], the three-level topologies of [4.20], [4.21] present higher conduction losses since there is always two devices conducting at the same time. Then, the topology of Fig. 4.1 is proposed to increase the efficiency of those applications where the input current is high.

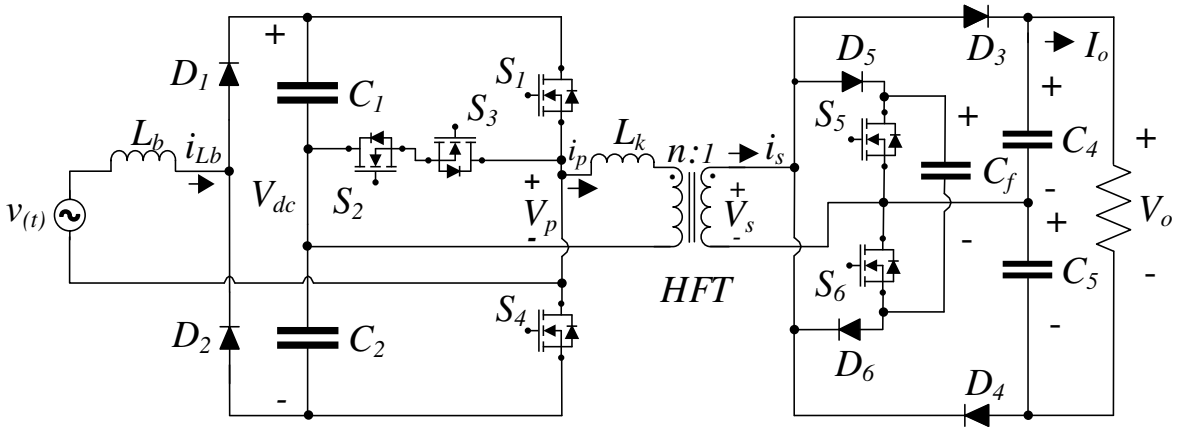


Figure 4.1: Circuit configuration of the proposed boost-based three-level isolated AC-DC PFC topology.

The proposed topology consists of a boost inductor L_b, two front-end diodes D_1 and D_2, which in conjunction with the T-Type bridge form by S_1-S_4 provide the PFC function. The T-Type bridge and the secondary-side topology configuration generate three voltage levels across the primary and secondary sides of the transformer, allowing for the full control of the dc-bus and output voltages as in the case of [4.20]-[4.21] utilizing a minimum number of semiconductor devices in comparison with traditional unidirectional SST topologies [4.3], [4.5].

This paper is organized as follows: The steady-state analysis of the converter for all operating modes is given in Section II; the soft-switching analysis for all devices is addressed in Section III; the calculations of the conduction losses for the entire power range is illustrated in Section IV. The experimental results for a 1-kW, 110-Vac prototype are evaluated in Section V. Lastly, the concluding remarks are provided in Section VI.

4.2 Steady-State Analysis

4.2.A Steady-State Waveforms

Fig. 4.2 shows the steady-state waveforms for one complete switching cycle T_{sw}, where the definition of the variables are listed in Table 4-I. The T-type bridge generates a three-level voltage across the primary side of the high-frequency transformer (HFT). At the primary side, a positive voltage is generated when S_1 is ON, a negative voltage when S_4 is ON, and a zero voltage when S_2 and S_3 are ON. As can be seen in Fig. 4.2, the dashed lines of S_2 and S_3 overlap during $[(1- D_p)T_{sw}/2]$ to generate a zero voltage across the primary terminals of the HFT.

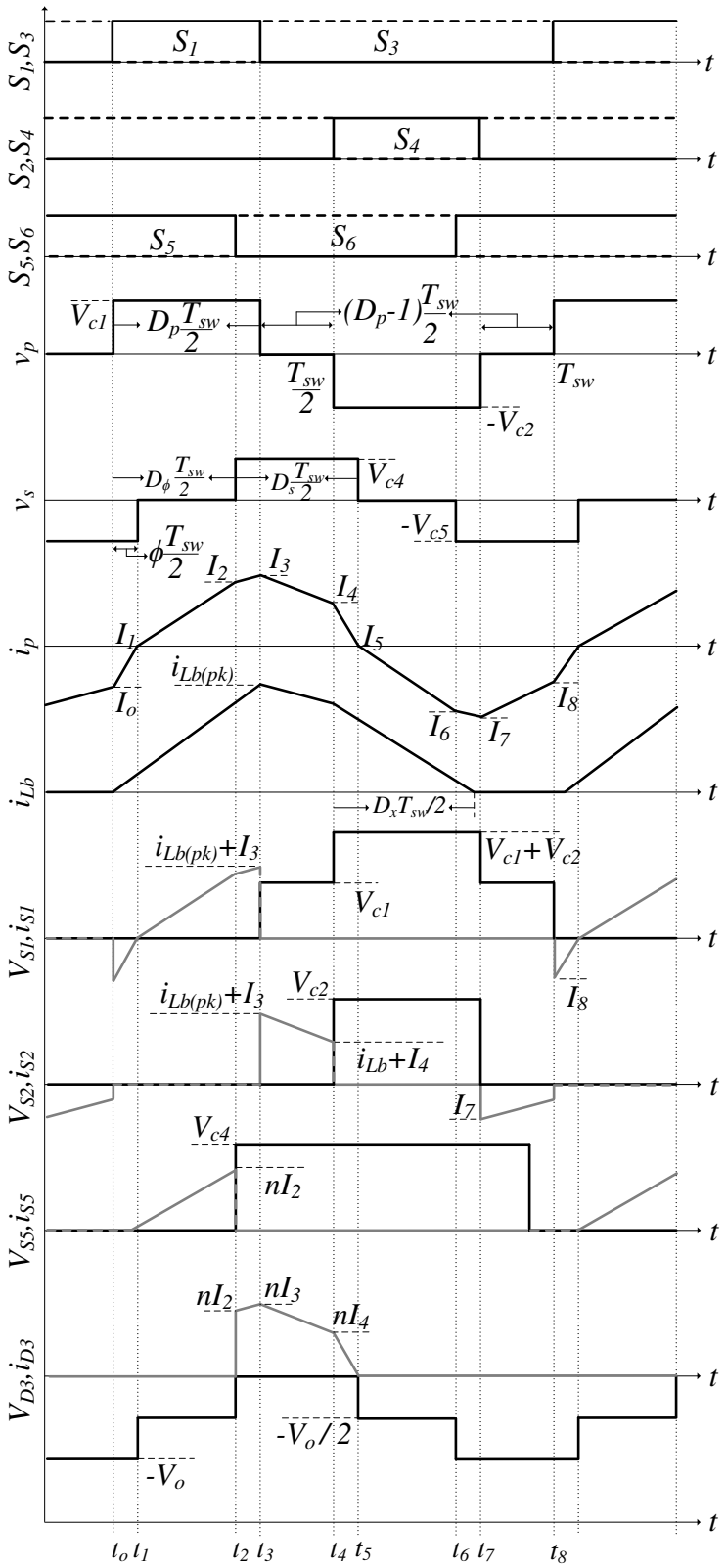


Figure 4.2: Steady-state waveforms of the proposed topology.

Table 4-I: Symbols and Unit Abbreviations

Symbols	Stand for (unit Abbreviation)
S_1, S_2, S_3, S_4, S_5, S_6	Gate signals for switches (V)
v_p, v_s	Primary and secondary voltages (V)
V_{S1}, V_{S2}, V_{S5},	Drain-source voltage of S_1, S_2, and S_5 (V)
V_{D3}	Anode-Cathode D_3 voltage (V)
i_p	Primary current (A)
i_{s1}, i_{s2}, i_{s5}	Current through S_1, S_2, and S_5
i_{D3}	Current through D_3
D_p, D_s, D_φ	Primary, secondary, phase-shift duty cycles
D_x	Boost inductor current duty cycle (from t_4 to $i_{Lb}=0$)
i_{Lb}	Boost inductor current (A)
V_{C1}, V_{C2}, V_{C3}, V_{C4}	Voltage of Capacitors C_1, C_2, C_3, C_4 (V)
n	Transformer turn ratio.

4.2.B Steady-State Operational Principles

Considering positive input ac voltage v_{in}(t), eight intervals occur over a complete switching cycle as displayed in Fig. 4.3. Similar analysis can be done when v_{in}(t) is negative.

1) [t_0-t_1] interval: switch S_1 is turned ON at zero voltage because initially the primary current i_p is negative and flows through the anti-parallel diode of S_1. The boost inductor current i_{Lb} conducts through D_1 and S_1 as shown in Fig. 4.3. The primary voltage v_p is equal to the voltage of C_1 whereas the secondary voltage v_s is equal to the negative voltage of C_5. The boost inductor is charging at a rate of [$v(t)/L_b$], and leakage inductance L_k is charging at rate of [$(V_{C1}+nV_{C5})/L_k$]. Both i_p and i_{Lb} have positive slope for the time duration of [$(D_\varphi + D_s - 1)T_{sw}/2$], and i_p can be calculated as:

$$i_p(t) = \frac{1}{L_k}\left(V_{C1} + \frac{nVo}{2}\right)(t - t_0) + I_0 \qquad (4.\ 1)$$

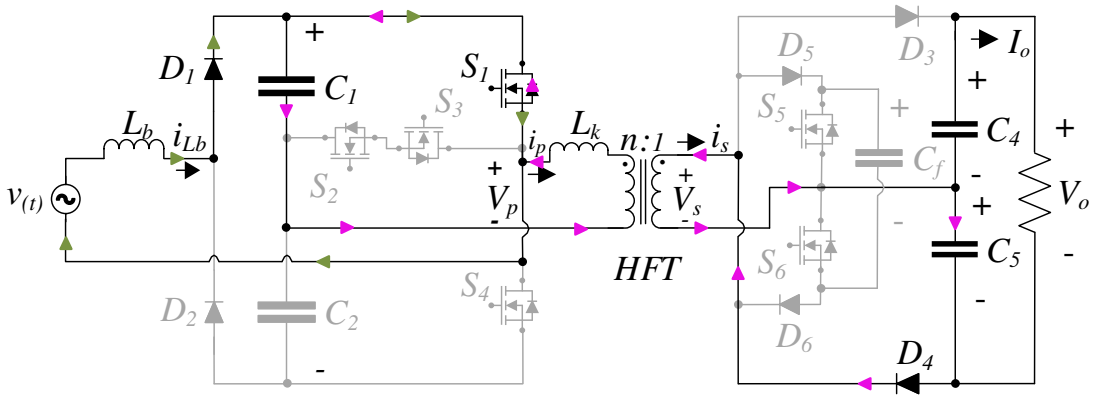


Figure 4.3: Proposed topology equivalent circuit for (t_0-t_1) *interval.*

At [$t = t_1$] (end of this interval), i_p is zero, which means [$I_1 = 0$] and I_0 equals to:

$$I_0 = -\frac{1}{2 f_{sw} L_k}\left(\frac{nVo}{2} + V_{C1}\right)\left(D_\varphi + D_s - 1\right) \tag{4. 2}$$

2) [t_1-t_2] interval: primary current i_p reverses its flow while S_5 is ON, then D_5 gets forward biased, and i_s circulates through D_5 and S_5 shorting the HFT secondary side. i_p conducts though S_1 at a rate of [V_{C1}/L_k]. The currents (i_{Lb}, i_p, i_s) conduction paths are illustrated in Fig. 4.4. Current i_{Lb} increases at the same rate as in previous stage. The primary current during this interval [(1 - D_s)T_{sw}/2] can be calculated as:

$$i_p(t) = \frac{V_{C1}}{L_k}(t - t_1) + I_1 \tag{4. 3}$$

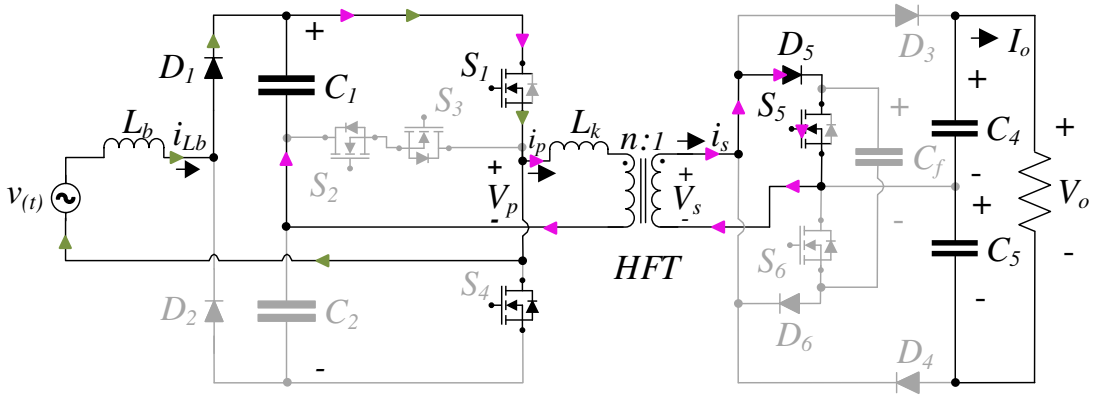


Figure 4.4: Proposed topology equivalent circuit for (t_1-t_2) *interval.*

I_1 is equal to zero (see Fig. 4.2), and I_2 is obtained from (4.3) as:

$$I_2 = \frac{V_{C1}}{2 f_{sw} L_k}\left(1 - D_s\right) \tag{4. 4}$$

3) [t_2-t_3] interval: switch S_5 turned OFF, primary i_s flows through D_3 and C_4, which makes the secondary voltage equals to the voltage across C_4. Current i_p still conducts through S_1 as in the previous stage, but at a rate of $[(V_{C1} - nV_o/2)/L_k]$. The equivalent circuit of this mode is depicted in Fig. 4.5. The interval time length is equal to $[(D_p - D_\varphi)T_{sw}/2]$ and primary current is

$$i_p(t) = \frac{1}{L_k}\left(V_{C1} - \frac{nV_o}{2}\right)(t - t_2) + I_2. \tag{4. 5}$$

At the end of this interval, i_p is at its peak value which can be obtain from (4.5) as:

$$I_3 = \frac{1}{2 f_{sw} L_k}\left(V_{C1} - \frac{nV_o}{2}\right)\left(D_p - D_\varphi\right) + I_2 \tag{4. 6}$$

4) [t_3-t_4] interval: switch S_1 turned OFF; primary current i_p freewheels through S_2 and S_3 whereas secondary current i_s still conducting though D_3. The boost inductor discharges though C_1 at a rate of $[(v(t)\text{-}V_{C1})/L_b]$ as shown in Fig. 4.6. With the primary terminals shorted, no energy is transferred to the output through HFT. Current i_p decreases at a rate of $[-nV_o/(2L_k)]$ as follows:

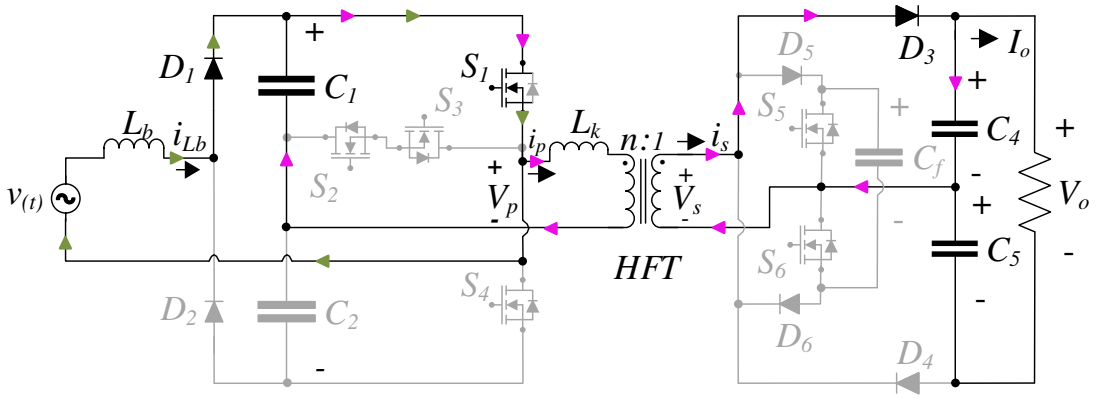


Figure 4.5: Proposed topology equivalent circuit for (t_2-t_3) *interval.*

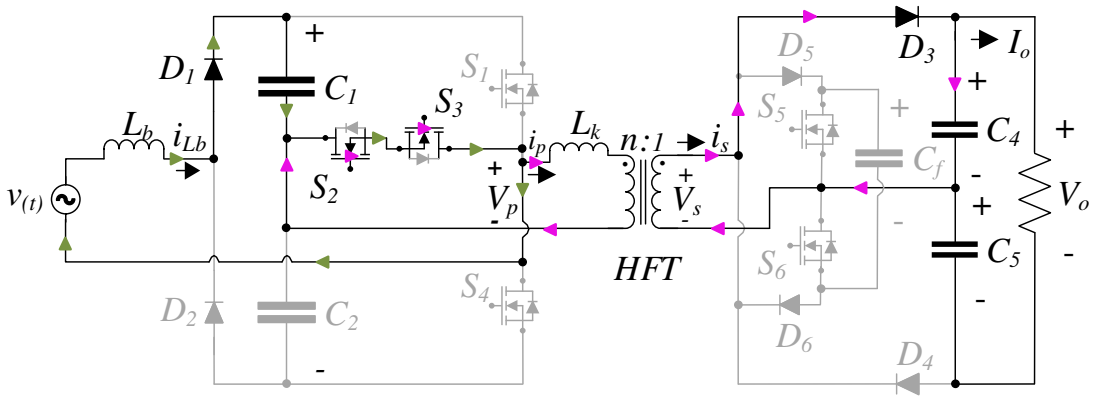


Figure 4.6: Proposed topology equivalent circuit for (t_3-t_4) *interval.*

$$i_p(t) = -\frac{nV_o}{2L_k}(t - t_3) + I_3 \tag{4. 7}$$

At [$t = t_4$], I_4 is calculated by:

$$I_4 = -\frac{1}{2f_{sw}L_k}\frac{nV_o}{2}\left(1 - D_p\right) + I_3 \tag{4. 8}$$

5) [t_4-t_5] interval: switch S_2 turned OFF; and primary current i_p continues to flow through C_2 and the anti-parallel diode of S_4. Secondary current i_s remains conducting through D_3 as in the previous stage. Boost current i_{Lb} flows through C_1, C_2, and anti-parallel diode of S_4 at a rate of [($v(t)$ – (V_{C1}+V_{C2}))/L_b] as shown in Fig. 4.7. Primary voltage v_p is equal to [$-V_{C2}$] and v_s is equal to [$nV_o/2$]. Current i_p is given by:

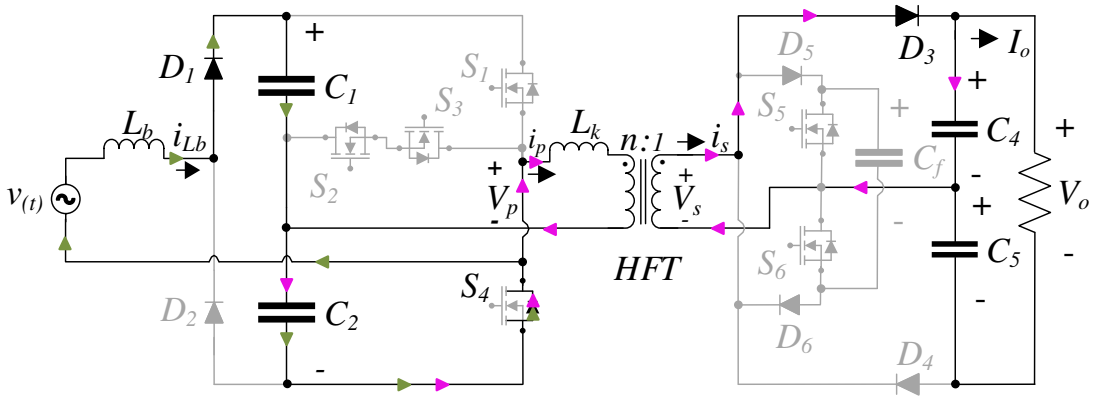


Figure 4.7: Proposed topology equivalent circuit for (t_4-t_5) *interval.*

$$i_p(t) = -\frac{1}{L_k}\left(V_{C2} + \frac{nV_o}{2}\right)(t - t_4) + I_4 \qquad (4.\ 9)$$

At the end of this state, [$i_p = I_5 = 0$].

6) [t_5-t_6] interval: switch S_4 turns ON. Primary current i_p changes from positive to negative direction and conducts through S_4 and C_2 at a rate of[$-V_{C2}/L_k$]. Secondary current i_s conducts through the secondary coil of the HFT and S_6. The boost current i_{Lb} decreases at the same rate as in *[t_4-t_5] interval*. The equivalent circuit of this mode is displayed in Fig. 4.8. The primary current i_p is given by:

$$i_p(t) = -\frac{V_{C2}}{L_k}(t - t_5) + I_5 \qquad (4.\ 10)$$

At the end of the interval $i_p = I_6 = -I_2$.

7) [t_6-t_7] interval: switch S_6 turned OFF, and secondary current i_s starts to conduct through C_5 and D_4. Primary current i_p continues to flow through S_4 and C_2 at a rate of [$(nV_o/2 - V_{C2})/L_k$]. In this mode, L_b discharges its energy completely and its current i_{Lb} reaches zero. The equivalent circuit is displayed in Fig. 4.9. Primary current i_p is expressed as:

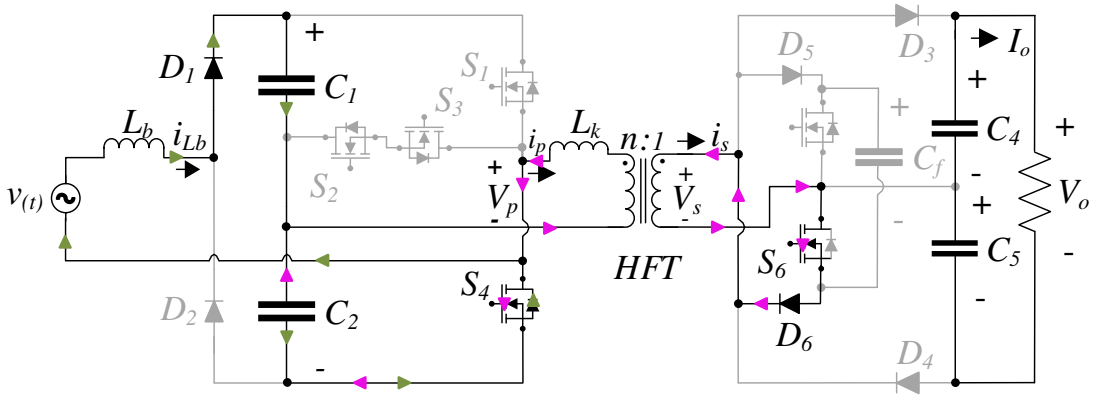


Figure 4.8: Proposed topology equivalent circuit for (t_5-t_6) *interval.*

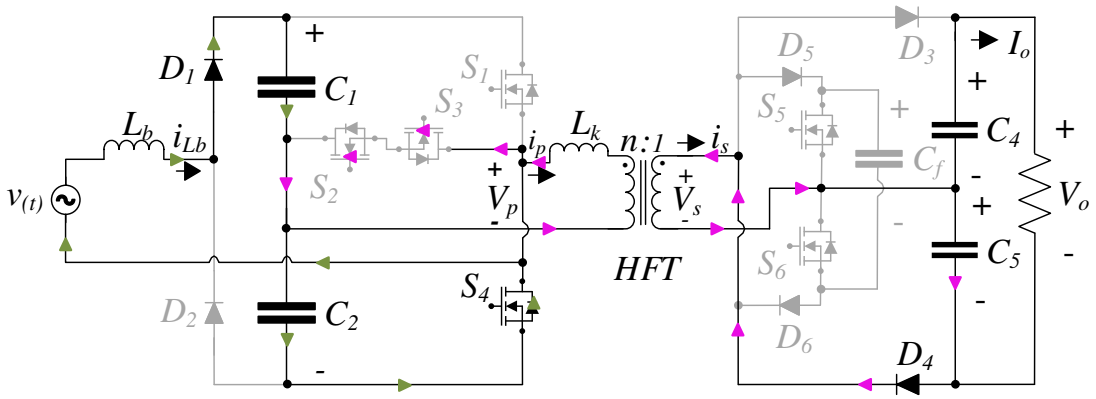


Figure 4.9: Proposed topology equivalent circuit for (t_6-t_7) *interval.*

$$i_p(t) = \frac{1}{L_k}\left(\frac{nV_o}{2} - V_{C2}\right)(t - t_6) + I_6 \qquad (4.\ 11)$$

At the end of this mode, i_p is at its negative peak which is equal to [$I_7 = -I_3$].

8) [t_7-t_8] interval: switch S_4 turned OFF and S_3 turns ON, shorting the primary winding of the HFT. Primary current i_p circulates through S_3 and S_2 at a rate of [$-nV_o/2$]. Secondary current i_s keeps conducting through C_5 and D_4. Secondary voltage v_s equals to [$-V_{C5}=V_o/2$] as shown in Fig. 4.10. Primary current i_p is calculated as:

$$i_p(t) = \frac{nV_o}{2L_k}(t - t_7) + I_7 \qquad (4.\ 12)$$

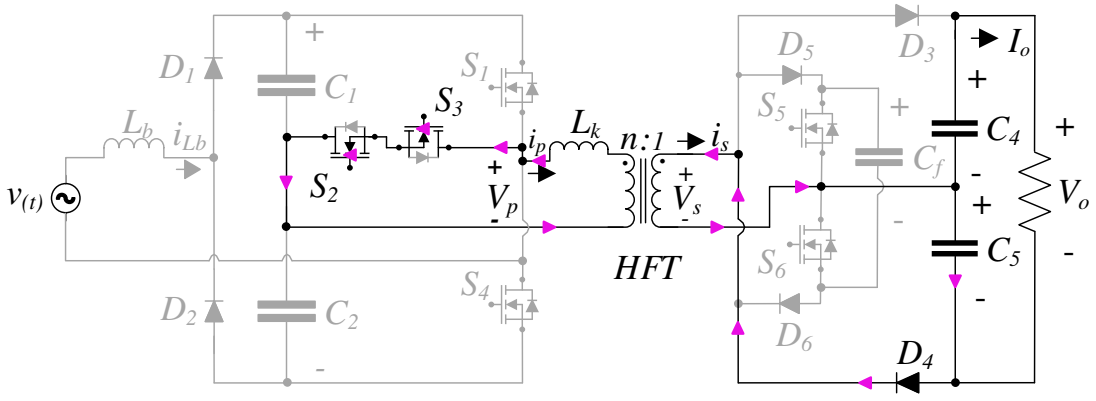


Figure 4.10: Proposed topology equivalent circuit for (t_7-t_8) *interval.*

At the end of this mode, [$i_p = I_1 = 0$].

4.2.C Output Power and DC-Bus Calculations

With reference to Fig. 4.2, when v_p is positive, i_p has three different positive slopes described by (4.1), (4.3), and (4.5). This is always true if [$D_\varphi \le D_p$]. The output power is calculated by integrating the product of the primary voltage v_p and primary current i_p over half of the switching period.

$$P_o = \frac{2}{T_{sw}} \sum \int_0^{1/T_{sw}} v_p(t) i_p(t) dt. \qquad (4.\ 13)$$

Computing (4.13), the resulting output power is determined as:

$$P_o = \frac{V_{dc} n V_o}{16 L_k f_{sw}} \left(D_p^2 + D_s^2 - D_s \left(2 + D_p \right) - 2 D_\varphi \left(D_p - D_s + 1 - D_\varphi \right) + 1 \right). \qquad (4.\ 14)$$

However, if [$D_\varphi > D_p$], and v_p is positive, i_p has only two different positive slopes described by (4.1) and (4.2) as presented in Fig. 4.11. The corresponding output power is calculated as:

$$P_o = \frac{V_{dc} n V_o}{16 L_k f_{sw}} \left(2 D_s + 2 D_\varphi + D_p D_s - D_s^2 - D_\varphi^2 - 2 D_s D_\varphi - 1 \right). \qquad (4.\ 15)$$

Due to the steady-state condition, the average voltage of the boost inductor over one switching period is zero; that is,

$$2 V_m \sin(\omega t)(D_x + 1) - V_{dc}(2 D_x - D_p + 1) = 0 \qquad (4.\ 16)$$

where D_x is the duty cycle of the second negative slope of the boost inductor current i_{Lb} as indicated in Fig. 4.2 and it can be calculated by assuming that the input power P_{in} is equal to the output power P_o.

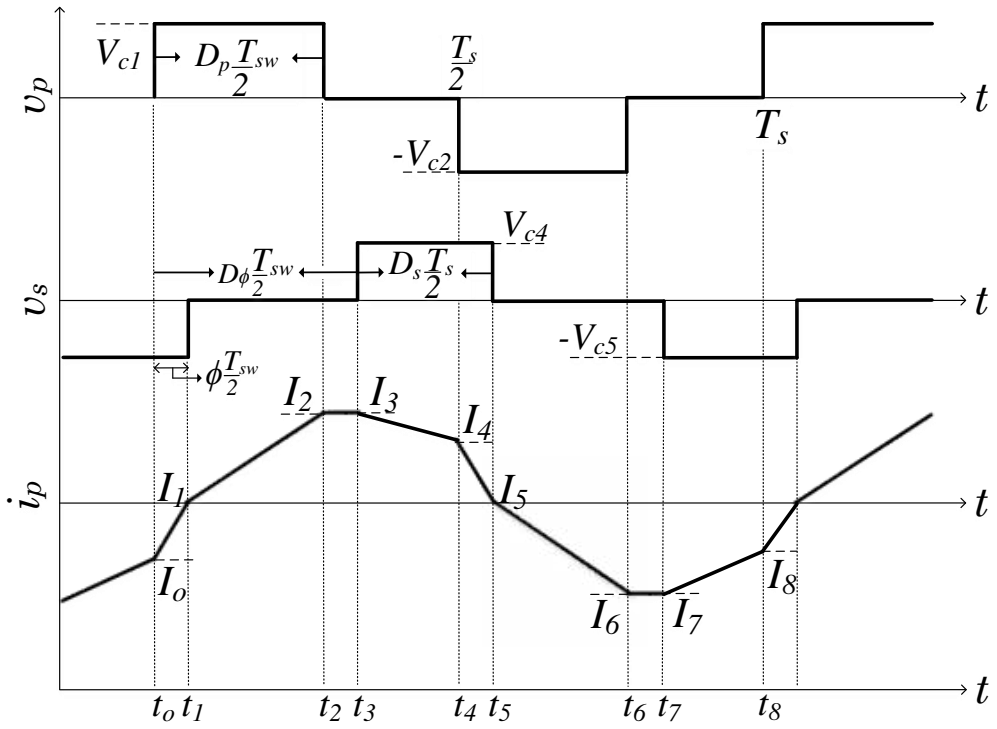


Figure 4.11: Steady-state waveforms representation for [$D_\varphi > D_p$].

$$\frac{1}{T_F}\int_0^{T_F} i_{Lb}(t)V_m \sin(\omega t)dt = I_o V_o, \tag{4. 17}$$

where T_F is the fundamental period and V_m is the magnitude of the input voltage. The boost inductor current i_{Lb} has three different slopes (i_{Lb1}, i_{Lb2}, i_{Lb3}) as shown in Fig. 4.2 and described in (4.18), (4.19), and (4.20).

$$i_{Lb1} = \frac{D_p T_{sw} V_m \sin(\omega t)}{2L_b}, \tag{4. 18}$$

$$i_{Lb2} = \frac{T_{sw}\left(2V_m \sin(\omega t) - V_{dc} + D_p V_{dc}\right)}{4L_b}, \tag{4. 19}$$

and

$$i_{Lb3} = i_{Lb2} + \frac{(V_{dc} - V_m \sin(\omega t)) D_x T_{sw}}{2L_b}. \quad (4.\ 20)$$

By inserting (4.18), (4.19), and (4.20) in (4.17), D_x is calculated as follows:

$$D_x = \frac{T_{sw} V_m \sin(\omega t)\left(V_{dc}\left(D_p^2 - 1\right) - 2V_m \sin(\omega t)\right) + I_o L_b V_o}{T_{sw} V_m \sin(\omega t)\left(2V_m \sin(\omega t) + V_{dc}\left(D_p - 1\right)\right)}. \quad (4.\ 21)$$

Now, V_{dc} can be determined as in (4.22) by placing (4.21) in (4.16). The dc-bus voltage is given by the following expression:

$$V_{dc} = \frac{\sqrt{T_{sw}^2 V_m \sin(\omega t)^4 \left(D_p^4 + 2D_p^2 + 1\right) - 64 D_p I_o L_b T_{sw} V_o V_m \sin(\omega t)^2 + 256 I_o L_b^2 V_o^2} + T_{sw} V_m \sin(\omega t)^2 \left(1 + D_p^2\right) - 16 I_o L_b V_o}{T_{sw} V_m \sin(\omega t)\left(D_p - 1\right)^2}. \quad (4.\ 22)$$

As shown in Fig. 4.2 there are three duty cycles (D_p, D_s, and D_ϕ). However, D_p and D_ϕ are the only controllable duty cycles. Under steady-state conditions, Fig. 4.12 presents P_o, V_{C1}, D_s, and V_o as a function of D_p where D_ϕ is a parameter. With reference to Fig. 4.12, D_ϕ has a minimal effect on P_o and V_o. As a result, D_p is used to control V_o.

Since V_{C1} depends on D_ϕ, V_{dc} is controlled by modulating D_ϕ. The secondary duty cycle D_s presented in Fig. 4.12 is highly nonlinear because it depends on the converter operating point (V_{dc} and V_o) and the converter duty cycles (D_ϕ and D_p). The expression that describe the secondary duty cycle D_s is given by:

$$D_s = \frac{V_{dc}\left(2 + D_p - 2D_\phi\right)}{nV_o + 2V_{dc}}. \quad (4.\ 23)$$

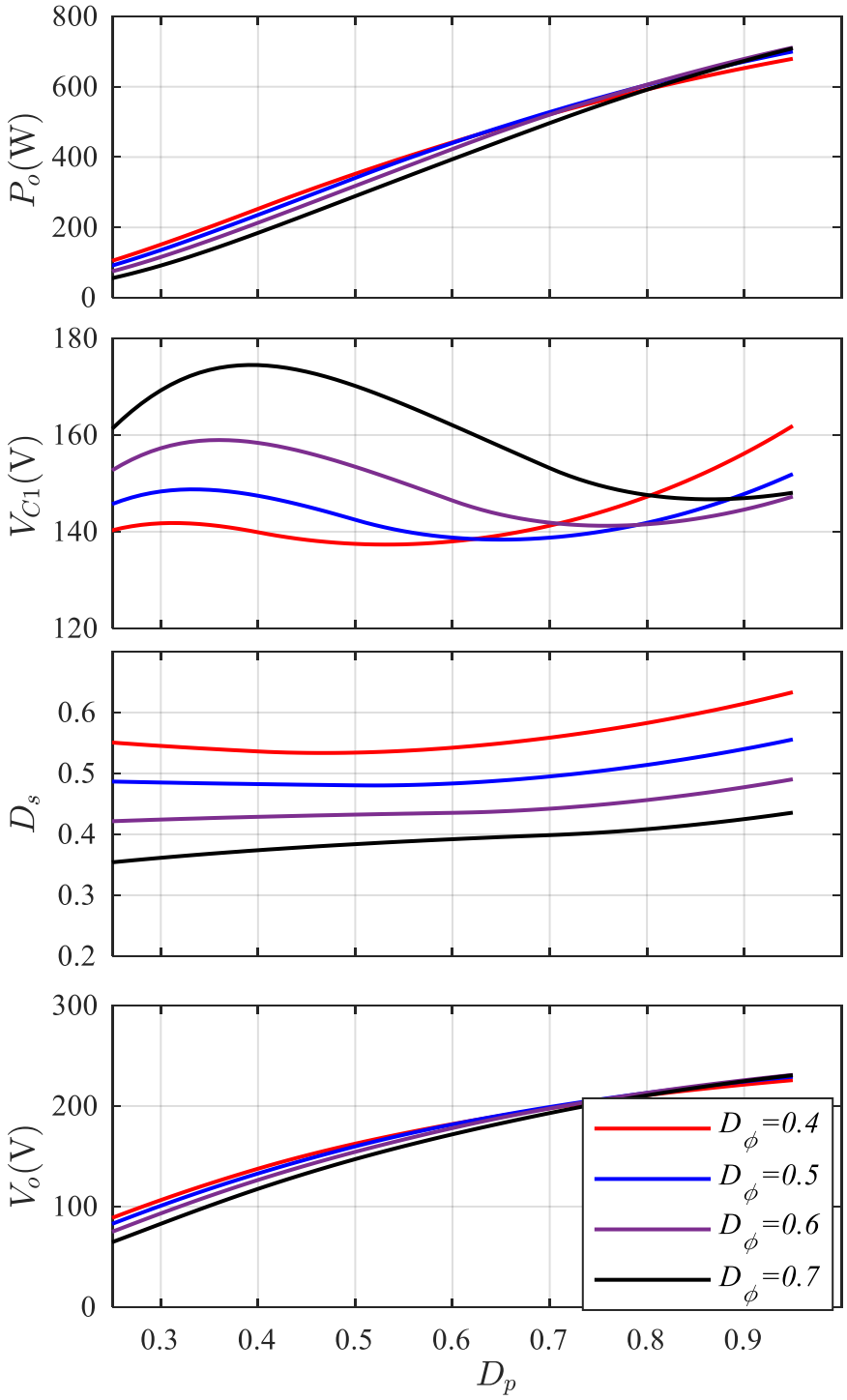


Figure 4.12: Theoretical waveforms representing the output power P_o, the input capacitor voltage V_{C1}, the secondary duty cycle D_s, and the output voltage V_o as a function of the primary duty cycles D_p and D_ϕ is a parameter.

4.3 Soft-Switching Analysis

Due to the symmetry of the transformer current waveforms, the soft-switching analysis in this section focuses only on S_1, S_2, and S_5. An identical evaluation can be performed for the complementary switches S_4, S_3, and S_6.

4.3.A Primary Switches

At the time when S_3 turns OFF (transition between [t_7-t_8] and [t_0-t_1] intervals), i_p flows through the anti-parallel diode of S_1. As a result, the voltage across S_1 drops from V_{C1} to zero, and then S_1 can be turned ON at zero voltage switching (ZVS). The switching action should occur while i_p is negative to guarantee S_1 turning ON at ZVS. Therefore, the soft-switching restriction on the primary duty cycle D_p can be obtained by solving (4.2), yielding the following:

$$D_p \geq \frac{2nV_o\left(1-D_\phi\right)\left(V_{C1}+nV_o\right)}{V_{C1}\left(4+3nV_o\right)}. \qquad (4.\ 24)$$

As the phase shift D_ϕ increases, the soft-switching region increases accordingly. Fig. 4.13 shows i_p when [$t = t_0$ (I_o)] as function of the primary duty cycle D_p where the phase shift D_ϕ is a parameter. As it can be seen from Fig. 4.13, for [$D_\phi > 0.5$], I_0 is negative for all values of D_p. However, for [$D_\phi = 0.5$ and $D_p < 0.7$], I_0 is positive and S_1 operates under hard switching. Ultimately, the converter operates under soft switching if D_p satisfies (4.24).

Prior to turning S_2 ON, primary current i_p is negative and conducting through S_4 as presented in Fig. 4.9. When S_4 turns OFF, primary current i_p continues to flow through S_3 and the anti-parallel diode of S_2, which represents the transition between [t_6-t_7], and [t_7-t_8] intervals. With a sufficient time delay applied to the S_2 gate signal V_{gS2}, i_{S2} discharges the stored energy in the parasitic capacitance C_{S2}, and S_2 turns ON at ZVS.

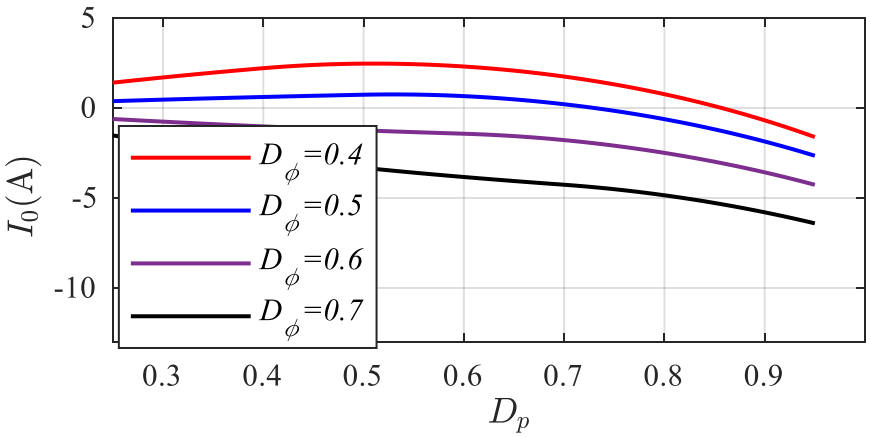


Figure 4.13: Theoretical waveforms representing I_0 (i_p when $t = t_o$) as a function of the primary duty cycle D_p while D_ϕ is a parameter.

4.3.B Secondary Switches

Secondary switches turn ON at zero current switching (ZCS) because switching action happens while secondary current i_s is conducting though one of the diodes (D_3, D_4). In addition, ZVS is achieved when a flying capacitor C_f is connected across the two switches (S_5, S_6) to vacillate the charging and discharging of the parasitic capacitance (C_{S5}, C_{S6}).

4.4 Converter Losses

4.4.A Conduction Losses

Each active device exhibits conduction losses based on the root mean square (RMS) current flowing through its internal resistance $R_{ds(ON)}$. The general equation which describes the RMS current through each switch is given by:

$$I_{RMS(Sn)} = \sqrt{\frac{1}{T_s}\int_{t_{Si}}^{t_{Sf}} \left(i_d^2\right) dt}, \qquad (4.\ 25)$$

where t_{Si} and t_{Sf} are the initial and final times of the conduction interval at which the drain current i_d flows through the switch.

Another source of conduction loss is the diode, which depends on the average current flowing through it and its forward voltage drop V_f. The average current of a diode is calculated as:

$$I_{AV(Dn)} = \frac{1}{T_s}\int_{t_{Di}}^{t_{Df}} I_F dt, \tag{4. 26}$$

where t_{Di} and t_{Df} are the initial and final times at which the forward current I_F conducts through the diode. S_2 and S_3 are ON when there is a current flowing through the central leg of the primary circuit to avoid conducting current via the anti-parallel diodes. The modulation scheme presented in Fig. 4.2 shows gate signals for S_2 and S_3.

With reference to Fig. 4.2 [$v_{in}(t) > 0$], Table 4-II provides the parameters for computing (4.25) and (4.26). Once the RMS and average currents of the switches and diodes are determined, the conduction power losses can be estimated by:

$$P_{CS(Sn)} = R_{ds(ON)} I^2_{RMS(Sn)}. \tag{4. 27}$$

$$P_{CD(Dn)} = V_f I_{AV(Dn)}. \tag{4. 28}$$

The datasheets of the switches and the diodes provide the actual values of $R_{ds(ON)}$ and V_f.

Figs. 4.14 and 4.15 show the theoretical waveforms of the RMS and average currents as a function of the primary duty cycle D_p for different values of phase shift D_φ.

Table 4-II: Switches and Diodes Conducting Forward Current

S_n	i_d	t_{Si}	t_{Sf}	D_n	I_F	t_{Di}	t_{Df}
S_1	i_p+i_{Lb}	t_1	t_3	D_1	i_{Lb}	t_o	$t_4 + (D_x\, T_{sw}/2)$
S_2	i_p+i_{Lb}	t_3	t_4	D_3	ni_p	t_2	t_5
S_4	i_p	t_4	t_7	D_{S1}	i_p	t_o	t_1
S_5	ni_p	t_1	t_2	D_5	ni_p	t_1	t_2

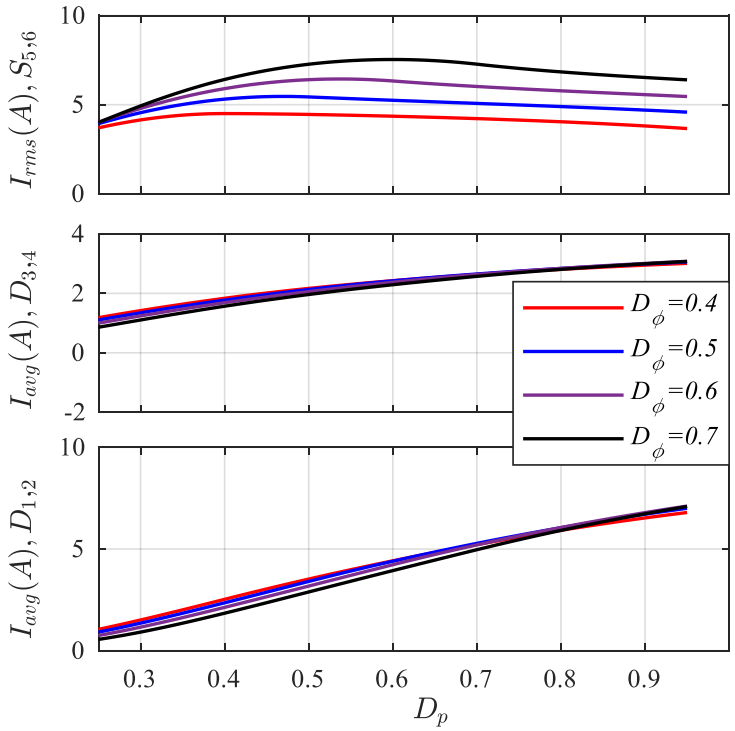


Figure 4.14: Theoretical waveforms representing *RMS* ($S_{5,6}$) and *average* ($D_{1,2,3,4}$) currents as a function of primary duty cycle D_p and D_ϕ is a parameter.

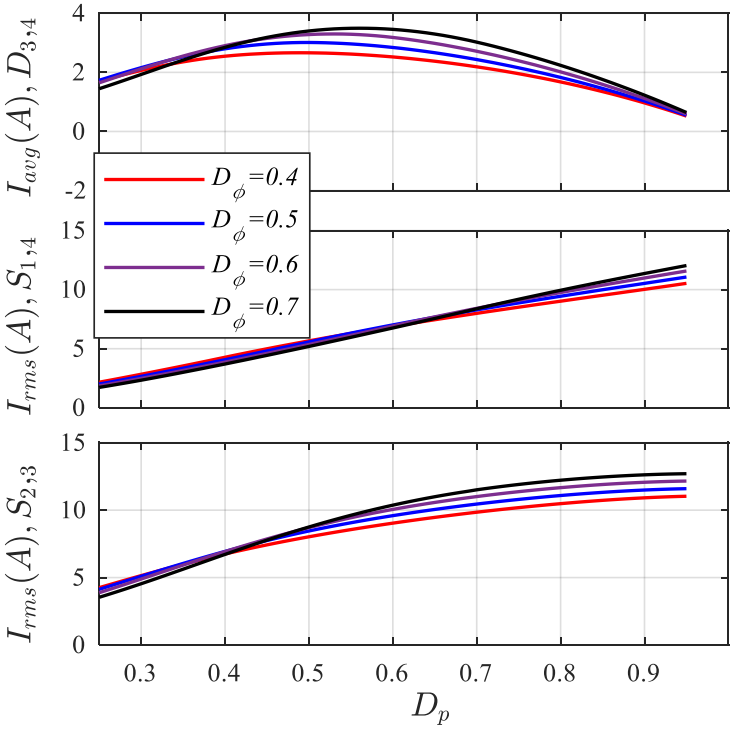


Figure 4.15: Theoretical waveforms representing *RMS* ($S_{1,4,2,3}$) and *average* ($D_{3,4}$) currents as a function of primary duty cycle D_p and D_ϕ is a parameter.

4.4.B Switching Losses

Switching losses depend on whether the converter operates under soft- or hard-switching. In case of soft-switching, prior to turning switches ON, the drain-source voltage Vds = 0 and only the switch turn-OFF losses are considered. The estimation of the turn-OFF losses can be determined based on the size of the output capacitance of the switches, the utilized semiconductor device, and the magnitude of the current at which the transistor turns OFF [4.22],[4.23]. Previous research details the analytical analysis of how to calculate switching-losses [4.15]. It is worth noting that the primary switches (S_1-S_4) turn OFF while the primary and boost inductor currents are conducting through them. Section II. B provides the primary current at the instant when the transistors turn OFF. The magnitude of the boost inductor depends on the converter operating point:

$$i_{Lb} = \frac{P_{\max}}{V_{pk} D_p}, \tag{4. 29}$$

where V_{pk} is the peak of the input voltage. At turn OFF, the magnitude of the current flowing through S_1, S_2, and S_5 are [I_3+i_{Lb}], [I_4+i_{Lb}], and [nI_2] respectively.

Fig. 4.16 shows the overall efficiency of the proposed converter as a function of the phase shift D_φ where the primary duty cycle D_p is a parameter. For low-power conditions where low D_p are required, there is a region where the converter is operating under hard switching. While for an example [$D_p > 0.5$], switches operate at soft switching for all the values of D_φ. However, there is trade-offs between obtaining high efficiency and high-power factor at the same time. That is because, low phase shift D_φ results in high efficiency, but at the same time results in low power factors. Further analysis regarding the optimized selection of D_p and D_φ is provided in the experimental section.

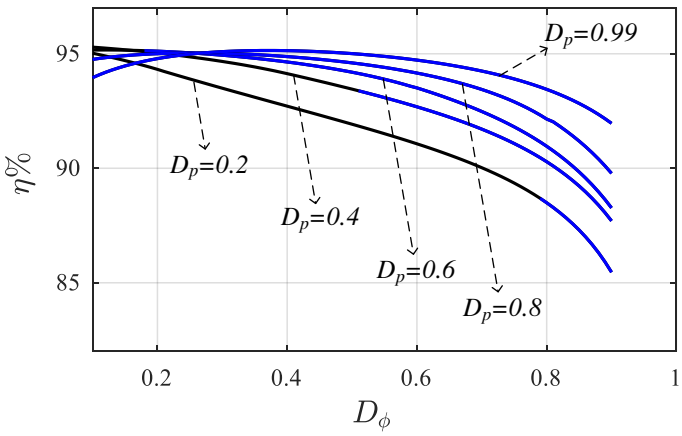


Figure 4.16: Efficiency as a function of the phase shift D_ϕ where primary duty cycle D_p is a parameter (blue line: soft-switching, black line: hard-switching).

4.5 Experimental Results

A 1-kW, 110-V_{RMS}, 20-kHz scale-down prototype was built and tested to demonstrate its feasibility and verify the proof-of-concept. In Fig. 4.17, S_1 turns ON at ZVS since [i_p < 0] and conducts through the anti-parallel diode D_{S1}. Prior to turning S_1 ON, the drain-source voltage V_{S1} equals to V_{C1}, that because S_2 and S_3 are circulating i_p and S_1 sustains only half of the dc-bus voltage ($0.5V_{dc}$). However, once S_1 turned OFF and i_p conducts through S_4 which makes S_1 withstands the full dc-bus voltage V_{dc} as shown in Fig. 4.17.

S_2 conducts positive current (primary current i_p) and negative currents [i_p+i_{Lb}]. It turns ON at ZVS while i_p is negative and conducting through anti-parallel diode (D_{S2}) as shown in Fig. 4.18. The drain-source voltage V_{S2} is half of the dc-bus voltage ($0.5V_{dc}$) as noted in Fig. 4.18.

Fig. 4.19 shows the ZCS and ZVS at turning S_5 ON. The switch turns ON while i_s is negative and conducting through the diode D_4. The active switches in the secondary side of the proposed topology sustain half of the output voltage $0.5V_o$ as shown in Fig. 4.19.

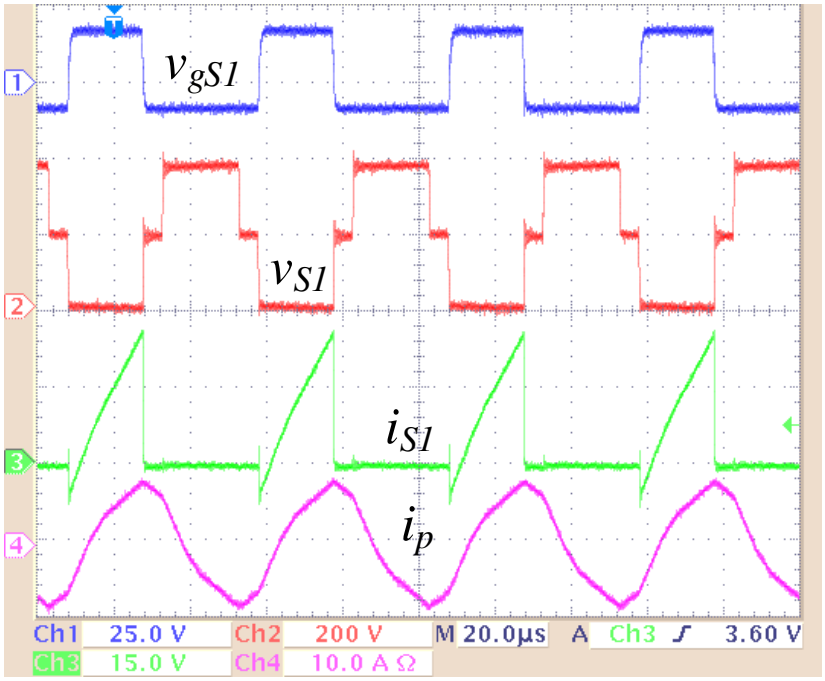


Figure 4.17: Experimental waveforms showing ZVS at turn ON switch S_1, gate-source signal (blue), drain-source voltage (red), current through the switch (green), and primary current (pink).

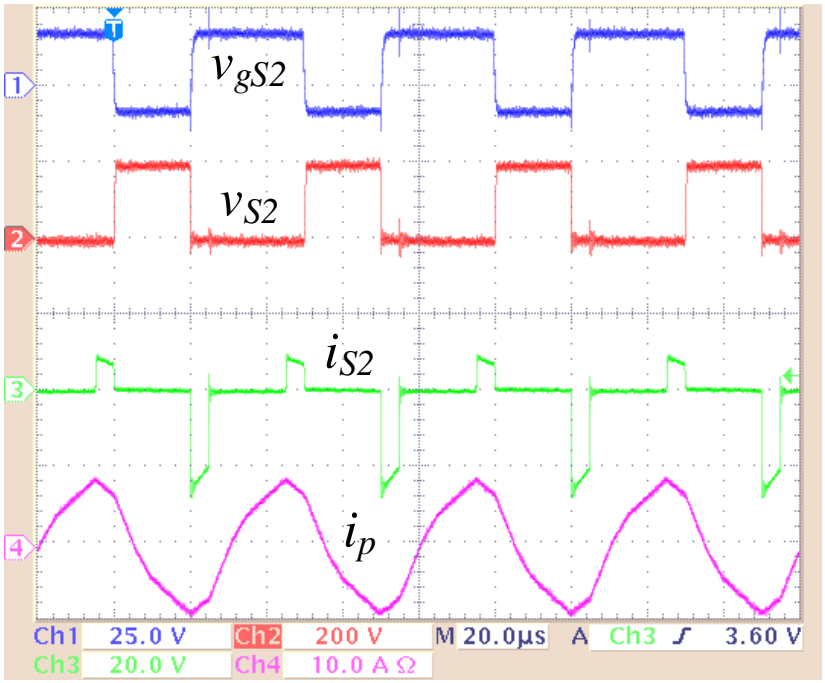


Figure 4.18: Experimental waveforms showing ZVS at turn ON for switch S_2, gate-source signal (blue), drain-source voltage (red), current through the switch (green), and primary current (pink).

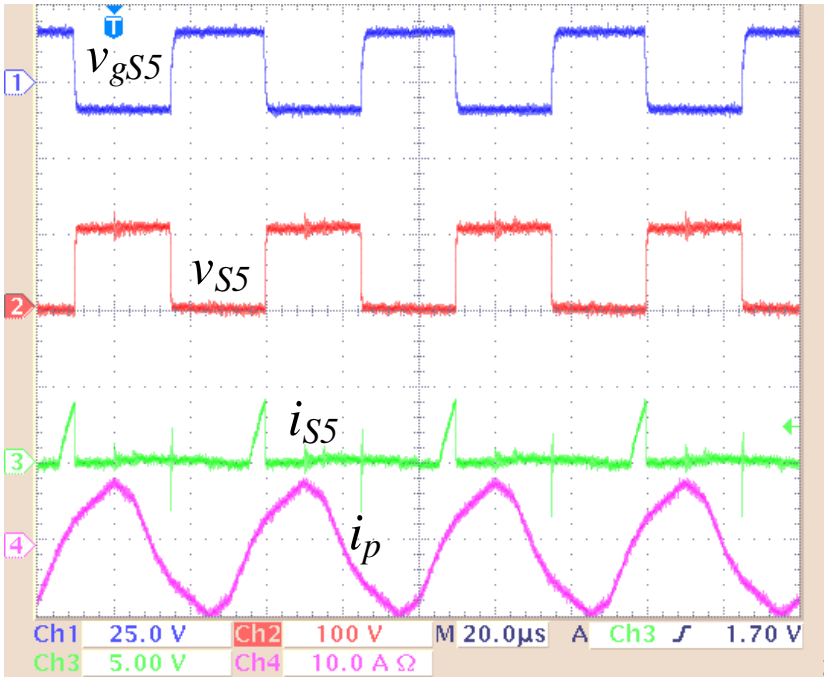
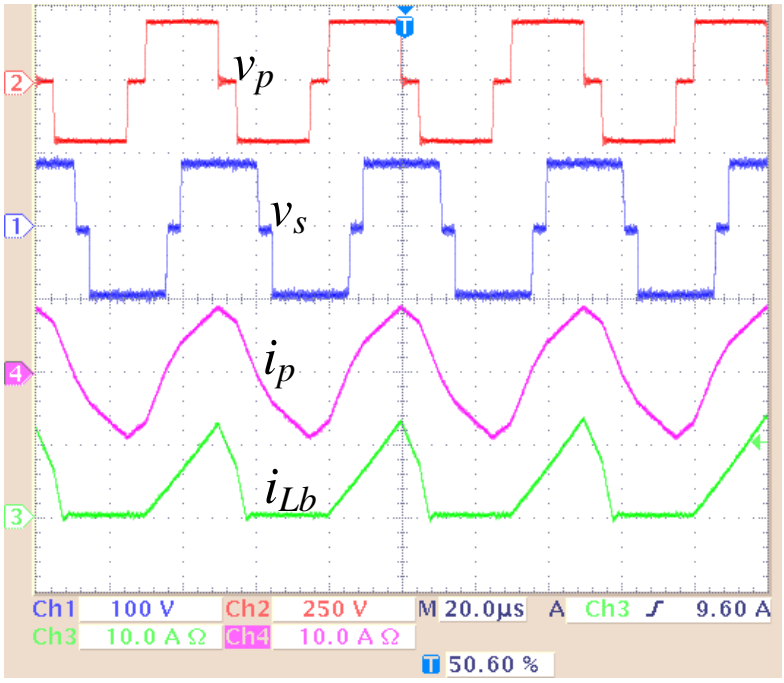


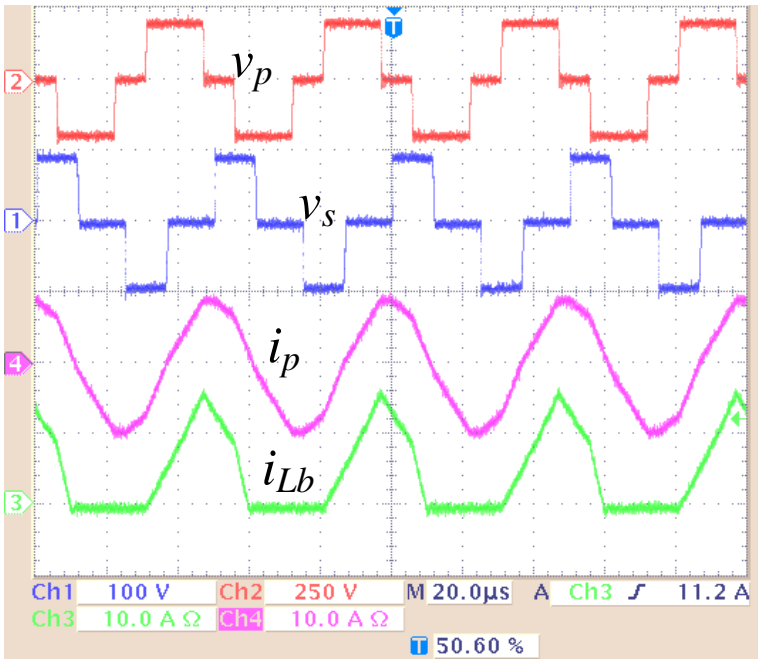
Figure 4.19: Experimental waveforms showing ZVS at turn ON for switch S_5, gate-source signal (blue), drain-source voltage (red), current through the switch (green), and primary current (pink).

The proposed isolated three level ac-dc power converter has two different mode operations. First, the primary current i_p has three different slopes which can be obtain for [$D_\phi < D_p$], as shown in Fig. 4.20(a). Second, the primary current has two different slopes as indicated in Fig. 4.20 (b), which is always true for [$D_\phi \geq D$].

Fig. 4.21 shows the efficiency of the primary side circuit, magnetic components, secondary side circuit, and overall efficiency as a function of the output power. The efficiency was measured for different phase shifts [D_ϕ = 0.4, 0.6, 0.8] in order to obtain the optimal selection of D_ϕ that result in a high efficiency operation. As it can be seen, the primary circuit tends to have high efficiency for high phase shift (i.e., [$D_\phi = 0.8$]). However, the magnetic components and secondary circuit show high efficiency for low phase shift (i.e., [$D_\phi = 0.4$]). Therefore, operating the converter around 50% phase shift results in a high efficiency.



(a)



(b)

Figure 4.20: Experimental results showing primary voltage v_p, secondary voltage v_s, primary current i_p, and boost inductor current i_{Lb} for **(a)** [$D_\phi \leq D_p$] and **(b)** [$D_\phi > D_p$].

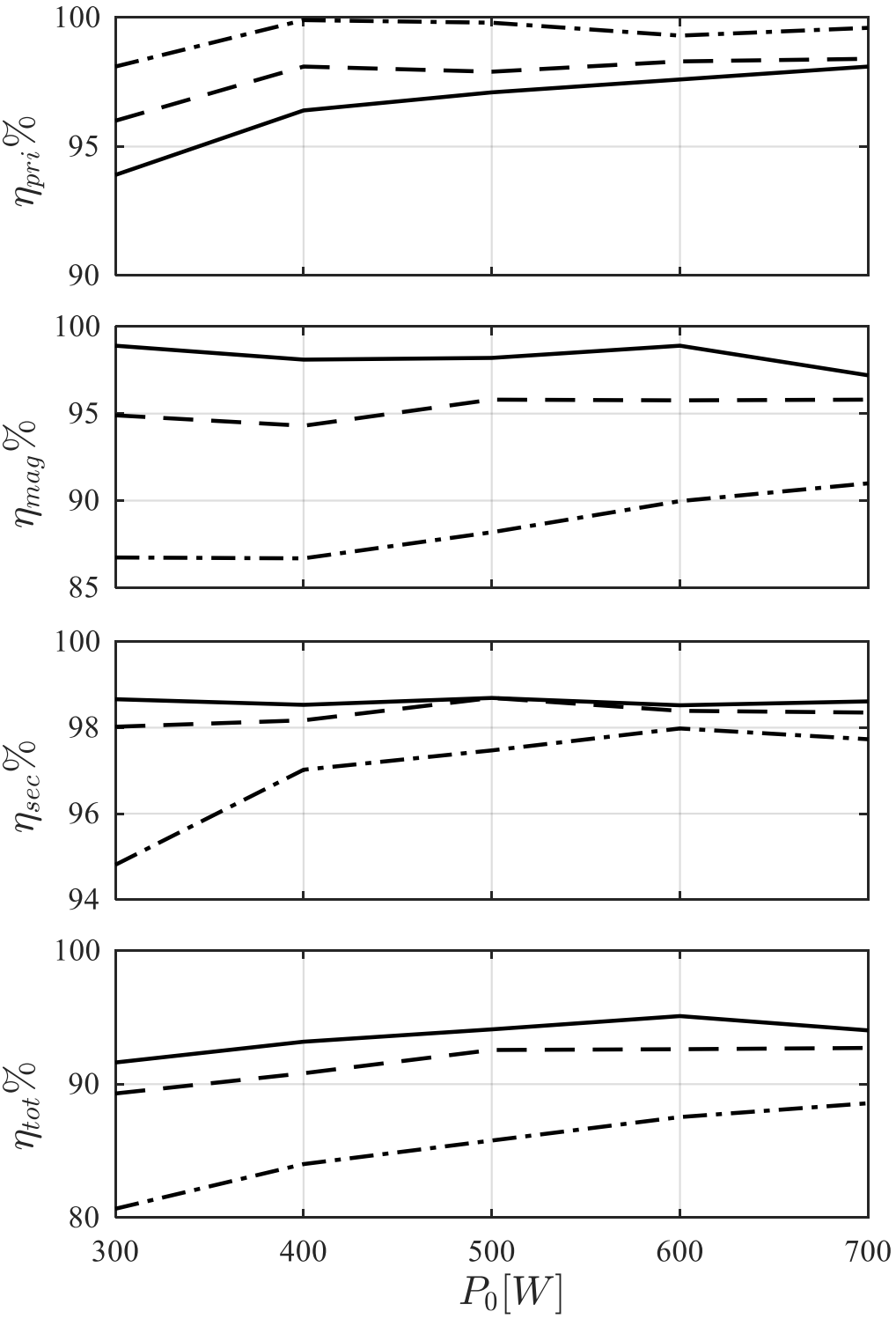


Figure 4.21: Experimental efficiency measured between input voltage and transformer primary terminals (η_{pri} %), transformer primary and secondary terminals (η_{mag} %), transformer secondary and output terminals (η_{sec} %), input and output terminal (η_{tot} %). Solid-line [$D_\phi = 0.4$], dashed-line [$D_\phi = 0.6$], and solid-dot-line [$D_\phi = 0.8$].

The main objective of the proposed topology is obtaining a high power factor at the input. One way to estimate the PF based on the experimental waveforms is calculating the true average input power and divided it by the apparent power.

$$PF = \frac{\overline{P_{in}}}{S_{in}}, \tag{4. 30}$$

where S_{in} is the apparent power calculated based on the input RMS current and voltage shown in Fig. 4.22 [$S_{in} = V_{in(RMS)}I_{in(RMS)}$], P_{in} is the true average power calculated from the average current and voltage presented in Fig. 4.23 [$P_{in} = V_{in(AV)}I_{in(AV)}$].

Fig. 4.24 presents the power factor PF as function of the primary duty cycle D_p for different phase shifts D_ϕ. With reference to Fig. 4.16, the optimal selection for the duty cycles are [$D_p >$ 0.75] and [$D_\phi <$ 0.6]. With those restrictions on duty cycles, the proposed converter operates at very high power factor > 0.99, and high efficiency > 95%.

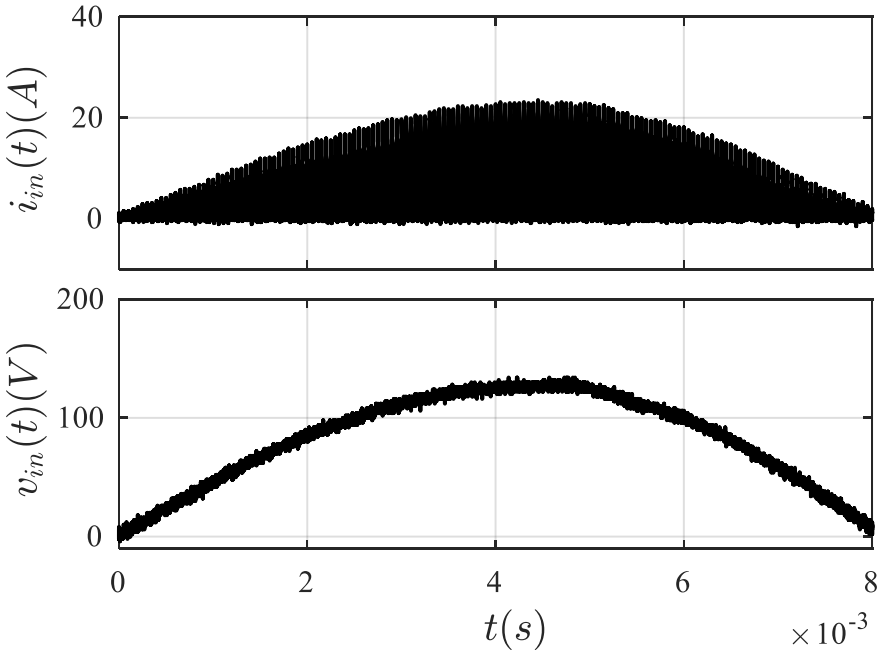


Figure 4.22: Input current $i_{in}(t)$ and voltage $v_{in}(t)$ for half of the fundamental frequency.

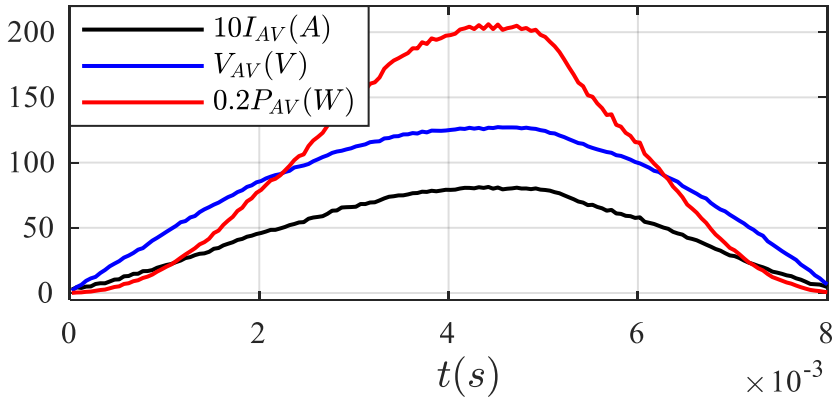


Figure 4.23: Experimental results of the average input current $I_{(AV)}$, voltage $V_{(AV)}$, and power $P_{(AV)}$ over half of the fundamental frequency.

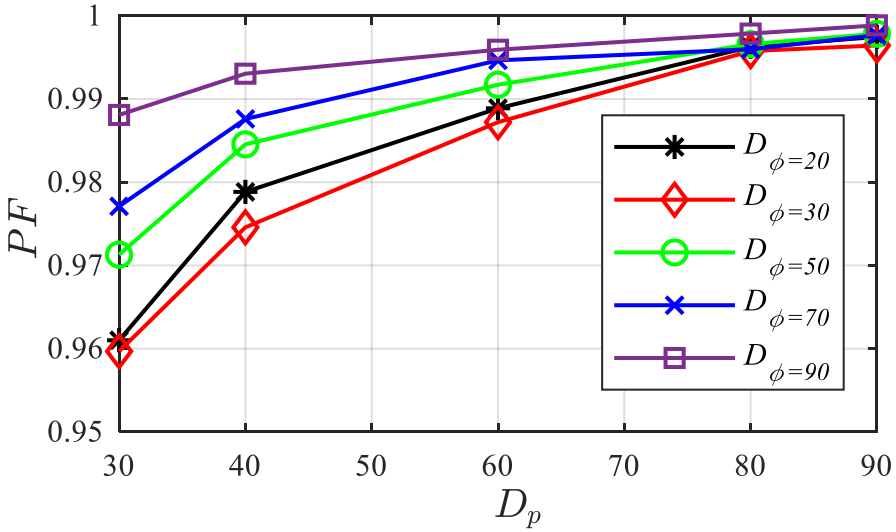


Figure 4.24: Experimental measurements presenting power factor (PF) as function of primary duty cycle (D_p) for different phase shift (D_ϕ).

4.6 Conclusion

The main goal of the proposed new topology was to draw ac-power at a high-power factor while controlling the dc-bus and output voltages. The study showed very high PF at high primary and phase shift duty cycles. For wide range of power, the proposed topology operated under soft switching. In particular, the secondary side switches operated under ZVS and ZCS without adding more restrictions on the primary duty cycle. Optimal selection of the primary and phase shift duty cycles resulted in high PF and high efficiency. At the secondary side, SiC MOSFETs (S_5, S_6) can

be replaced by IGBTs to eliminate the extra two diodes (D_5, D_6) which may lead to a potential future research.

4.7 References

[4.1] X. Lu, J. M. Guerrero, K. Sun, J. C. Vasquez, R. Teodorescu and L. Huang, "Hierarchical Control of Parallel AC-DC Converter Interfaces for Hybrid Microgrids," in *IEEE Trans. on Smart Grid*, vol. 5, no. 2, pp. 683-692, March 2014.

[4.2] F. Blaabjerg, Zhe Chen and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," in *IEEE Trans. on Power Electronics*, vol. 19, no. 5, pp. 1184-1194, Sept. 2004.

[4.3] D. Rothmund, G. Ortiz, and J. W. Kolar, "SiC-based unidirectional solid-state transformer concepts for directly interfacing 400V DC to medium-voltage AC distribution systems," in *Proc. IEEE 36th Int. Telecommun. Energy Conf. (INTELEC)*, Vancouver, BC, Canada, Oct. 2014, pp. 1–9.

[4.4] M. Yilmaz and P. T. Krein, "Review of Battery Charger Topologies, Charging Power Levels, and Infrastructure for Plug-In Electric and Hybrid Vehicles," in *IEEE Trans. on Power Electronics*, vol. 28, no. 5, pp. 2151-2169, May 2013.

[4.5] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 186–198, Sep. 2013.

[4.6] C. Li and D. Xu, "Family of Enhanced ZCS Single-Stage Single-Phase Iso lated AC–DC Converter for High-Power High-Voltage DC Supply," *IEEE Trans. on Industrial Electronics,* vol. 64, no. 5, pp. 3629-3639, May 2017.

[4.7] R.W.A.A. De Doncker, D.M. Divan, M.H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Trans. on Industry Applications,* vol. 27, no. 1, pp. 63-73, Jan./Feb. 1991.

[4.8] B. Zhao, S. Qiang, W. Liu, Y. Sun, "Overview of Dual-Active-Bridge isolated bidirectional DC-DC converter for high-frequency-link power-conversion system," *IEEE Trans. on Power Electronics,* vol. 29, no. 8, pp. 4091-4106, August 2014.

[4.9] B. Thomas, M. Akos, D. Dujic, "Power Electronic Traction Transformer: Efficiency Improvements Under Light-Load Conditions," *IEEE Trans. on Power Electronics,* Vol. 29, no. 8, Aug 2014.

[4.10] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality ac–dc converters," IEEE Trans. Ind. Electron., vol. 51, no. 3, pp. 641–660, Jun. 2004.

[4.11] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, “A review of single-phase improved power quality AC–DC converters,” IEEE Trans. Ind. Electron., vol. 50, no. 5, pp. 962–981, Oct. 2003.

[4.12] M. Pahlevaninezhad, P. Das, J. Drobnik, P. K. Jain, and A. Bakhshai, “A novel ZVZCS full-bridge DC/DC converter used for electric vehicles,” *IEEE Trans. Power Electron.,* vol. 27, no. 6, pp. 2752–2769, Jun. 2012.

[4.13] R. W. A. A. De Doncker, D. M. Divan and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," in *IEEE Trans. on Industry Applications*, vol. 27, no. 1, pp. 63-73, Jan.-Feb. 1991.

[4.14] F. Krismer, J. W. Kolar, “Efficiency-Optimized High-Current Dual Active Bridge Converter for Automotive Applications*”, IEEE Trans. on Industrial Electronics,* Vol. 59, No. 7, July 2012.

[4.15] G. G. Oggier, G. O. Garcia, A. Oliva, ‘Switching Control Strategy to Minimize Dual Active Bridge Converter Losses,” *IEEE Trans. on Power Electronics,* vol. 24, no. 7, pp. 1826-1838, July 2009.

[4.16] S. Falcones, X. Mao, R. Ayyanar, “Topology Comparison for Solid State Transformer Implementation,” *IEEE Power and Energy Society General Meeting,* pp. 1-8, 2010.

[4.17] S. Hwang, X. Liu, J. Kim, H. Li, “Distributed digital control of modular-based solid-state transformer using DSP+FPGA,” *IEEE Trans. on Industrial Electronics,* vol. 60, no.2, Feb. 2013.

[4.18] Y. Choi, “A highly power-efficient LED back-light power supply for LCD display,” *J. Display Technol.,* vol. 9, no. 5, pp. 383–384, May 2013.

[4.19] P. M. Barbosa, F. Canales, J. M. Burdío, and F. C. Lee, “A three-level converter and its applicationto power factor correction,” *IEEE Trans. Power Electron.,* vol. 20, no. 6, pp. 1319–1327, Nov. 2005.

[4.20] L. A. Garcia Rodriguez, V. Jones, A. R. Oliva, A. Escobar-Mejía and J. C. Balda, "A New SST Topology Comprising Boost Three-Level AC/DC Converters for Applications in Electric Power Distribution Systems," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 2, pp. 735-746, June 2017.

[4.21] O. Aldosari, L. A. G. Rodriguez, G. G. Oggier and J. C. Balda, "A Three-Level Isolated AC-DC PFC Power Converter Topology with Reduced Number of Switches," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*.

[4.22] C. G. Steyn, “Analysis and optimization of regenerative linear snubbers,” in *IEEE Trans. on Power Electronics,* vol. 4, no. 3, pp. 362-370, July 1989.

[4.23] M. Schweizer and J. W. Kolar, “Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications,” in *IEEE Trans. on Power Electronics,* vol. 28, no. 2, pp. 899-907, Feb. 2013.

APPENDIX 4.A

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April 14, 2020

To whom it may concern,

This letter is to verify that Mr. Obaid Martha Aldosari, ID 010768784, is the first author and did at least 51% of the work for the paper titled "A boost-based T-type PFC unidirectional solid-state transformer for medium-level power applications".

Kind Regards,

Juan Balda

Dr. Juan Carlos Balda

University Professor, Department Head and Major Advisor to Mr. Obaid Martha Aldosari

DESIGN TRADE-OFFS FOR MEDIUM- AND HIGH-FREQUENCY TRANSFORMERS FOR ISOLATED POWER CONVERTERS IN DISTRIBUTION SYSTEM APPLICATIONS

O. Aldosari, L. A. Garcia Rodriguez, J. C. Balda and S. K. Mazumder, "Design Trade-Offs for Medium- and High-Frequency Transformers for Isolated Power Converters in Distribution System Applications," *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Charlotte, NC, 2018, pp. 1-7.

Abstract

Medium- and high-frequency transformers (MFTs/HFTs) are a fundamental component in many isolated power-converter topologies proposed for electric distribution applications (e.g., solid-state power substations). Previous work presented detailed transformer design methodologies and addressed core loss limitations for different core materials and operating frequencies. However, MFT/HFT designs become significantly challenging for high power levels that are typical of distribution systems (e.g., greater than 100-kVA). Furthermore, few references include specific requirements in the design methodology like desired leakage and/or magnetizing inductances (which are normally specified for high-power applications).

A design methodology for MFTs/HFTs is presented in this paper that accounts for tradeoffs like having a given leakage inductance for maximum power transfer (e.g., in the case of dual-active bridges (DABs)) or a given magnetizing inductance (to either attain a certain power transfer or to limit the power semiconductor currents). The design methodology is verified via finite-element analysis (FEA) using ANSYSTM and an experimental prototype.

5.1 Introduction

Nowadays, several applications of power electronics in electric power distribution systems are envisioned due to advances in high-voltage power semiconductor technologies, in particular, those enabled by wide bandgap power devices [5.1]. High-voltage silicon-carbide (SiC) MOSFETs are commercialized up to 1.7-kV with 3.3-kV and 6.5-kV devices to be commercialized soon. These devices have lower switching losses than silicon IGBTs so they can be operated at much higher switching frequencies leading to reductions of passive component sizes. These applications of power electronics often require stepping down or up a particular voltage level using a transformer. Examples are (a) solid-state transformers based on DABs requiring a certain value of the transformer leakage inductance for maximum power transfer [5.2], and (b) flyback converter topologies , or (c) input-output continuous converter topologies [5.3] where the transformer that store energy requires a given magnetizing inductance and ideally no leakage inductance to avoid adverse effects [5.4].

New cores based on amorphous and nanocrystalline materials enable size reductions of inductors and transformers in the medium-frequency range due to their higher flux densities when compared to ferrite cores. However, high-power applications require stacking several cores of these materials (due to the size limitations of commercial cores) or, if possible, use large expensive custom cores to satisfy area-product requirements. As a result, the design becomes more complex due to several tradeoffs among the transformer specifications. With the goal of simplifying the design, a methodology for high-power MFTs/HFTs considering system specifications (e.g., desired leakage and/or magnetizing inductances) and constraints (e.g., temperature rise, operating frequency, or volume) is presented and verified via ANSYS^{TM} finite-element analysis (FEA) and experimental results.

The paper is organized as follows: Section II reviews different core materials currently available for high-power applications and illustrate a simple technique to estimate temperature rise as a function of rated power, Section III describes the proposed design methodology, Section IV considers a case study and evaluates FEA results, Section V presents a scaled-down prototype as a verification of the proposed tradeoff strategies and Section VI provides the research conclusions.

5.2 Materials Suitable for High-Power MFTs/HFTs

Selecting the proper core material is a critical decision leading to a successful MFTs/HFTs design. In the last decades, intensive research has been done on a variety of different magnetic materials (e.g., nanocrystalline, amorphous and ferrite) in terms of cost, power loss, and size [5.5]. However, it is very challenging and time consuming to choose the right material to meet specific application's requirements, especially at high-power levels. For this reason, the following subsections will provide an overview and comparison between these magnetics materials (A), and describe a simple technique for selecting the core material over a wide range of power ratings subject to a specified temperature rise (B).

5.2.A Core Material Review

Well-known materials for designing MFTs/HFTs are nanocrystalline, amorphous and ferrite [5.5]. Table 5-I shows a general comparison between these materials [5.6]. At high-power levels, nanocrystalline and amorphous are the two main materials for designing MFTs (e.g., f = 20 kHz) due to their low core losses (low eddy current losses), high saturation flux and high permeability [5.6],[5.7]. The low prices and flux densities (0.3-0.5 T) of the soft ferrite material make them only a suitable choice for low-power HFTs applications [5.8].

Table 5-I: Core Material Comparison [5.6]

Material	*Pros*	*Cons*
Nanocrystalline	High B_{sat} (1.2 T) Low losses @ high power High permeability	High cost
Amorphous	High B_{sat} (1.55 T) High permeability Reasonable cost	Medium losses and large sizes @ high power levels
Ferrite	Low losses and Low cost @ low-power levels	Low B_{sat} (0.5 T) Production difficulty and large sizes @ high power levels

5.2.B Temperature Rise Considerations

It is initially desired for simplicity to design MFTs/HFTs for high-power levels without a detailed design of the thermal management system (e.g., forced convection, liquid cooling). However, the temperature rises with different slopes for different magnetic materials as the rated power increases. To have good estimations about temperature changes as function of the rated power, the following assumptions are made:

Turns ratio [$N = 1$] (minimum area product, worst-case scenario).

Desired temperature rise [$\Delta T = 50$ °C].

Operation frequency[$f = 20$ kHz].

Power losses (in cores and windings) are a percentage of the maximum output power which is based on evaluating multiple design results for different power levels and the considered core material. The assumed values were 0.28 % for nanocrystalline and 0.54 % for amorphous.

The optimal flux density B_{opt} is given by [5.9] as:

$$B_{opt} = \frac{\left(h_c k_a \Delta T\right)^{\frac{2}{3}}}{\sqrt[3]{4}\left(\rho_w k_w k_u\right)^{\frac{1}{12}}\left(k_c K_c f^{\alpha}\right)^{\frac{7}{12}}}\left(\frac{K_v k_{sf} k_u f}{\sum VA}\right)^{\frac{1}{6}}. \quad (5.\ 1)$$

The minimum area product A_p is then calculated as follows [5.9]:

$$A_p = \left(\frac{\sqrt{2}\sum VA}{K_v B_{opt} k_f K_t f \sqrt{k_u \Delta T}}\right)^{\frac{8}{7}}; \quad (5.\ 2)$$

where the values of the constants are shown in Table 5-II [5.9].

The temperature rise ΔT (°C) as function of the area product A_p with assumed total power losses P_{losses} is estimated by [5.10] as:

$$\Delta T = 450\left(\frac{P_{losses}}{K_s \sqrt{A_p}}\right)^{0.826}; \quad (5.\ 3)$$

where [K_s = 39.2] is a constant used to calculate the surface area for C cores [5.10]. The material specifications and properties obtained from manufacturer datasheets are shown in Table 5-III.

Table 5-II: Constant Values of Optimal Flux and Area Product

Variable	Value	Variable	Value
coefficient of heat transfer $h_c(10w/m^2)$	10	Dimensionless quantity k_a	40
Initial wire resistivity $\rho_w\ (\Omega * m)$	$1.78*10^{-8}$	Dimensionless quantity k_w	10
Window utilization factor k_u	0.4	Dimensionless quantity k_c	5.6
Waveform factor square wave K_v	4	Core stacking factor k_{sf}	0.95
$K_t = \sqrt{h_c k_a / \rho_w k_w}$	$48*10^{-3}$	Expected temperature ΔT(°C)	50

Table 5-III: Material Coefficients [5.10]

Parameters	Nanocrystalline	Amorphous
K_C	2.3 w/m^3	1.3617 w/m^3
α	1.32	1.51
β	2.12	1.74
B_{sat}	1.2 T	1.56 T

A MATLAB® code was generated to evaluate the above equations and approximate the temperature rise at different power levels. Fig. 5.1 shows that the nanocrystalline material has a lower ΔT compared to the amorphous material, making it a better choice for designing a 120-kVA and 20-kHz MFT [5.11].

In general, the core and winding losses increase due to the increase of the area product as the rated power increases. Furthermore, the amorphous material results in a low B_{opt} so the area product is large requiring a large number of turns due to its large cross sectional area. In addition, the core losses will be large due to the resulting product of [(P_{loss}/m^3)*$volume$].

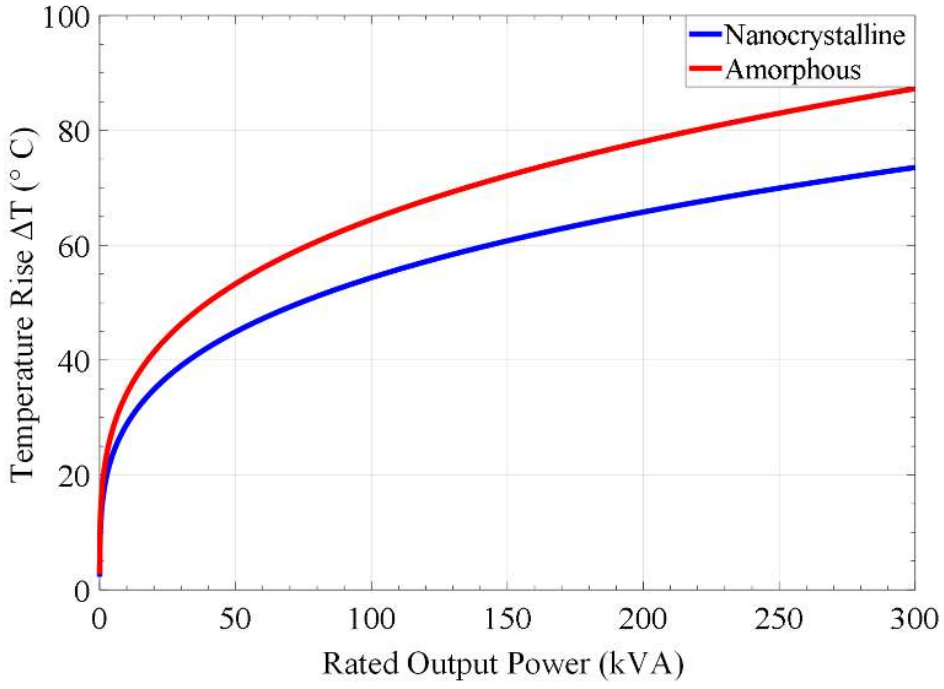

Figure 5.1: Estimated temperature rise ΔT as a function of rated power using nanocrystalline (blue) and amorphous (red) core materials.

As a result, the numerator in (5.3) is relatively larger than the denominator, which makes the temperature rise higher than that for the nanocrystalline material. The main drawback of the latter is its relatively high price. Efficiency and cost are important tradeoffs between these two materials.

King Magnetics® provides C cores which are made from nanocrystalline ribbon materials that have a high saturation flux density B_{sat}, low magnetostriction, low noise and relative magnetic permeability μ_r higher than 30,000 H/m [5.12]. The largest commercial core is 85x106x171 mm, weights 6,600 grams and has an area products of 4193.3 cm^4. This core can be used to design a 64-kW (max) MFTs assuming $\Delta T = 50$ °C. For a design with a higher rated power, designer should consider stacking cores in parallel to increase the area product if the window area is enough to fit the need number of turns.

5.3 Design Methodology for High-Power MFTs/HFTs

5.3.A Magnetizing and Leakage Inductance Requirements

Obtaining the specified magnetizing inductance L_m^* and leakage inductance L_k^* when designing MFTs/HFTs is very challenging at high-power levels. The main goal is to keep L_m^* at the value constrained by:

$$L_m^* = \frac{V_{rms}}{2\pi f\left(I_{rms} C_f\right)}, \tag{5. 4}$$

while maintaining the flux density close to its optimal value. The new variable C_f introduced in (5.4) has a range between 0 and 1 (i.e., $[0 < C_f \leq 1]$), where its value depends on the type of isolated power converter. Lower values of C_f result in a significantly larger L_m^* value, which is necessary to avoid a high magnetizing current as in the case of DAB converters where C_f is at least 0.25 (which means that the magnetizing current I_m should be less than 25 % of the primary current I_p [5.2]).

However, a certain leakage inductance L_k^* is required for DAB-based MFTs/HFTs to maximize the transferred power [5.2]; i.e.:

$$L_k^* = \frac{V_p}{2d\pi^2 P_o f}\phi(\pi - \phi), \tag{5. 5}$$

where ϕ is the phase-shift between primary and secondary transformer voltage waveforms, V_p is the primary voltage, d is the duty cycle of the voltage waveforms, and P_o is the output power. The L_m and L_k inductances depend on the core physical dimensions and winding arrangements around the core [5.9], [5.10]; specifically:

$$L_m = \frac{N^2 S_F A_c \mu_o \mu_r}{l_c + l_g \mu_r}\left(1 + \frac{l_g}{\sqrt{S_F A_c}}\ln\left(\frac{2C}{l_g}\right)\right)[H], \tag{5. 6}$$

$$L_k = \frac{\pi(MLT)N^2}{N_L}\left(\sum d_{iso} + \frac{\sum d_a}{3}\right)10^{-9}[H], \tag{5. 7}$$

where S_F is the number of cores needed to achieve the required area product A_p; μ_o and μ_r are the air and material permeabilities; l_c is the mean length of the magnetic path; C is the window length of the core; MLT is the mean length of the turns; N is the number of turns [5.9]; l_g is the air-gap length; N_L is the portion of the dimension C covered by the windings; d_{iso} is the distance between primary and secondary windings and d_a is the diameter of the Litz wire as shown in Fig. 5.2. However, the core and winding geometries in the case of DAB-based converters should be a tradeoff in favor of achieving the required magnetizing inductance since the leakage inductance can be increased by adding an external inductor. The number of turns is determined in [5.10] as:

$$N = \frac{V_{rms}}{k_v B_{max} A_c f}, \tag{5. 8}$$

where k_v is the waveform factor.

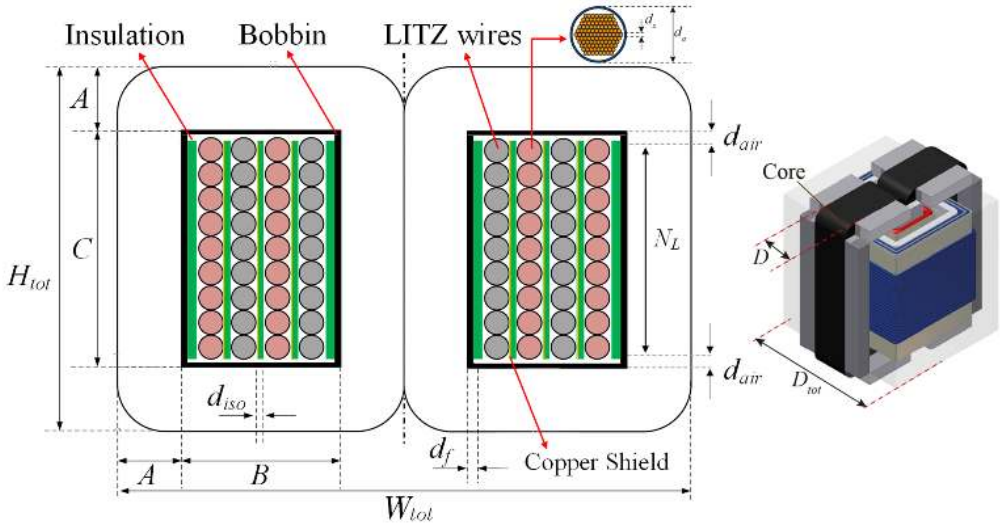

Figure 5.2: Main physical parameters of a MFT/HFT.

In the case of topologies like flyback converters, C_f is 1.0, which implies that the magnetizing current I_m is equal to the primary current I_p. As a result, the magnetizing inductance L_m in this case is much smaller than for the DAB case. From (5.6), L_m can be reduced to the desired value by introducing an air-gap of length l_g according to:

$$l_g = 2NI_{rms}\frac{\mu_o}{B_o} - \frac{l_c}{\mu_r}. \qquad (5.9)$$

Equation (5.9) considers the case of a shell-type transformer implemented by using two C-cores [5.13]. However, the value of the leakage inductance should be minimal to avoid undesired voltage spikes across the converter's power devices.

5.3.B MFTs/HFT Design Steps

The general objective of the transformer design is to maximize efficiency while minimizing transformer weight or volume subject to the specified temperature rise and inductances. Thus, the MFTs/HFTs design largely follows the procedure illustrated in Fig. 5.3.

The suggested main steps for designing MFTs/HFTs are the following:

Step 1: Design parameters are specified based on the application's requirements that take into account the desired magnetizing inductance L_m^* using (5.4) by selecting the proper value of C_f.

Step 2: The saturation flux density B_{sat}, and the Steinmetz coefficients k, α and β are obtained from the manufacturer datasheet of the selected core material.

Step 3: The optimal flux density B_{opt} is calculated using (5.1) that considers that minimum loss point (i.e., copper and core losses are equal).

Step 4: The minimum area product A_p^* is calculated using (5.2) and selecting a core whose area product $A_p > A_p^*$.

Step 5: Winding arrangements and dimensions are made based on the application specifications as explained in the above subsection (A).

Step 6: Air-gap length l_g is calculated using (5.9) to meet the desired L_m^* that was obtained in (5.4).

Step 7: Magnetizing inductance evaluation based on the structure of the cores and winding coil dimensions around the central core. The actual L_m can be calculated using (5.6), and then compared to the desired L_m^* (5.4).

Step 8: Leakage inductance evaluation based on the structure of the cores and the distance between primary and secondary coils, the actual L_k can be calculated using (5.7), and then compared to the desired L_k^*. The windings should be as close as possible to each other to minimize the leakage inductance in case of flyback converters. For that reason, the secondary windings are wound around the primary windings with the minimum distance constrained by the required isolation distance.

Step 9: Finite-Element Analysis (FEA) is performed for design verification of the previous steps. The flux density distribution B through the cores is visualized using ANSYS™ simulations as it can be seen in the following section. If the cores experience high magnetic fields B, the core dimensions and the air-gap length should be modified (increased) based on (5.9) to reduce the flux fields towards its optimal level.

Step 10: Volume calculation is very important, particularly, for applications characterized by space limitations. If the volume specification is not fulfilled, a new optimization design iteration can be considered by selecting a different operating flux density in terms of the optimal volume in *Step 3*. However, there is a tradeoff between efficiency and power density.

Step 11: Core and winding losses are the two main transformer losses. There are many approaches to calculate power core losses (i.e., separation of losses, Preisach model and Jiles-Atherton model based on the hysteresis model). The core loss calculation here is based on the Improved Generalised Steinmetz Equation (IGSE) due to the square waveform excitation [5.14].

Step 12: The resulting temperature rise ΔT is calculated using (5.3) to ensure that the specified limit (in Step 1) is not exceeded. In addition, the required isolation level is evaluated by calculating the distance between conductors d_{iso} per the procedure given in [5.15]:

$$d_{iso} = \frac{V_{iso}}{k_{iso} E_{ins}}, \tag{5. 10}$$

where V_{iso} is the isolation voltage level and it should comply with ANSI/IEEE C57.12.01, k_{iso} is the safety margin specified by the designer based on the application criteria and E_{ins} is the dielectric strength for the material isolating the primary voltage from the secondary voltage. If the requirements are not fulfilled, a new iteration is initiated considering two options: changing the core dimensions in *Step 4*, or winding arrangement in *Step 5*.

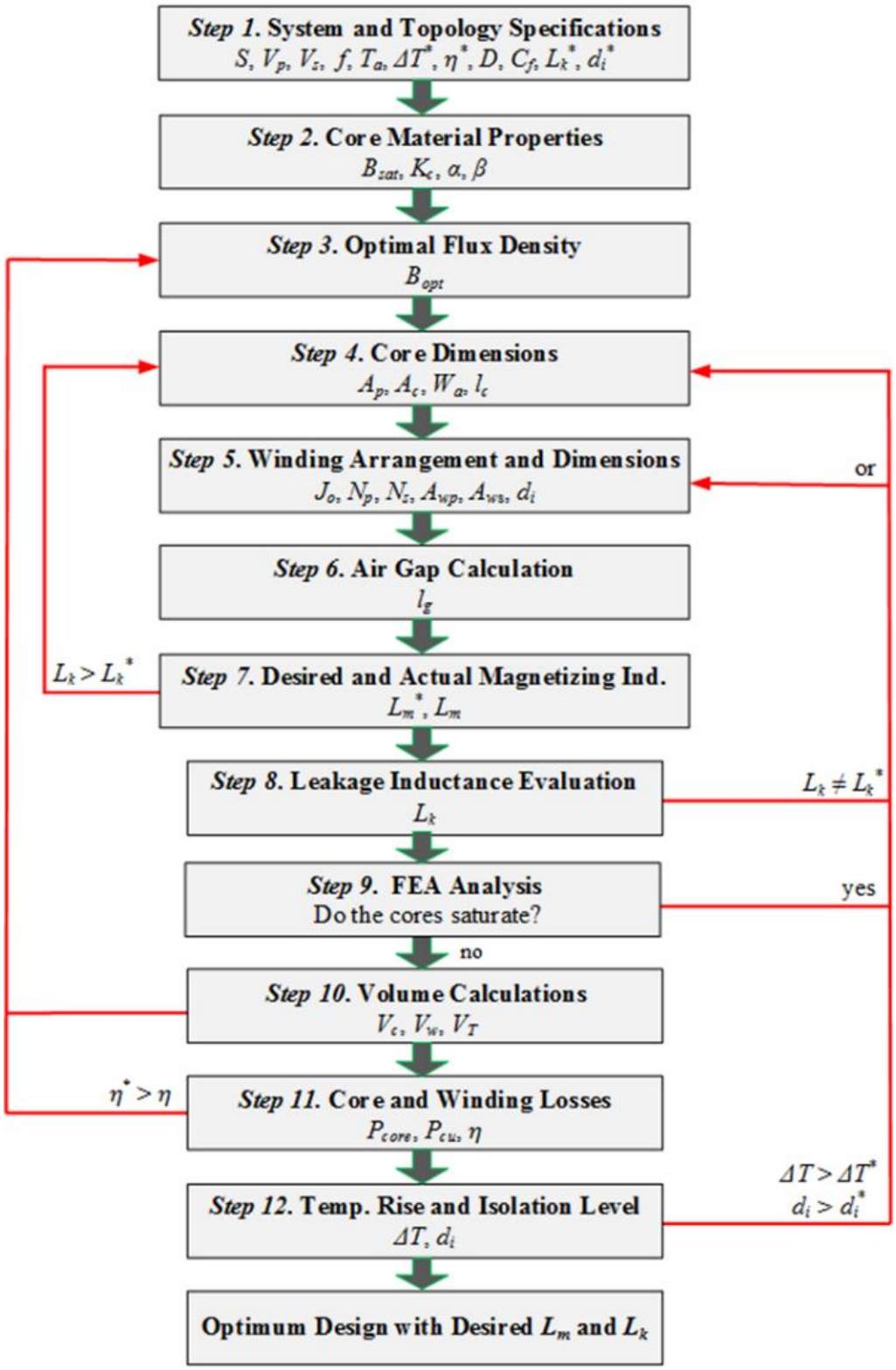

Figure 5.3: MFTs/HFTs design flow chart.

5.4 High-Power Case Study Design Results

Table 5-IV presents the specifications and requirements of the case study for designing a MFT where energy storage is required (120-kVA, 20-kHz, 1020-V_{rms}, [N_p/N_s = 1]). Based on the given specifications and requirements, the optimal flux density B_{opt} was calculated as 0.147 T, being a good compromise between efficiency and volume.

Fig. 5.2 illustrated the main physical dimensions of the selected shell-type transformer to achieve the required magnetizing inductance and a low leakage inductance. In case of a topology like the flyback converter, the isolation distance d_{iso} determines the minimum distance between windings in order to meet the leakage inductance requirement. The flux density distribution inside the cores is shown in Fig. 5.4 where the flux densities B are within the material allowable limits. The sharp edges of the core are the regions where the higher magnetic fields are located, while most of the core structure experience density fields between (0.161 T green) and (0.096 T blue) which is a perfect range for the calculated optimal flux. The temperature rise of the designed MFT was calculated as low as 48 °C due to nanocrystalline material which has low losses at the operation frequency of 20-kHz. As the power level increases, challenges arise in terms of obtaining the required L_m^* and L_k^* inductances. Ssubstantial power losses in the cores and windings may require complex cooling systems [5.16]. which compromise the transformer size and weight. Also, the required voltage isolation level increases with increased power levels.

Table 5-IV: Specifications and Results For MFT/HFT

Specified Parameters	**Required**	**Calculated**
Magnetizing Inductance L_m	≤ 68 μH	30 μH
Leakage Inductance L_k (μH)	Small as possible	1.11
Efficiency η (%)	≥ 99	99.7

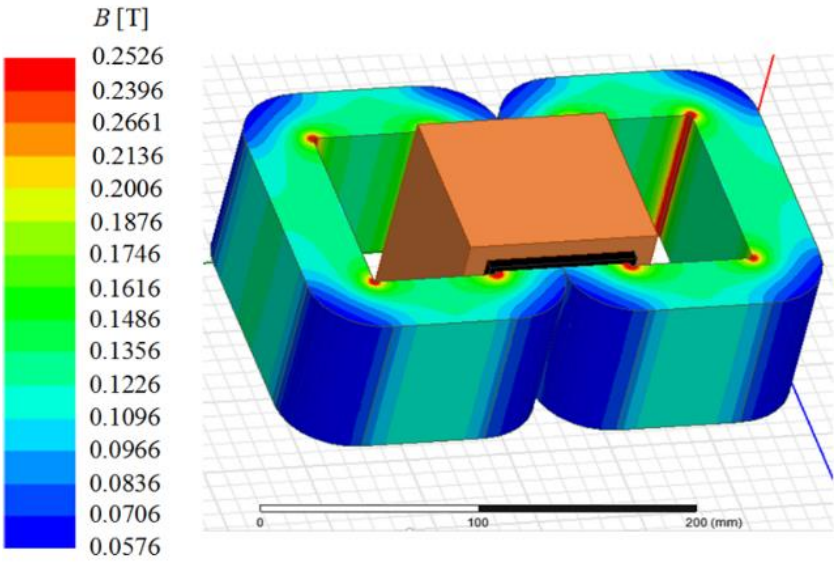

Figure 5.4: ANSYS^{TM} flux density values inside the cores.

5.5 HFT Scale-Down Prototype and Results

A scale-down prototype of a HFT based on a flyback converter topology was built for verification of the proposed design methodology. The main specification parameters of the 1020-W high-frequency transformer are given in Table 5-V.

Leakage inductance has to be as small as possible to avoid unwanted voltage spikes across the terminal of the transformer and converter's switches. Meanwhile, the magnetizing inductance values satisfies (5.4) to guarantee power transfer from primary to secondary side at rated voltage and current. However, having a slightly larger magnetizing [$L_m > L_m^*$] is accepted as a tradeoffs to keep leakage inductance as small as possible.

Table 5-V: Specified Parameters of The HFT Prototype

Parameters	**Values**
Rated Power	1020 W
Primary DC Voltage	120 V_{DC}
Primary RMS Current	8.5 A_{RMS}
Turns Ratio	1:1
Switching Frequency	100 kHz

The main physical parameters of the cores been used for this prototype (Fig. 5.2) are shown in Table 5-VI. The calculated value for the magnetizing inductance with an air-gab of l_g = 0.87 mm was obtained from (5.6) as [L_m = 38.1 µH] which is very close to the measured prototype value [L_{exp} = 40.5 µH] measured by the 4192A LF impedance analyzer which means an error of less than 6.5 %. The calculated value for the leakage inductance was calculated from (5.7) as [L_k = 1.19 µH] where the experimental value is [L_{kexp} = 1.04 µH]. The error between these two values was calculated as 14.4 % assuming that there is no space between turns which makes N_L at its minimum value. The built high frequency transformer prototype is shown in Fig. 5.5.

Table 5-VI: Physical Parameters for The HFT Prototype

A	10 mm	*F*	53 mm	Mean path length	12.8 cm
B	11 mm	d_f	1.25 mm	Eff. cross area	1.56 cm^2
C	33 mm	d_a	2.07 mm	Weight	146 g
D	20 mm	d_{iso}	0.0762 mm	Number of turns	8
E	31 mm	d_{air}	11.251mm	Area product	7.26 cm^4

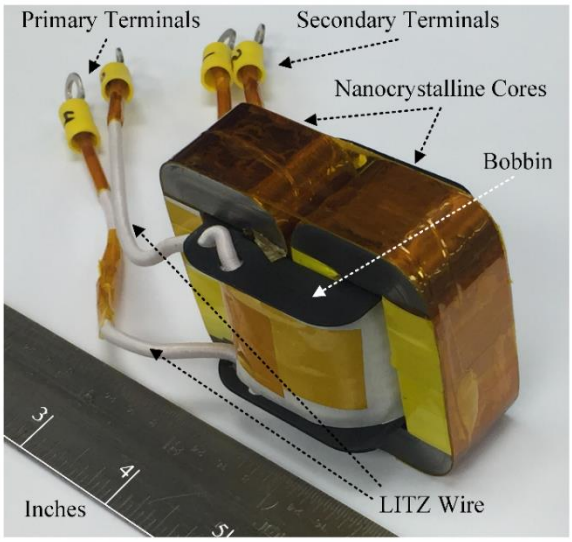

Figure 5.5: Prototype of 1020 kW, 120 V_{rms} and 100 kHz high frequincy transformer "Photo by author".

The primary-to-secondary stray capacitance between the windings must be very small to avoid undesired interactions between primary and secondary windings. For that reason, a copper shield was inserted between the two windings to reduce the total capacitance. Measurements were performed over a wide range of frequencies to make sure the transformer parameters are constant. Fig. 5.6 shows the magnetizing inductance L_m, Fig. 5.7 shows the leakage inductance L_k, and Fig. 5.8 shows the stray primary-to-secondary windings capacitance C_{ps} as a function of frequency. From 50-kHz to 150-kHz, the passive components (L_m, L_k and C_{ps}) have low changes as (10 %, 0.9 % and 0.4 %) respectively.

After verifying that the values of the magnetic components are close to the designed values calculated from the design equations, a flyback converter capable of switching at 100-kHz with an input voltage of 120-V_{DC} and a peak current of 15-A was constructed as shown in Fig. 5.9. Table 5-V provides the main specifications of the built HFT and Table 5-VI its main dimensions.

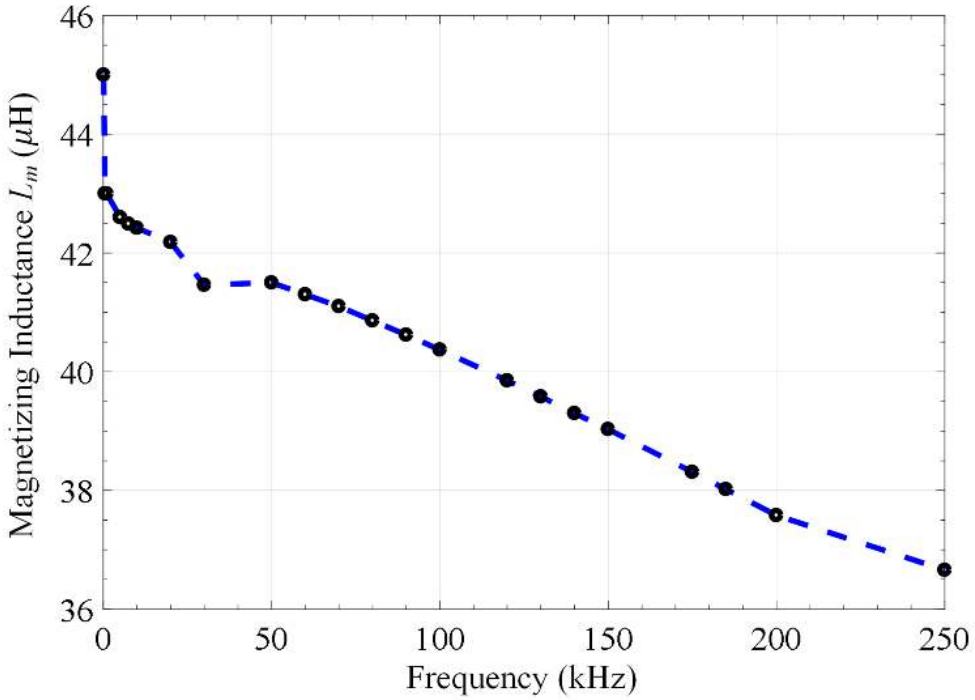

Figure 5.6: Magnetizing inductance L_m as function of the frequency.

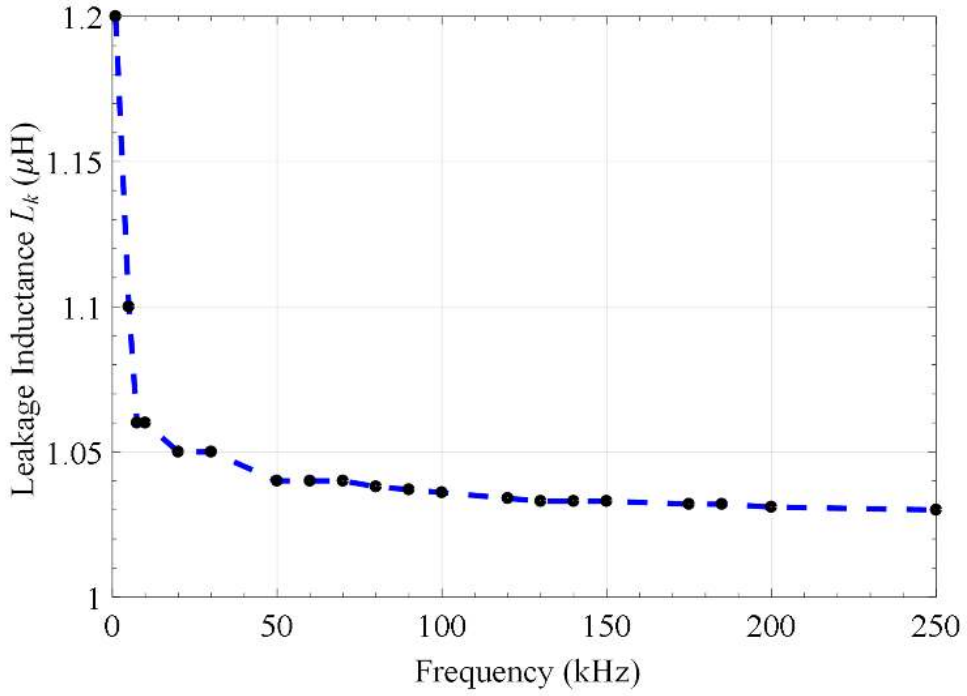

Figure 5.7: Leakage inductance L_k as function of the frequency.

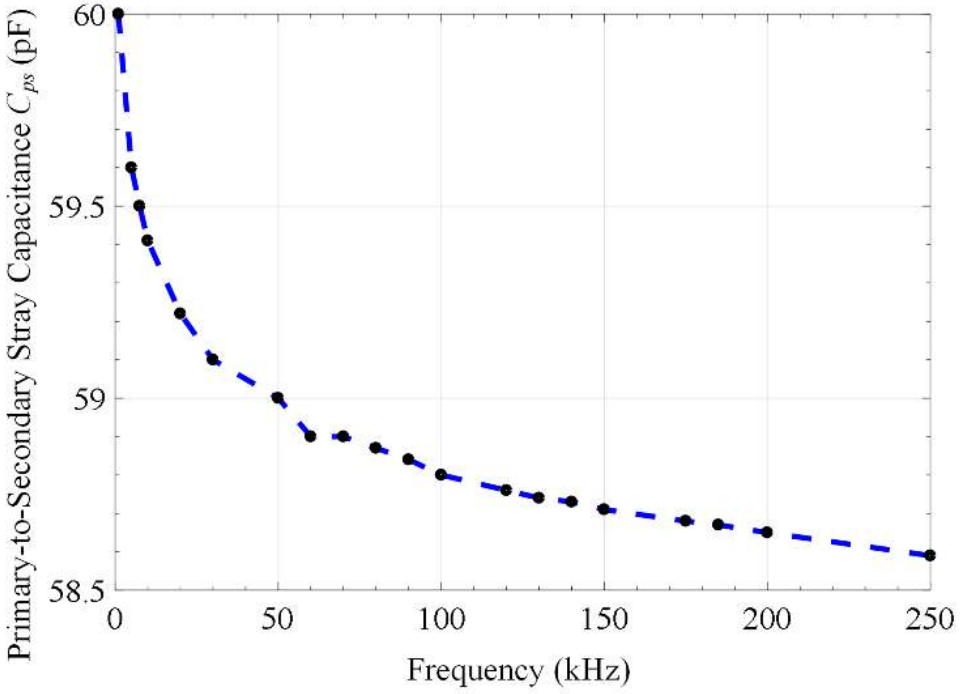

Figure 5.8: Primary-to-secondary stray capacitance C_{ps} as function of the frequency.

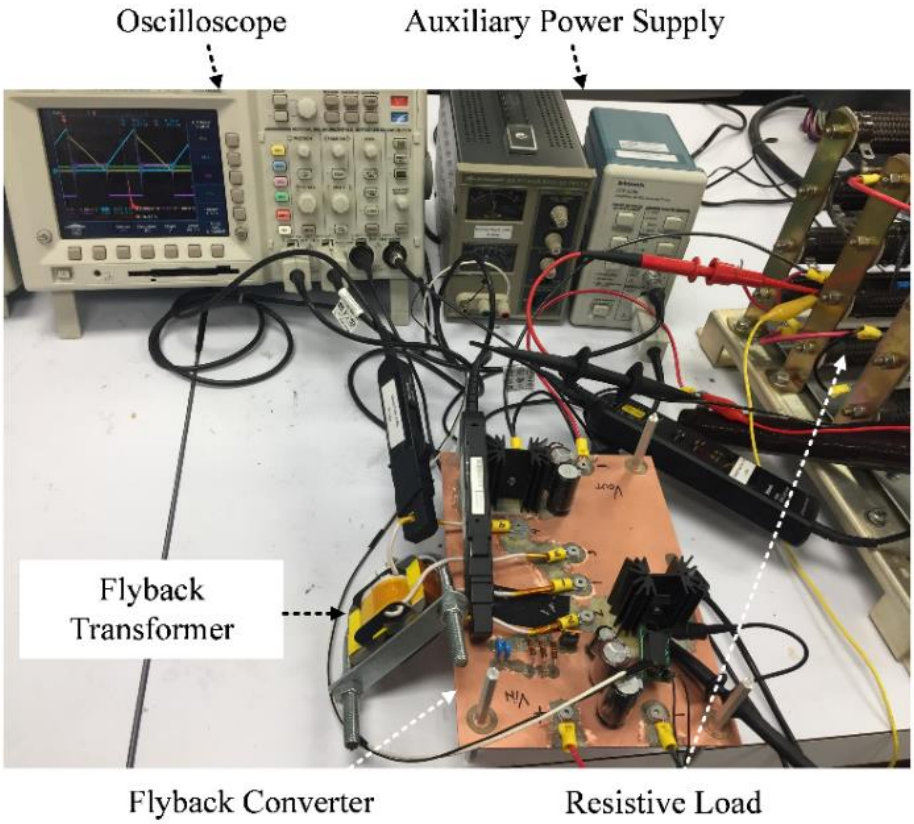

Figure 5.9: Flyback converter experimental setup "Photo by author".

Fig. 5.10 shows the transformer primary and secondary currents at rated conditions of delivering 450-W to a 35-Ω resistive load. The small current spikes that appear in the leading edge of the primary current are caused by the transformer's parasitic capacitance [5.10].

The selected operating condition for the flyback converter was the boundary conduction mode (BCM) due to its improved performance in comparison with the continuous and discontinuous modes of operation [5.17]. Because of the BCM operation with a duty cycle of 50 %, the voltage conversion ratio is 1, so the output voltage is the same as the input voltage as shown in Fig. 5.11. The drain to source voltage of the SiC MOSFET is also shown in Fig. 5.11 where it is seen that the voltage spikes across the transistor are due to the presence of the leakage inductance L_k.

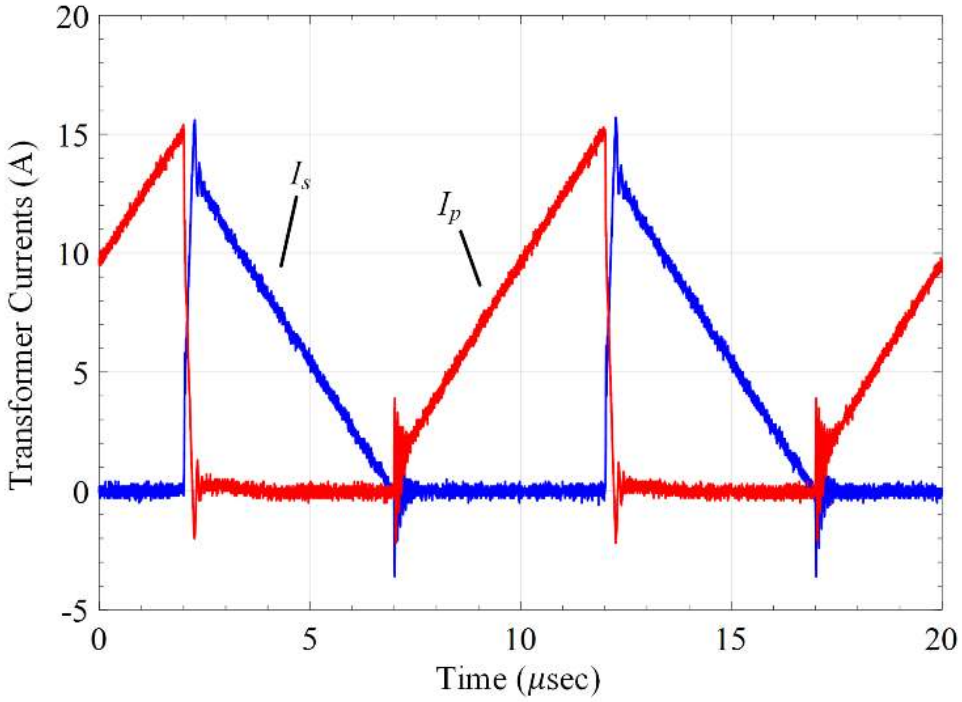

Figure 5.10: Primary I_p and secondary I_s flyback transformer currents when the input voltage V_{in} is 120 V.

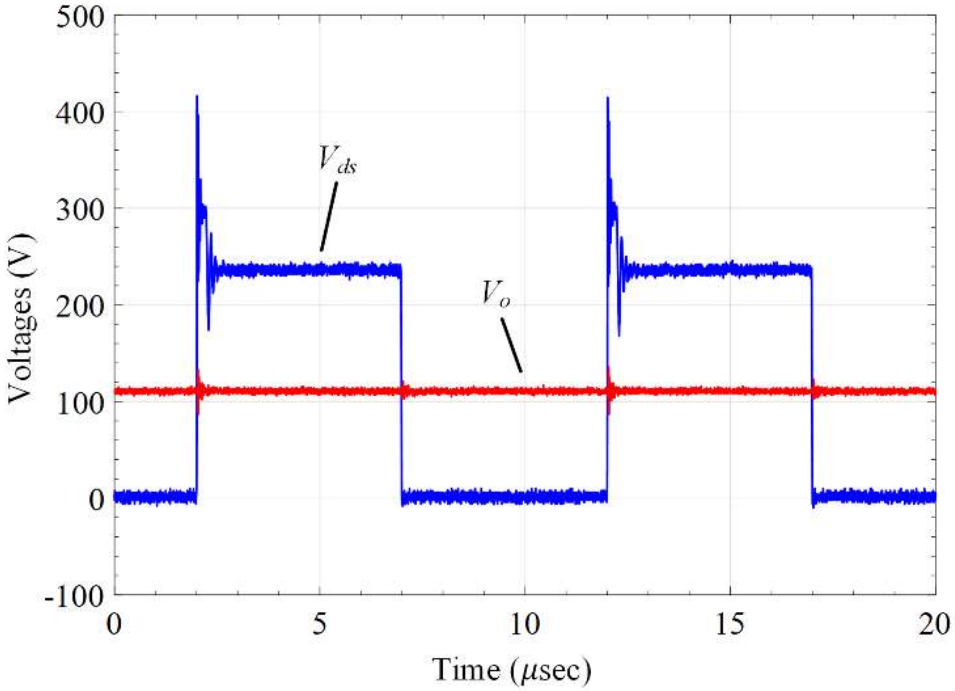

Figure 5.11: SiC MOSFET drain-to-source voltage V_{ds} and flyback converter output votlage V_o when the input voltage V_{in} is 120 V.

Those voltage spikes can be reduced to a desire lower level at the expense of reducing the efficiency of the converter [5.18]. For this particular case, the voltage spikes were limited to 450-V using a snubber based on passive components since the rated voltage of the implemented devices was 1200-V.

5.6 Conclusions

Designing MFTs/HFTs for high power levels is challenging due to system specifications and constraints (e.g., magnetizing and leakage inductances, voltage insulation level, temperature rise, efficiency) which drive the design in opposite directions so the designer must make several tradeoffs. A new simple technique to compare different core materials in terms of temperature rise was presented followed by a designed methodology that considers inductance specifications by specifying the value of the new variable C_f. The feasibility of the proposed ideas were verified through ANSYS™ simulations and a scaled-down prototype. The experimental results agreed fairly well with the theoretical calculations and simulations.

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5.7 References

[5.1] Haitham Abu-Rub; Mariusz Malinowski; Kamal Al-Haddad, "Recent Advances in Power Semiconductor Technology," in *Power Electronics for Renewable Energy Systems, Transportation and Industrial Applications* , 1, Wiley-IEEE Press, 2014, pp.832.

[5.2] Y. Du, S. Baek, S. Bhattacharya and A. Q. Huang, "High-voltage high-frequency transformer design for a 7.2kV to 120V/240V 20kVA solid state transformer," *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, Glendale, AZ, 2010, pp. 493-498.

[5.3] S.K. Mazumder, "A modular and flexible high-frequency-link transformer with a reduced device count and zero high-side devices", *Final Project Report, submitted to the U.S. Department of Energy*, April 2018.

[5.4] G. N. Wooding and A. S. De Beer, "The effect of leakage inductance and snubbing on electromagnetic interference generated by a flyback converter," *AFRICON, 2011*, Livingstone, 2011, pp. 1-5.

[5.5] R. Burdt *et al*., "Evaluation of Nanocrystalline Materials, Amorphous Alloys and Ferrites for Repetitive-Magnetic Pulse Compression Applications," *2005 IEEE Pulsed Power Conference*, Monterey, CA, 2005, pp. 843-847.

[5.6] S. Vaisambhayana, C. Dincan, C. Shuyu, A. Tripathi, T. Haonan and B. R. Karthikeya, "State of art survey for design of medium frequency high power transformer," *2016 Asian Conference on Energy, Power and Transportation Electrification (ACEPT),* Singapore, 2016, pp. 1-9.

[5.7] T. Kauder and K. Hameyer, "Performance Factor Comparison of Nanocrystalline, Amorphous, and Crystalline Soft Magnetic Materials for Medium-Frequency Applications," in *IEEE Transactions on Magnetics*, vol. 53, no. 11, pp. 1-4, Nov. 2017.

[5.8] M. Jafari, Z. Malekjamshidi, G. Lei, T. Wang, G. Platt and J. Zhu, "Design and Implementation of an Amorphous High-Frequency Transformer Coupling Multiple Converters in a Smart Microgrid," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 2, pp. 1028-1037, Feb. 2017.

[5.9] W. G. Hurley, W.H. Wölfle, Transformers and Inductors for Power Electronics: Theory, Design and Applications, 1st ed., Wiley, 2013.

[5.10] C. William, T. McLyman, Transformer and Inductor Design Handbook, 4th ed., Taylor & Francis Group, 2011.

[5.11] K. Warnakulasuriya, F. Nabhani and V. Askari, "Development of a 100kW, 20 kHz Nanocrystalline Core Transformer for DC/DC Converter Applications," *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Nuremberg, Germany, 2016, pp. 1-8

[5.12] [Online]. Available: http://www.kingmagnetics.com/nanocrystalline-c-core.html [Accessed Oct. 04, 2017]

[5.13] N. Mohan, T. Underland and W. Robbins, Power Electronics: Converters, Applications, and Design, 3rd Edition.

[5.14] J. Li, T. Abdallah, C.R. Sullivan, "Improved calculation of core loss with nonsinusoidal waveforms," in *Proceedings of the IEEE Industry Applications Society Annual Meeting*, pp. 2203–2210, October, 2001.

[5.15] G. Ortiz, J. Biela, J. W. Kolar, "Optimized design of medium frequency transformers with high isolation requirements," *36th IEEE Industrial*

[5.16] A. Atalla et al., "Advancements in high power high frequency transformer design for resonant converter circuits," *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, 2016, pp. 1-8.

[5.17] L. A. Garcia Rodriguez and J. C. Balda, "A comparison of isolated DC-DC converters for microinverter applications," *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA, 2013, pp. 2084-2091.

[5.18] E. O. Lindstrom, L. A. Garcia-Rodriguez, A. R. Oliva and J. C. Balda, "Designing an optimum non-dissipative LC snubber for step-up flyback converters in DCM," *2017 IEEE 8th Latin American Symposium on Circuits & Systems (LASCAS)*, Bariloche, 2017, pp. 1.

APPENDIX 5.A

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November 13, 2019

To whom it may concern,

This letter is to verify that Mr. Obaid Martha Aldosari, ID 010768784, is the first author and did at least 51% of the work for the paper titled "Design Trade-Offs for Medium- and High-Frequency Transformers for Isolated Power Converters in Distribution System Applications".

Kind Regards,

Dr. Juan Carlos Balda

University Professor, Department Head and Major Advisor to Mr. Obaid Martha Aldosari

RESEARCH CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

6.1 Research Conclusions

Two novel three-level isolated AC-DC PFC converters were presented throughout the dissertation. In particular, Chapter 2 introduced the first topology accomplishing the following:

- Same advantages as the previous three-level topologies [6.1], [6.2] but with less number of active devices. The secondary switches sustained half of the output voltage, whereas those ones in a similar converter (i.e., DAB) must sustain the full output voltage.

Chapter 3 was an extension of Chapter 2 modified the proposed topology to operate under soft-switching. A new circuit configuration was introduced by adding a flying capacitor in the secondary side to achieve soft switching over the entire power range. Moreover, a close-loop algorithm was implemented to show the converter response to a step load change. The analysis under steady-state including soft switching conditions and efficiency evaluation were performed and demonstrated through a 25-kW simulation case study and a 900-W experimental prototype. Chapter 3 had the following contributions:

- Adding a flying capacitor resulted in the secondary switches turning ON at ZVS and ZCS over the full range of power without any restrictions on duty cycles.
- The two active switches in the secondary side continued to sustain half of the output voltage, which in return increased the flexibility of operating the proposed topology at a high output voltage.
- The total price of the secondary bridge should be less than those of other existing three-level converters (i.e., NPC, DAB). The total cost of the proposed converter should decrease substantially especially when IGBT switches are used. That is because an IGBT does not

have body diode and there is no need to connect diodes (D_5, D_6) in series with the switches (S_5, S_6). For example, assuming that the components shown in Table 6-I are available to be used in the three different converters (i.e., H-bridge, proposed converter, and NPC converter), the total cost of each converter can be estimated as:

[$\mathbf{C_{H\_Bridge}} = 4(\$158.4)_{IGBTs} + 1(\$32.78)_{Output\_capacitor} + 2(\$165.5)_{Gate\text{-}driver} = \$997.38$].

[$\mathbf{C_{Proposed}} = 2(\$124.82)_{IGBTs} + 2(\$10.22)_{Output\_capacitor} + 1(\$165.5)_{Gate\text{-}driver} + 2(65.87)_{Diode} + 1(3.13)_{Flying\_capacitor} = \$570.45$].

[$\mathbf{C_{NPC}} = 4(\$124.82)_{IGBTs} + 2(\$10.22)_{Output\_capacitor} + 2(\$165.5)_{gate\text{-}driver} + 2(\$62.88)_{Diode} + 1(\$3.13)_{Flying\_capacitor} = \$979.61$].

Fig. 6.1 shows that the H-bridge could be estimated 75% more expensive and NPC is 71% more expensive than the proposed converter.

Table 6-I: Components Used for Cost Comparison

Converter Type	Components	Part Number	Rated Voltage	Quantity Needed
H-Bridge	IGBT	FF400R12KE3	V_o	4
	Output Capacitor	B32374A4506J080	V_o	1
	Gate driver	L5066601	-	2 (two channel)
	Diode	None	-	-
	Flying capacitor	None	-	-
Proposed	IGBT	FF400R06KE3	$V_o/2$	2
	Output Capacitor	C4ATHBW5200A3NJ	$V_o/2$	2
	Gate driver	L5066601	-	1 (two channel)
	Diode	MEO450-12DA	V_o	2
	Flying capacitor	FKP1O131507D00KSSD	$V_o/2$	1
NPC	IGBT	FF400R06KE3	$V_o/2$	4
	Output Capacitor	C4ATHBW5200A3NJ	$V_o/2$	2
	Gate driver	L5066601	-	2 (two channel)
	Diode	MEO500-06DA	$V_o/2$	2
	Flying capacitor	FKP1O131507D00KSSD	$V_o/2$	1

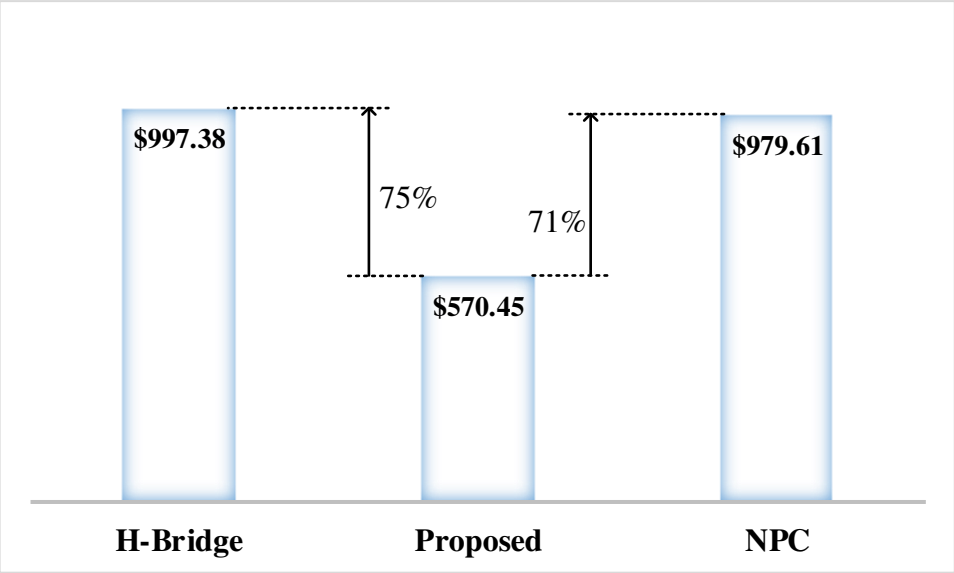

Figure 6.1: Total cost comparison for the H-Bridge, Proposed, and NPC converters.

- In comparison with the topology presented in [6.1], which claimed 93% efficiency, the first proposed topology showed higher efficiency of 94.5%. Most of the total power losses, 55%, dissipated across the magnetics elements. The primary and secondary bridges dissipated 33% and 12 % of the total losses, respectively.
- The proposed topology operated with a closed-loop control algorithm to obtain high power factor and regulate the dc-bus and output voltages within desired limits. The system response was evaluated at a sudden load change applied to the output terminals. The results showed that the proposed topology and control technique operated as expected following the reference signals.

Chapter 4 explained in detail the full characteristics of the second proposed topology where the primary (NPC) inverter was replaced by a T-type converter to further decrease the number of devices. The following goals were attained:

- Conduction losses were reduced by eliminating the two freewheeling diodes present in the NPC inverter. In the NPC inverter, the diodes conduction losses are significant, especially

when the output load increases. When this happens, the control generates a minimal primary duty cycle to avoid a high dc-bus voltage, and the primary current conducts through the freewheeling diodes for most of the switching cycle. Furthermore, the T-type inverter conducts the primary and boost inductor currents through only one switch during [$D_pT_s/2$]. However, the NPC inverter conducts the same currents for the same period through two switches.

- A new modulation scheme was established for the second topology to reduce the switching conduction losses and achieve high efficiency. It showed that the common-source switches (S_2, S_3) turned ON at the same time to circulate the primary current instead of conducting through the body diodes, which in turn minimized the conduction losses of these two switches. Consequently, the proposed topology based on T-type inverter shows an efficiency of 95.8% higher than that one for the NPC topology.

It was indicated that the magnetic losses are the largest loss component. Hence, the design of medium-frequency transformer is very important topic. For completeness, chapter 5 gave detailed steps for designing a high frequency transformer and addressed the design trade-offs that need to be considered. In particular:

- The magnetic design equations were rearranged to estimate the temperature rise as function of the output power for a specific material. Also, a new equation was determined which can lead to the required magnetizing inductance for different power converter topologies.
- FEA simulation was included in the design steps to provide essential information regarding the flux-density strength and distribution, temperature rise, and saturation state.

6.2 Recommendations for Future Work

There are several new topics worth exploring since the proposed topologies are new; in particular:

1) Connecting two coils in the secondary side to split the secondary current in half, with the goal of increasing the efficiency of the secondary bridge.
2) Connecting the primary bridges in parallel and cascading secondary bridges in series while using a fixed duty cycles to control both the input dc-bus voltage and output voltage (refer to Fig. 1.7).
3) Appling a nonlinear control to the proposed topology instead of using the classical PI control with the goal of improving the load step response.
4) Optimizing the magnetics design in order to improve the overall efficiency.
5) Selecting a better device (e.g., SiC MOSFETs) that should improve overall efficiency.
6) For high-power applications, the start-up time and discharge of the flying capacitor need to be considered and investigated.

6.3 References

[6.1] L. A. Garcia Rodriguez, V. Jones, A. R. Oliva, A. Escobar-Mejía and J. C. Balda, "A New SST Topology Comprising Boost Three-Level AC/DC Converters for Applications in Electric Power Distribution Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 2, pp. 735-746, June 2017.

[6.2] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen and J. W. Kolar, "Optimal ZVS Modulation of Single-Phase Single-Stage Bidirectional DAB AC–DC Converters," in *IEEE Trans. on Power Electronics*, vol. 29, no. 8, pp. 3954-3970, Aug. 2014.