A three-phase to three-phase series-resonant power converter with optimal input current waveforms, Part I: control strategy

A Three-Phase to Three-Phase Series-Resonant Power Converter With Optimal Input Current Waveforms. Part I: Control Strategy

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Abstract—**Application of the technology of series-resonant power conversion is expanding into the field of multiphase ac to ac conversion. For this class of power converters a strategy is developed that facilitates full control of input and output waveforms, only limited by physical borders. Basic concepts and physical background of this strategy are presented, and tested by way of computer simulations. The strategy is found to be worthwhile for multiphase-input multiphase-output series-resonant power converters, for both ac and dc power conversion.**

I. Introduction

THE SERIES-RESONANT (SR) power converter has been a subject of intensive research in recent years. Numerous authors have reported on such various subjects as small signal analysis [1], large signal analysis [2], side effects of transformers [3], [4], control methods [5], new topologies [6], and multiphase SR converters [7]–[9]. From the last of these it appears that the SR converter, which up until very recently has been employed primarily as a dc to dc voltage scaling and regulating device, is now being employed in dc to ac and multiphase links as well. In these applications the original operation modes for which the SR converter has been developed have been changed in several ways. In these new operating modes, efficiency, which was a primary design goal for the class of dc to dc SR converters, is hampered somewhat because of waveforms that are not fully "resonant" any more. Nevertheless, the SR converter can be an interesting device for multiphase applications because it

1) guarantees turn-off of semiconductor devices under all, including transient, operating conditions

2) can generate smooth voltage and current waveforms at both output and input sides

3) is inherently short-circuit proof.

This paper, which is closely linked to a companion paper [10], presents a novel control strategy for multiphase-input multiphase-output SR power converters. The implementation and results of this control strategy are presented in [10].

After reviewing some basics in SR power converters, a hierarchy of control mechanisms is presented, together with their respective theoretical backgrounds and practical limitations. The respective controllers are then presented in a simulation context. Some typical results are shown.

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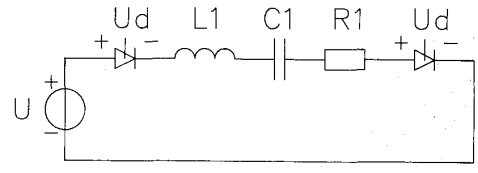

Fig. 1. Representation of resonant circuit during operation of the converter.

II. Switching Model

In order to develop a control and protection system for a multiphase series-resonant power converter we will start with a very simple representation of the basic circuit. Fig. 1 depicts a resonant circuit as it could be represented during a specific operation cycle in a power converter. For the sake of argument we will restrict our analysis in this section to lossless circuits, i.e., the series resistance of the resonant circuit $R1$ and the switch voltage drops Ud are assumed to be zero. With these assumptions the mathematical analysis of the operation of the circuit is straightforward, and can be found in numerous papers [2], [12]–[14]. As we intend to develop means to construct converter equipment for relatively high power levels, we will further restrict the discussion to +type continuous conduction mode (see [14]) operation of the converter. Only this operation mode seems to be feasible for use with thyristor switching devices.

In general, a resonant current halfcycle can be thought of as being composed of a number of current segments, which are separated by closing and/or opening actions of semiconductor switches. In order to operate the power circuit with minimal switching losses, we will try to use the smallest possible number of switching actions and current segments per resonant halfcycle. The minimum number of current segments that could be used to transfer power in a predictable manner in a multiphase converter system has been shown to be two in [6]. The number of switches operated at the segment border is dependent on the configuration of the power circuit. Most existing series-resonant power converter topologies use a switching pattern in which at the segment border two semiconductor switches are turned off and two others are turned on. A new circuit topology that has been developed recently [6] uses only one switch to turn off and one other to turn on. This also appears to be the minimum number of

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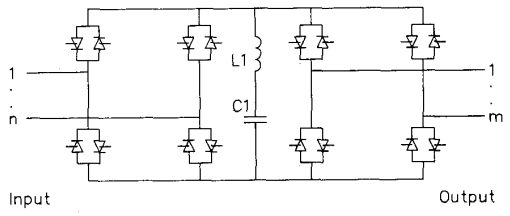

Fig. 2. Schematic of the power circuit of an n-phase to m-phase series-resonant power converter.

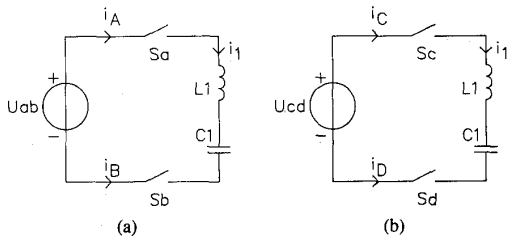

Fig. 3. (a) Connection of resonant circuit during the first current interval. (b) Connection of resonant circuit during the second current interval.

switches that can be used to separate two segments, which means that in that particular converter an absolute minimum number of switching actions is attained.

In view of this small number of switch actions, it seems to be natural to use a topology similar to the one presented in [6] for our purpose as well. As will be shown in the following, this is indeed possible. An m-phase to n-phase version of the power circuit is depicted in Fig. 2. Note that topologically input and output terminals of the circuit are equivalent. Apart from being elegant, this feature makes a very modular construction of the power circuit possible. As a first approach to arriving at an understanding of the operation of this class of converter equipment, we will focus on the flow of power in the resonant circuit.

III. Power Flow During One Halfcycle

In Fig. 3(a) the resonant circuit is depicted as it would be connected during the first segment of a resonant current halfcycle. The switches *SA* and *SB* are to represent the semiconductor switches actually used, and the ideal voltage source *Uab* could be any low-impedance current path outside the converter. The direction of current flow in the terminals *A* and *B*, which are connected through *SA* and *SB* to the resonant tank circuit, is dictated by the direction of current in the resonant circuit. Clearly, currents *Ia* and *Ib* will flow in opposite directions.

The circuit as connected during the second and last current segment is indicated in Fig. 3(b). The resonant tank is now connected to a low-impedance path *Ucd* via switches *SC* and *SD*, respectively. Similar to the situation in the first current segment, currents *Ic* and *Id* need to have opposite signs.

Because we have stated before that only one switch is turning on and only one switch turning off at the segment border, we can conclude that either terminal *A* has to be the same physical terminal as *C*, or that *B* has to correspond physically with *D*. When we assume that the first case (A = C) applies, then the circuit for both the first and the second current segment can be drawn schematically as in Fig. 4(a). In Fig. 4(b) the second case (B = D) is depicted.

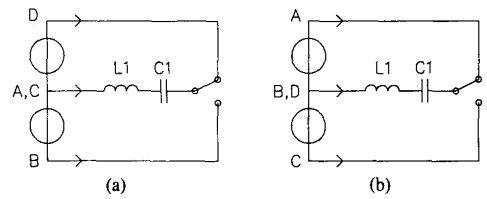

Fig. 4. (a) Representation of both first and second current segment connections for the case in which terminal *A* is equal to terminal *C*. (b) The same for the case in which terminal *B* equals terminal *D*.

If we take a closer look at the flow of power during the two current segments, we can see that for the first case the power flowing into the resonant tank during the first and the last current segment, respectively, can be described by

$$P1 = Uba * Ib \tag{1}$$

$$P2 = Udc * Id. \tag{2}$$

The sign of the power flow during the first and the last current segments, respectively, follows from

$$\text{sign}(P1) = \text{sign}(Uba) * \text{sign}(Ib) \tag{3}$$

$$\text{sign}(P2) = \text{sign}(Udc) * \text{sign}(Id). \tag{4}$$

If we want the net energy flow into the resonant circuit to be zero, as would be the case if a so-called *Vc* peak predictor technique [11] is used, the signs of *P*1 and *P*2 need to be opposite. If not, the switching sequence would try to either store net energy in or extract net energy from the resonant tank. From (3) and (4) it can be seen that, as the signs of currents *Ib* and *Id* are equal (see Fig. 4), to fulfill this need the signs of *Uab* and *Ucd* need to be opposite. A similar result applies to the second case (B = D). This observation can be restated as follows:

> For a minimal loss switching cycle, during which no net energy is stored in the resonant circuit, the one terminal out of three that is to carry current in a unique direction needs to carry a voltage in between the voltages of the other two terminals involved in this particular cycle.

This observation is of major importance for the discussion to follow. It will be referred to as "the micropower requirement."

Note that in a practical situation, if thyristors are used, the switching pattern for the complete resonant halfcycle would be completely defined by the commutation requirement. A closer look would reveal that in order to obtain natural commutation of the current at the segment border, the first current segment would always have to extract energy from the resonant circuit, and the second segment would always have to deliver energy to it. It follows that, once we have located the three terminals in which current is to flow during the resonant halfcycle being considered, the actual switch selection is only a matter of some straightforward logic.

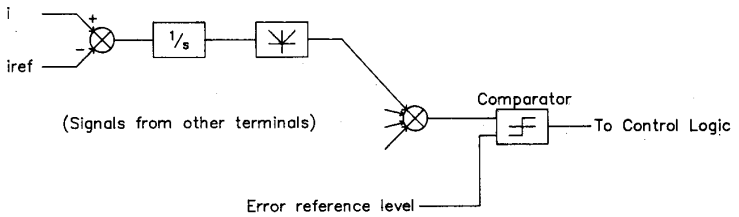

Fig. 5. Schematic of the ASDTIC current controller subsystem.

IV. Hierarchical Control System

In this section we will give an overview of the many superimposed control systems that together will operate the series-resonant converter in a safe and predictable manner.

A. ASDTIC Controller

ASDTIC stands for analog signal to discrete time interval controller. This lengthy name covers a method to control a nonuniform pulse-area modulating process such as could be present, for example, in a dc-dc buck chopper with varying input voltage [15]. The concept has been enlarged recently to cover multiphase power systems as well [7]. An important item in this context is that, unlike the great bulk of state-of-the-art control systems for multiphase converters, we will try to control all terminal currents, at both the input and the output.

In the general case of an n-to-m phase converter for this purpose a set of $(n + m)$ current reference signals is defined. These signals normally would have only a low-frequency content. The difference of the reference signals and their respective $(n + m)$ actual currents are integrated to obtain $(n + m)$ error signals Qi. Physically, the Qi would represent a lack or excess of charge transferred to the particular terminal. The sign of the error signal then indicates the direction of current flow needed in the particular terminal to decrease the error. The purpose of our controller then would be to minimize the sum of the magnitudes of these error signals. At any instant when the sum-of-errors exceeds a predefined level, the controller will try to create a resonant halfcycle in such a way as to lower the sum-of-errors. The process has been described more fully in [7]. An impression of this subsystem is depicted in Fig. 5.

B. Fast Power Controller

In order to be able to generate a resonant halfcycle, a process is needed that will select three terminals from the manifold $(n + m)$ in which current will flow during this particular halfcycle. Clearly any set of three will need to conform to the micropower requirement. As multiple sets might apply to this, we need a second criterion to obtain a unique set. The following procedure has been developed:

1) Locate the terminals with the most positive and the most negative error signal. Note that this corresponds to locating a terminal for positive current flow and another for negative current flow. We will name these terminals $L+$ and $L-$. In the case of only positive or only negative error signals, repeat.

2) Out of the remaining $(n + m - 2)$ terminals select those which together with $L+$ and $L-$ constitute a set which conforms to the micropower requirement.

3) In the case of multiple solutions to 2, select the terminal with the largest magnitude of error signal. In the case of no solution, go back to 1.

Note that, as priority is given to those terminals that have a large error signal, the procedure will automatically correct large deviations from the desired behavior first. We obtain a working set of three terminals, and as stated before the resonant halfcycle is by now fully defined and can be initiated. However, if in step 1 or 3 no appropriate terminals can be selected, the procedure will be looping until eternity. A discussion of sources of such looping and solutions to it will be given in the following sections.

C. The Current Offset Controller

Because of Kirchhoff's current law, the sum of all converter terminal currents will be zero. However, it is entirely possible for us to generate a set of current reference signals that do sum to nonzero. In this situation at least one terminal current will deviate from its reference value. In time this deviation would in our ASDTIC control system be integrated to a large total error signal, causing the converter to run at maximum speed. However, because physics forbids it, whatever the switching action taking place in the converter, it won't be able to lower the total error signal, and we will lose control of the system.

Of course, in a practical situation, we would try to construct our circuits in such a way that the sum of references would be zero. Unfortunately, this is impossible to achieve over a large temperature range. Therefore, we have opted for a solution to this problem using feedback. A simple and effective method was developed in which the sum of all $(n + m)$ error signals Qi is integrated and used to correct (the dc content of) one or more current reference signals. The system is depicted in Fig. 6. On the left-hand side the ASDTIC integrators shaping the $(n + m)$ error signals are shown. First the sum of the error signals is calculated and integrated. To obtain adequate stability in this second-order control system, a proportional action is introduced as well, which indicates that the system will function as a PI controller. The loop is closed by adding the output of the controller to at least one of the current reference signals.

Note that if further restrictions to a particular set of terminal currents are made, such as could be the case when driving a floating load, more control loops of similar composition will be needed. This reflects the fact that in such a situation we actually don't have $(n + m - 1)$ degrees of freedom to choose our current reference signals, but less.

Incorporation of the needed number of controllers of this type in our system will guarantee that the looping of our

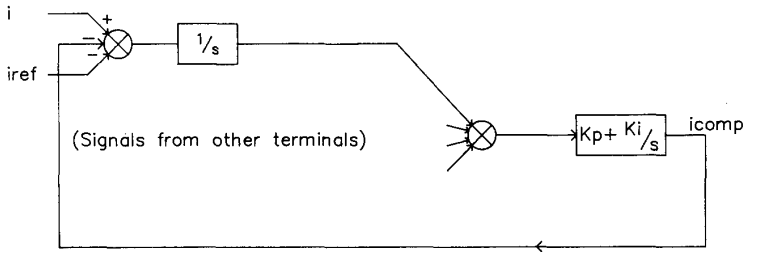

Fig. 6. Circuit schematic of the current offset controller.

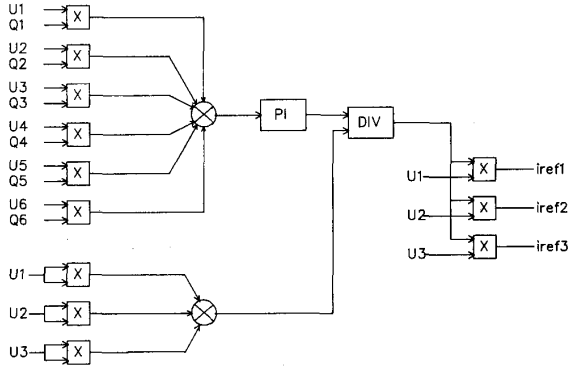

Fig. 7. Circuit schematic of the power controller.

control system in the 1 → 1 → 1 etc. mode will stop after a limited number of iterations.

D. The Slow Power Controller

Because of the law of conservation of energy, and because we have an essentially lossless converter system, a further restriction applies to our choice of current reference signals. Similar to the discussion in the last section, here the converter system will not tolerate having net energy stored in it or extracted from it. If we were to define our current reference signals to store energy in or extract energy from the converter system, physics would force the actual currents to deviate from these references, and control would be lost. The control system would start looping, because no set of three terminals conforming to the micropower requirement could be found.

Up to this point the discussion has greatly paralleled the one in the last section. However, the construction of a control loop that is to correct current reference signals is less obvious here.

A rather intuitive approach was taken, simulated, found to work, and later made plausible by mathematical means. By simulation of the operation of the converter system we found that in the case of mismatch between actual and "reference" power levels the deviation of actual terminal currents from their reference values was dependent on the corresponding terminal voltage. As the deviation between current and reference is shown by the error integrator signal Q, we expected to obtain some estimate of the power mismatch by multiplying the error signals with their associated terminal voltage. This concept appeared to work fine in a simulation context. The control system circuitry is shown in Fig. 7 for the case of a three-phase to three-phase converter. The theoretical background of the control philosophy has been presented in [11] and will not be treated here.

E. Simulation of the Converter System

As has been indicated already, a computer simulation of the converter system, using the concepts mentioned above, was set up. In order to obtain an acceptable simulation speed and changeover ease a special-purpose program was written in Pascal. The basic construction of the program is much the same as the large-signal analysis reported in [2]. Key values for the operation of the resonant circuit are computed directly, assuming that terminal voltages remain constant during a resonant halfcycle. At the end of each halfcycle terminal voltages and control system parameters are updated.

V. Results

Some results of the computer simulations are shown in Figs. 8–10. A three-phase to three-phase power converter system, dimensioned for a 15-kVA power level, is simulated. Nominal input and output voltages are both 220-V rms, Y connection.

Fig. 8 shows the operation of the simulated converter system at start-up and during steady state operation. In this simulation the input of the converter is connected to a 220-V 20-Hz three-phase source, and the converter system is loaded with 10-Ω resistances in Y connection, which corresponds to full load. The output voltage reference levels are set to 220 V, 50 Hz. In Fig. 8 it can be seen that at start-up, where output voltages are zero, a large amount of charge (and power) is initially transferred to the output terminals in order to arrive at the desired output voltage level. After this relatively short phase the output voltages are closely tracking their respective reference levels.

Fig. 9 illustrates the operation of the simulated converter when a large offset current is injected in one of the input terminals. The output of the offset controller system is shown in trace L. At a simulation time of 25 ms the polarity of the offset current is inverted. Trace L shows that the offset controller system reacts accordingly in a minor fraction of the 50-Hz power frequency cycle.

As a last example of the operation of the control system Fig. 10 shows the operation with step-wise load and frequency changes. After start-up of the converter system at full load (10 Ω), at a simulation time of 10 ms the load is changed to half (20 Ω). Trace M in Fig. 10 shows the output of the power controller, whose response resembles a typical second-order

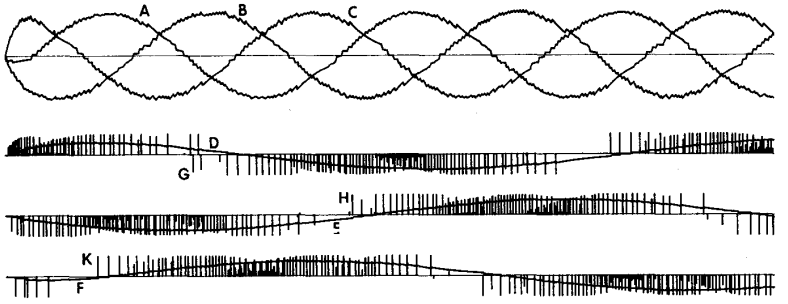

Fig. 8. Simulation of the converter system at start-up and during steady-state operation. Traces *A*, *B*, *C*: output voltages, traces *D*, *E*, *F*: filtered input currents, traces *G*, *H*, *K*: unfiltered input currents. Simulation time runs from 0 to 50 ms.

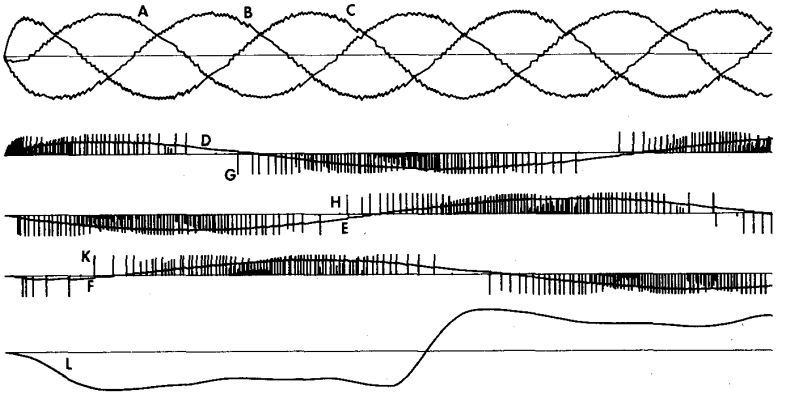

Fig. 9. Simulation of the converter system with large offset current injection showing operation of the offset controller. Trace *L*: output of offset controller. Other signals as in Fig. 8.

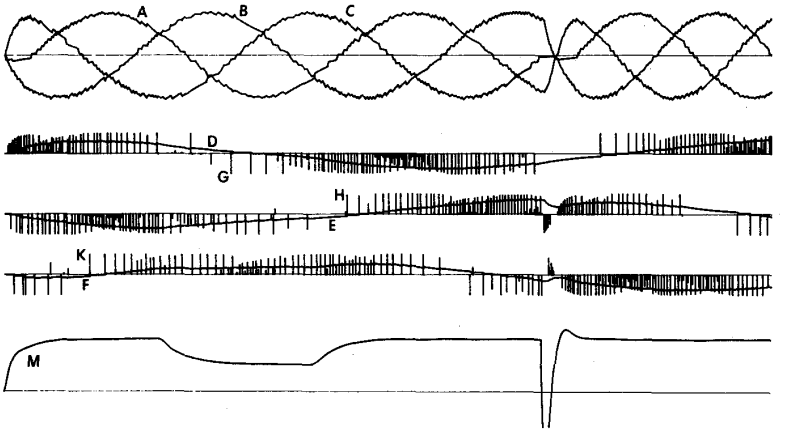

Fig. 10. Simulation of the converter system with step-wise changes in loading, output frequency, and phase. Trace *M*: output of power controller. Other signals as in Fig. 8.

control system. Traces *D* - *F* show the response of the input currents, which in a fraction of a grid frequency cycle are adjusted to their new levels. At a simulation time of 20 ms full load is restored.

At a simulation time of 35 ms in Fig. 10 a step-wise change in output frequency and phase is ordered. The output voltages, which are shown in traces *A*–*C* and the output of the power controller in trace *M*, show the typical operation of the control system. Immediately after the change in reference levels, the voltages at the output terminals are changed to their new values. As this change assumes a rapid discharge/charge action of the output filter capacitors, a large transient in the power controller signal is induced. However, no stability problems are encountered.

Conclusions

A novel control scheme is presented that fully exploits the capabilities of HF power converters and facilitates the

extraction of currents at a unity power factor from the supply side, even under transient conditions.

The control scheme takes into account losses and inaccuracies in the control electronics without deteriorating the intended waveforms.

Through computer simulations it has been shown that, in particular, the input current wave shapes are drastically improved compared to the state-of-the-art.

The controller system generates current references that do comply with both Kirchhoff's current conservation law and the energy conservation law.

The control scheme is indispensible for converters that need current references for the generation of pulse patterns.

Furthermore, it opens up the way to constructing HF power converters having optimal power factors, closely approaching 1, on both the source and load sides.

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