A Three-Phase to Three-Phase Series-Resonant Power Converter With Optimal Input Current Waveforms. Part II: Application and Results

HENK HUISMAN

Abstract—**A 15-kw three-phase to three-phase prototype series-resonant power converter is constructed. The converter features sinusoidal output voltage and sinusoidal input currents. The control concept and necessary electronics, as well as the layout of the power circuit, are discussed. Measurement results show that low distortion levels are achieved for both the output voltages and the input currents. Measurements show the very fast (in milliseconds) reaction capabilities of this type of equipment.**

I. Introduction

CONVERSION of multiphase power to multiphase power has for a long time been generally judged as one of the most complicated issues in the field of power electronics. Switch operation in converting equipment interfacing two or more asynchronous multiphase ac grids appears to be very complicated, to say the least. Only for a limited number of power circuit topologies does an analytical approach to the problem of switch operation appear to be possible. By now the theory concerning "classical" cycloconverter equipment is well known [1], [2]. Operation of this kind of equipment, however, is possible only in a restricted range of frequencies, and the apparatus turns out to be bulky because of the large low-frequency filters required. Theoretically, however, a three-phase to three-phase ac power converter, which is the most common member of the multiphase converter family, would not need bulky energy storage devices. In such a power converter, loaded symmetrically, the total power flow would be constant in time.

This paper describes the physical implementation of a series-resonant (SR) ac to ac multiphase power converter. The control concept for this converter has been presented in a companion paper [3], and we will assume throughout this paper that the reader is acquainted with its contents.

The paper starts with an overview of the control electronics needed for the operation of the power circuit. Following this, attention is given to several critical parts of these electronics, and to the physical layout and construction of the power circuit.

The second part of the paper is concerned with the actual operating characteristics of the converter system. Some typical waveforms are shown, together with data concerning distortion.

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The author is with the Laboratory for Power Electronics, Department of Electrical Engineering, Delft University of Technology, P. O. Box 5031, 2600 GA Delft, The Netherlands.

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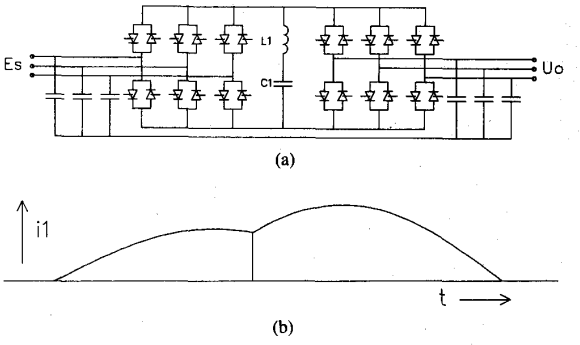


Fig. 1. (a) Power circuit of the converter. (b) One halfcycle of resonant current in the power circuit.

II. Overview of the Control Electronics

In a very general sense, the control electronics of any electrical power converter should

1) control the power circuit in order to obtain desired operation
2) protect the power circuit against overload conditions

In a practical implementation of any control system, however, these two functions often cannot be clearly distinguished.

This applies to the system to be presented here too. Many elements of the protection scheme are implemented in a diffuse manner in all parts of the control electronics. Therefore, we will not treat the functions of control and protection as separate entities. The operation of the control electronics will be discussed with reference to Fig. 1(a) and (b). Note that, where appropriate, instead of the three-phase to three-phase converter we will discuss the more general case of an n-phase to m-phase power converter. The control system presented is intended to be capable of handling any converter system with a total number of terminals $(n + m)$ greater than 2.

Operation of the converter system is started when the ASDTIC subsystem generates a signal indicating that a current flow is needed in one or more terminals of the power circuit. When this signal is detected, a procedure is started in order to obtain a "working set" of three terminals that together can be switched to generate a resonant current pulse. This implies

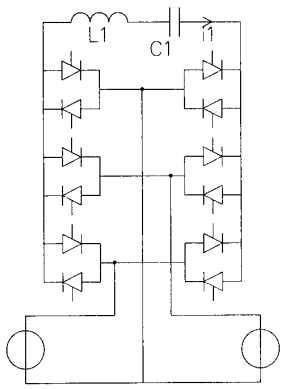


Fig. 2. Representation of the active power circuit after terminal selection.

that the remaining $(n + m - 3)$ terminals of the power circuit will not be serviced by this particular resonant halfcycle. The selection criteria are explained more fully in [3]. If a working set is obtained, we are left with a virtual three-terminal power circuit, as indicated in Fig. 2.

The thyristor switches to be fired for the first current interval can be defined from the polarities of the voltages and current reference signals. After these switches are fired, current for the first segment starts to flow, and operation of the *Vc*peak predictor circuit is started. When at a certain instant the predictor circuit indicates that the time has come to switch over to the second current segment, the thyristor for this segment is fired, thereby automatically turning off one of the "first segment" thyristors. At the end of the second segment, when the resonant current returns to zero, the thyristors turn off, and after a device-dependent turnoff time tq the whole process can be repeated. In Fig. 3 the whole process is depicted in a state diagram. Note that some additional measures have been taken for the condition in which the *Vc*peak-predictor signal doesn't show up. From the state diagram we can conclude that we will need at least the following electronic functions:

A. a measurement of turn-off time
B. a current control circuit
C. a terminal selector circuit
D. logic to decode the thyristor switches to be fired
E. a *Vc*peak-predictor circuit
F. a current zero detector
G. measurements of terminal currents and voltages

All of these functions are active on a halfcycle by halfcycle basis. Referring to [3] we will also need at least two controllers that operate on a larger time scale. These are

H. an offset controller
I. a power controller

The actions of these subcircuits are supervised by means of a digital control circuit, which closely follows the state diagram depicted in Fig. 3. The practical implementation of the subcircuits will be discussed in the following sections.

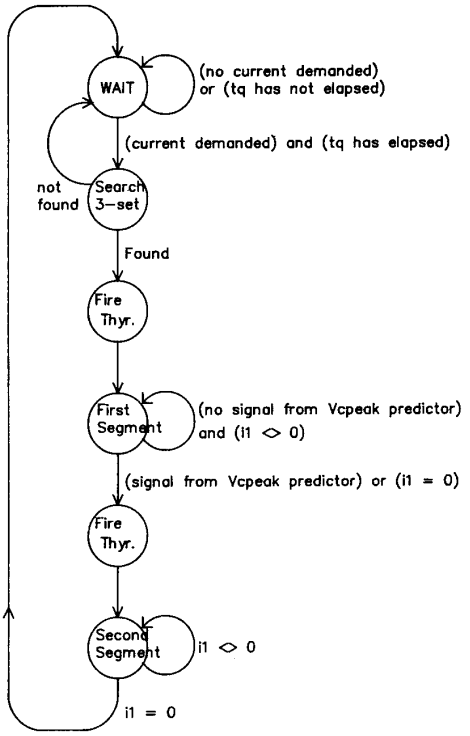


Fig. 3. State diagram representing the operation of the digital control electronics of the converter system.

III. Measurement of Turn-Off Time (A)

Turnoff time (tq) is measured in order to guarantee that thyristors that have been conducting are turned off properly before forward voltage is applied again. The circuit consists mainly of a digital flip-flop which is set when a gate pulse is applied to the thyristor, and reset when the thyristor anode has been negative with respect to the cathode for a time longer than tq. The outputs of all $4*(n + m)$ flip-flops are combined in order to obtain a signal that is used in the digital control circuit.

IV. Current Control Circuit (B)

The current control circuit is divided into two main sections. First, there is an identical controller for each of the $(m + n)$ individual terminals of the power circuit, which serves the current or voltage control for that particular terminal. Second, the error signals of the individual terminals are combined so as to obtain a total error signal, whose digital representation is used in the digital control circuit.

The individual controllers are capable of performing either current or voltage control. When set up for the current control mode, operation is similar to a so-called ASDTIC [4] control system. The extentions to ASDTIC needed to cater to multiphase operation are discussed in [3], and will not be treated here. In order to be able to control voltage as well, another extention to the ASDTIC concept is made. This extention will be discussed with reference to Fig. 4.

In Fig. 4(a) the circuit setup for a current ASDTIC controller is shown, and Fig. 4(b) depicts the same for a

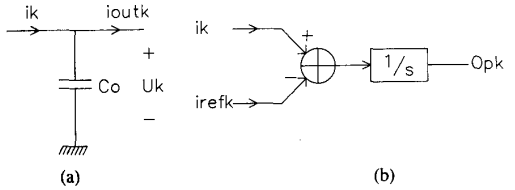


Fig. 4. Comparison of voltage ASDTIC (ripple) controller (left) and current ASDTIC controller (right).

voltage ASDTIC (ripple) controller. The outputs of the respective controllers are given by

$$Op_k = A_u \cdot (U_k(t) - U_k \text{ ref } (t))$$

$$Op_k = \frac{A_u}{C_o} \cdot \int (i_k(t) - i_k \text{ out } (t))\, dt$$

$$- A_u \cdot U_k \text{ ref} \qquad \text{for the voltage controller} \tag{1}$$

$$Op_k = \frac{Rsh}{\tau} \cdot \int (i_k(t) - i_k \text{ ref } (t))\, dt$$

$$\text{for the current controller.} \tag{2}$$

With appropriate scaling, the formulas are identical except for the second term on the right-hand side of (1). This term can be interpreted as corresponding to the charging current of the filter capacitor (Co). Note that the error signal has the same shape for both voltage and current control, and that the polarity of the error signal dictates the direction of current flow needed to decrease the error.

V. Terminal Selector Circuit (C)

Once the ASDTIC control system has signaled to the digital control circuit that a new current pulse is needed, the terminal selector circuit commences operation in order to find a "working set" of three out of the total of $(m + n)$ terminals. A "working set" is defined as a set of three terminals that together fulfill the following conditions:

1) The one terminal out of three that is to carry current in a *unique* direction carries a voltage level in between the voltages on the remaining two terminals.
2) The sum of the magnitudes of the three corresponding error signals for the working set is greater than the corresponding sum of any other set.

The theoretical background of and a software implementation for these conditions are discussed in [3]. We will zoom in on the practical implementation here.

The method used to obtain a working set is as follows. First, the error signals of all $(n + m)$ terminals are compared sequentially in order to obtain the terminals with the largest positive and negative errors, respectively. Note that this corresponds to terminals with negative and positive current flow, respectively. After obtaining these two terminals, the remaining $(n + m - 2)$ terminals are checked sequentially together with the first two for condition 1) above. If a working set is found, processing continues with firing the thyristors of the first current segment. If not, a new search is made from scratch. Note that the set found with this algorithm will not necessarily comply exactly to condition 2) above. However, it will be obvious that, in general, a close approximation to condition 2) can be reached.

TABLE I
Possible Switching Modes for the Four Thyristors Corresponding to One Terminal of the Power Circuit. A Thyristor in the Nonconducting State is Denoted as a "0", the Conducting State as "1"

Th3	Th2	Th1	Th0
0	0	0	0
0	0	0	1
0	0	1	0
0	1	0	0
1	0	0	0

VI. Decoding of Thyristor Switches (D)

Decoding of thyristor switches is implemented locally for every terminal of the power circuit. Because every terminal is associated with four thyristor switches, we need a device that will translate the signals generated during the terminal selection process to four separate signals for the individual thyristors. The main part of this decoding system is implemented as a bipolar PROM device. In order to generate "clean" gate-drive signals, the PROM outputs are latched into a set of D-flip-flops at the desired moments. In order to understand the table programmed in the PROM devices, we will first give an overview of the coding of the signals involved.

The four thyristors associated with the particular terminal can be uniquely coded by two bits, one of which ($b1$) will represent the direction of current flow in the particular terminal and the other ($b0$) the direction of current flow in the resonant circuit. In order to arrive at a compact notation, the two-bit index obtained by this method can be further reduced by substituting the decimal equivalent of the two-bit notation. From our choice for a switching mode in which only two thyristors at a time are conducting, it follows after inspection of Fig. 1(a) that a maximum of one of the four thyristors will be conducting. This observation leads us to the representation of possible switch operation in Table I.

Note that, during normal operation, the direction of the resonant current is forced by the polarity of the voltage on the resonant capacitor $C1$ (see [5]) and can be obtained easily by latching this polarity at the appropriate current zero crossing. Therefore, in order to obtain our PROM table, the only extra information needed is

1) Will a thyristor be switched on at all?
2) What is the direction of terminal current ($b1$)?

In our implementation of the control electronics, this informa-

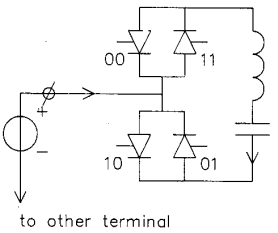


Fig. 5. One branch of thyristors corresponding to one terminal of the power circuit.

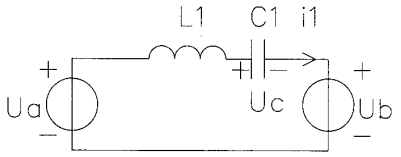


Fig. 6. Simplified power circuit model as used for the computations in the *Vc*peak-predictor.

tion can be derived from the following data:

1) Is this particular terminal chosen during the selection phase?
2) Is this the first or second current segment?
3) Of the working set, is this terminal carrying the highest, the lowest, or the middlemost voltage?
4) What is the direction of current flow as given by the error signal?

For the actual derivation we will use the general rules that have been stated in [6]

1) The first current segment will transfer energy from the resonant circuit to the outside world.
2) The second current segment will do the opposite.

An example will illustrate the application of these rules. Assume that we have obtained the following information:

1) the terminal is chosen
2) negative direction of resonant current
3) second current segment
4) highest voltage of working set
5) positive terminal current

The situation this terminal is in is depicted in Fig. 5. It can be seen that a positive current flow will indeed transfer energy to the resonant circuit, which means that during the second current segment one of the thyristors will be switched on. The actual thyristor to fire is then easily decoded to be (positive terminal current, negative resonant current) = = ($b1$ = 1, $b0$ = 0) = = Thyristor 2.

Applying the rules for all combinations of input signals (which, happily enough, can be automated to some extent) will generate our PROM table.

VII. *Vc*PEAK-PREDICTOR (E)

In order to obtain smooth operation of the whole converter circuit, it is desirable to be able to control the value of the peak voltage on the resonant capacitor at a predescribed level [6]. This can be achieved by controlling the instant of turnover from the first current segment to the second. The function of the *Vc*peak-predictor circuit is to generate a signal that indicates this particular instant. The prediction technique is based on a simplified model of the power circuit, which is presented in Fig. 6. The circuit in Fig. 6 can represent the power circuit for either the first or the second current segment, where for the sake of argument the filter capacitors are represented by ideal voltage sources. If the voltages Ua and Ub and the initial values of state variables $i1$ and u_c are known, the development of the circuit in time can be computed by using the tools of network analysis. The necessary computations have been presented in [6] and will not be repeated here. They lead to the following fundamental equation for the predicted capacitor voltage:

$$V_{cpred} = U_{a2} - U_{b2} + \sqrt{\frac{L_1}{C_1} \cdot i_1^2 + (U_{a2} - U_{b2} - U_c)^2} \quad (3)$$

where U_{a2} and U_{b2} designate the values of U_a and U_b during the second current segment.

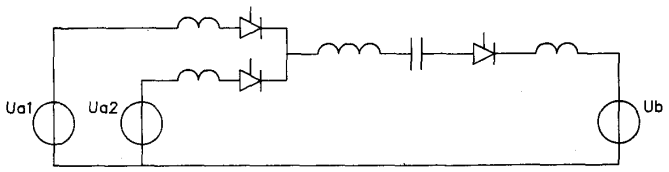
The application of the technique would be straightforward for a converter system that would be considerate enough to conform to our idealized model. However, some years of experience in the application of the technique have shown that some refinements may need to be implemented in a particular application. The main sources of deviation are

1) The model does not include losses in the power circuit. As a result, the peak capacitor voltage will be slightly below the set point of the predictor. This deviation can be diminished by adding an "effective voltage loss" at the appropriate place in the predictor circuit.

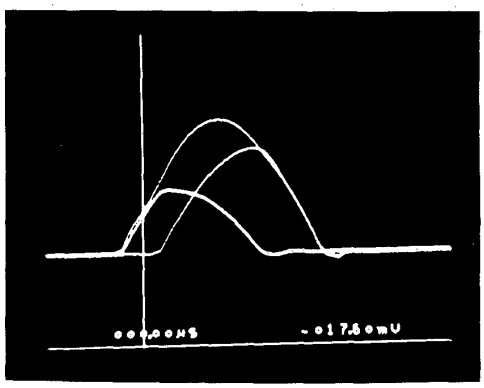
2) The model does not take the voltage ripple at the terminals of the power circuit into account. It can be shown that this deviation can be eliminated by making slight adjustments to the scaling factors of the capacitor and terminal voltages.

3) Because of delays in the control electronics and (especially) in the turn-on of the thyristor switches, the real start of the second current segment can be up to several microseconds later than the moment indicated by the predictor circuit. This leads, like 1) above, to a peak capacitor voltage below the set point. A countermeasure could be to raise the set point a little. However, the deviation introduced by the delay is dependent on a myriad of parameters, and it is hard to prove whether such a countermeasure would not lead to too high a capacitor voltage at some operating point.

4) In reality, turnover from the first to the second current segment does not take place instantly, but is intentionally delayed by the introduction of commutation inductances. This means that a middle current segment is introduced, where three thyristors are conducting simultaneously. The schematic of this particular situation is given in Fig. 7(a). Currents in the circuit branches are shown in Fig. 7(b). During the middle current segment both the voltage on the left-hand side of the model in Fig. 7(a) and the circuit impedance are changed. Although we cannot state this with certainty, simulations suggest that the peak capacitor voltage will, again, always arrive below its set point.



(a)



(b)

Fig. 7. (a) Representation of the power circuit during commutation from the first to the second current segment and (b) current waveforms through the three thyristors involved.

In spite of these deviations from the set point we have experienced that a scrupulously designed and well-trimmed *Vc*peak-predictor circuit can maintain the peak capacitor voltage between quite narrow margins. Results of the actual implementation will be shown in the section on measurements.

VIII. Current Zero Detector (F)

The function of the current zero detector is to generate an indication whenever the value of the resonant current $i1$ arrives in a small window area around zero. This indication is used by the digital control system to denote that either the first or the second current segment is finished.

IX. Offset Controller (H)

In an ideal converter system, where the sum of all current reference signals is set to zero and the error integrators are initialized to zero at start-up, the sum of all error integrator signals would remain at zero during operation. However, because of scaling errors, limited voltage range, and offsets, in a real converter system the sum of the integrator signals will soon deviate substantially from zero, which disturbs the functioning of the control mechanism. The problem and the solution to it are described more fully in [3]. In this converter system we have decided to correct current reference signals for the input terminals only.

X. Power Controller (I)

The power controller is a subsystem that is used to calculate input current reference signals that lead to an input power factor of 1. The amplitude of these reference signals is adjusted to the actual power demand. The background of the system has been discussed in [3] and will not be treated here. The power controller presented in [3] has been extended in order to provide for some phase shift at the input terminals as well. To the set of input current reference signals another set is added. This second set provides for reactive current only, and does not influence the basic operation of the power controller system. For a three-phase input the second set can be constructed in the following way:

$$I\,\text{ref}\,r2 = G * (Us - Ut)$$

$$I\,\text{ref}\,s2 = G * (Ut - Ur)$$

$$I\,\text{ref}\,t2 = G * (Ur - Us)$$

where G is a constant with the dimension of a conductance, which we have implemented with a potentiometer. Note that G can be either positive or negative (or zero). One polarity of G is associated with capacitive-type behavior, and the other with inductive-type. The polarity to correspond to either type depends on the phase sequence of the three-phase grid. It can be computed easily that the real power associated with this set is zero. Note that we could even draw "reactive" current from a three-phase dc grid. Clearly, our normal definitions concerning what is "reactive" (and "real") do not cover this situation. We will not discuss the matter any further, but refer to some recent work that describes the state of the discussion [7]–[12].

XI. The Power Circuit

In this section we will discuss the dimensioning of the power circuit and its physical layout, and present some results of the operation of the circuit.

One of the major decisions in designing a power electronics circuit lies in the choice of the semiconductor switches. The desired power (ca. 15 kW) and voltage (380 V rms, 50 Hz, three-phase) levels indicate that thyristor switches probably would be the most practical devices. After some research and calculations we decided to opt for the type SKFT 110/10 DS, which is a two-thyristor module with an isolated baseplate. Both the isolation and module features are extremely helpful when constructing a prototype converter system.

The simulations presented in [3] has provided some further insight with respect to the actual stresses on the semiconductors. Most of the design of the power circuit has been founded on worst-case values for current and voltage, which could be present when it is used as a dc to dc converter. This design method is somewhat conservative for the type of (ac to ac) operation the converter normally would be used in, but it has provided us with a rugged experimentation tool.

Some of the basic design decisions are as follows:

1) The peak capacitor voltage has to be higher than the worst-case terminal-to-terminal voltage. The latter can be computed to be 620 V, which is two times the peak value of a phase-to-neutral voltage. In order to obtain the lowest possible voltage level on the thyristors, we have set the peak capacitor voltage to 730 V. This leaves us a worst-case margin of 110 V for turning off the thyristors. On the other hand, the voltage that the thyristors need to block in a symmetrical configuration then would be $0.5*(Vc\text{peak} + 620) = 675$ V. This value can (and will) be exceeded because of asymmetries, leakage, and overshoot. However, as the voltage rating of the thyristors used is 1000 V, we obtain an adequate safety margin.

2) With this peak capacitor voltage the values of the resonant capacitor and inductance can be obtained by simulation. The simulation [3] provided the following values:

$$C1 = 4 \text{ uF}$$

$$L1 = 63 \text{ uH}.$$

The worst-case stresses on these components can be computed quite easily for the dc-dc conversion case and were found to be

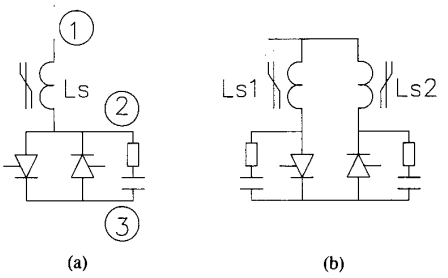
$$i1 \text{ rms} = 109 \text{ A}.$$

$$i1 \text{ peak} = 176 \text{ A}.$$

Note that the current/uF ratio for the resonant capacitor $C1$ is quite high. We were lucky to find some newly developed types that could successfully withstand this load.

3) A major problem in the design of any thyristor power circuit is to restrict both di/dt and dV/dt values for thyristors to a predictible maximum. Usually the maximum value of dV/dt is set by using an $R/L/C$ snubber combination, as indicated in Fig. 8(a). This second-order network will transform a voltage step occurring between nodes 1 and 3 to a voltage rise with predictable slope between nodes 2 and 3. Inductor Ls generally needs to be of a saturating type because otherwise its presence would interfere too much with the basic operation mode of the converter system. It has to be noted that for a working design the (voltage-dependent) thyristor (junction) capacitances need to be taken into account.

A complication arises because of a nasty interference of the reverse-recovery current of one thyristor with the operation of the snubber network of its neighbor in Fig. 8(a). The peak of the reverse-recovery current easily could be high enough to drive the snubber inductance Ls close to or into saturation, ruining the performance of the snubber altogether. One designer's solution to this interference could be to keep the reverse-recovery current peak very low. The only design parameter that allows this peak value to be manipulated (with every other parameter already being set) is the slope of the current before turn-off of the thyristor. Therefore, we started to tackle the problem by specifying very large (15 uH on a total resonant inductance of 63 uH) commutation inductances. We observed that the reverse-recovery peak would be kept low indeed, but also that the actual value of the peak, being very device-dependent, is hard to predict and very dependent on operating temperature.



(a) (b)

Fig. 8. (a) (left) Usual snubber circuit configuration. (b) (right) Modified configuration without interference through reverse-recovery current.

Our experiments have shown that a much better way to tackle the problem is to separate the snubber inductances Ls for the two thyristors into two inductances $Ls1$ and $Ls2$, which leads to the configuration of Fig. 8(b). After this modification we found that with the same amount of magnetic material used for the Lsi the value of the dV/dt had decreased from over 1200 V/μs to a mere 200 V/μs.

The modified snubber network would allow larger values of di/dt, up to the specified limit (200 A/μs) for the thyristors. However, because of the "clean" current waveforms (see Fig. 7(b)) obtained through the thyristors, we have not changed the commutation inductances to lower values.

Because of slight asymmetries in circuit construction and device behavior and parasitic resonances in the prototype, very short (1 μs) voltage spikes rising above 1000 V were sometimes present on the thyristors. We have successfully applied VDR devices to clip these spikes near 950 V, protecting the thyristors from accidental firing.

XII. Operation of the Prototype

The operation of the prototype converter system will be illustrated by some measurement results. The measurements cover the following subjects:

1) response to a voltage step
2) response to a frequency step
3) combination of 1) and 2)
4) distortion of the output voltage
5) distortion of the input currents

The relevant signals for these five subjects are shown in Fig. 9(a)–(e), respectively.

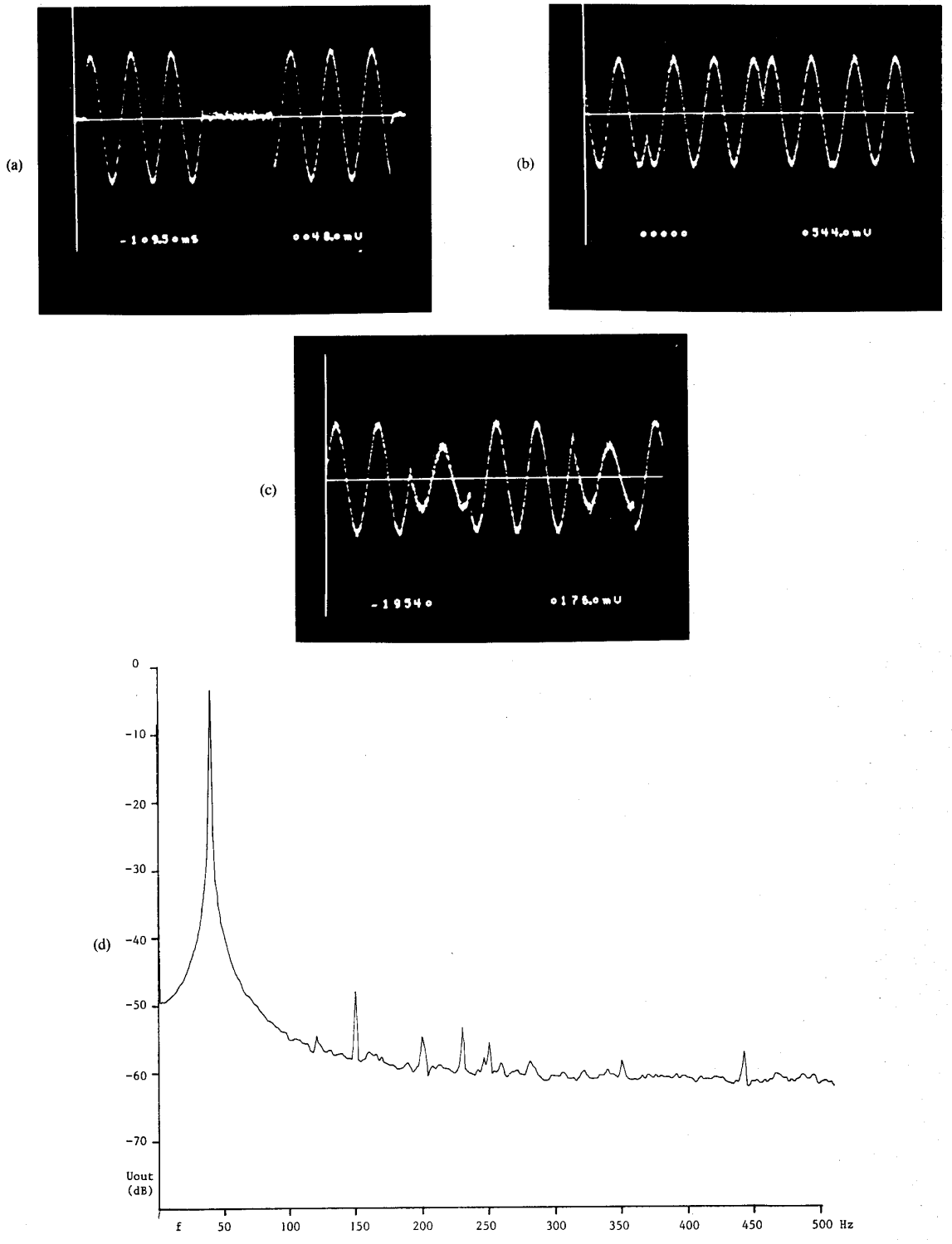


Fig. 9. (a) Response of the converter output voltage to a change in reference value. The phase voltage is switched between zero and 300-V peak; the frequency is 50 Hz. (b) Response of the converter output voltage to a change in frequency. The output frequency is switched between +20 and −20 Hz. (c) Response of the converter output voltage to a change in both frequency and amplitude. The frequency is modulated between +20 and −20 Hz (phase reversal), the amplitude of the phase voltages between 250 and 150 V. (d) Frequency spectrum of the converter output voltage. Horizontal scale: frequency, 0 to 500 Hz; Vertical scale: output voltage, 10 dB/div. (e) Frequency spectrum of the converter input current. Horizontal scale: frequency, 0 to 500 Hz; Vertical scale: input current, 10 dB/div.

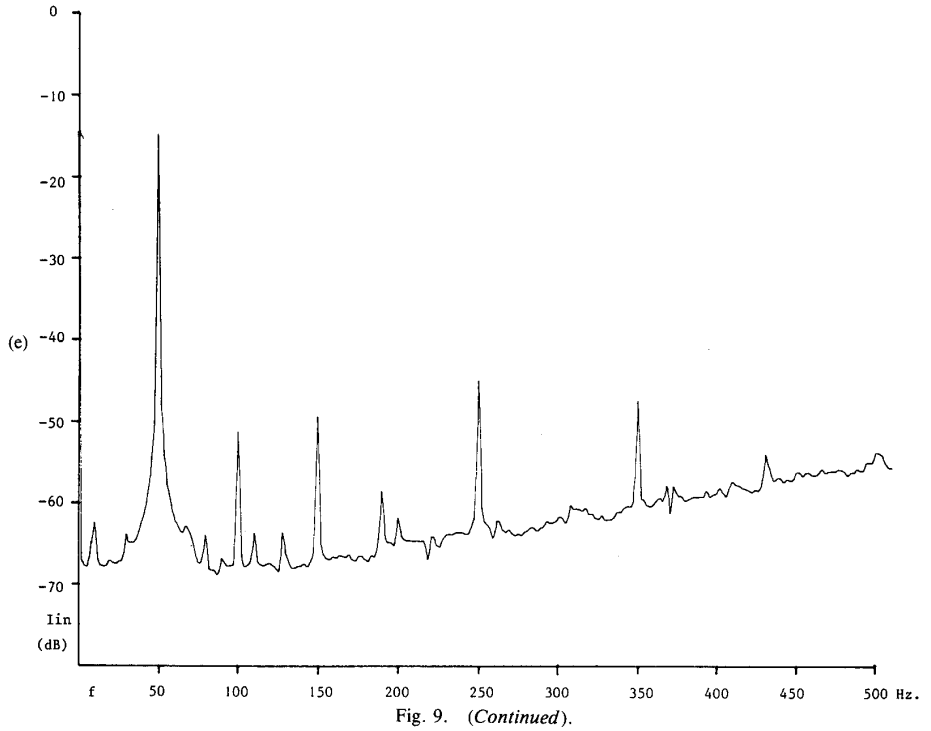


Fig. 9. (*Continued*).

Fig. 9(a) shows operation of the converter system when the output phase voltages are modulated between zero and 300-V peak, 50 Hz, at 80 percent of rated load. The figure shows the voltage between two output terminals. Clearly, the converter system is capable of reacting very quickly to these transient phenomena. The rise and fall times of the output waveforms were measured to be 1.3 ms, which is very close to the theoretical minimum.

Fig. 9(b) depicts the response of the converter output to frequency inversion. The outputs are modulated between +20 and −20 Hz (phase reversal), at a peak value of the phase voltage of 250 V.

Fig. 9(c) shows the combination of the modulation of frequency and amplitude. Here the converter outputs are switched between 250 and 150 V, at frequencies of +20 and −20 Hz, respectively. It is shown again that the converter outputs follow their reference values with high speed. The capability of fast frequency and amplitude modulation can be a very interesting feature in the field of electrical drive techniques.

Fig. 9(d) plots the frequency spectrum of 0 to 500 Hz of the voltage difference between two output terminals. The generated frequency is 40 Hz. It can be seen that major harmonics at 120 and 200 Hz, etc., as well as hum are at least 45 dB below the fundamental component.

The distortion of the input currents of the converter system, as indicated in the plot of Fig. 9(e), is substantially higher than the distortion of the output voltages. The major harmonics in the input currents all are more than 30 dB below the fundamental at 50 Hz. The higher distortion seems to be caused mainly by the undamping effect of the negative differential imput impedance of the converter system on parasitic inductances and capacitances in the utility grid.

The efficiency of the converter system was measured to be 91 percent at full load.

As a last test of the capabilities of the converter system, the input was connected to a "three-phase dc grid" composed of +110 V, −110 V, and ground. Even under this uncommon ccndition the converter was able to deliver voltage waveforms with low distortion to a load. When the "reactive" current at the input was set to zero, the ground terminal could be switched off without any change in the operation of the converter. The validity of our control method for any number of input and output terminals is supported by this observation.

XIII. Conclusions

A converter system has been presented that is capable of transforming the multiphase ac power of any frequency (including dc) and voltage between design limits to the multiphase ac power of any frequency (including dc) and voltage.

In particular, the system is capable of

1) both step-up and step-down voltage scaling
2) instantaneous phase reversal of the output voltages
3) almost instantaneous (1.3 ms) switch on/off of full output power
4) generating or absorbing reactive power at both input and output terminals
5) operation at high efficiency levels
6) generating nonsinusoidal waveforms.

A comprehensive theory, covering the general operating

characteristics of multiphase to multiphase series-resonant converters has been expanded and applied to a three-phase to three-phase design.

A novel technique, which is capable of controlling multiphase to multiphase power converters with an optimum power factor at both source and load terminals, has been applied to a 15-kW prototype.

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