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A Tightly Regulated Triple Output Asymmetrical Half Bridge Flyback Converter

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Abstract

In this paper, a tightly regulated triple output asymmetrical half bridge flyback (ASHF) converter is proposed. In order to regulate all output voltages, pulse frequency modulation (PFM), pulse width modulation (PWM) and phase delay (PD) are used simultaneously. In comparison with the conventional PWM-PD method, the interactions among the control variables are minimized and the operating range is increased. By the utilization of a multi winding transformer, the auxiliary transformer and the blocking capacitor are eliminated and the size and cost of the proposed converter is reduced. The operation principle of the converter is explained and the modes of operation are investigated. Based on the results, the steady state characteristics of the converter are explored. A 24V/10A, 12V/5A, 5V/10A hardware prototype is built and tested to verify the analysis results and the voltage regulation of the triple outputs of the proposed converter.

Key Words: Asymmetrical half bridge flyback, PFM-PWM-PD method, Triple outputs

I. INTRODUCTION

Multiple output DC/DC converters are widely used in switched-mode power supplies (SMPS) due to their competitive cost and size. In order to achieve a tightly regulated output voltage, various post regulation schemes have been proposed. Representative realizations include synchronous switch post regulation (SSPR) which utilizes an auxiliary switch, PWM-PD and PWM-PFM control, mag-amp approaches.

Among them, a multiple output converter using several control variables is advantageous in cost saving and size reduction because it operates without additional switches. A forward-flyback converter using the PWM-PFM method has been proposed [1], [2]. However, the voltage ratio between the two outputs is prefixed and the load range is highly limited.

An asymmetrical half bridge converter with PWM-PD control has been studied [3]. Although the output voltages are well regulated, the input voltage range is narrow and auxiliary circuitries are required for the third output.

In this paper, a tightly regulated triple output asymmetrical half bridge flyback converter (ASHF) is proposed. The converter is controlled by the proposed PFM-PWM-PD method and the interactions among the controllers are minimized. As a result, the input voltage and load range can be increased. In addition, the auxiliary transformer for the third output voltage in a conventional power stage is eliminated through the utilization of the multi windings from the existing transformers.

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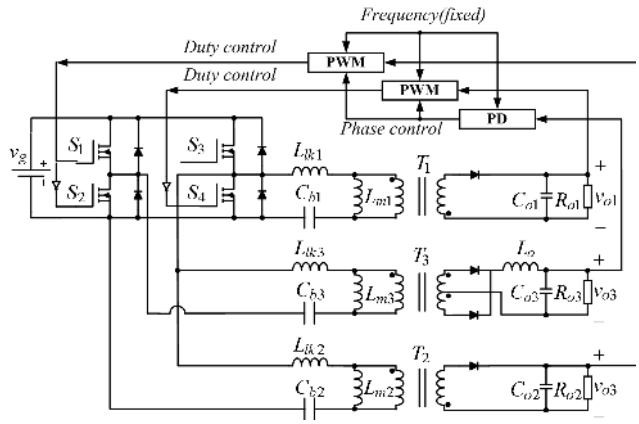
This paper is organized as follows. The circuit configuration and operation principle of the proposed converter are explained in Section 2. In Section 3, the modes of operation of the proposed converter are examined. Then the steady state characteristics such as the dc voltage gains and the interactions among the three output voltages are investigated. A 320V-400V input range, 24V/10A, 5V/10A and 12V/5A hardware prototype is built to demonstrate the performance of the proposed converter. The experimental results are illustrated in Section 4. The conclusions are summarized in Section 5.

II. OPERATING PRINCIPLE OF THE PROPOSED PFM-PWM-PD METHOD

A circuit diagram of the ASHF with the PWM-PD method referred to in [3] is shown in Fig. 1(a). The auxiliary transformer, T_3 and the blocking capacitor, C_{b3}, are required for v_{o3}. The ASHF PWM converter, which is a main topology of the proposed method, has been widely used as a front end dc/dc converter due to the following advantages: 1) clamped switch voltage to the input voltage; 2) ZVS of MOSFETs and ZCS of the rectifier diode; 3) fixed switching frequency.

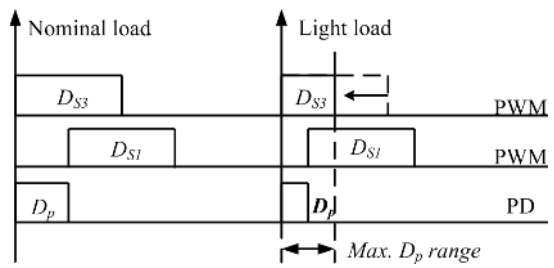
The operating principle of a conventional PWM-PD is shown in Fig. 2(a). The first and second output voltage, v_{o1} and v_{o2}, are regulated using duty ratios of S_1 (D_{S1}) and S_3 (D_{S3}) respectively. The third output voltage, v_{o3}, is controlled by the phase delay ratio (D_p) between the gate driving signals for S_1 and S_3. Since D_p is generated by the difference between D_{S1} and D_{S3}, the maximum range of D_p is dependent on the actions of v_{o1} and v_{o2}. This means the interactions among the converters are strong and the input voltage and the load range



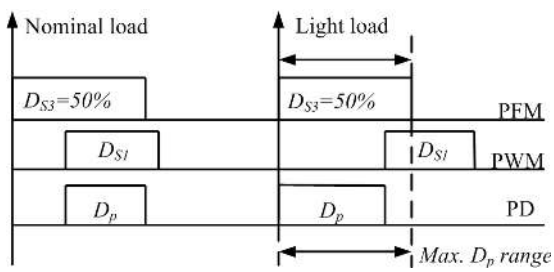
(a) The conventional ASHF converter with PWM-PD

(b) The proposed ASHF converter with PFM-PWM-PD

Fig. 1. The circuit diagram of the conventional and proposed converter.



(a) PWM-PD control scheme



(b) Proposed PFM-PWM-PD control scheme

Fig. 2. Operating principle of the proposed converter.

are limited. These problems result in an increase in the input capacitance to satisfy the hold-up requirement [4].

In the proposed ASHF converter with the PFM-PWM-PD method from Fig. 1(b), the transformer T_3 and the DC blocking capacitor C_{b3} in Fig. 1(a) are eliminated by utilizing the multi windings of the transformers, T_1 and T_2. Due to the connection of the multi windings, the voltages across the windings are similar to the conventional converter. The operating principle of the proposed converter is shown in Fig. 2(b). The PFM method is applied for the regulation of v_{o1} and its duty ratio, D_{S3}, is fixed to 50%. Thus, the maximum range for D_p is equal to D_{S3} and it is independent of the load current. To reduce the interaction, v_{o2} is controlled by the PWM method which uses D_{S1} as a control variable in this paper.

III. Steady State Characteristics of the Proposed Converter

A. Mode analysis of the proposed converter

The modes of operation of the ASHF converter with PWM control have been explained in previous studies [5]–[9]. In this paper, the operations of the proposed converter which includes a dual ASHF and a multi winding transformer are investigated. The key operating waveforms of the proposed converter are shown in Fig. 3. To simplify the analysis, the current of L_o is assumed to be constant.

M1(t_0–t_1): S_3 is turned on. The input voltage, v_g, increases the current of the magnetizing inductance, L_{m1}. Due to the dot convention in the T_1, rectifier diode, D_{rH}, is turned off. S_2 is turned on and the stored energy in C_{b2} is released to R_{o2} through L_{m2} and L_{lk2}. The equations are written as (1) and (2). The energy is transferred from v_g to v_{o3} through the multi winding of T_1 and T_2. This mode ends when S_2 is turned off.

$$\begin{aligned} i_{Llk1}(t) = {} & \frac{v_g - v_{Cb1}(t_0)}{Z_o}\sin(\omega_o t) \\ & + \left(\frac{N_{1p}v_{o3}}{N_{1t}R_{o3}} + i_{Lm1}(t_0)\right)\cos(\omega_o t) \end{aligned} \tag{1}$$

$$\begin{aligned} v_{Cb1}(t) = {} & v_{Cb1}(t_0)\cos(\omega_o t) + v_g(1-\cos(\omega_o t)) \\ & + \left(\frac{N_{1p}v_{o3}}{N_{1t}R_{o3}} + i_{Lm1}(t_0)\right)Z_o\sin(\omega_o t) \end{aligned} \tag{2}$$

where, $\omega_o = \dfrac{1}{\sqrt{(L_{lk1}+L_{m1})C_{b1}}}$, $Z_o = \sqrt{\dfrac{L_{lk1}+L_{m1}}{C_{b1}}}$

M2(t_1–t_2): The body diode of S_1 is turned on by the negative current of L_{lk2}. To achieve ZVS, S_1 is turned on during this period. Since the polarities of the voltage across L_{lk2} and L_{m2} are opposite, i_{Llk2} is increased and i_{Lm2} is decreased. Thus, the current becomes zero due to the relation of (3) and then D_{rL} is turned off softly.

$$i_{DrL}(t) = \frac{N_{2p}}{N_{2s}}(i_{Llk2}(t) - i_{Lm2}(t)) \tag{3}$$

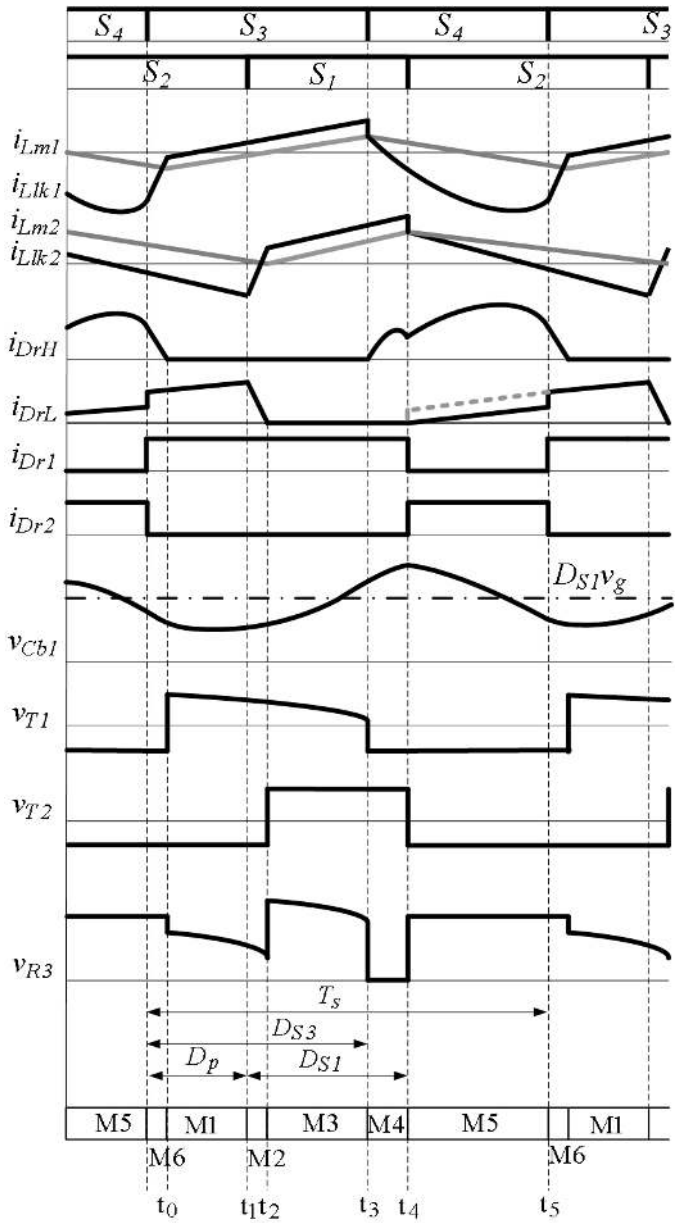


Fig. 3. The steady state waveforms of the proposed converter.

M3(t_2–t_3): i_{Lm2} is increased linearly by v_g and C_{b2} is charged through the current. The energy is transferred from v_g to v_{o3} through T_1 and T_2. The current equation of this mode is expressed in (4).

$$i_{Llk2}(t) = i_{Lm2}(t_2) + \frac{v_g - V_{Cb2}}{L_{m2} + L_{lk2}} t + \frac{N_{2p}}{N_{2t}} I_{Lo} \tag{4}$$

where, V_{Cb2} and I_{Lo} are the averaged values of C_{b1} and L_o. They are equal to $D_{S3} v_g$ and the load current of v_{o3} respectively.

M4(t_3–t_4): S_3 is turned off at t_3. The stored energy in C_{b1} is released to R_{o1} through L_{lk1}. Thus, resonance between L_{lk1} and C_{b1} starts. D_{rH} becomes conductive and the voltage across L_{m1} is clamped to the reflected v_{o1}. The current and voltage equations in this mode are defined in (5) and (6).

$$\begin{aligned} v_{Cb1}(t) &= v_{Cb1}(t_3)\cos(\omega_1 t) + i_{Llk1}(t_3) Z_1 \sin(\omega_1 t) \\ &\quad + \frac{N_{1p}}{N_{1s}} v_{o1}(1 - \cos(\omega_1 t)) \end{aligned} \tag{5}$$

$$\begin{aligned} i_{Llk1}(t) &= i_{Lm1}(t_3)\cos(\omega_1 t) \\ &\quad + \frac{\frac{N_{1p}}{N_{1s}} v_{o1} - v_{Cb1}(t_3)}{Z_1} \sin(\omega_1 t) \end{aligned} \tag{6}$$

where, $\omega_1 = \dfrac{1}{\sqrt{L_{lk1} C_{b1}}}$, $Z_1 = \sqrt{\dfrac{L_{lk1}}{C_{b1}}}$.

To achieve the monotonic slope in voltage gain for v_{o3} with respect to D_p, the turns ratios of T_1 and T_2 should be designed so that the voltage summation of v_{T1} and v_{T2} becomes almost zero during this period. Current commutation occurs in the rectifiers for v_{o3} due to a low v_{R3}. Thus, the current of the tertiary winding in T_1 is reflected to the secondary winding and it is added to the reflected current from the primary winding. The increased i_{DrH} during this mode is marked in Fig. 3.

M5(t_4–t_5): The body diode of S_2 is turned on by the positive current of L_{lk2} and L_{m2}. The stored energy in C_{b2} is released to R_{o2} and i_{Llk2} is linearly decreased because v_{Cb2} is constant. D_{rL} conducts and L_{m2} is reset by the reflected v_{o2}. Thus, i_{Lm2} is also decreased linearly. The current difference between i_{Llk2} and i_{Lm2} flows to the load. The current equation of this mode is given by:

$$i_{Llk2}(t) = i_{Lm2}(t_4) - \frac{V_{Cb2}}{L_{m2} + L_{lk2}} t \tag{7}$$

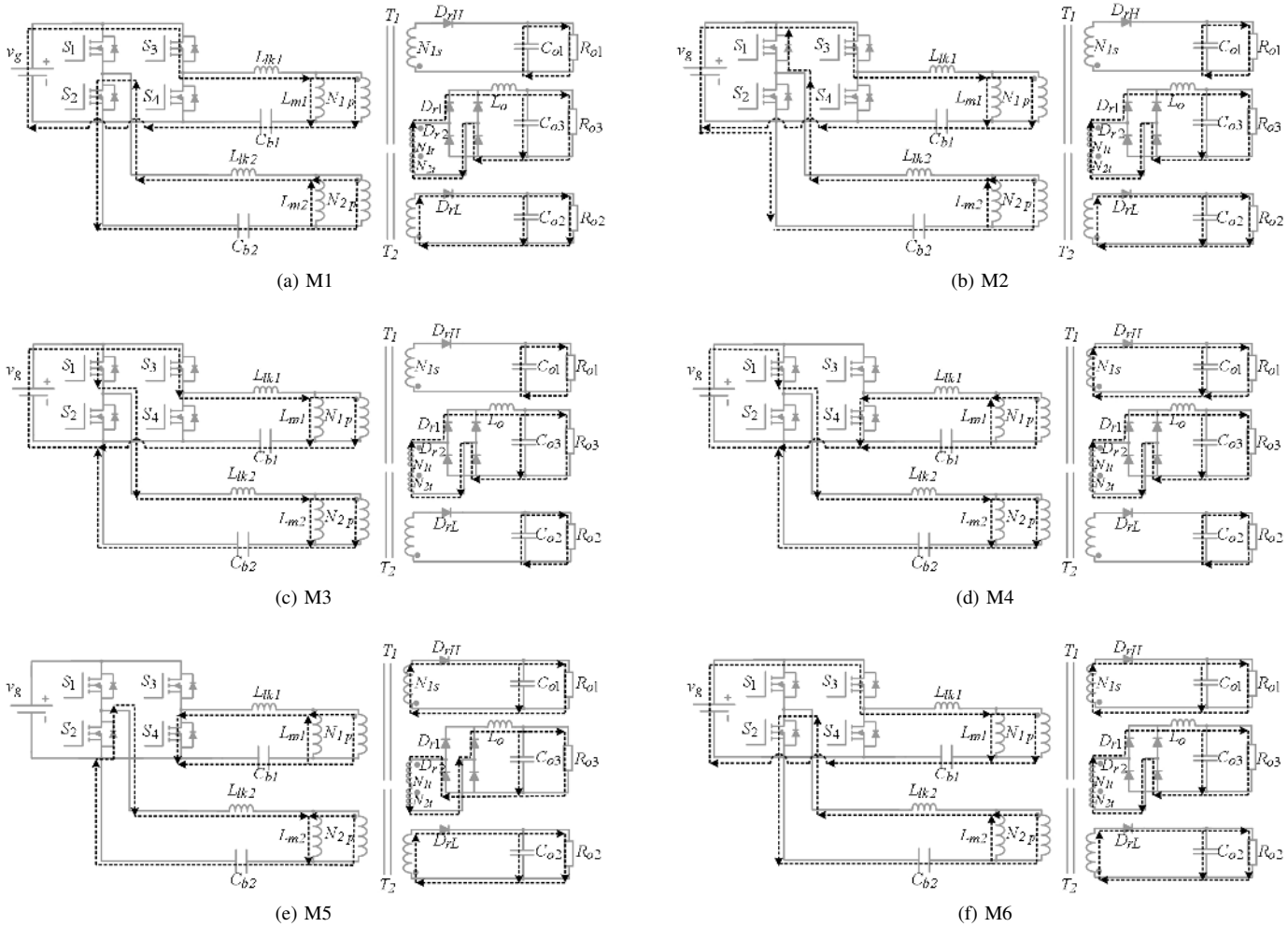
Due to the dot convention, the current relation in T_2 is expressed as (8). Thus, the reflected dc current of I_{Lo} is subtracted from the reflected current of the primary winding of T_2.

$$i_{DrL} = \frac{1}{N_{2t}} \left(N_{2p}(i_{Llk2} - i_{Lm2}) - N_{2s} I_{Lo} \right) \tag{8}$$

M6(t_5–t_6): S_4 is turned off and the body diode of S_3 conducts. Due to the positive voltage across L_{lk1}, the current is increased while the current of L_{m1} is decreased by the reflected v_{o2}. When the two currents meet, D_{rH} is turned off softly due to the similar relation of (3).

B. Voltage gains of the proposed converter

The voltage gain of v_{o1} according to the switching frequency can be found from the modes of operation. To simplify the explanation, the transition modes, M2 and M6, are neglected because the time duration of these modes is much shorter than the switching period. Derivation of the voltage gain is similar to the LLC resonant converter case except that the resonant elements of the proposed converter only store the energy from the input voltage during $D_{S1} T_s$. The resonant frequency of this period which is defined in (1) and (2) is used. The usage of the half wave rectifier is also considered.



(a) M1 (b) M2 (c) M3 (d) M4 (e) M5 (f) M6

Fig. 4. The modes of operation of the proposed converter.

The voltage gain for v_{o1} is expressed as (9).

$$M_1 = \frac{v_{o1}}{v_g} = \frac{2N_{s1}\sin\left(\frac{\pi D_{S3}}{2}\right)}{N_{p1}\sqrt{\left(\frac{k_1+1}{k_1}-\frac{1}{{\omega_n}^2}\right)^2+Q^2\left(\frac{1}{\omega_n}-\omega_n\right)^2}} \quad (9)$$

$$Q=\frac{Z_2}{R_{ac}},\ R_{ac}=\frac{4R_{o1}{N_{p1}}^2}{\pi^2{N_{s1}}^2},\ k_1=\frac{L_{lk1}}{L_{m1}},\ \omega_n=\frac{\omega_s}{\omega_2}$$
$$Z_2=\sqrt{\frac{L_{m1}}{C_{b1}}},\ \omega_2=\frac{1}{\sqrt{L_{m1}C_{b1}}},\ k_2=\frac{L_{lk2}}{L_{m2}} \quad (10)$$

where, ω_2 is the modified resonant frequency, Z_2 is the modified characteristics impedance, ω_n is the normalized switching frequency, Q is the quality factor, R_{ac} is the reflected load resistance to the primary side of T_1 while k_1 and k_2 are the inductance ratios between the magnetizing and resonant inductance. The obtained voltage gain for v_{o1} is compared with the results of the circuit simulation. The PLECS toolbox in MATLAB with a practical switching circuit model is utilized. It shows that the simplified analytical voltage gain function is good enough to obtain the initial design strategies for all load conditions.

The voltage gain for v_{o2} was found in previous studies [5]–[9] because it is controlled by the PWM method. Due to the inductive output filter in Fig. 1(b), the averaged value of the rectified voltage, v_{R3}, is the same as v_{o3}. To find out the relation between v_{o3} and D_p, the waveforms in Fig. 3 are used. For the steady state voltage gain, the average value of v_{Cb1} is used to obtain a simple design equation.

$$v_{Cb1} \cong D_{S3} v_g \quad (11)$$

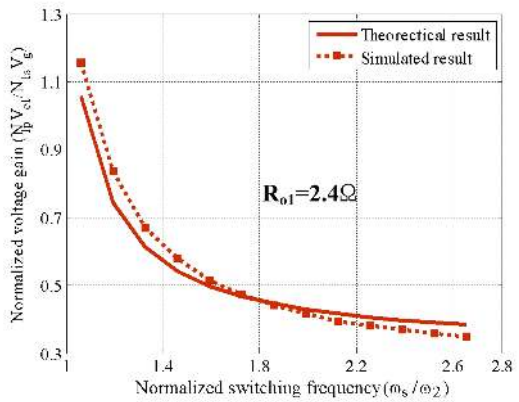
The winding voltages of the primary side in T_1 and T_2 through the multi windings are summarized in Table 1. Applying (11), the gains for the other output voltages in fixed switching frequency can be approximated.

$$\frac{V_{o1}}{v_g} \cong \alpha\frac{N_{1s}}{N_{1p}}D_{S3},\ \frac{V_{o2}}{v_g} \cong \frac{N_{2s}}{N_{2p}}D_{S1} \quad (12)$$

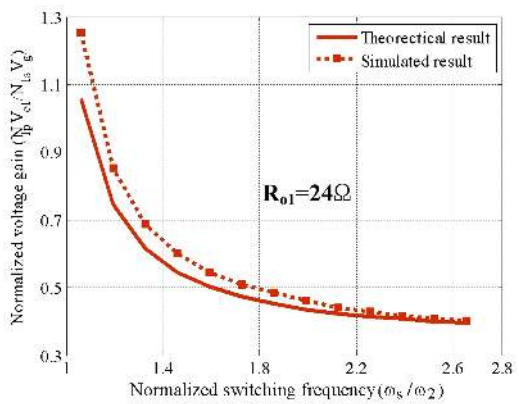
The compensation factor, α, should be multiplied because the voltage gain for v_{o1} is affected by the switching frequency and α is obtained from the gain curve in Fig. 5. v_{o3} is calculated by the averaged value listed in Table 1. The approximated voltage gain is shown in Fig. 6. The slope of the voltage gain becomes zero when D_p is less than $(D_{S3}-D_{S1})$. This means

TABLE I
RECTIFIED WINDING VOLTAGE (v_{R3}) AND OPERATING MODE

$D_{S3} \leq D_{S1} + D_p$			$D_{S3} > D_{S1} + D_p$		
mode	v_{R3}	time duration	mode	v_{R3}	time duration
M5	$\left\lvert -\frac{N_{1t}}{N_{1s}} v_{o1} - \frac{N_{2t}}{N_{2s}} v_{o2} \right\rvert$	$(1 - D_{S3})$ $-(D_{S1} + D_p - D_{S3})$	M5	$\left\lvert -\frac{N_{1t}}{N_{1s}} v_{o1} - \frac{N_{2t}}{N_{2s}} v_{o2} \right\rvert$	$(1 - D_{S3})$
M1	$\left\lvert \frac{N_{1t}(1-D_{S3})v_g}{N_{1p}(1+k_1)} - \frac{N_{2t}}{N_{2s}} v_{o2} \right\rvert$	D_p	M1	$\left\lvert \frac{N_{1t}(1-D_{S3})v_g}{N_{1p}(1+k_1)} - \frac{N_{2t}}{N_{2s}} v_{o2} \right\rvert$	D_p
M3	$\left\lvert \frac{N_{1t}(1-D_{S3})v_g}{N_{1p}(1+k_1)} + \frac{N_{2t}(1-D_{S1})v_g}{N_{2p}(1+k_2)} \right\rvert$	$D_{S3} - D_p$	M3	$\left\lvert \frac{N_{1t}(1-D_{S3})v_g}{N_{1p}(1+k_1)} + \frac{N_{2t}(1-D_{S1})v_g}{N_{2p}(1+k_2)} \right\rvert$	D_{S1}
M4	$\left\lvert -\frac{N_{1t}}{N_{1s}} v_{o1} + \frac{N_{2t}(1-D_{S1})v_g}{N_{2p}(1+k_2)} \right\rvert$	$D_{S1} + D_p - D_{S3}$	M4	$\left\lvert \frac{N_{1t}(1-D_{S3})v_g}{N_{1p}(1+k_1)} - \frac{N_{2t}}{N_{2s}} v_{o2} \right\rvert$	D_{S3} $-(D_{S1} + D_p)$



(a) Voltage gain @ $R_{o1} = 2.4\Omega$



(b) Voltage gain @ $R_{o1} = 24\Omega$

Fig. 5. Gain comparison between the model in (9) and Switching circuit simulation.

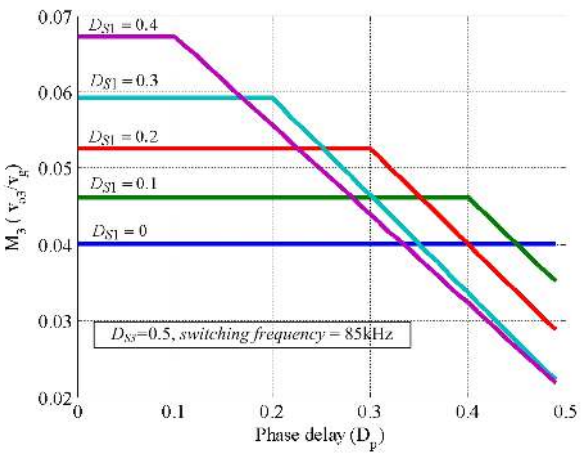


Fig. 6. Approximated gain curve for v_{o3} according to D_{S1} and D_p.

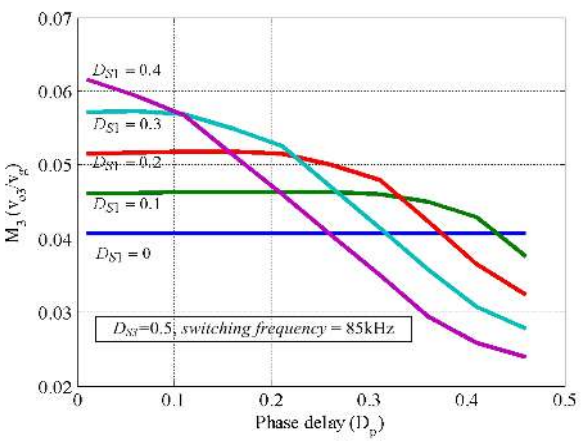


Fig. 7. Simulated gain curve for v_{o3} according to D_{S1} and D_p.

that the effect of a phase delay occurs within the overlapped area between D_{S3} and D_{S1}. Also, the operating range of D_p is limited by D_{S3}. Thus, the minimum for D_{S1} is required to prevent abnormal operation.

To verify the analytical gain function, the voltage gain for v_{o3} is obtained through the switching circuit simulation as shown in Fig. 7. The gain difference between the analytical and simulated result is small when D_{S1} is low, but as D_{S1} increases, the error becomes large. However, the approximated gain curve can be used in the initial design process.

The interactions between the three output controls are investigated. The effects of D_{S1} and D_p in v_{o1} (M_1) are illustrated in Fig. 8. When f_s=120kHz and f_s = 150kHz, almost no variations are observed (flat planes). This means the variations according to D_{S1} and D_p variances are negligible during operation. Although a small variation is observed in the low switching frequency (85kHz), it is less than 0.01.

The effects of D_p and f_s in v_{o2} (M_2) are shown in Fig. 9. It is observed that M_2 is not affected by the variation of D_p and f_s when D_{S1} = 0 and 0.2. In the case of D_{S1} = 0.4, the

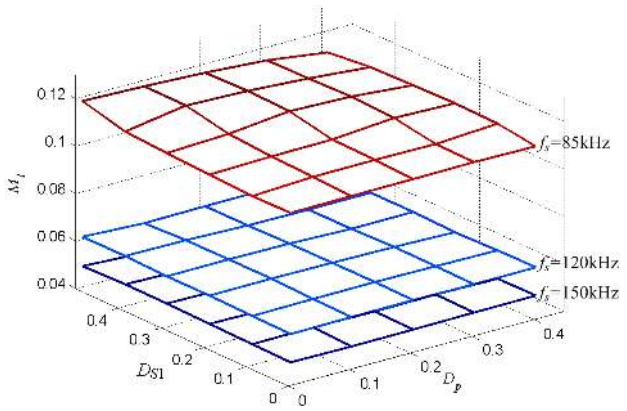


Fig. 8. The interactions of D_{S1} and D_p to M_1.

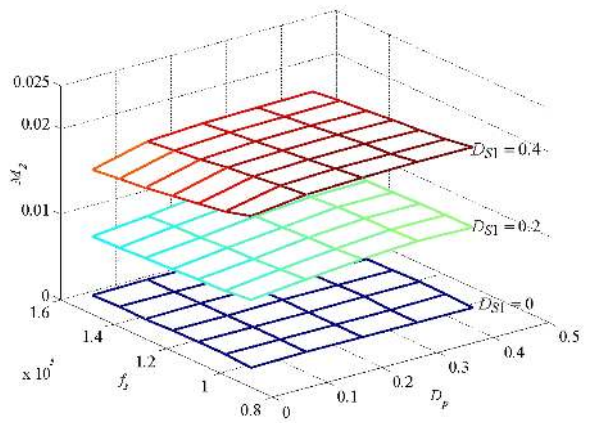


Fig. 9. The interactions of f_s and D_p to M_2.

variation is less than 0.005.

From the results, the interactions among the control variables are small in the PFM-PWM-PD method. Therefore the input and load range can be widened.

IV. Experimental Verification

In this section, a hardware prototype is built and tested to verify the analysis results and to demonstrate the voltage regulation of the three output voltages in the proposed converter. The designed circuit parameters are listed in Table 2. T_1 is manufactured using the sectional winding technique in [10]. The leakage inductance of T_1 is utilized as a series resonant inductor. A small size output filter inductor using a bar type ferrite core is applied to L_o.

To verify the output voltage regulation of the proposed converter three feedback loops with a dsPIC33FJ16GS502 are implemented. The steady state waveforms under 380V of input voltage are shown in Fig. 10. The waveforms and phase delay are similar to the analysis results in Fig. 3.

The experimental dc voltage gain for v_{o3} is measured and shown in Fig. 12. The curves show good agreement with the result in Fig. 7.

TABLE II
The Parameters of the Proposed Converter

Device	Value	Device	Value
c_{o1}	6mF	$N_{1p} : N_{1s} : N_{1t}$	17:2:1
c_{o2}	13.2mF	$N_{2p} : N_{2s} : N_{2t}$	42:3:3
c_{o3}	1.5mF	L_{m1}/L_{lk1}	135uH/45uH
T_1	EER4950s	L_{m2}/L_{lk2}	300uH/50uH
T_2	EER3542s	L_o	3.3uH
MOSFET	FQA18N60	Core forL_{lk2}	EI20
Diode	KCH30A10	C_{b1}	33nF
f_s(kHz)	80 – 140	C_{b2}	1uF
Core forL_o	Bar core (φ = 6]mm, l = 35mm)		

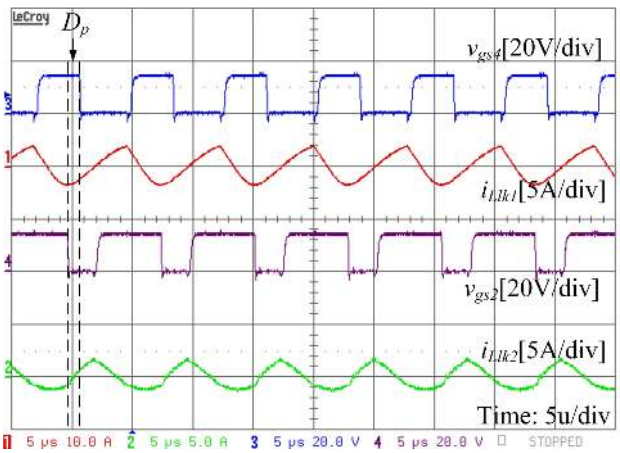
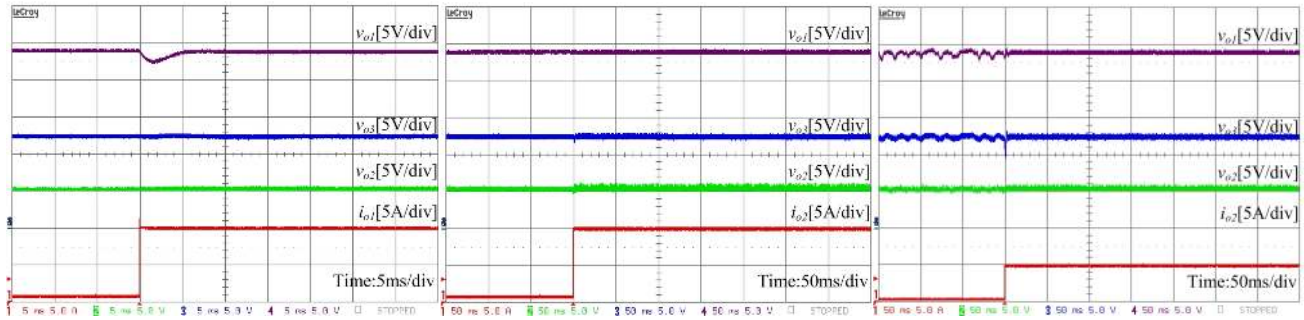


Fig. 10. The steady state waveforms under @v_g = 380V, full load.

The results of the output voltage regulation are illustrated in Fig. 11. The load current is changed from 10% to 100%. For the step load change of i_{o1}, the voltage variation (in Fig. 11(a)) of v_{o1} is less than 2V (8.3%) in the transient period using a PFM control loop. Almost no voltage variations are observed in v_{o2} and v_{o3}. In the case of an experiment where i_{o2} is changed, v_{o2} is also well regulated by PWM control and a small variation is shown in Fig. 11(b). In the case of a change in i_{o3}, v_{o3} is regulated less than 2V in the transient period. The other output voltages are regulated within 0.5V. In the steady state, all output voltage variations according to the load current are almost zero as shown in Fig. 11.

V. Conclusions

This paper proposes a tightly regulated triple output ASHF converter with PFM-PWM-PD control. The auxiliary circuitries in the conventional approach such as a transformer and a blocking capacitor are eliminated by the utilization of the multi windings of the proposed converter. The modes of operation were explained and the steady state characteristics were investigated. From the analysis result, the minimum interactions among the control variables were verified. The proposed converter and control scheme were implemented with a 24V/10A, 5V/10A and 12V/5A hardware prototype using a 16bit digital controller. The measured voltage gain and operating waveforms verified the analysis results and tight output voltage regulation in the steady state for different loads was confirmed.



(a) i_{o1} : 1A → 10A (b) i_{o2} : 1A → 10A (c) i_{o3} : 0.5A → 5A

Fig. 11. The regulation performances of the output voltages respect to the load change.

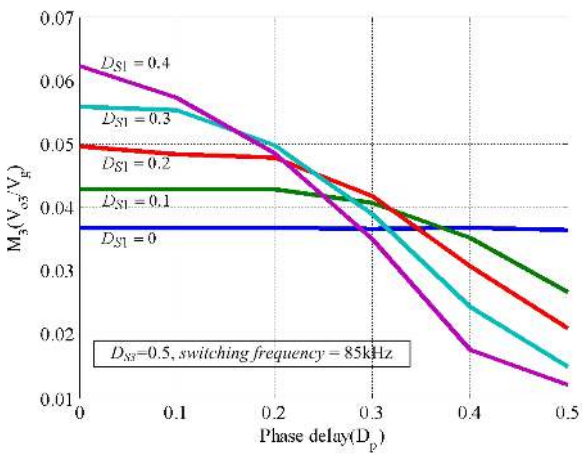


Fig. 12. The measured voltage gain (M_3) according to D_{S1} and D_p.

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