01 Aug 2004

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Recommended Citation

L. Zhang et al., "A Time Domain Approach to Estimate Current Draw from SMT Decoupling Capacitors," *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility (2004, Santa Clara, CA)*, vol. 2, pp. 377-382, Institute of Electrical and Electronics Engineers (IEEE), Aug 2004.
The definitive version is available at https://doi.org/10.1109/ISEMC.2004.1349819

A Time Domain Approach to Estimate Current Draw from SMT Decoupling Capacitors

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Abstract

A time domain approach to investigate and predict impedances and scattering parameters of a DC power bus is proposed. This approach is based on a cavity model and is achieved using a circuit simulation tool – SPICE. A SPICE-based circuit model for triangular power plane segments is described, verified and applied to simulate both the frequency and time domain characteristics of an irregularly shaped two-layer PCB board. Furthermore, the current draw from a surface mount technology (SMT) decoupling capacitor is simulated and estimated using this approach. Near-field electromagnetic loop probes are used to validate the current estimation qualitatively. Additionally the frequency bandwidth of this SPICE model is investigated using network analyzer and time domain reflectometry.

Keywords

Cavity model, equivalent circuits, SPICE, arbitrarily shaped power planes, current draw, near-field electromagnetic loop probe, VNA, TDR

I. INTRODUCTION

Power integrity is an essential consideration in power bus design for high-speed digital circuits. Power integrity often requires delivering high current with huge transients. It is best understood and managed by the concept of target impedance in the frequency domain. DC power and ground plane noise is a crucial topic in power integrity research, wherein the high frequency switching noise (delta I noise) is a common problem in printed circuit board design [1]. Delta – I noise can cause signal integrity problems and can be a potential source of radiated electromagnetic interference (EMI) [2]. The noise voltages induced in the power bus pair are correlated to the self-impedance or transfer impedance of the power bus. Thus predicting the self-impedance or the transfer impedance of the power plane pair is a key stage in predicting the characteristics of the power bus.

There is already a considerable amount of prior research on the power bus characteristics in the frequency domain. Several full-wave electromagnetic numerical simulation methods are appropriate for this area. A circuit extraction approach based on a mixed-potential integral equation (CEMPIE) was applied to model DC power bus structures with discontinuities[3], [4]. This method can be used to simulate irregular geometries. However the time and computer memory consumption will significantly increase if finer mesh is required. Finite Difference Time Domain (FDTD) is also a wide band approach to model power bus structures [5]. To reach a steady state solution, however, FDTD may require a large number of time steps.

For signal integrity or power integrity engineers, the time domain information including transient voltages and currents may be more valuable and helpful in power bus design, since the current and voltage waveforms can give more explicit and straightforward views of the signals rather than frequency domain parameters, such as impedance. A modeling method based on two-dimensional discrete transmission lines or discrete coupled multi-conductor transmission lines can give both frequency and time domain information for power supply and ground planes [6]. This paper provides a faster and more straightforward way to access the time domain information.

This paper proposes a circuit model based on a cavity model to anticipate the power delivery issues. The cavity model was described by T. Okoshi in 1972 [7]. Subsequently it was developed and applied to simulate and model several aspects of DC power bus design [8], [9], [10], [11]. This prior work generally focused on the frequency domain characteristics. However in Na's paper, there is an example of a time domain application [8]. Most of this earlier work was related to power planes with regularly shaped geometries.

Generally, the shapes of PCB power planes are irregular. However any geometry can be divided into some fundamental shape elements, such as rectangular and triangular shapes. The circuit model based on the cavity model for a rectangular power plane geometry was already developed and verified [8]. In Section 2 of this paper, a circuit model

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is proposed and developed for predicting the impedance of isosceles right triangular patches on the basis of their closed-form impedance matrix formulation [12], [13]. This model will be validated in Section 3.

Hence, using the segmentation method [14] to combine rectangular and triangular power plane regions, both time and frequency domain characteristics of an irregularly-shaped two-layer PCB board can be calculated. An experimental circuit board was built and investigated. Good agreement between experimental measurements and simulations were obtained and are discussed in Section 4.

Consequently, in Section 5 this circuit model was used to estimate the current draw from SMT decoupling capacitors on a DC power bus. The near-field magnetic probing method was implemented to qualitatively validate this approach.

II. THE TIME DOMAIN APPROACH

For an isosceles right triangular patch as shown in Figure 1, a typical element of the transfer impedance matrix can be expressed as

$$Z_{ij} = j\omega\mu d\sum_{m=0}^{+\infty}\sum_{n=0}^{+\infty}\frac{e_m^2 e_n^2 T(x_i,y_i)T(x_j,y_j)}{2[(m^2+n^2)\pi^2 - a^2k^2]} \qquad (1)$$

where

$$T(x,y) = \cos(k_x x)\cos(k_y y)\mathrm{sinc}(k_x W_x/2)\mathrm{sinc}(k_y W_y/2)$$
$$+(-1)^{m+n}\cos(k_y x)\cos(k_x y)\mathrm{sinc}(k_y W_x/2)\mathrm{sinc}(k_x W_y/2)$$

$$e_m = \begin{cases}1, & m=0\\ \sqrt{2}, & m>0\end{cases},\quad e_n = \begin{cases}1, & n=0\\ \sqrt{2}, & n>0\end{cases}$$

$$k = k' - jk'' = \omega\sqrt{\mu\varepsilon} - j\omega\sqrt{\mu\varepsilon}(\tan\delta + (\sqrt{2/\omega\mu\sigma})/d)/2,$$

and i and j are the indices of the ports.

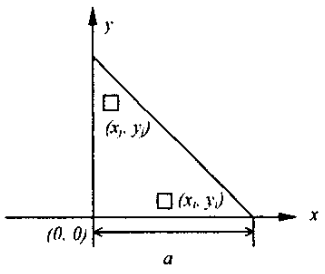

Figure 1. An isosceles right triangular microstrip patch showing the locations of the ports i and j.

As in the case of rectangular patches [8], the transfer impedances in (1) can be represented by a SPICE equivalent circuit model in Figure 2. Values for the relevant circuit parameters are shown in (2). In this equation, $\omega_{mn} = 2\pi f_{mn}$, where f_{mn} is the resonant frequency of each mode. In order to express (2) as a linear SPICE network, ω in the third term of the denominator is approximated by ω_{mn}. This is reasonable because the third term would become significant at the parallel resonance frequencies [8].

$$Z_{ij}(\omega) = \sum_{m=0}^{+\infty}\sum_{n=0}^{+\infty}\frac{N_{mni}N_{mnj}}{1/(j\omega L_{mn}) + j\omega C_{mn} + G_{mn}} \qquad (2)$$

where

$$L_{mn} = \frac{d}{2\omega_{mn}^2 a^2 \varepsilon}$$
$$C_{mn} = \frac{2\varepsilon a^2}{d}$$
$$G_{mn} = (2a^2\varepsilon/d)\omega(\tan\delta + \sqrt{2/(\omega\mu\sigma)}/d)\Big|_{\omega=\omega_{mn}}$$

and

$$N_{mni} = e_m e_n[\cos(k_x x_i)\cos(k_y y_i)\mathrm{sinc}(k_x W_x/2)\mathrm{sinc}(k_y W_y/2)$$
$$+(-1)^{m+n}\cos(k_y x_i)\cos(k_x y_i)\mathrm{sinc}(k_y W_x/2)\mathrm{sinc}(k_x W_y/2)]$$

$$k_{mn} = \sqrt{k_x^2 + k_y^2} = \sqrt{(\frac{m\pi}{a})^2 + (\frac{n\pi}{a})^2} = 2\pi f_{mn}\sqrt{\mu\varepsilon}$$
$$k_x = \frac{m\pi}{a}, k_y = \frac{n\pi}{a}$$

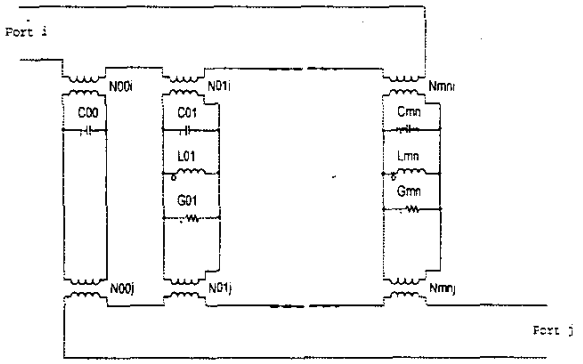

Figure 2. An equivalent circuit for the impedance between ports i and j in a triangular region.

III. SPICE MODEL VALIDATION

The power plane geometry in Figure 3 is an isosceles right triangular patch with two ports at (2.83, 2.83) cm and (5, 5) cm respectively. The self-impedance at port 1 and the transfer impedance between port 1 and port 2 were calculated using the model described in Figure 2. The cavity model method initially yields the self and transfer impedance as a function of angular frequency for ports on a power ground plane pair. Subsequent results obtained using the cavity model in this manner are referred to as cavity model results. Alternatively the equivalent circuit (e.g. as in Figure 2) can be simulated in SPICE using a swept frequency. Results obtained in this manner are referred to as SPICE model results. The SPICE model results for self and transfer impedances are compared with the cavity model results in Figure 4 and Figure 5. Cavity model results for these two figures were obtained from (1).

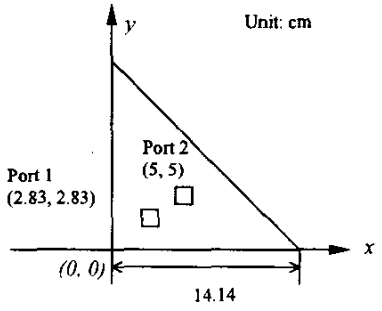

Figure 3. A triangular power plane geometry containing two ports.

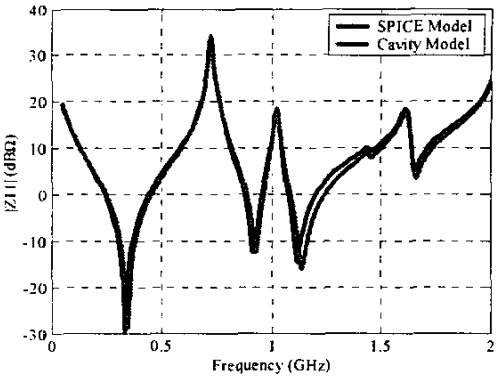

Figure 4. Self-impedance at Port 1 for the power plane geometry shown in Figure 3.

An irregularly shaped PCB board was built as shown in Figure 6. The segmentation method was implemented to combine the SPICE models for triangular and rectangular patches together. The segmentation method was described thoroughly in T. Okoshi's paper [12]. The self-impedance at port 1 was simulated by SPICE and cavity models and compared with experimental measurements. The result is shown in Figure 7. The impedance was measured with an HP8753D network analyzer.

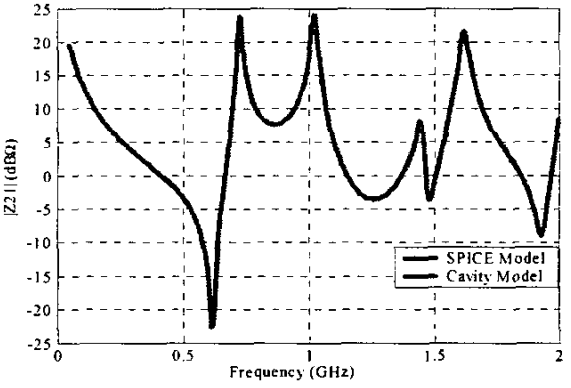

Figure 5. The transfer impedance between Port 1 and Port 2 for the power plane geometry shown in Figure 3.

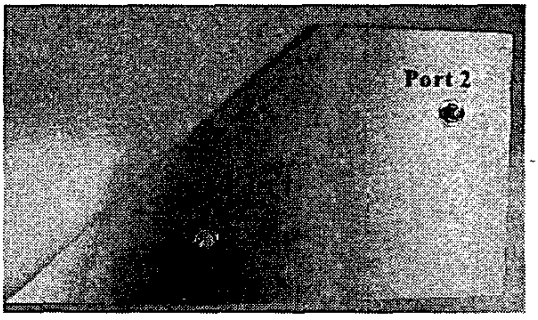

Figure 6. An arbitrarily-shaped test board.

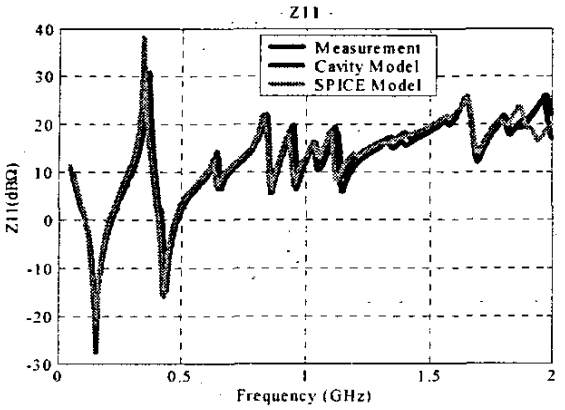

Figure 7. Numerical simulations compared with experimental measurements for the irregular patch geometry shown in Figure 6.

IV. PREDICTING CURRENT DRAW FROM SMT DECOUPLING CAPACITORS

A test board was built to verify this approach in time domain applications. This board contains an SMA port and a 10 nF SMT decoupling capacitor. It is difficult to measure the exact current draw from the SMT decoupling capacitor directly. An alternative method using a near field loop probe was implemented to investigate the characteristics of the current flowing through the capacitor qualitatively.

A picture of the near field electromagnetic scanning system is shown in Figure 8. Its functional and structural diagram is shown in Figure 9.

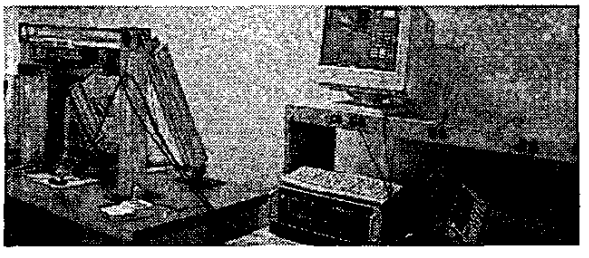

Figure 8. Near field scanning system.

In the time domain, the voltage induced into the loop probe can be expressed as

$$V = \frac{d\Phi}{dt} = \frac{d(BS)}{dt} = \frac{d(\mu HS)}{dt} = \mu S \frac{dH}{dt} = \frac{\mu S}{2\pi r}\frac{di}{dt} \qquad (3)$$

assuming that the magnetic intensity within the range of the probe loop is uniform, and determined only by the distance from the current and the current magnitude. In (3), S represents the area of the loop probe, H is the magnetic intensity and r is the distance from the current draw. Thus the measured voltage from the probe is the derivative of the current flowing through the capacitor. From this relationship between the current and the measurement from the loop probe, the simulation by the SPICE circuit can be qualitatively validated.

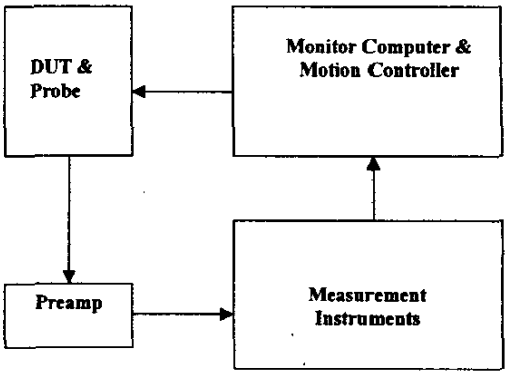

Figure 9. The diagram of the scanning system.

The probe was set over the top of the SMT capacitor as shown in Figure 10. The relevant quantities in (3) are represented schematically in Figure 11. A 100KHz square wave was impressed into the SMA connector in the test board. The rise time of the wave was 50 ns. The corresponding voltage at the capacitor was measured by an Agilent Infiniium oscilloscope as shown in Figure 12.

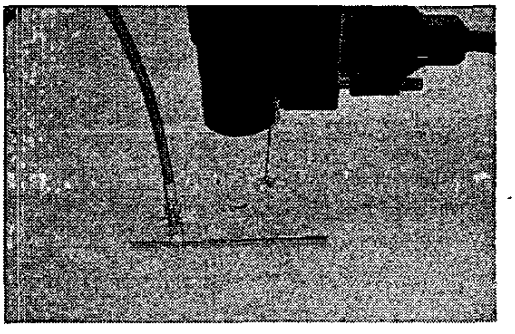

Figure 10. The probe beside the capacitor.

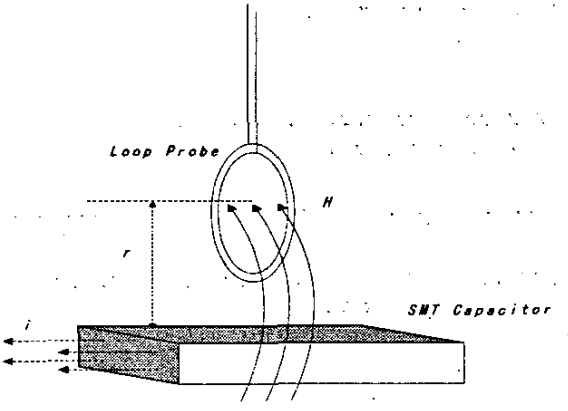

Figure 11. Probe over capacitor package.

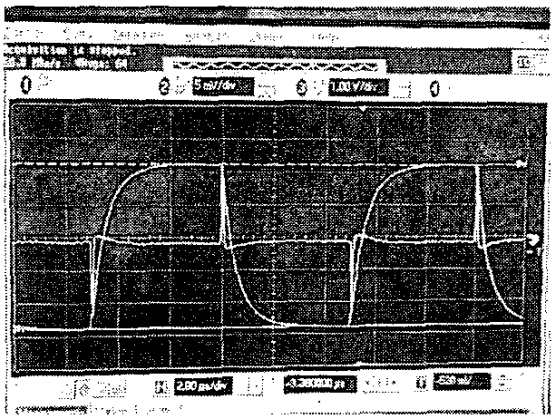

Figure 12. Voltage and current at the decoupling capacitor.

Figure 13 shows the voltages at the source (Port 1) and at the decoupling capacitor (Port 2). SPICE simulations and direct measurements are shown for the voltage at each port.

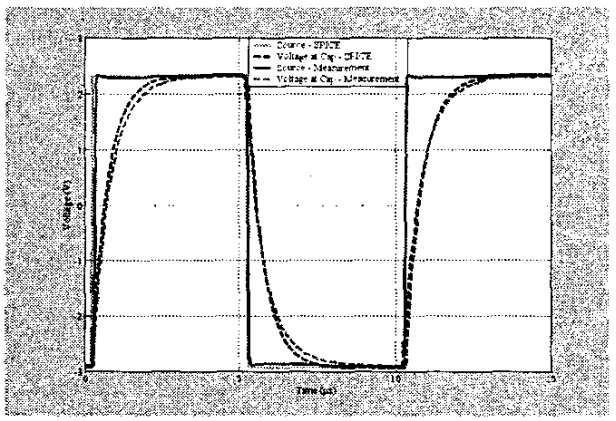

Figure 13. Simulated and measured voltages at ports 1 and 2.

The derivative of the simulated current waveform is plotted and compared with the measured signals in Figure 14. Note that the waves in these two figures are out of phase relative to the clock signal because the pre-amplifier used in the measurement has a 180° phase shift.

To further investigate the effect of bandwidth on this SPICE model, a step signal with a faster rise time was impressed into the board by a TDR (Time Domain Reflectometry) instrument. The rise time is approximately 50 ps. Prior to the TDR measurement, the input impedance at Port 1 was measured using a HP 8753D network analyzer. Input impedance comparisons are shown in Figure 15. The circuit simulation result for the voltage signal at the TDR port is compared with the TDR display in Figure 16.Voltage transitions associated with the cable between the board and the TDR occur within the first microsecond of Figure 16. An expanded view of this time range is shown in Figure 17.

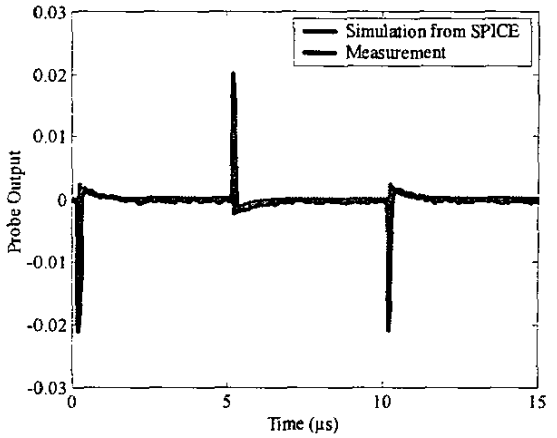

Figure 14. The comparison between the loop measurement and the SPICE simulation for the test board shown in Figure 10.

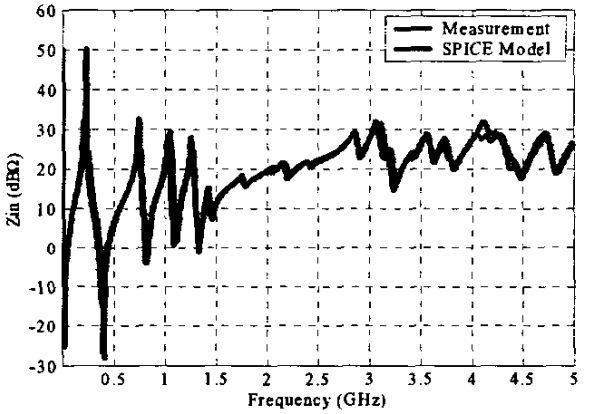

Figure 15. Input impedance at high frequencies for the test board shown in Figure 10.

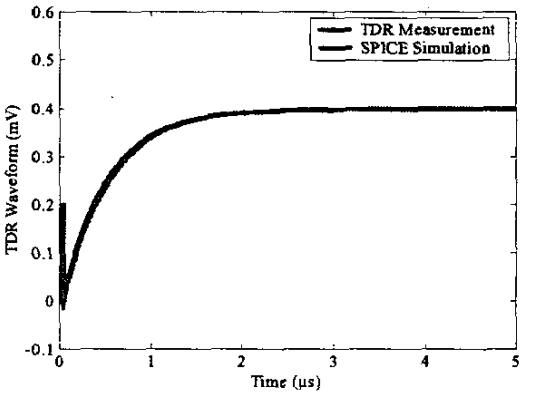

Figure 16. A comparison of the TDR measurement with the SPICE simulation for the test board shown in Figure 10.

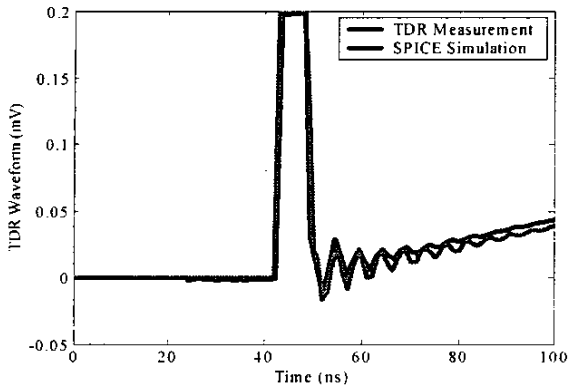

Figure 17. Expanded view of Figure 16 show in the voltage transitions.

V. CONCLUSION

An equivalent lumped circuit based on the cavity model was developed for predicting the impedance matrix and time domain characteristics of triangular microstrip patches. This equivalent circuit can be solved using SPICE tools. Furthermore, combined with the circuit models for rectangular microstrip patches using the segmentation method, this circuit model can be used to simulate arbitrarily shaped PCB boards, because any geometry can be approximately meshed into rectangles and isosceles triangles if the mesh is fine enough. A real board was built to test this time domain approach. The measured and simulated port voltages in the time domain (Figure 13) seem to agree to within a small fraction of a volt. Also, near field probes yield a current derivative waveform that closely resembles the spice results (Figure 14). In the frequency domain, the measured and simulated input impedances of the test board are generally comparable in shape and seem to agree with a few dB over the frequency range considered. The present circuit approach provides signal integrity engineers with a perspective to investigate both the time domain and the frequency domain characteristics in power bus design.

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